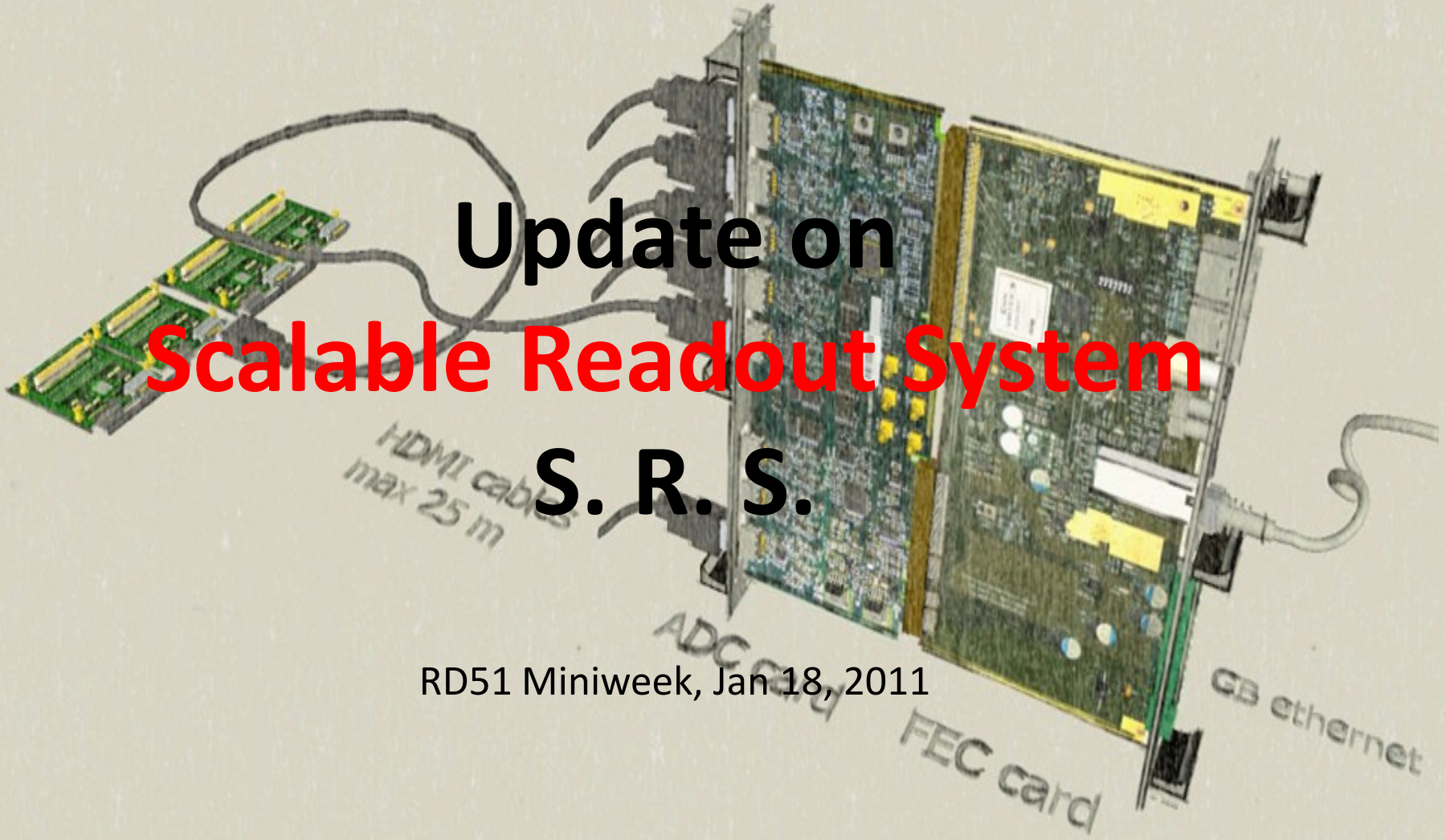


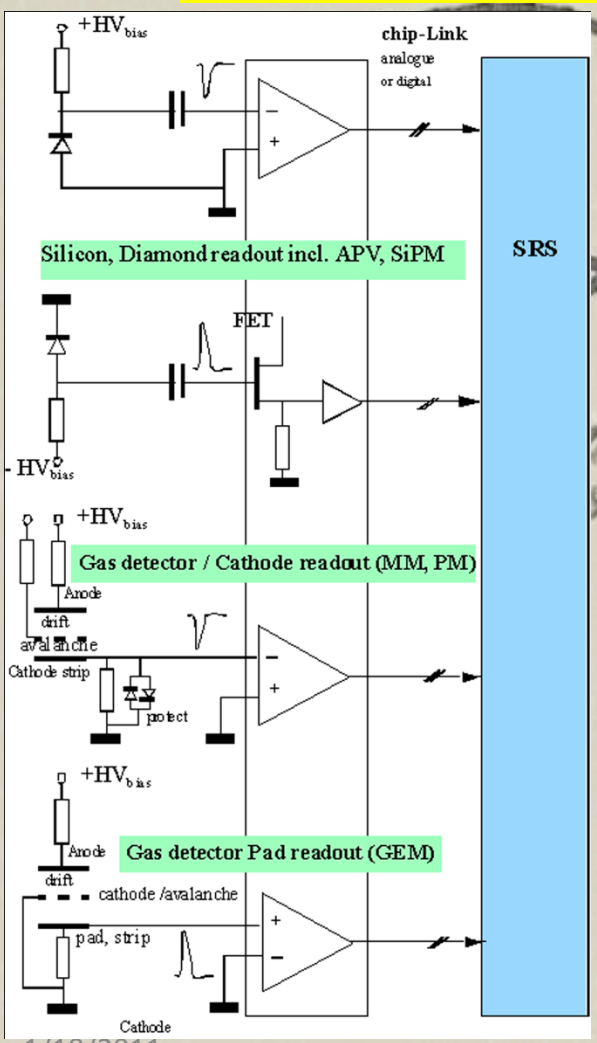
Update on
Scalable Readout System
S. R. S.

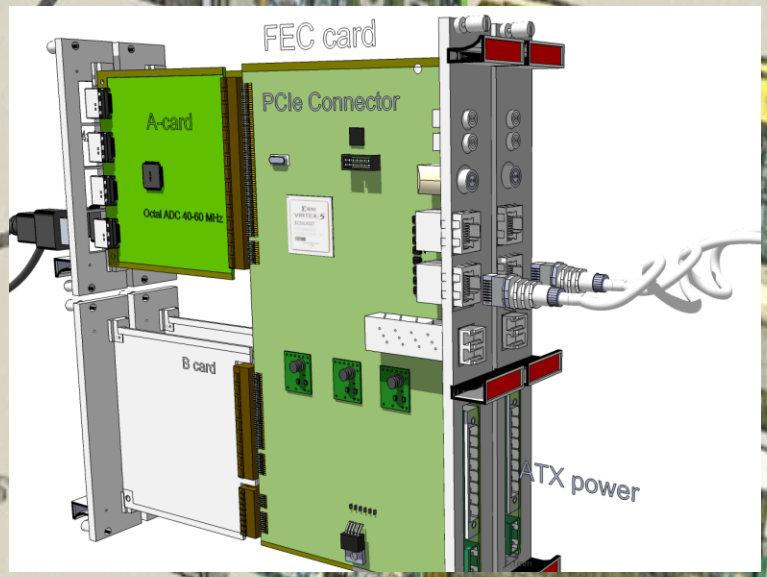
RD51 Miniweek, Jan 18, 2011

RD51 user requirement

SRS is the common solution to multichannel detector variety

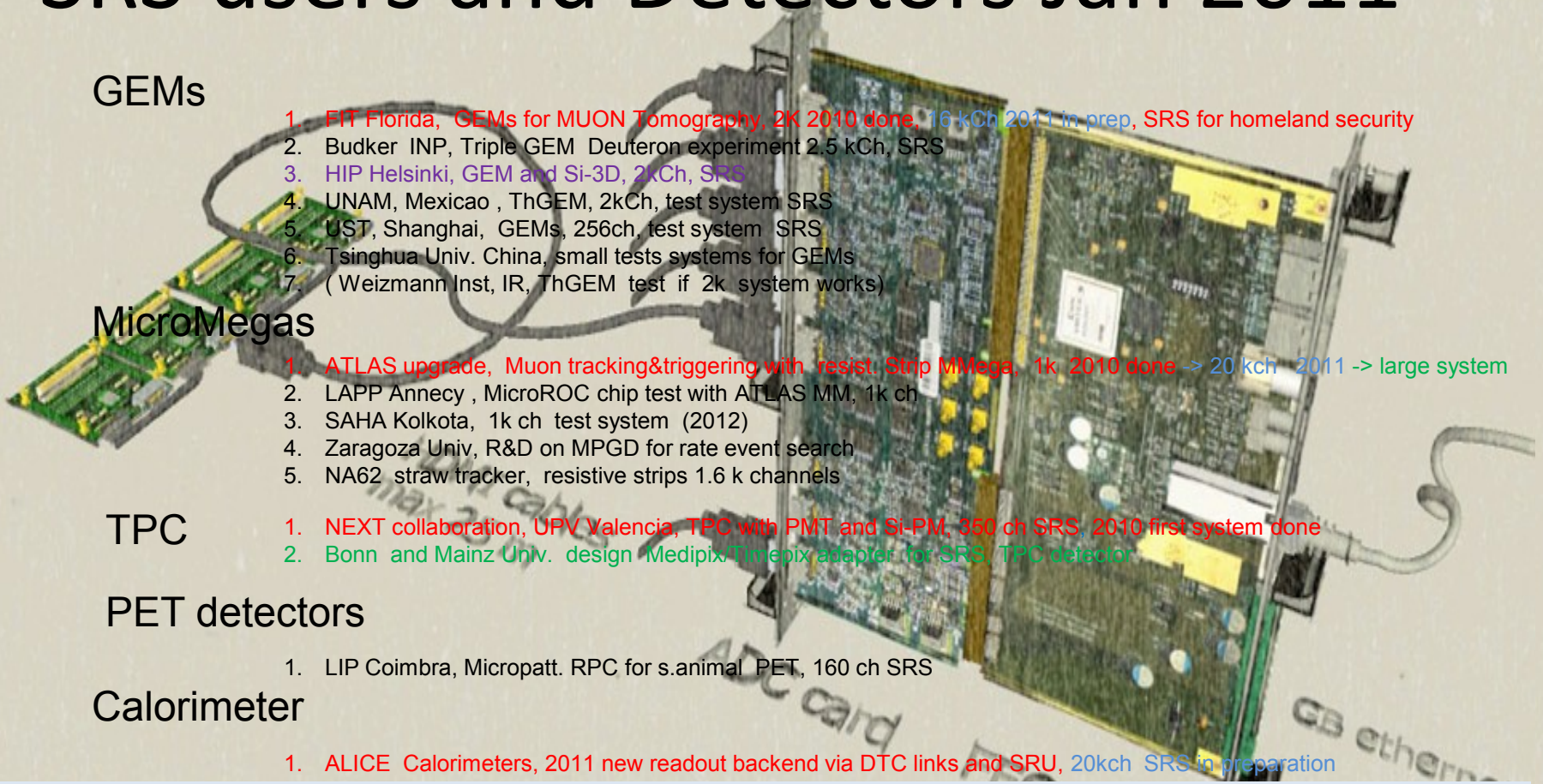
SRS going strong into 2011: 4 major detectors 11 test systems





- Small set of modular components
- Performance at low cost
- Scalability from 100 to 1000.000 channels
- Plugin-choice of frontend ASICs
- Open developer platform for physics algorithms
- Supported Software made for Physics

SRS users and Detectors Jan 2011



GEMs

1. FIT Florida, GEMs for MUON Tomography, 2K 2010 done, 16 kCh 2011 in prep, SRS for homeland security
2. Budker INP, Triple GEM Deuteron experiment 2.5 kCh, SRS
3. HIP Helsinki, GEM and Si-3D, 2kCh, SRS
4. UNAM, Mexicao , ThGEM, 2kCh, test system SRS
5. UST, Shanghai, GEMs, 256ch, test system SRS
6. Tsinghua Univ. China, small tests systems for GEMs
7. (Weizmann Inst, IR, ThGEM test if 2k system works)

MicroMegas

1. ATLAS upgrade, Muon tracking&triggering with resist. Strip MMega, 1k, 2010 done -> 20 kch 2011 -> large system
2. LAPP Annecy , MicroROC chip test with ATLAS MM, 1k ch
3. SAHA Kolkota, 1k ch test system (2012)
4. Zaragoza Univ, R&D on MPGD for rate event search
5. NA62 straw tracker, resistive strips 1.6 k channels

TPC

1. NEXT collaboration, UPV Valencia, TPC with PMT and Si-PM, 350 ch SRS, 2010 first system done
2. Bonn and Mainz Univ. design Medipix/Timepix adapter for SRS, TPC detector

PET detectors

1. LIP Coimbra, Micropatt. RPC for s.animal PET, 160 ch SRS

Calorimeter

1. ALICE Calorimeters, 2011 new readout backend via DTC links and SRU, 20kch SRS in preparation

Color code:

red: systems deployed, or in construction at end 2010

blue: medium sized systems in construction 2011

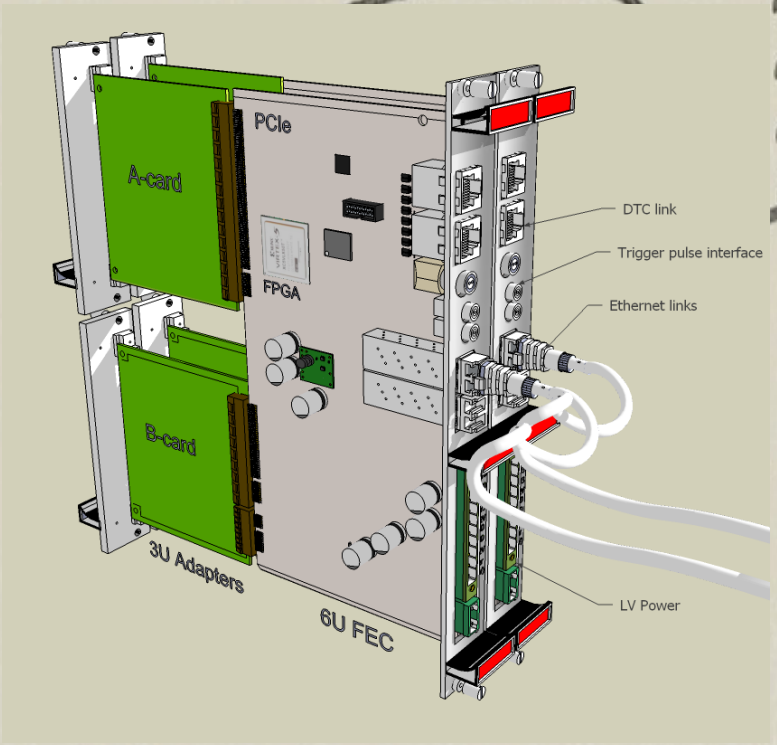
cyan: small system under construction in 1Q 2011

black: small SRS systems in preparation 2Q 211

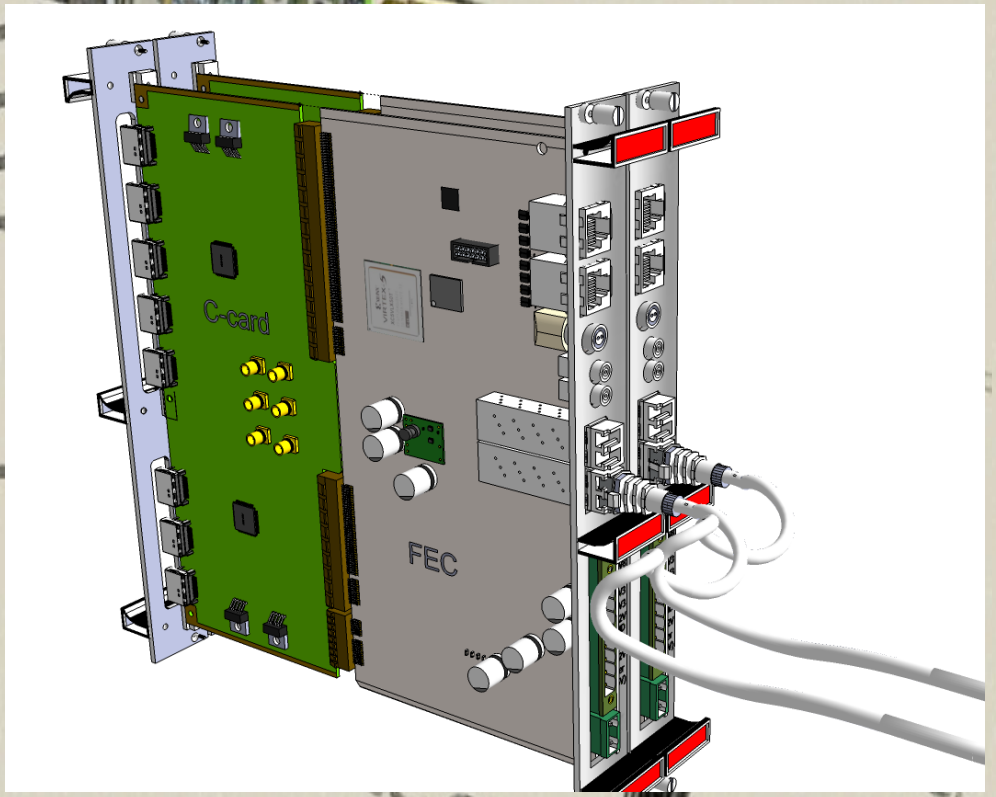
green: new SRS chip frontend project

FEC and adapter cards

up to 14 units in one 6U x220 Europa Chassis



3U adapter cards (A+B)



6U adapter cards (C)

1st SRS system cards

Digitizer V1.0

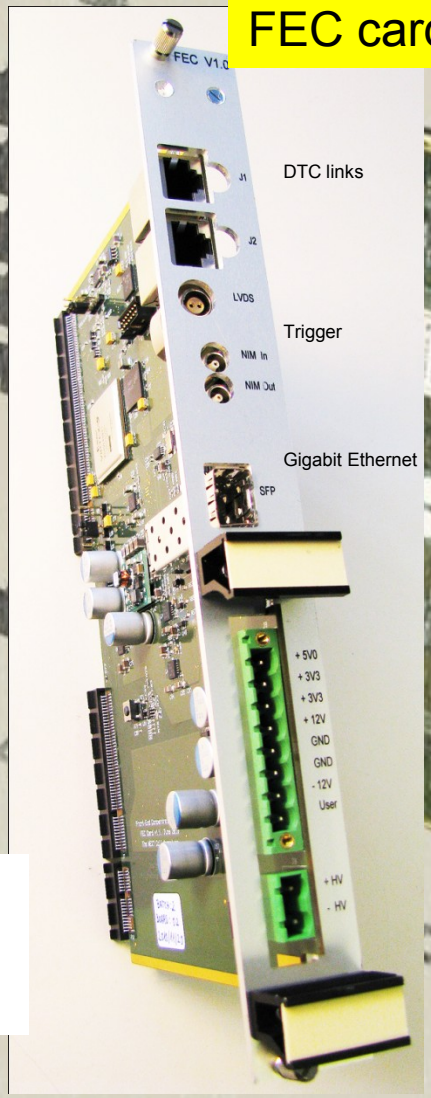
2010
18 cards produced
2011
15 new version 1.1

2x octal ADC 40 MHz , 12 bit TI ADS 5281
8x HDMI type A connector, 19 pin (Molex 47151-1001 , do not use SAMTEC)

de-emphais adapter and cable lenght configurator

HDMI interface for 16 hybrids
16 ADC's 12 bit 40 MHz

FEC card V1.2



2010
22 cards produced
2011
15 new version 6

665
1 NIM in (Trigger min 50 ns)
1 NIM out (Busy)
1 LVDS differential user defined

1 RJ45 for general use
1 RJ45 for DTC link

1 HV connector (user defined)
1 Power connector Phoenix 8pin 5,08 pitch

FPGA with GBE interface
ADC deserilizer, trigger interface

Design your own SRS adapter?

->FEC interface is important

A-card signals PCIe x16:

PCIe x16	32 bit bus alternat. 16 differential I/Os
	4x5V, +12V, -12V, (more on PCIex1)
	20 differential LVDS
	I2C, JTAG
	Acard_present, Acard_Pwer_good
	2.5-Gigabit (GBTA) 3 diff. Pairs

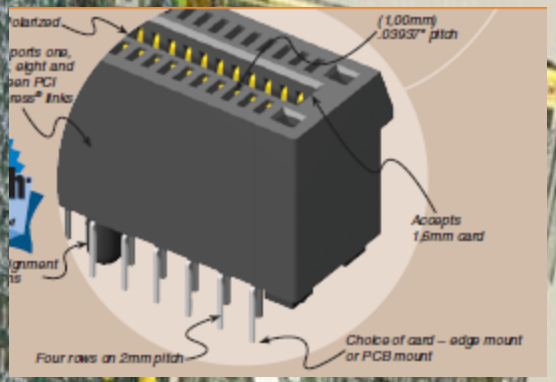
B-card signals PCI x8

16 bit bus, alt. 8 differential I/Os
I2C
Bcard_present, Bcard PWGood
2.5-Gigabit (GBTA) 3 diff. Pairs

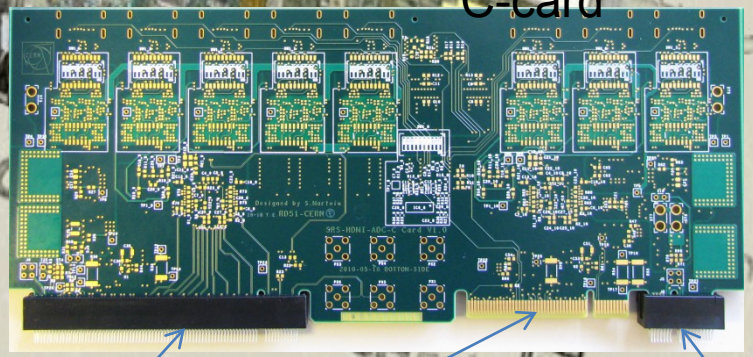
Power connector PCIe_x1 from F.Panel

5 x +5V, 2x +12V, 2 x -5V
7 x GND

PCIe-straddle mount

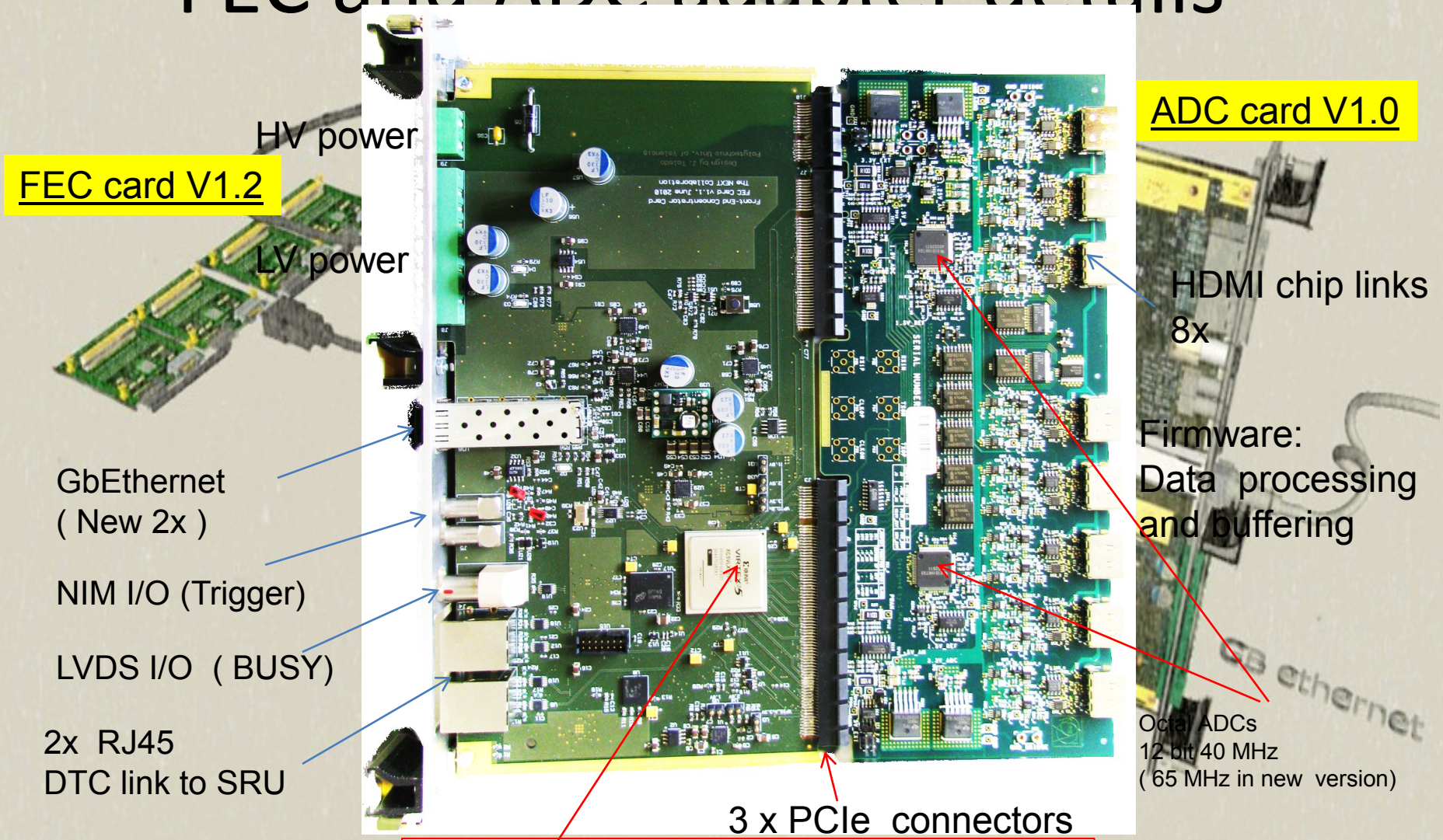


C-card

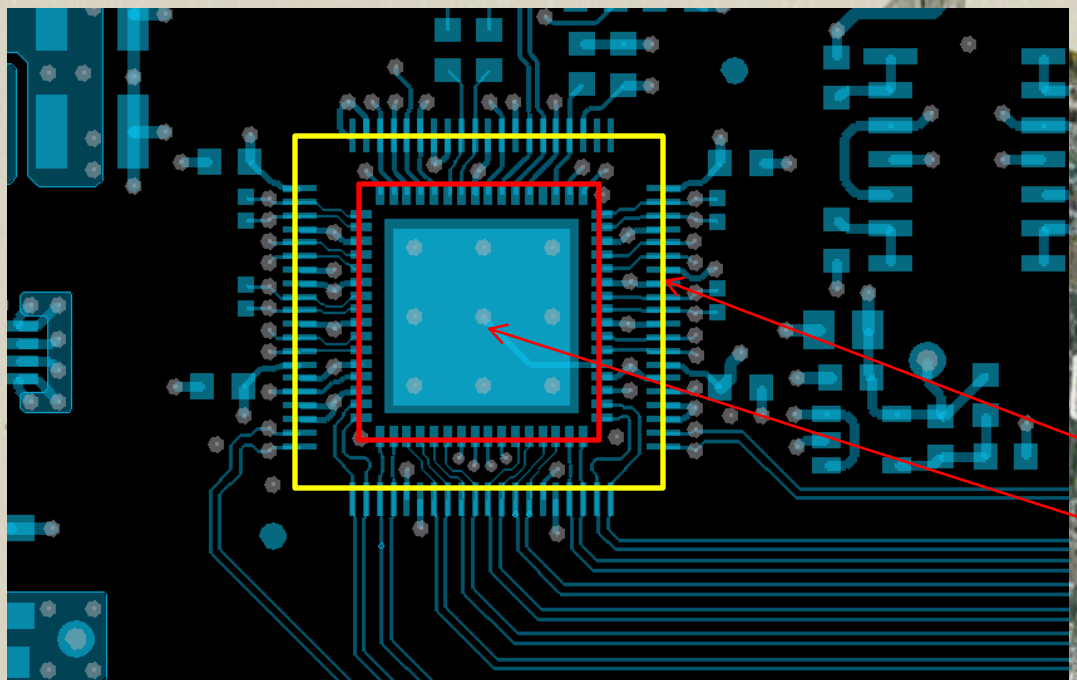


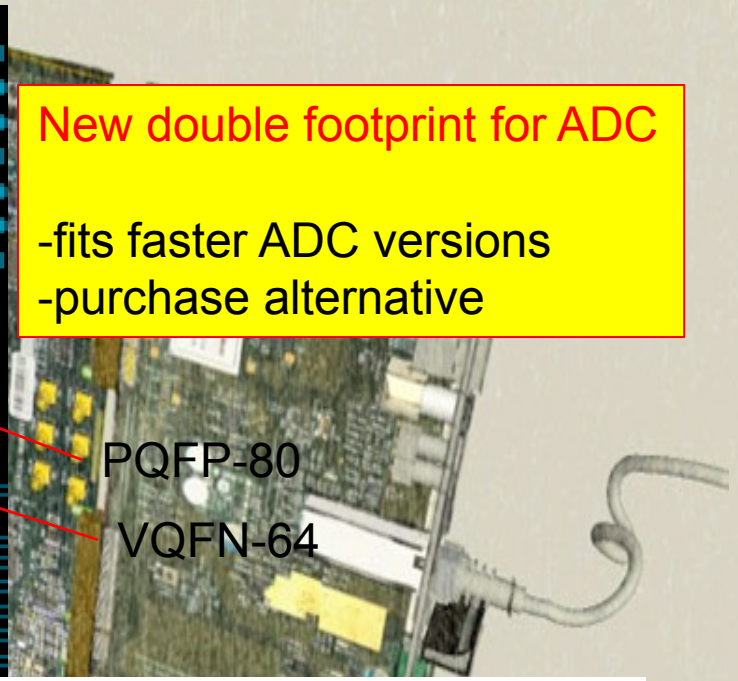
Note: we do NOT use the PCIe protocol

FEC and ADC adapter details



Revised ADC Card v1.1





New double footprint for ADC

-fits faster ADC versions
-purchase alternative

MODEL	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CHANNELS
ADS5281	12	50	8
ADS5282	12	65	8
ADS5287	10	65	8
ADS5270	12	40	8
ADS5271	12	50	8
ADS5272	12	65	8
ADS5273	12	70	8

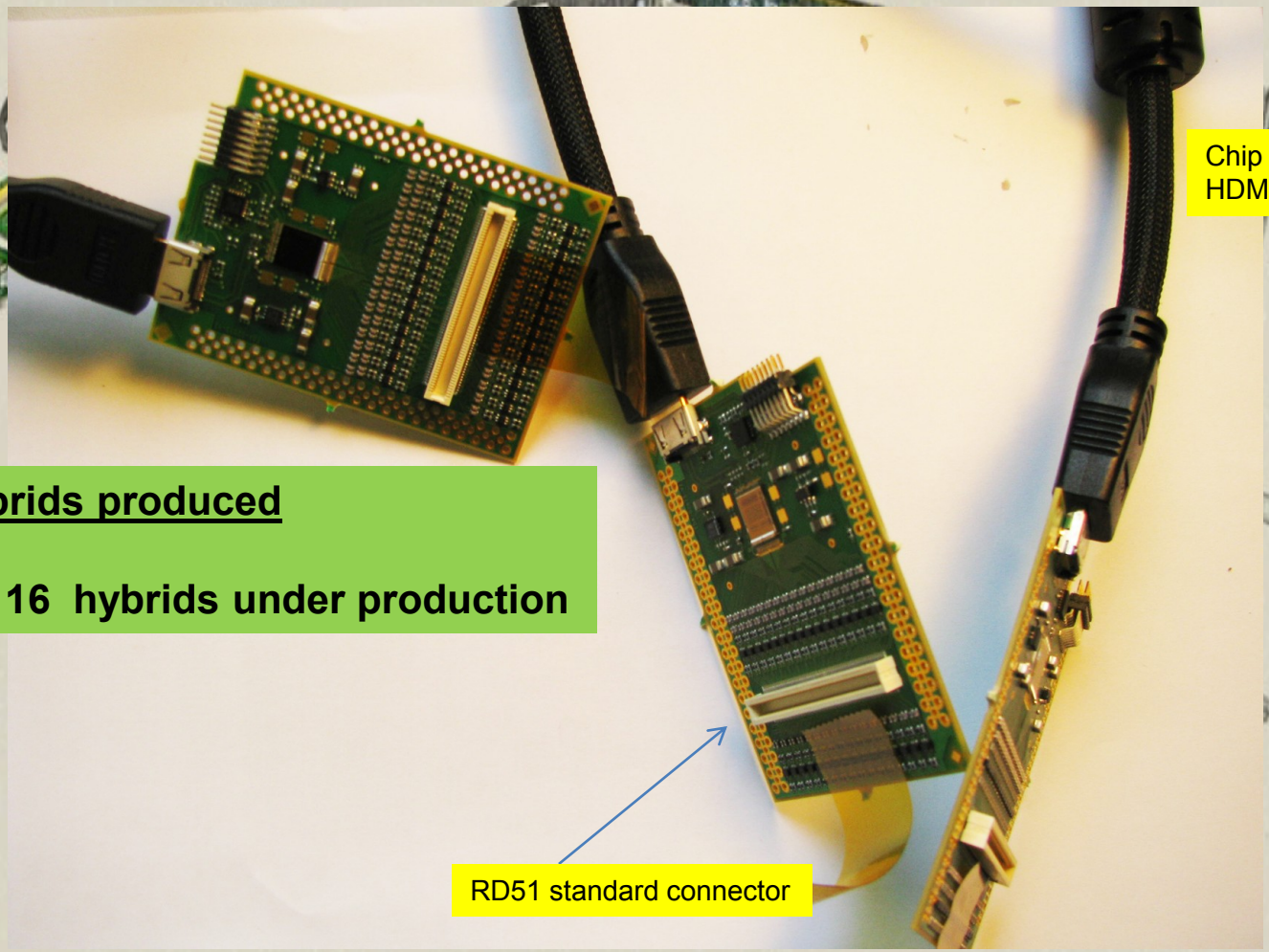
FEC card revision V6

(co-design CERN-UPV Valencia)

- **New FPGA**: Virtex 6 (faster and significantly more resources for Online firmware)
- **Dual SFP+** on Front panel (separated Data and Control via GBe)
- **More I/Os** on PCIe (more applications)
- **4 x GTX transceiver (5 GBps)** on interface connector A (fast applications)
- **Remote FPGA configuration** via Ethernet (reconfiguration from distance)
- **LDO's** replace switching regulators (less noise, and operation in magnetic field)
- **DDR3** pluggable memory (optional large data buffer)

High priority plans: Cadence schematics database to be finalized, PCB Layout by mid Feb, V6 FECs by end march

1st SRS Hybrid: APV 25 based

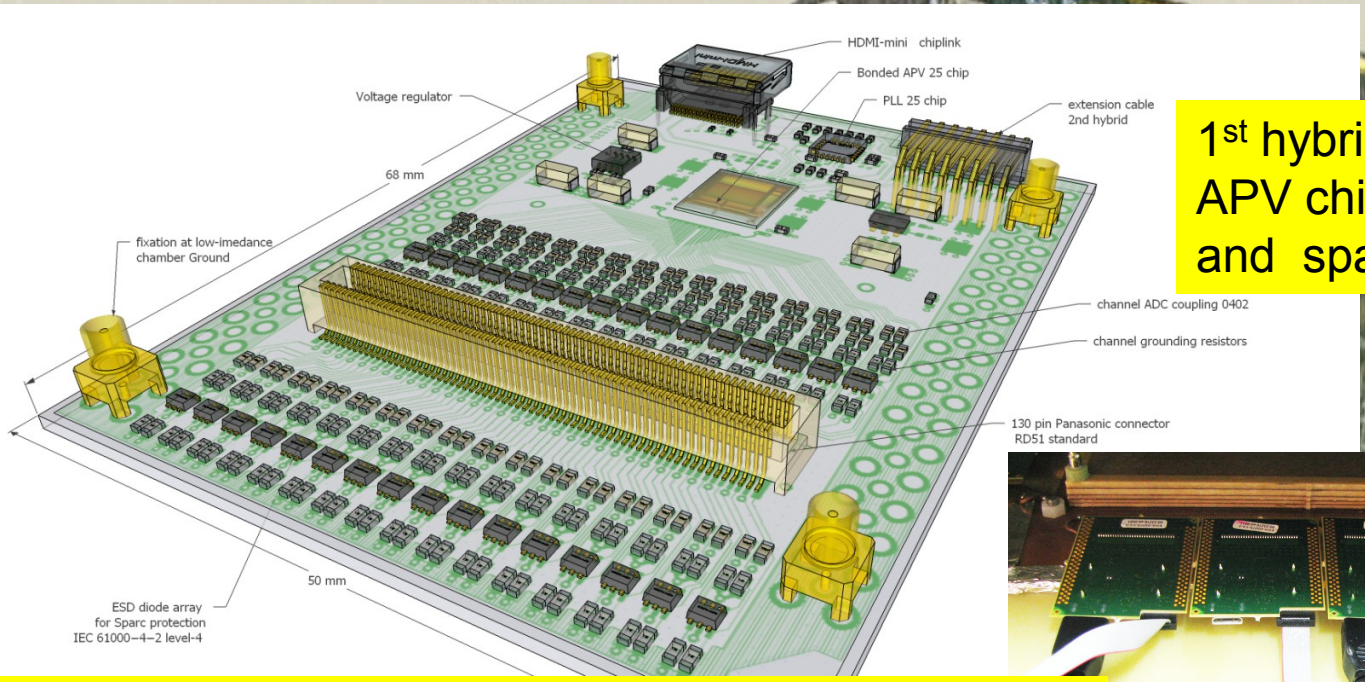


2010: 15 hybrids produced

2011: 250 + 16 hybrids under production

SRS hybrid concept

-keep the backbone system
-exchange the ASIC hybrid on the detector



1st hybrid with 128 channel APV chip and HDMI readout and sparc protection

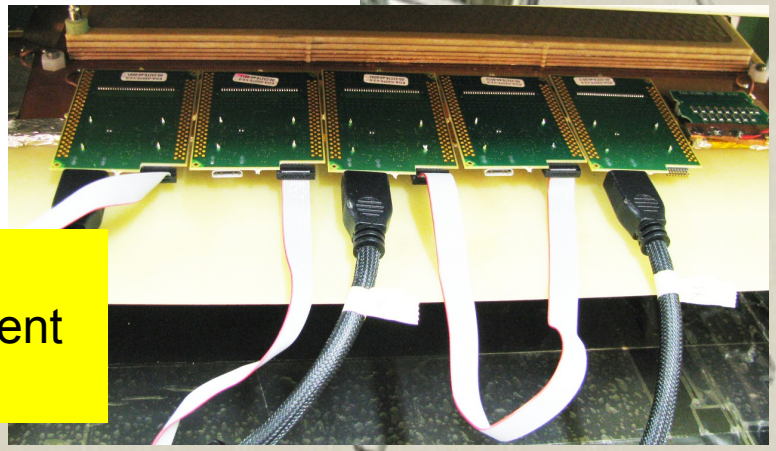
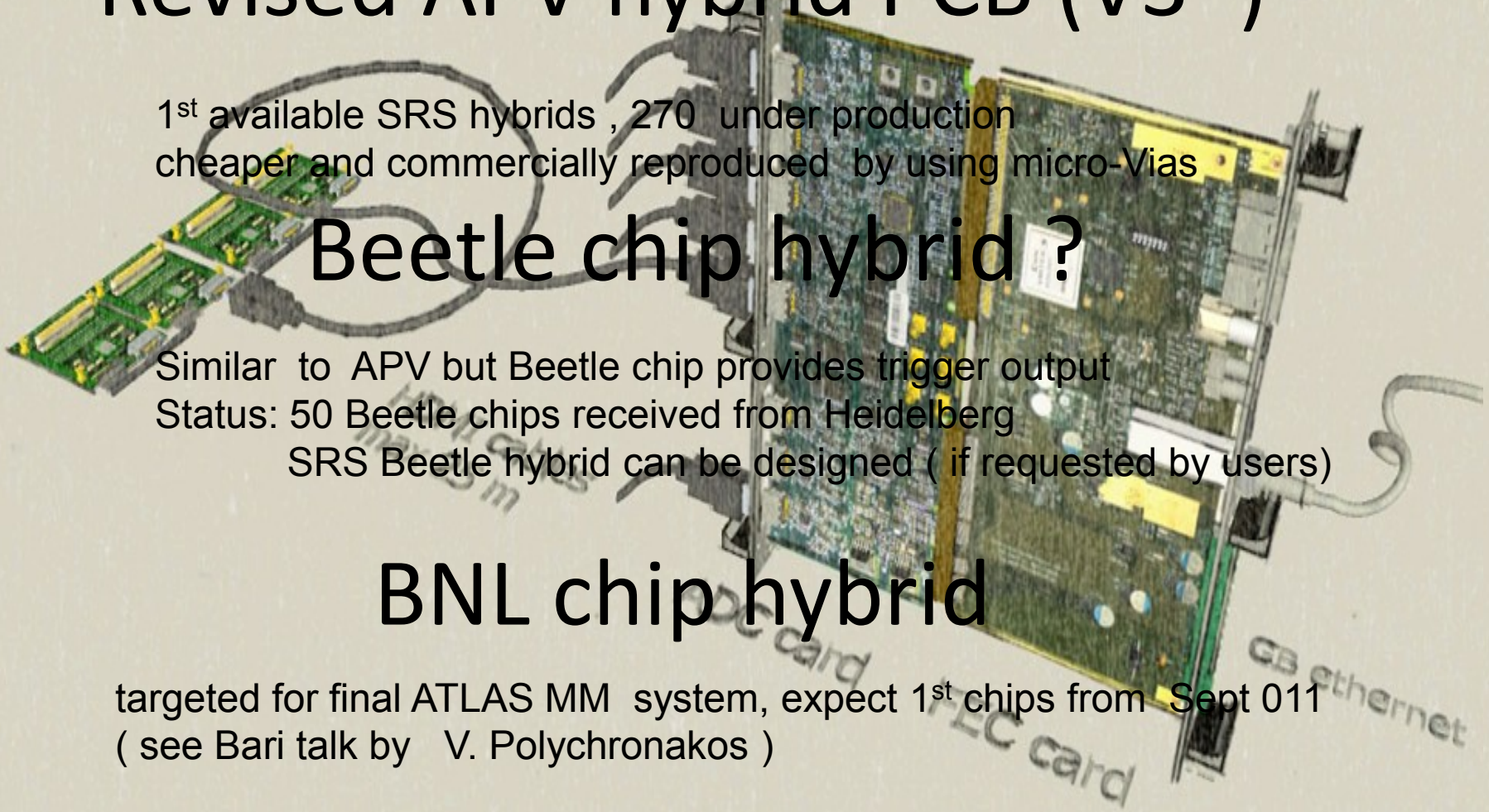


photo of APV hybrids on GEM chamber readout via HDMI cables

All SRS hybrids have a standard detector- and readout- interface. Individual hybrids have different readout ASICs

Hybrid APV25-S1 radhard, with Panasonic socket on hybrid: AXK5SA3277YG
Link interface HDMI-mini , hybrid power 3V3 500 mA max via HDMI cable
Extension interface for 2nd hybrid via Samtec FFSD-08-D-04.00-01-N cables (4.0 inch)
Protection diodes: NUP4114UPXV6T1G (15A clamp in1 ns, 1pF added capacity, reverse biased, quad package)
Lateral very low Impedance Ground & Clickin-fixation holes on hybrid for SAMTEC Jack MMXCX-P-P-H-ST-SM1
Readout chip: APV25-s1. 128 analogue channels. Wire bonded to hybrid in 2 layers.
Phase lock chip PLL25-LPCC radhard

Revised APV hybrid PCB (V3*)



1st available SRS hybrids , 270 under production
cheaper and commercially reproduced by using micro-Vias

Beetle chip hybrid ?

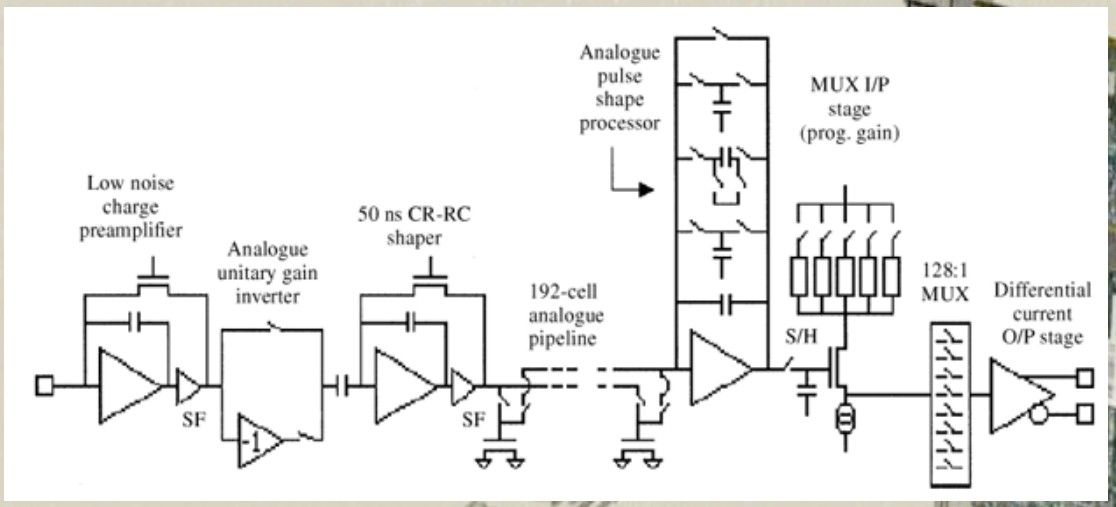
Similar to APV but Beetle chip provides trigger output
Status: 50 Beetle chips received from Heidelberg
SRS Beetle hybrid can be designed (if requested by users)

BNL chip hybrid

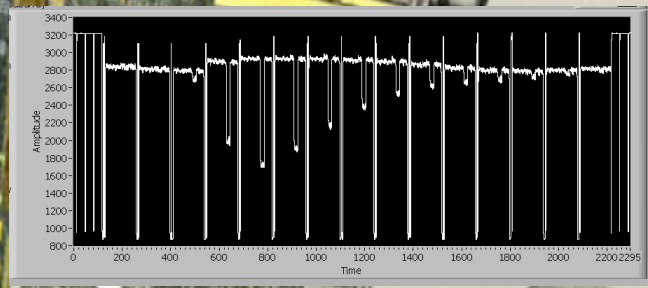
targeted for final ATLAS MM system, expect 1st chips from Sept 011
(see Bari talk by V. Polychronakos)

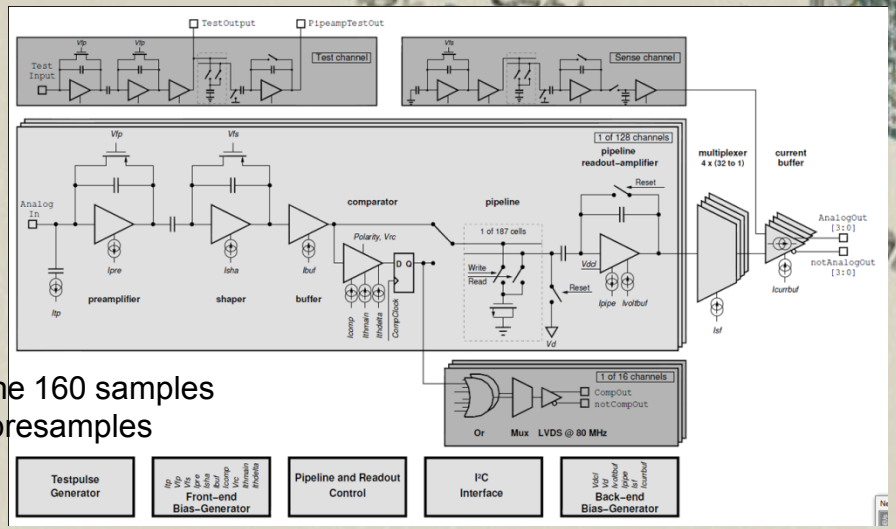
* technical details on EDMS http://edms.cern.ch/nav/EDA-02075-V3-0

APV and Beetle chip



APV: Analogue serial output





pipeline 160 samples
+ 16 presamples

Beetle:

Analogue serial output

Digital serial output

Trigger output

HDMI chip links*

HDMI mini on hybrid side

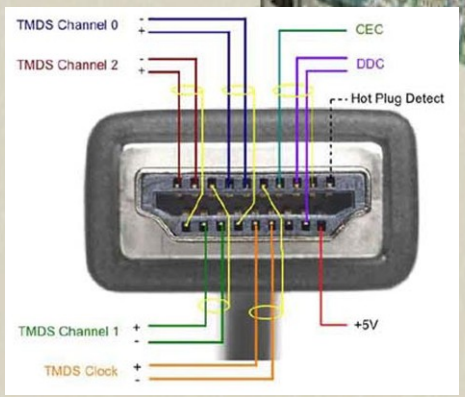
Multicomp part No 1901119

Length extension up 25 m

10 m	Multicomp 18-94192670
15 m	PRO SIGANL MC34971

3M cable 3m Part No 3548381282808

3	high speed shielded channels 3 GHz
1	Clock to hybrid
1	Controls line
1	Power line

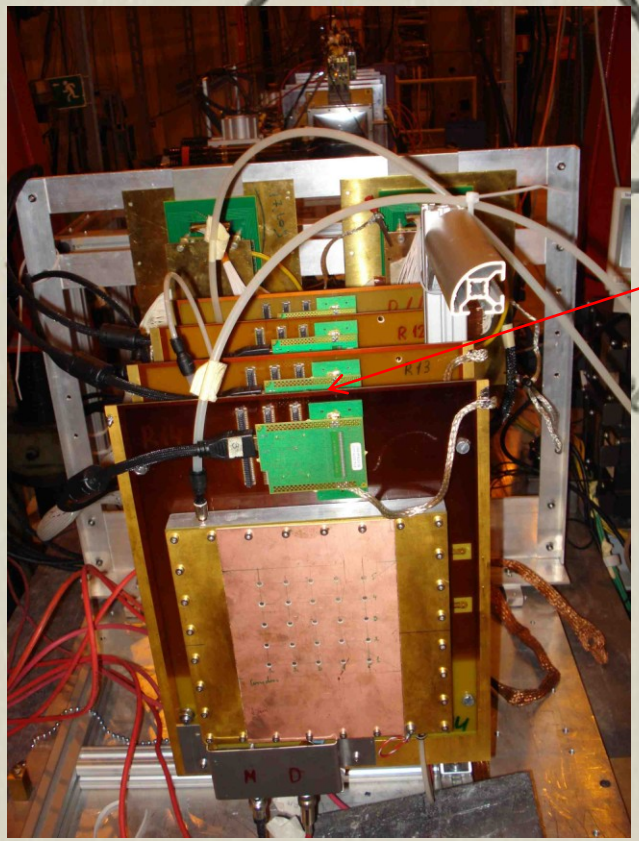


- SRS looking into an industry-standard optical chip link , in particular monitoring the USB-3 formum , i.e .Intel's Lightpeak

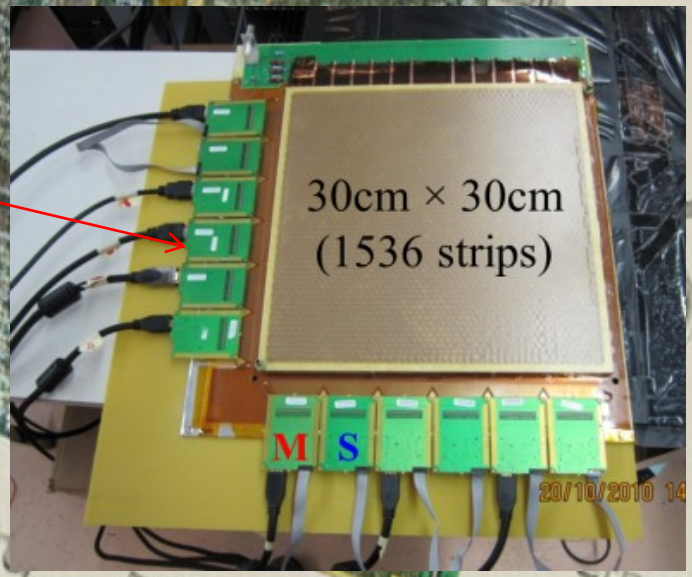
2010: First small SRS Systems

ATLAS **MicroMega**:
In H6 testbeam (see MM talks)

FIT: Muon Tomography with **GEM**
(see RD51-Note-2010-004)



SRS
Hybrids
with APV25

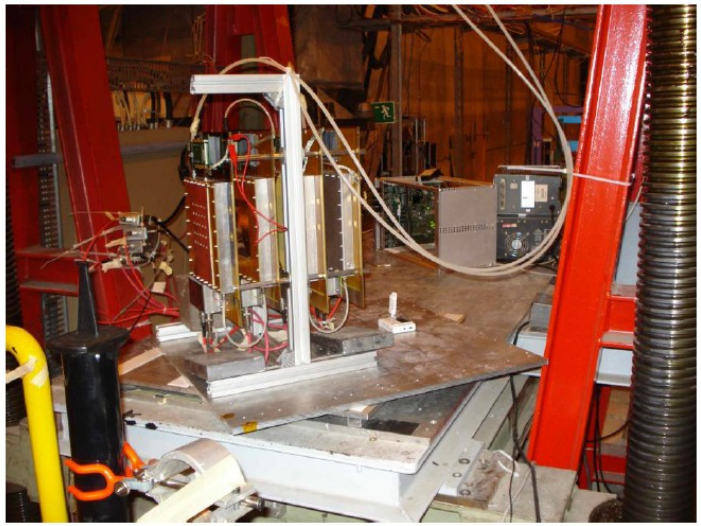


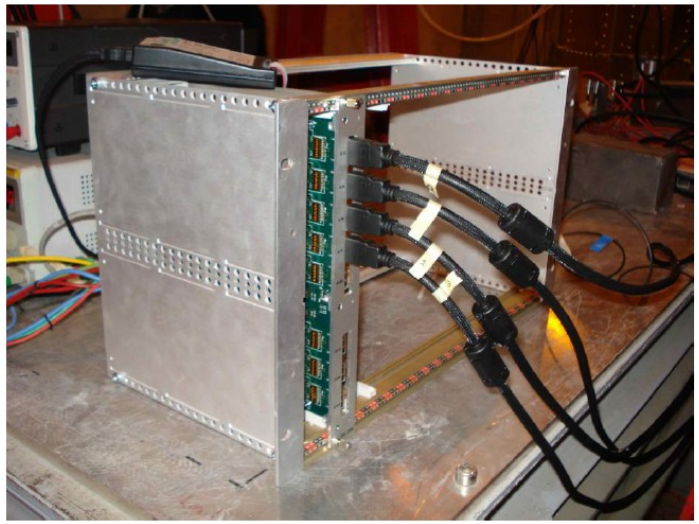
ATLAS Micromegas status report:

New readout electronics (CERN)

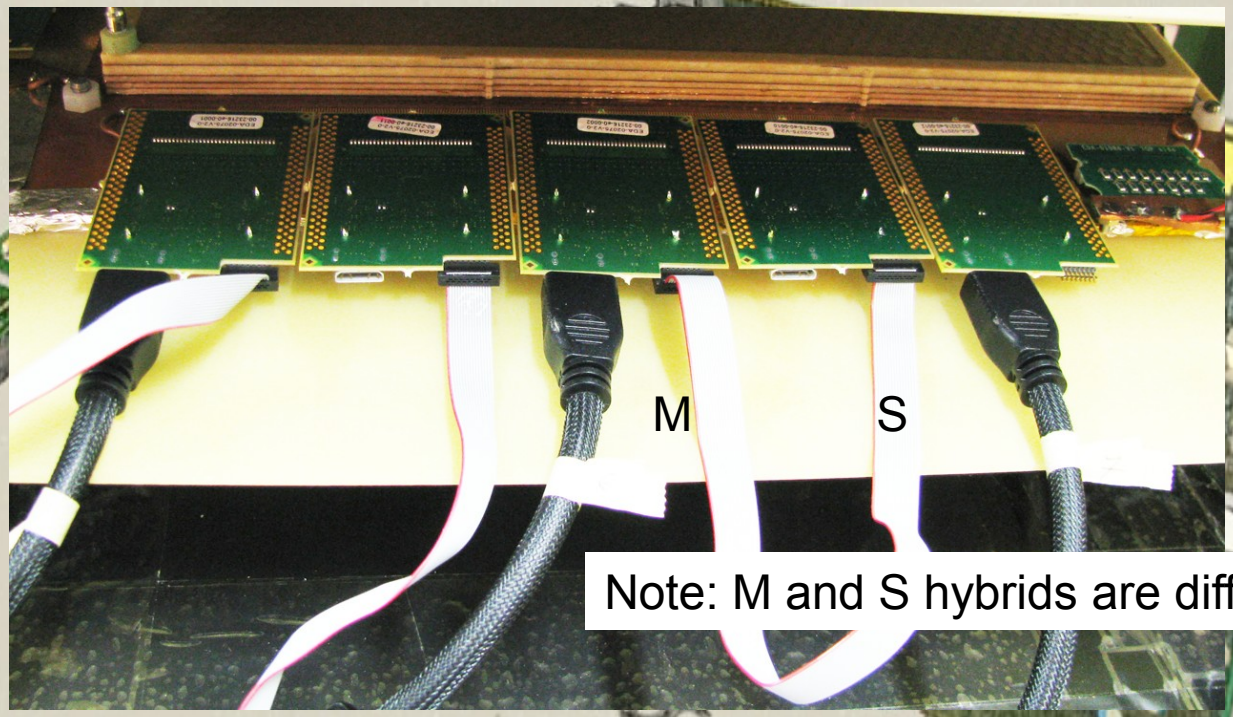
APV25 & Scalable Readout System

- Four chambers read out through 1 APV25 chip each (CMS Si tracker chip, 128 channels, variable number of 25 ns time samples)
- SRS Front-end card (H. Muller et al.), 1 FEC for up to 16 APV25 chips)
- Data transfer via ethernet; DAQ system: ALICE Date
- Worked flawlessly, simple and reliable (first try 1 week before test beam)





Hybrids on GEM chamber



Note: M and S hybrids are different !

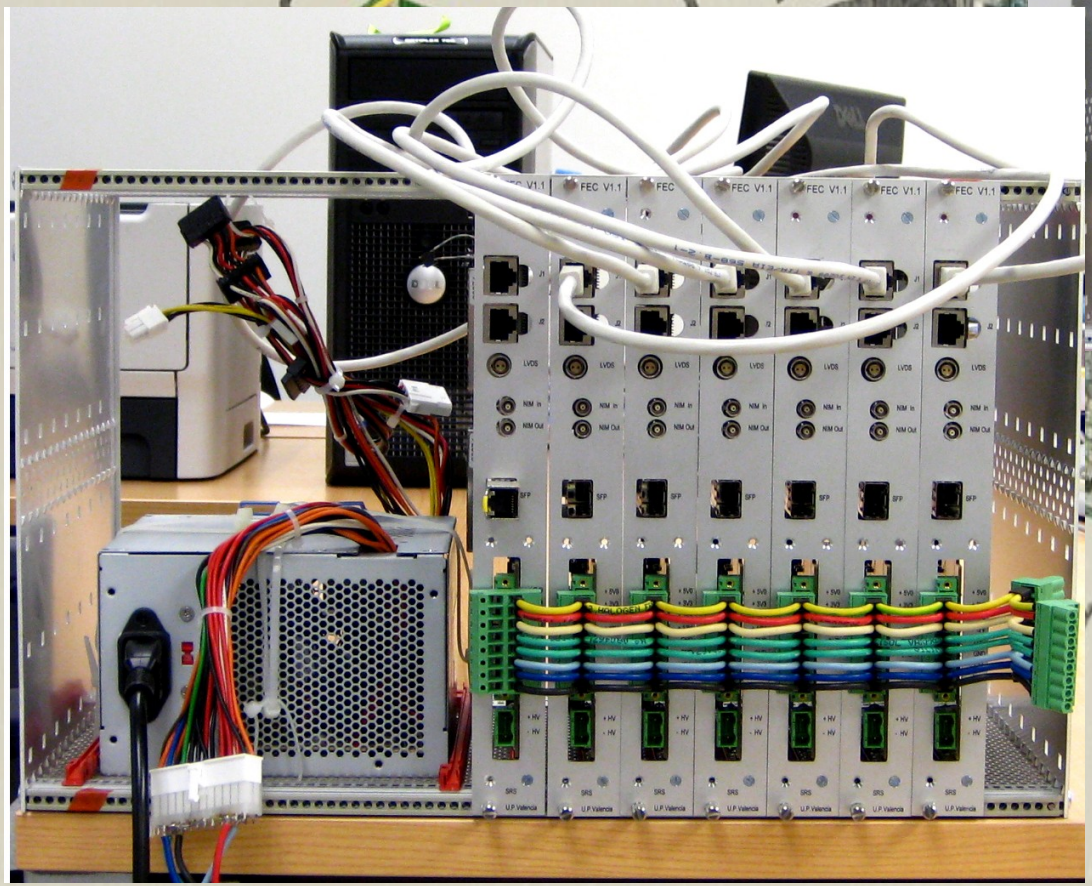
IMPORTANT for 10x10 standard GEMS: ask Rui for a modified frame

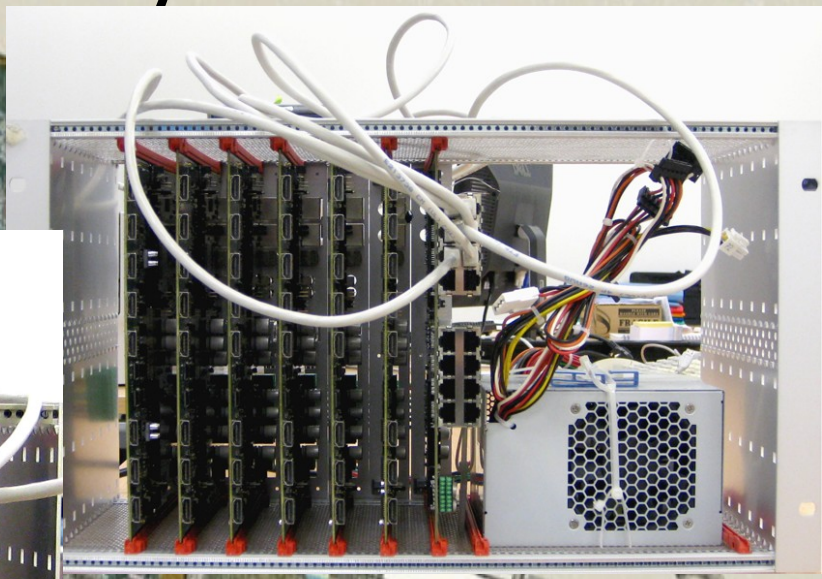
Flat cable 4 inch
Samtec FFSD-08-D0401N

Master-Slave configuration:
1 HDMI cable= 2 hybrids

Medium-sized SRS systems

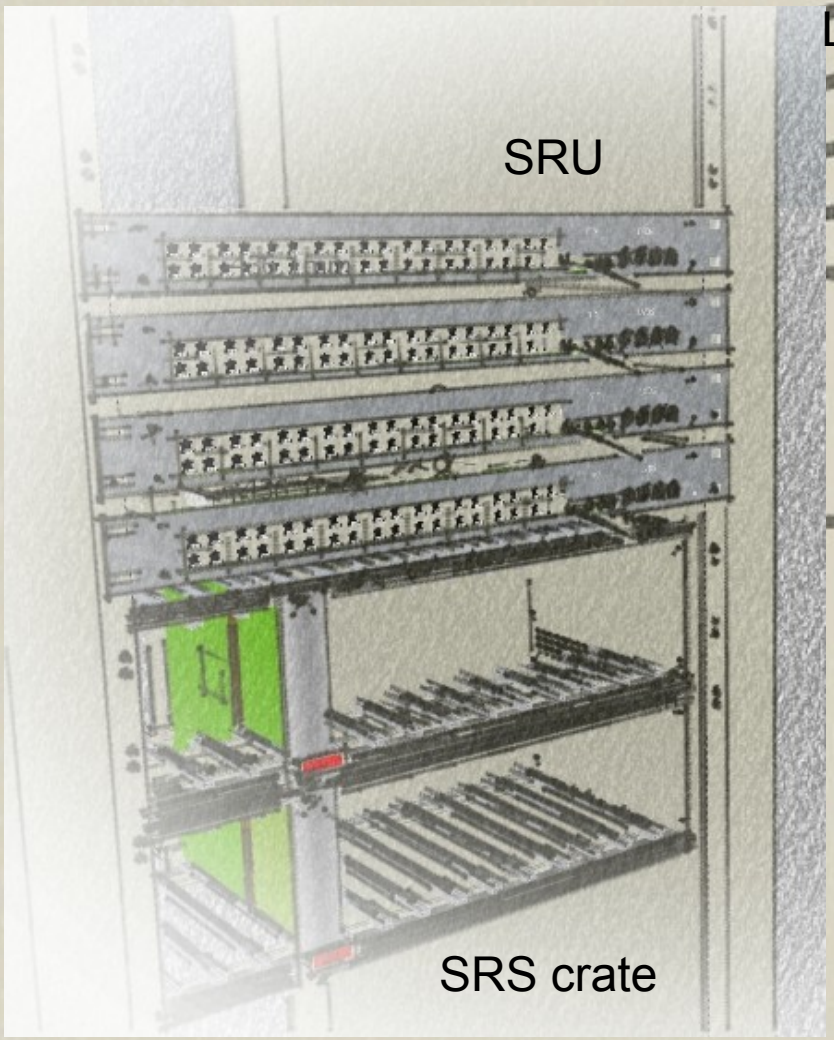
Photo: SRS crate NEXT collaboration



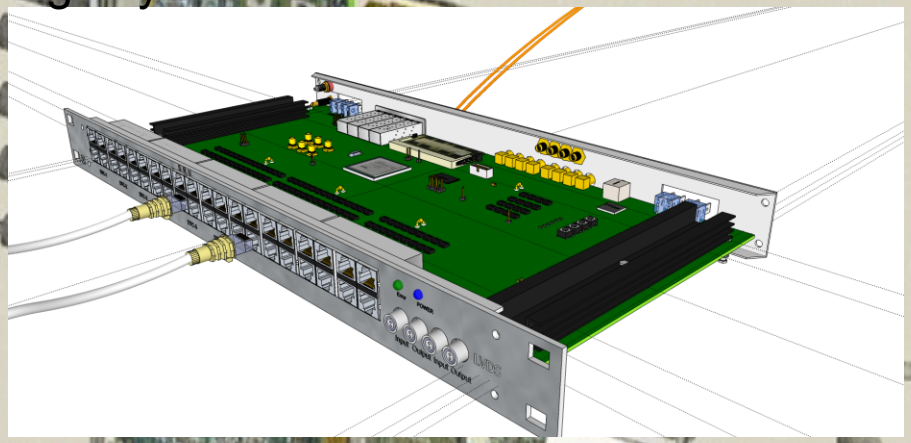


7 FEC & ADC cards
in an ATX-powered crate

Towards Large SRS systems



Large systems > 16 k channels need this box:



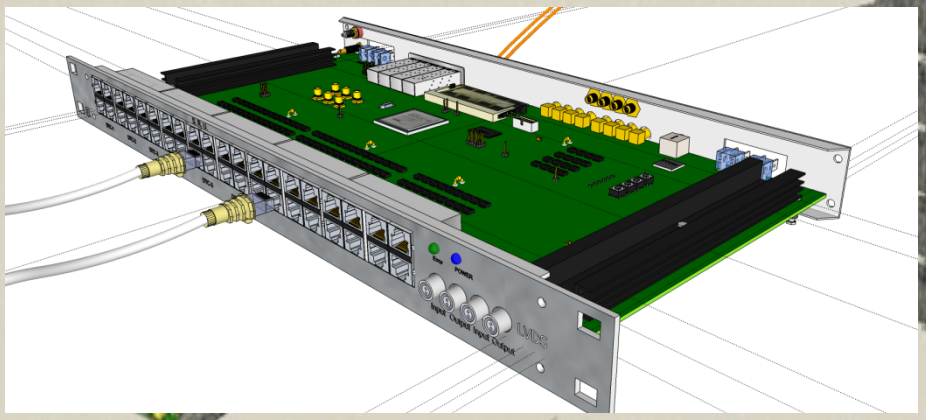
Scalable Readout Unit (SRU)

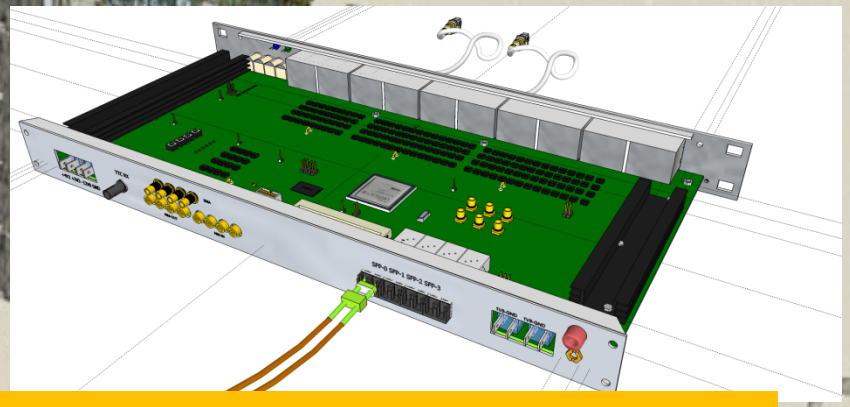
SRU groups units of
40 FEC cards (84k channels)
into a **10 Gbit Ethernet readout cluster**

Left side: Rack mounted system with
4 readout clusters (335 k channels)

SRU design effort 2010

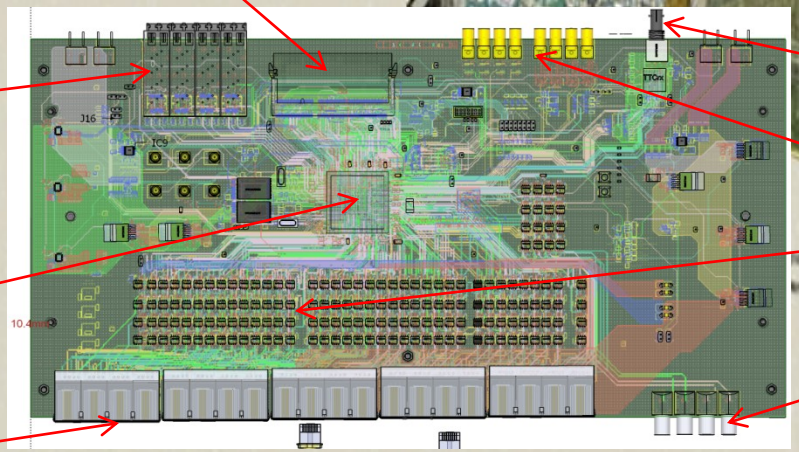
Schematic co-design Cadence: Sorin Martoiu + Fan Zhang, PCB Layout: Intrasys Inc. , Component Mounting Firstec SA
PCB outlines and chassis mechanical: Google Sketchup Pro8 and Layout 3 by H.Muller





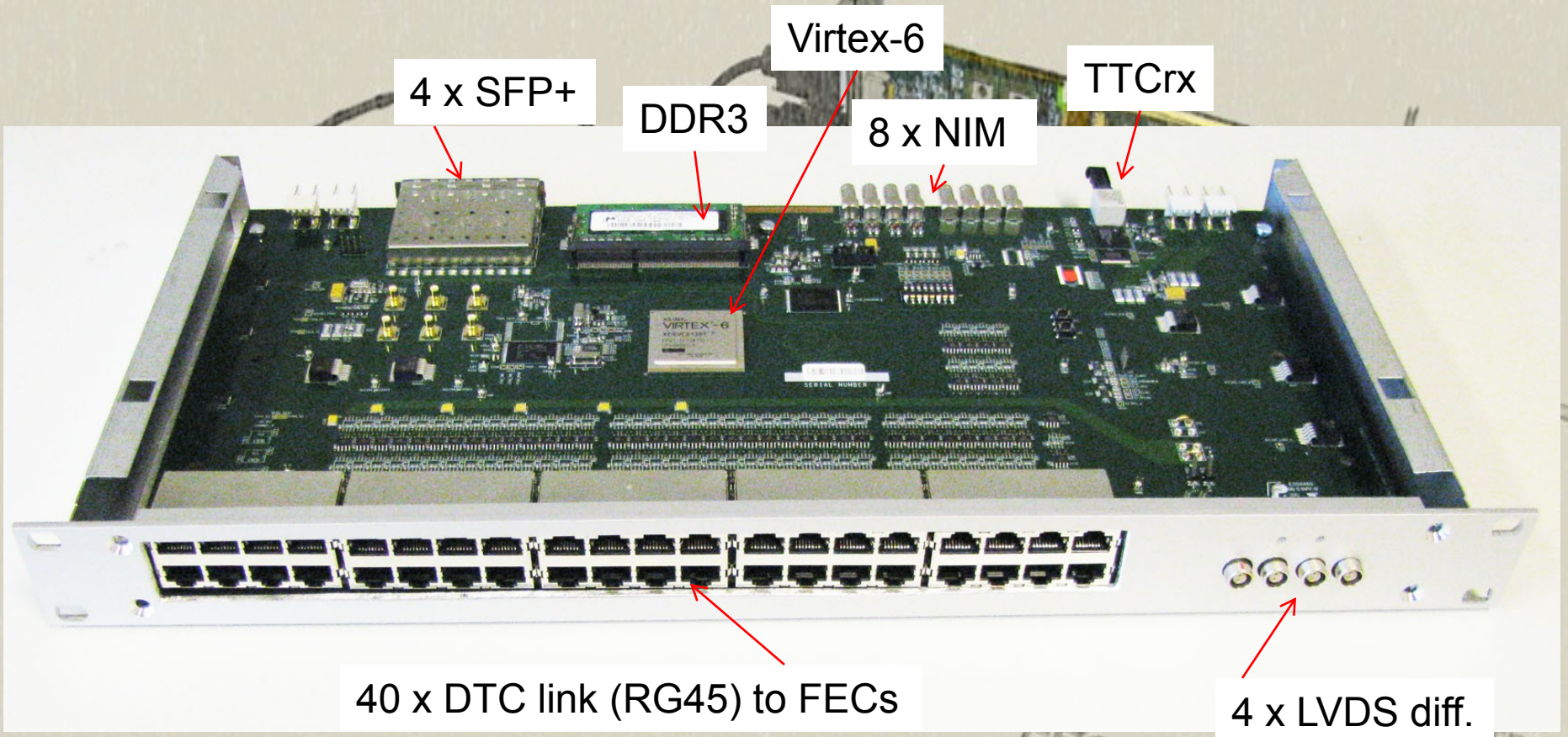
Front side:
40 DTC links

Back side:
GbEthernet 4x, Power, TTCrx, Trigger



1st SRU box

(status 15 Jan. 2011)

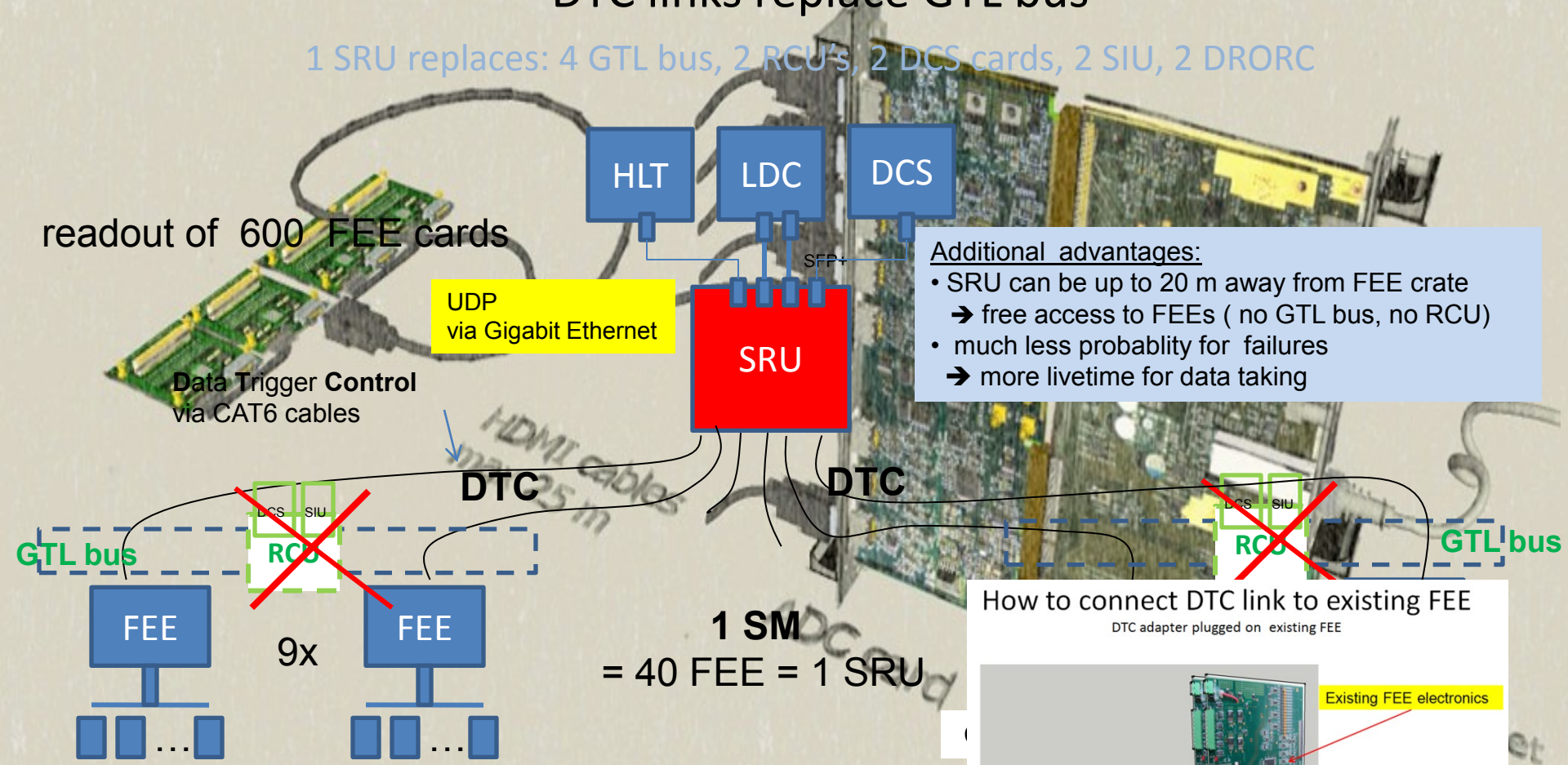


25 SRU's ready for production by Firstec
2 SRU's under power / test

1st SRU user: readout backend of Alice EMCaL/DCaL

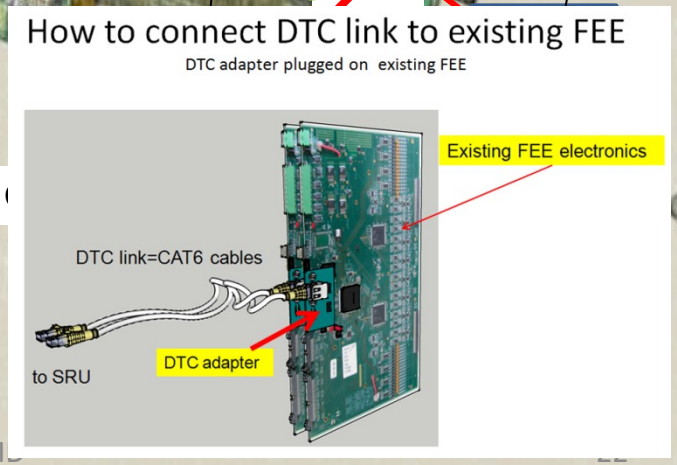
DTC links replace GTL bus

1 SRU replaces: 4 GTL bus, 2 RCU's, 2 DCS cards, 2 SIU, 2 DRORC



Additional advantages:

- SRU can be up to 20 m away from FEE crate
  ➔ free access to FEEs (no GTL bus, no RCU)
- much less probablity for failures
  ➔ more livetime for data taking



Work on DTC link for EMCal: Fan Zhang
➔Generic DTC link for SRS to be adressed

Power for SRS

ATX Power => SRS Adapter => SRS

ATX power up 1 kW very cheap (but noisy)

➔ SRS ATX adapter adds EMI filtering and more Voltages

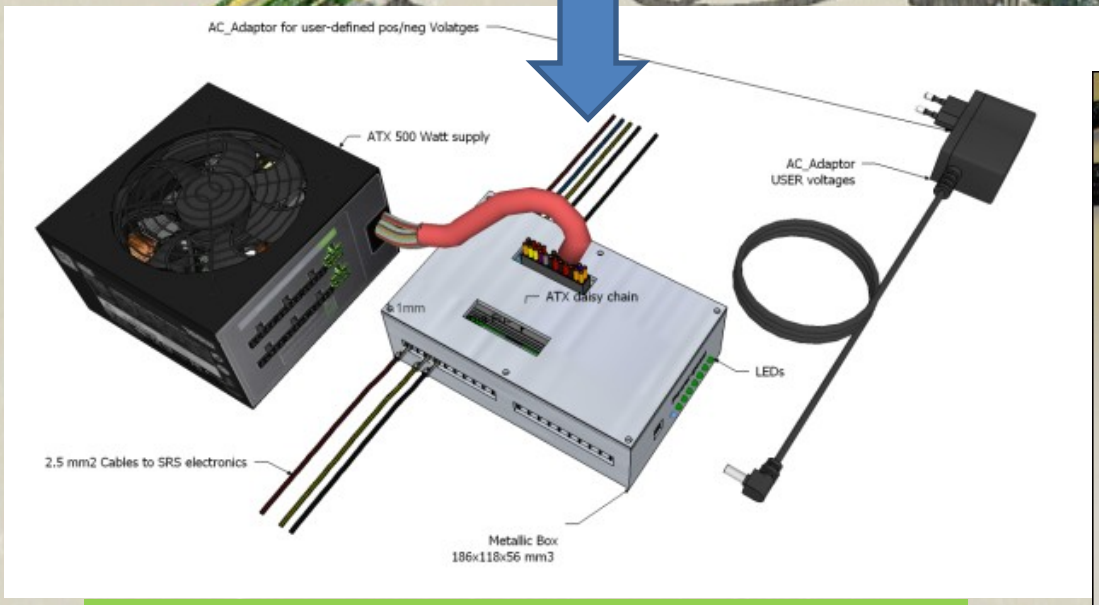
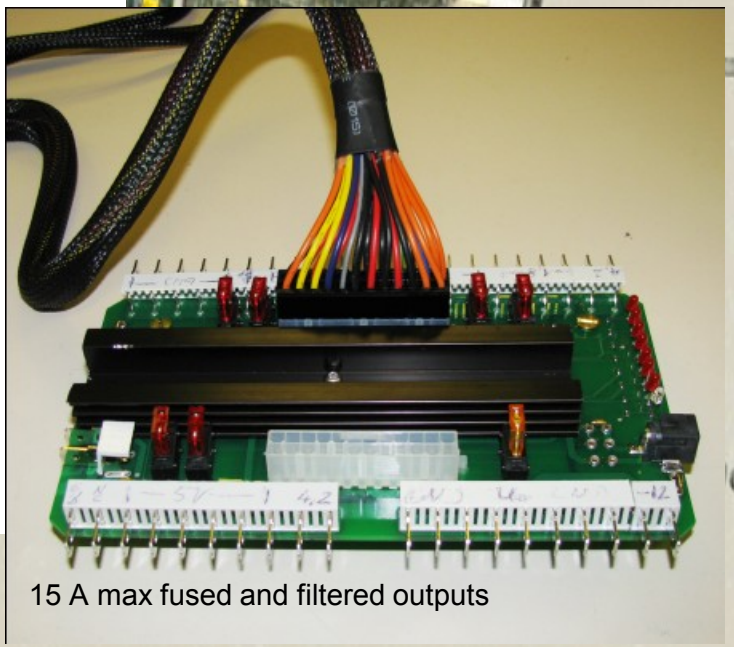


Photo 1st ATX adapter

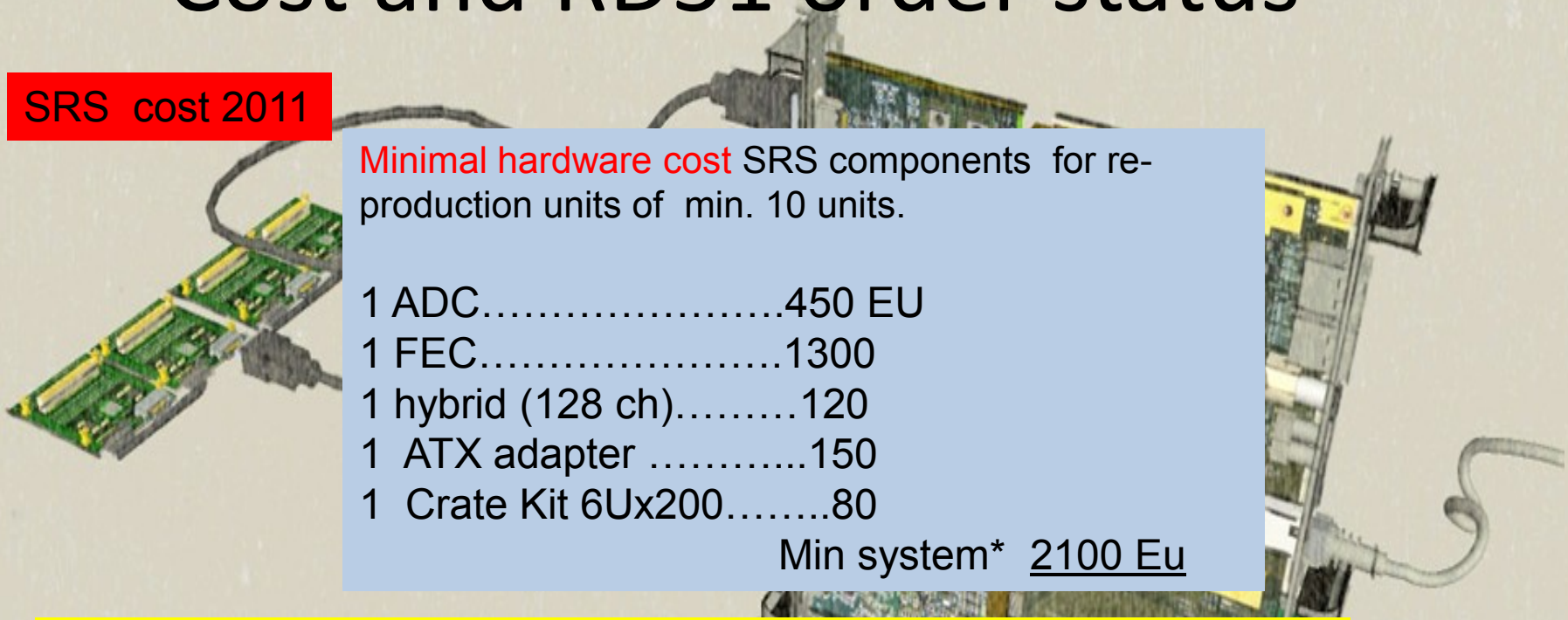


15 A max fused and filtered outputs

1st ATX adapters in use by ATLAS MM more in production

Cost and RD51 order status

SRS cost 2011



Minimal hardware cost SRS components for re-production units of min. 10 units.

1 ADC…….450 EU
1 FEC…….1300
1 hybrid (128 ch)……120
1 ATX adapter ……...150
1 Crate Kit 6Ux200……..80

Min system* 2100 Eu

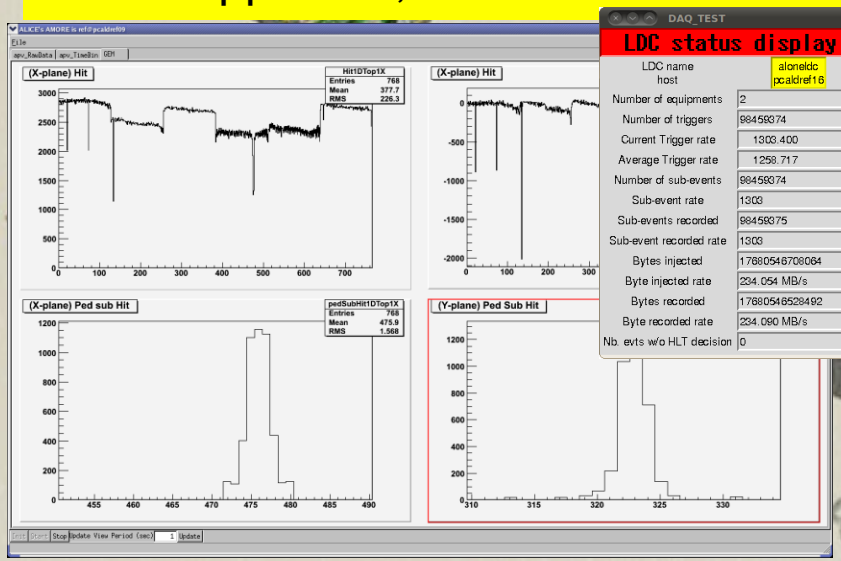
More than 30 FEC, 30 ADC and 280 hybrids
on order, becoming a logistic problem for SRS team
→transfer of SRS hardware to commercial production is aimed for
→ 1st industry contacts via CERN KTN (ongoing)
→ YOUR national industry contact should contact us

* pure component & production cost, add cables, connectors, computer,

DAQ and monitoring Software for SRS

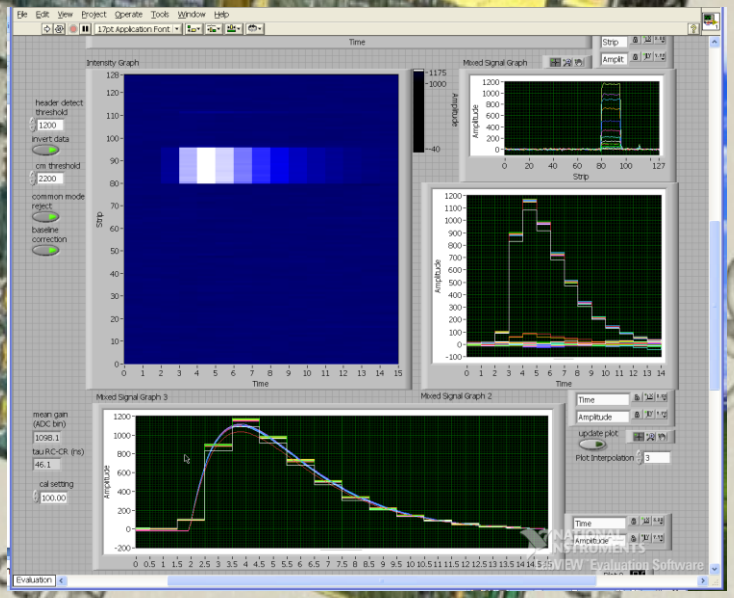
1) DATE[1]/Root/AMORE (DEFAULT):

- full DAQ/monitoring system
- separate slow control
- full supported , MoU with ALICE



2) Labview (under development [2])

- laboratory based
- monitoring and debugging



3) Stand-Alone [3] (ATLAS MM see talk)

- slim DAQ
- no monitoring and debugging

4) Other standard DAQ systems

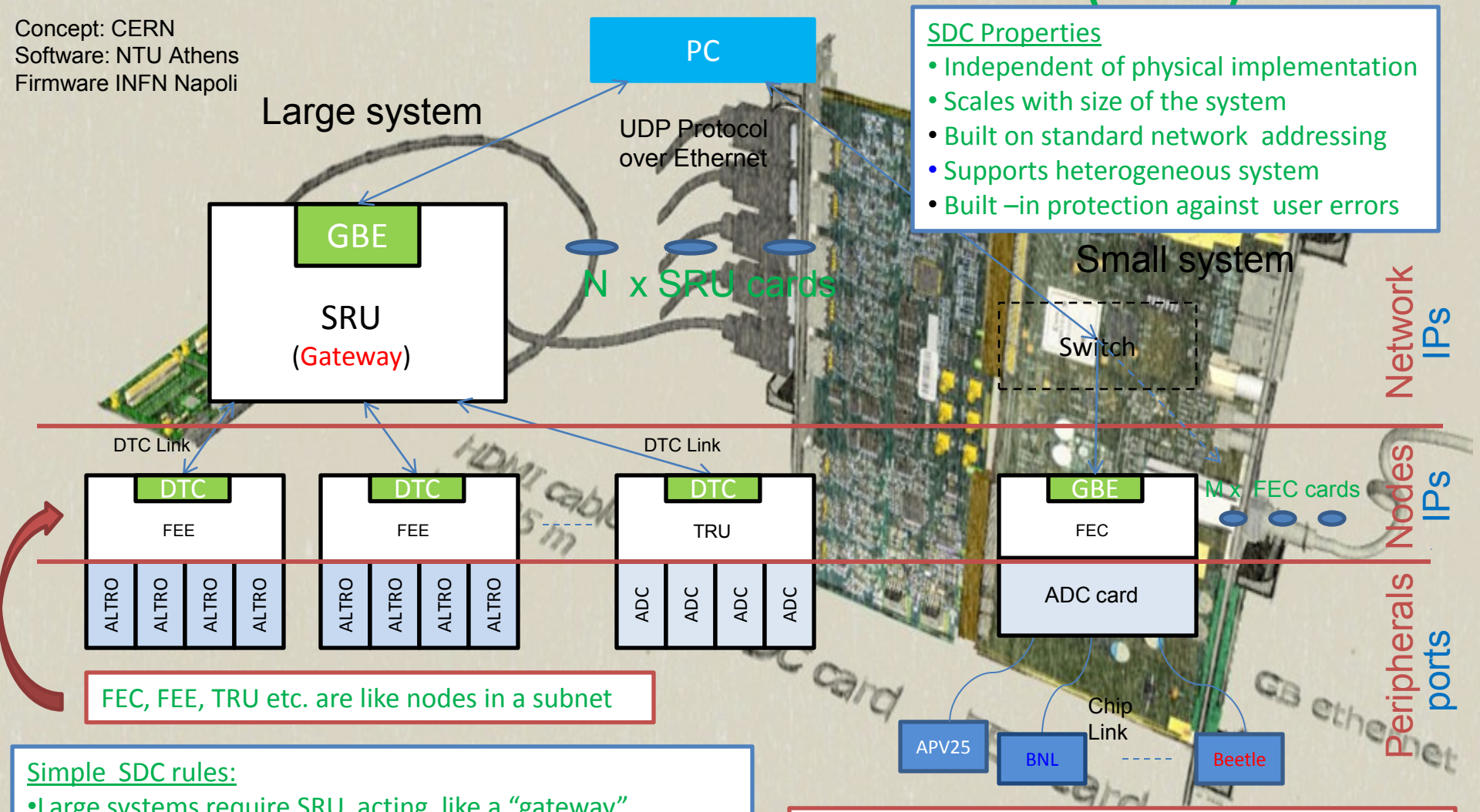
user driven open project

1 CERN ALICE AID group , CERN Root
2 INFN Napoli
3 ATLAS MM (Marcin Byszewski)

New and important

Scalable Detector Controls (SDC)

Concept: CERN
Software: NTU Athens
Firmware INFN Napoli



SDC Properties
- Independent of physical implementation
- Scales with size of the system
- Built on standard network addressing
- Supports heterogeneous system
- Built –in protection against user errors

FEC, FEE, TRU etc. are like nodes in a subnet

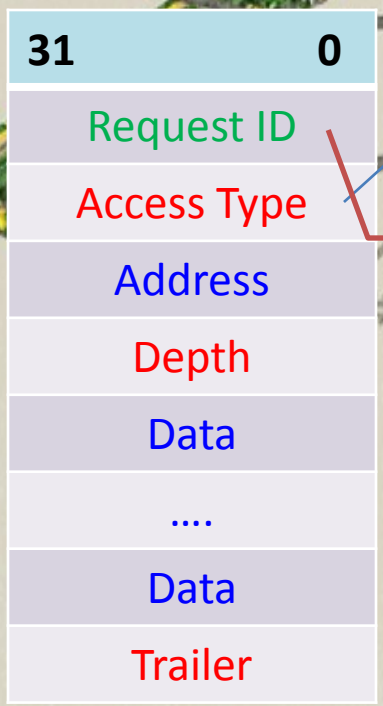
Simple SDC rules:
- Large systems require SRU acting like a "gateway"
- Each connected node (FEE, TRU ..) has its own IP
- Each type of node - peripheral has a unique *port number.*

Node peripherals: are like services on network nodes
- different chips/hybrids /virtual components

Controls Data Format

Available at FEC level from UDP:

Data Format



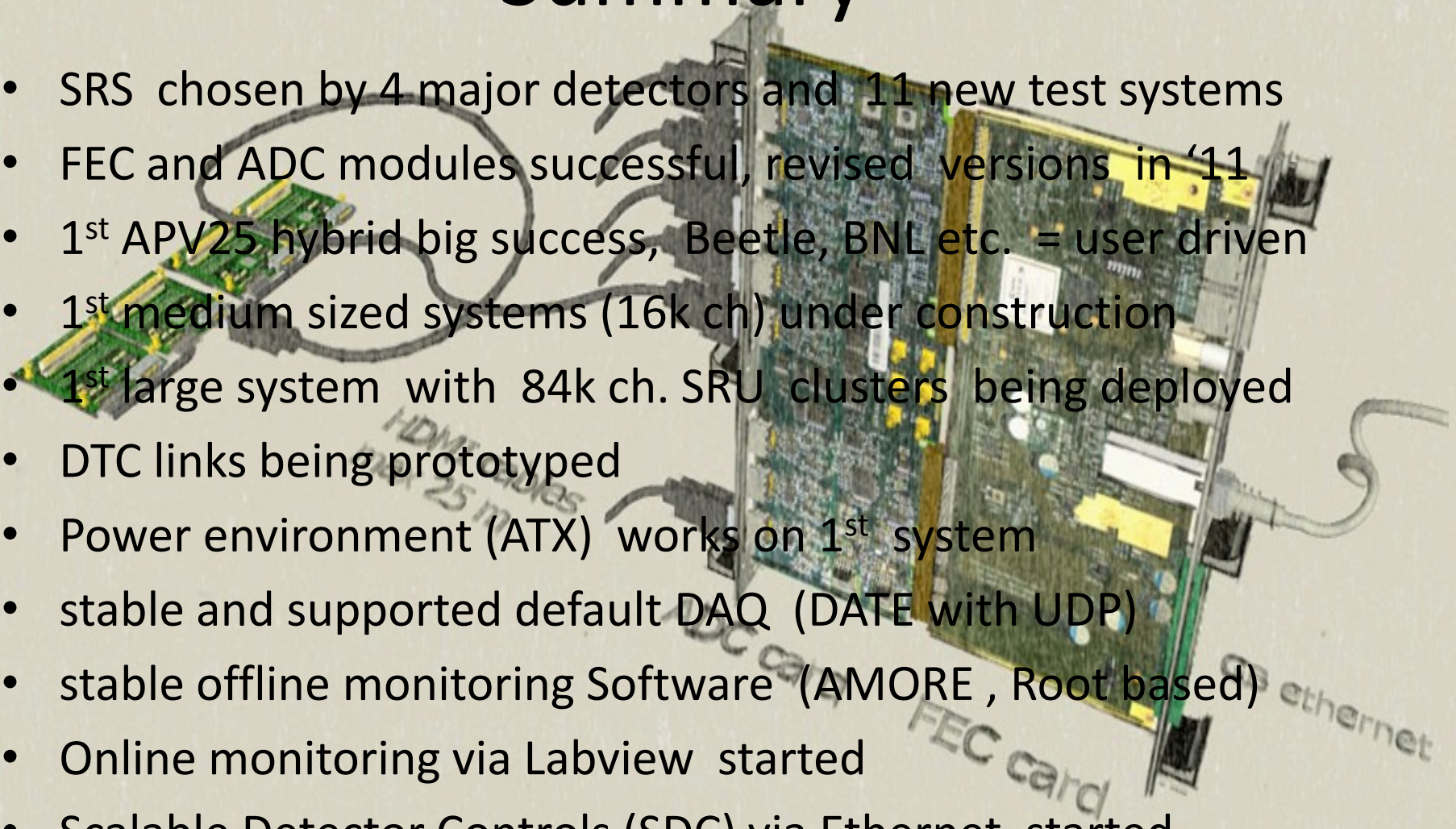
- Access type
  - Write Burst
  - Write Single
  - Read Burst
  - Read Single
  - Broadcast
  - etc

Commands:
RESET, SOR, EOR,…

- Address (According to different applications, 32-bit address could be divided into several areas. (For example: chip addr + reg addr))
  - Single: The register address
  - Burst: The address of the first register to access
- Depth
  - Single: 1
  - Burst: The number of registers to be accessed
- Data
  - The data to be written into the register
- Trailer
  - Checksum or something else

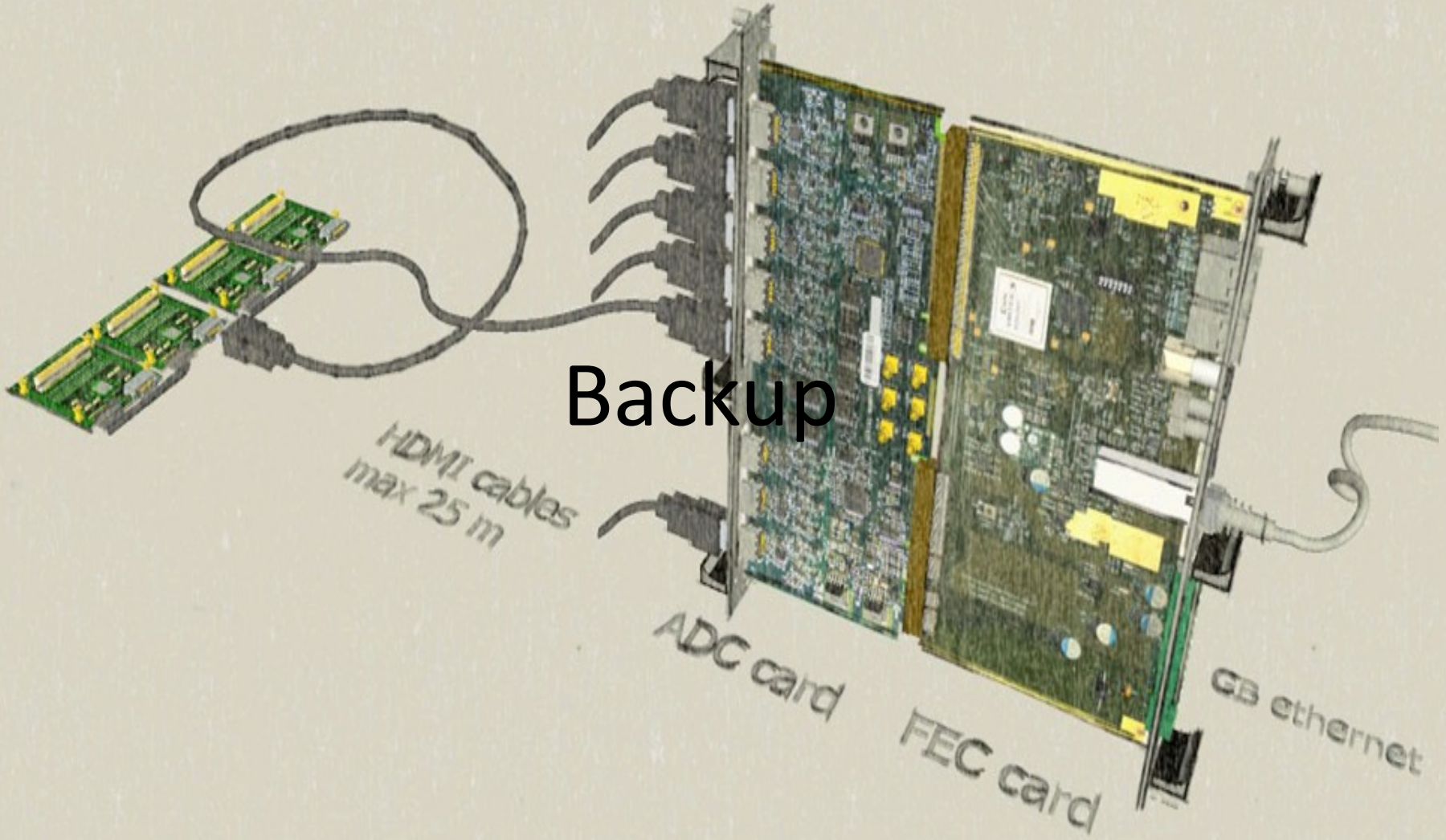
•Request-reply matching mechanism;
•The reply will contain this ID

Summary

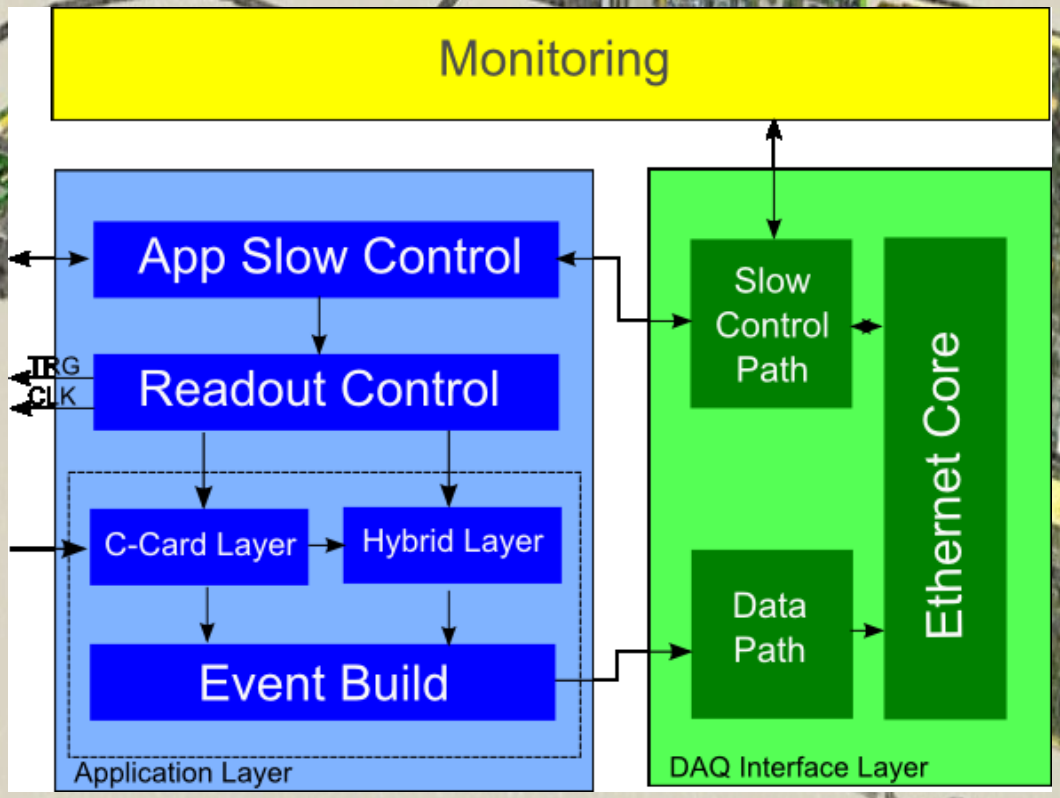


- SRS chosen by 4 major detectors and 11 new test systems
- FEC and ADC modules successful, revised versions in ‘11
- 1st APV25 hybrid big success, Beetle, BNL etc. = user driven
- 1st medium sized systems (16k ch) under construction
- 1st large system with 84k ch. SRU clusters being deployed
- DTC links being prototyped
- Power environment (ATX) works on 1st system
- stable and supported default DAQ (DATE with UDP)
- stable offline monitoring Software (AMORE , Root based)
- Online monitoring via Labview started
- Scalable Detector Controls (SDC) via Ethernet started

Backup



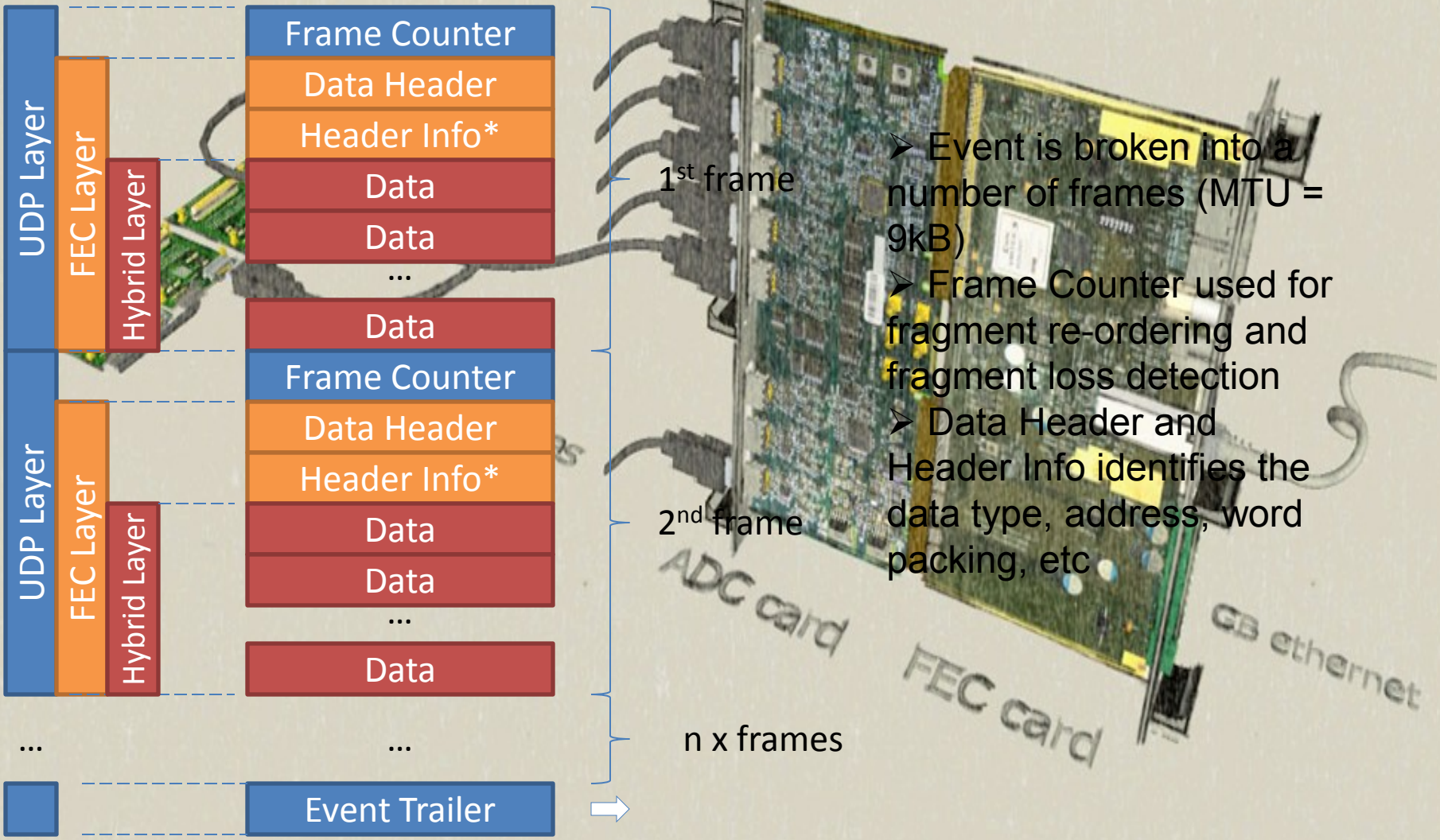
SRS Firmware



Open applications for SRS developers

SRS Core firmware

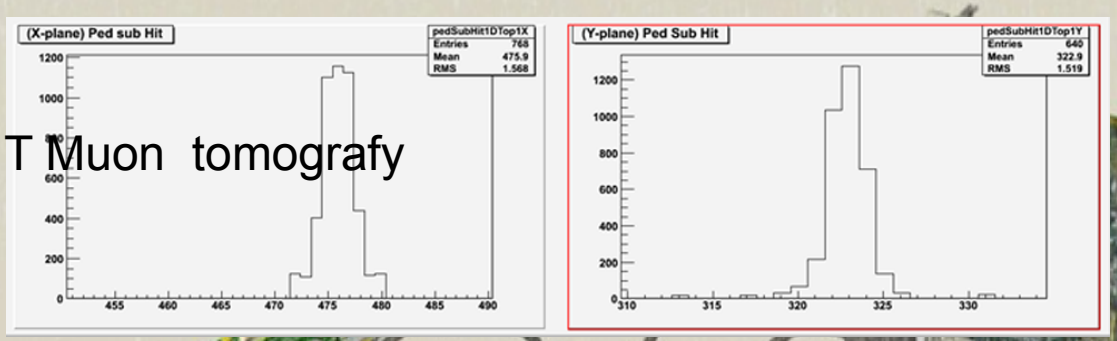
SRS UDP data protocol

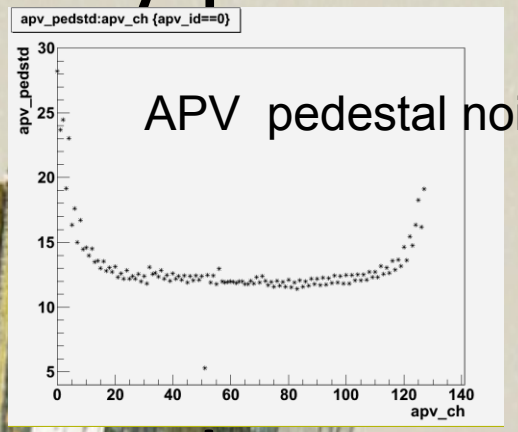


- Event is broken into a number of frames (MTU = 9kB)
- Frame Counter used for fragment re-ordering and fragment loss detection
- Data Header and Header Info identifies the data type, address, word packing, etc

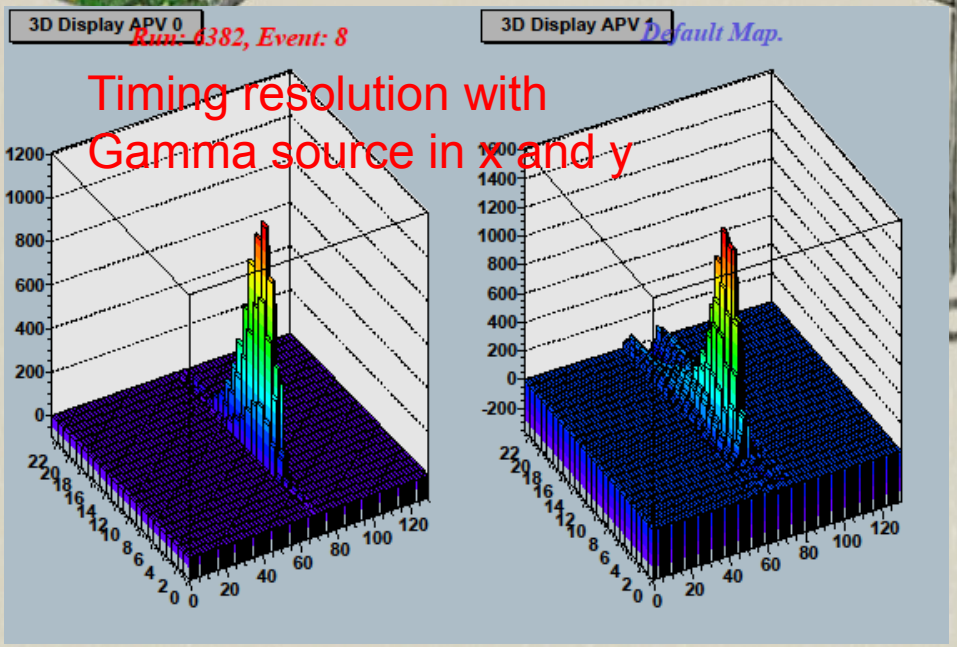
SRS Cosmic event on GEM x-y planes

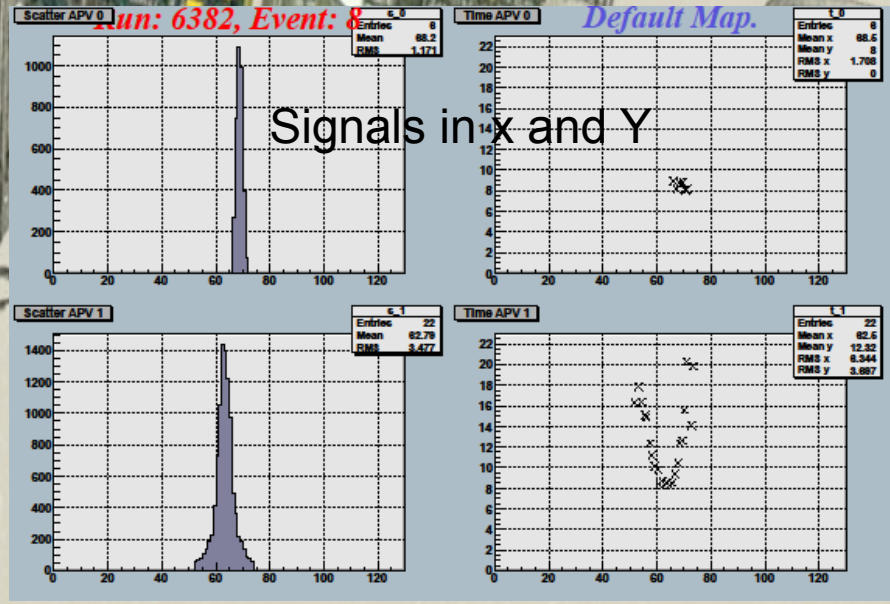
FIT Muon tomografy



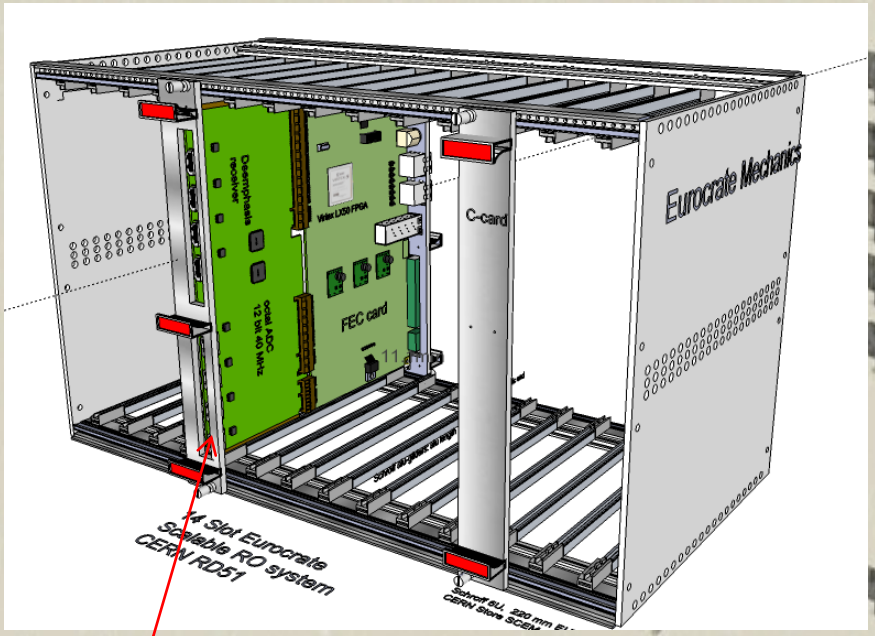


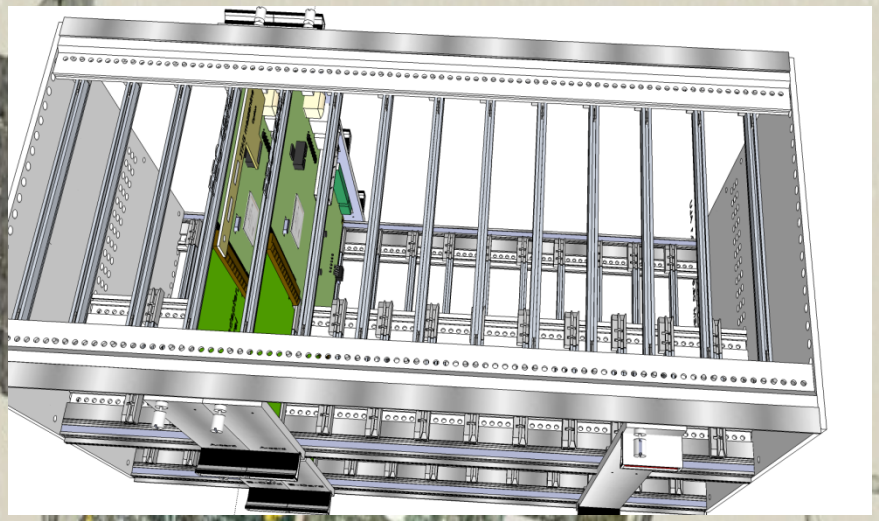
SRS: Atlas MicroMegas x-y planes





Crate and power

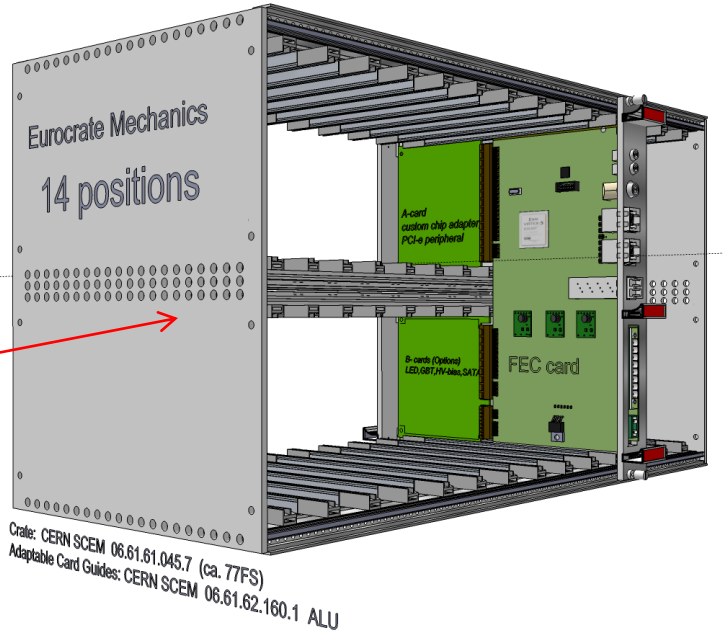




Chassis: 6U x 220 mm Eurocrate

Chassis 6U x 220, KIT CERN SCEM SCEM 06.61.61.045.7

Fabricant ATOS http://www.atos-racks.com/fiche,ferroviaire,78.html

C-card adapters = 6U cards

A +B cards = 3U dividing bar