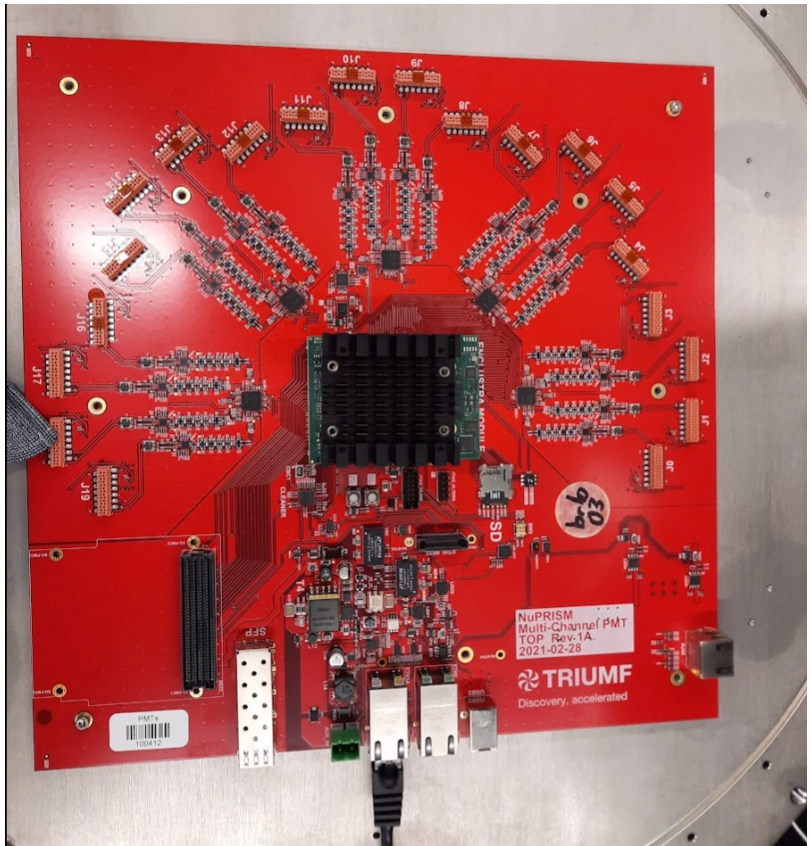
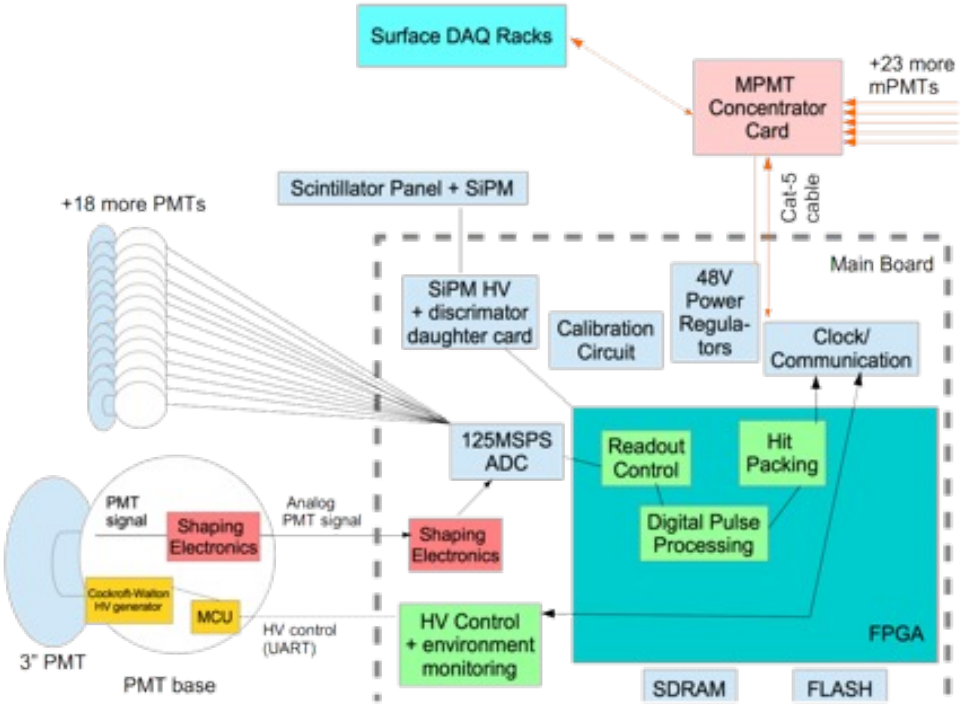
Canadian Electronics Status

T. Lindner

mPMT Electronics Overview

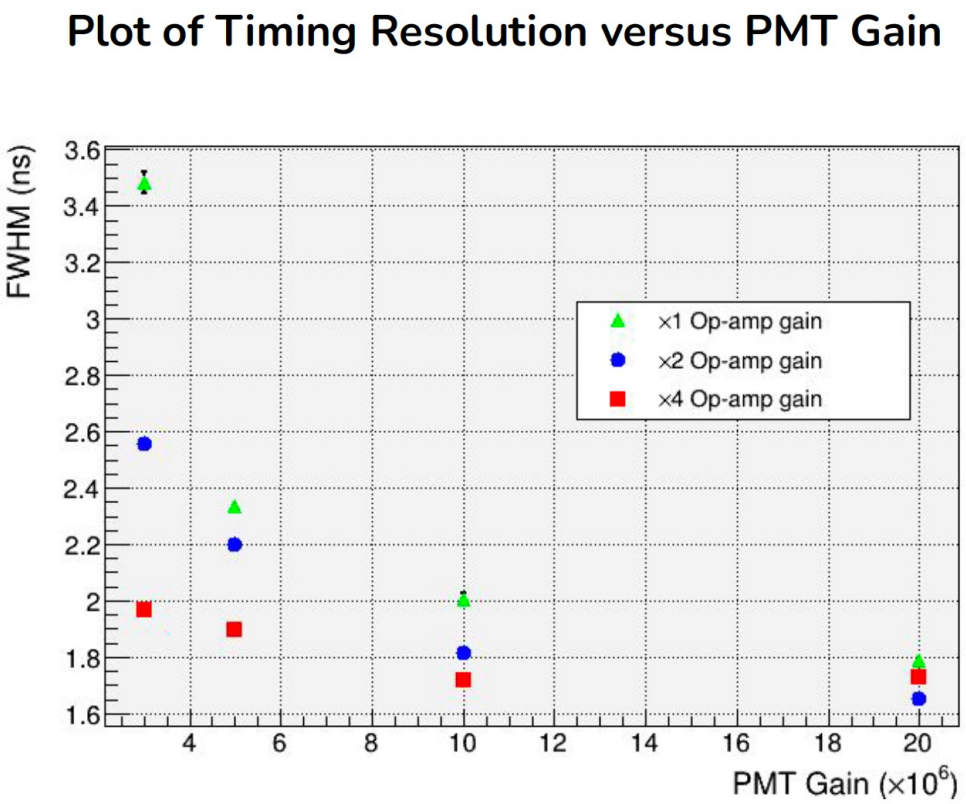
- PMT signal digitization using 125MHz ADC, with pulse finding and feature extraction in FPGA.
- PMT power generated on PMT base with Cockroft-Walton circuit.
- Single cat-5 network cable connected to mPMT mainboard, provides power/communication/clock/trigger.





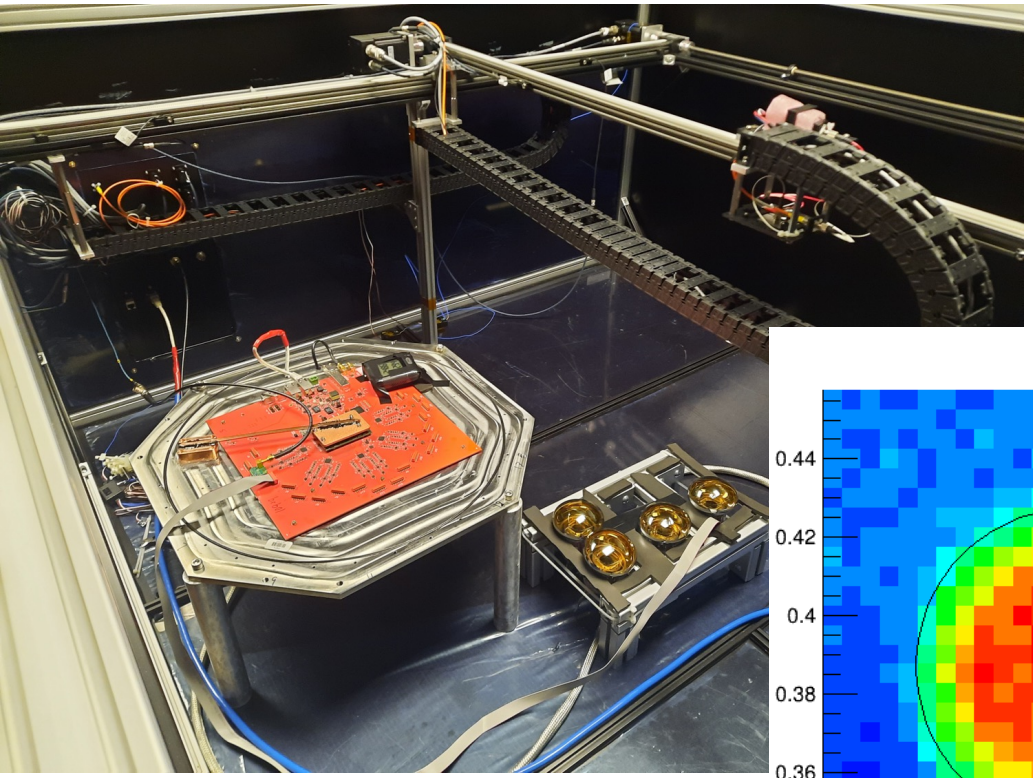
Timing Resolution Measurement

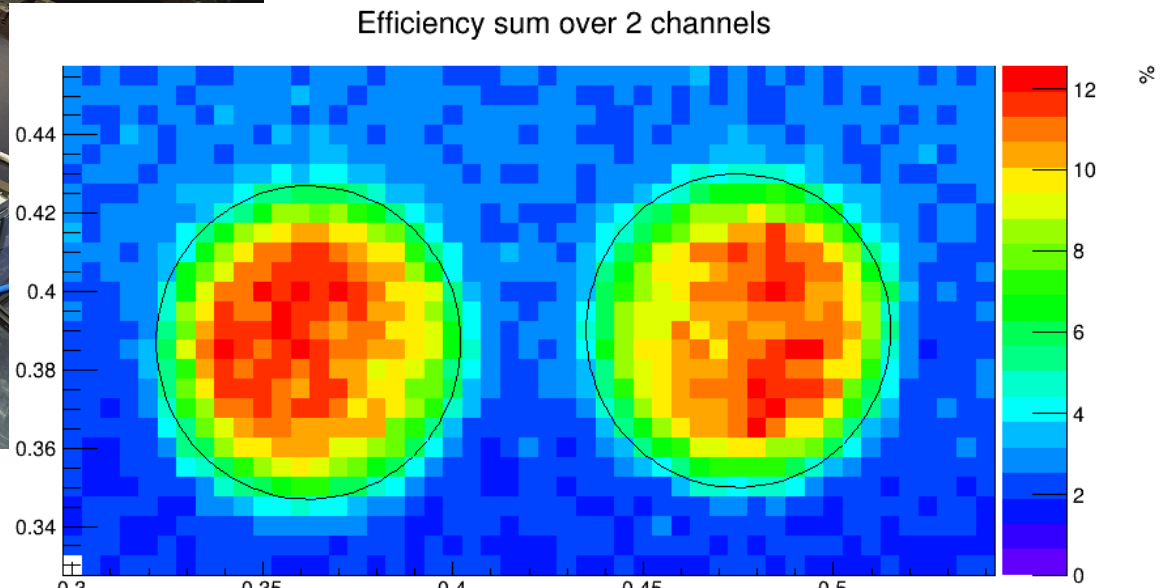
- Restarted measurements of timing resolution to help finalize shaping circuit design and dynamic range choice.
- Measuring timing resolution for different PMT gain and amplifier gain.
- Want to disentangle intrinsic PMT dependence of TTS on gain vs worsening TTS because of lower signal to noise.
- Need to finalize choice of PMT gain and shaping circuit within next 2-3 months



TRIUMF Test Stand

- Have a 2D gantry system at TRIUMF for scanning pulsed LED across photosensor. Test stand being commissioned.
- Plan to use it for both individual PMTs and assembled mPMT
- So far have made scans with two PMTs.





Integration mPMT Tests

- Now starting tests with an assembled mPMT (16 PMTs) in test stand.
- First step is just turning all PMTs and equalizing gain.
- Have found two worrisome problems so far
  1. One of the PMTs has ‘gone bad’
     - symptoms of ‘bad ‘PMT are
       - High current: ~16uA of HV
       - Measured voltage doesn’t match setpoint voltage
       - No PMT pulses seen
     - This is third PMT PMT that has gone bad. Have send two of the bad PMTs to Poland for testing
  2. Bad PMT seems to be causing the mainboard itself to turn off. Don’t understand why yet. To be investigated more.

Upcoming Xilinx Tests at TRIUMF

- Most of the tests at TRIUMF have been done using mPMT mainboards with Altera FPGA.
- But we are switching to Xilinx FPGAs for the production WCTE mPMTs.
- Between WUT and TRIUMF have solved last problems with the communication between Xilinx FPGAs and the PMT microcontrollers.
- Priority now is doing extensive tests now with mPMTs + PMTs with Xilinx FPGAs.
  - This will be final key tests before we are ready for the mainboard mass production
- The 100 production Xilinx FPGAs have arrived at TRIUMF and WUT.

Status of Mainboard Component Purchase and Delivery

- We are purchasing and receiving components for a pre-production of mPMT mainboards (QTY=4) and production mainboards (QTY=102).
- Obviously, has been difficult to purchase components.
- TRIUMF engineer has replaced most of the unavailable components.
- We have 11 components which we have ordered, but haven't been delivered yet and a couple components we haven't ordered at all (and all the analog shaping passives)
- Latest stated delivery date for some of the components is Oct 2022.
- R&D needs to finish on several items in order to make final purchases:
  - Analog shaping
  - Finalize light pulser scheme
  - Firmware backup scheme
  - MCC-mPMT Interfaces (clock, trigger, etc)

Mainboard Electronics Schedule

- Need to finish all mainboard R&D in next 3 months
- want to be ready for pre-production mainboard manufacture in Nov 2022 once last components arrive.
- Main production of mainboards in Jan-Apr 2023.

TRIUMF

Backup

TRIUMF

Timing Analysis

PMT gain	Op-amp gain	1PE PH (mV)	Dynamic range	eTTS (FWHM)	Comments
$1x10^7$	4	25	0-40PE	1.727ns	Should be best S/N. Best eTTS? Same eTTS as $2x10^7$. So no effect of electronics timing resolution? Ideal case?
$1x10^7$	2	13.9	0-72PE	1.817ns	eTTS is 5% larger than for op-amp=4 case (ideal?); implied electronics timing resolution: 0.56ns (FWHM)
$1x10^7$	1	7	0-142PE	1.992ns	eTTS is 15% larger than for op-amp=4 case; implied electronics timing resolution: 0.99ns (FWHM)
$5x10^6$	4	13	0-77PE	1.899ns	Same pulse height as $1x10^7$ / op-amp=2 case. So could guess that this configuration has ~5% higher eTTS compared to ideal case.
$5x10^6$	2	6.5	0-155PE	2.184ns	Same pulse height as $1x10^7$ / op-amp=1 case. 15% increase in eTTS compared to $5x10^6$ / op-amp=4. Implied electronics timing resolution of 1.22ns (FWHM) Why worse than $1x10^7$ / op-amp=1 case?

- Currently targeting a choice of PMT gain * op-amp gain that gives 0-70PE of dynamic range. Electronics timing resolution seems acceptable at this S/N.

Bad PMT killing mainboard

- Have found that the bad PMT in integration mPMT is causing some failure that is causing mainboard to reboot.
- Slowed down PMT ramp rate and checked currents (in uA). Can see current steadily rising until mainboard reboots.
- Power measured by POE switch confirms that the mainboard reboots and then recovers.
- Daryl doesn't understand problem and is concerned; needs investigating!