Opportunities in vertexing and tracking

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UK meeting on future e+e- Higgs/EW/top/... Factory

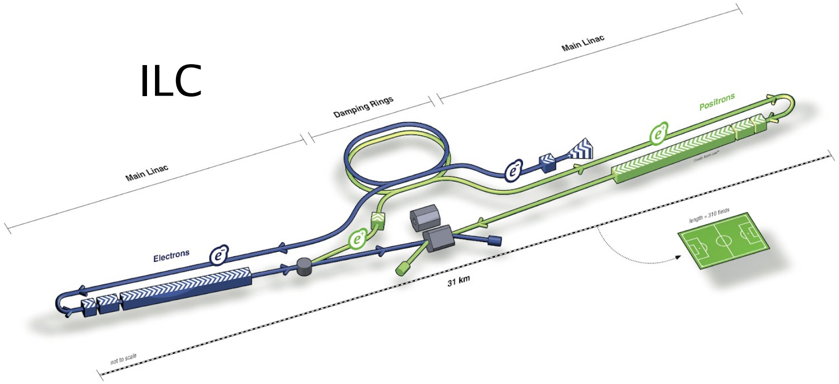
Oxford, 5 July 2022

Outline

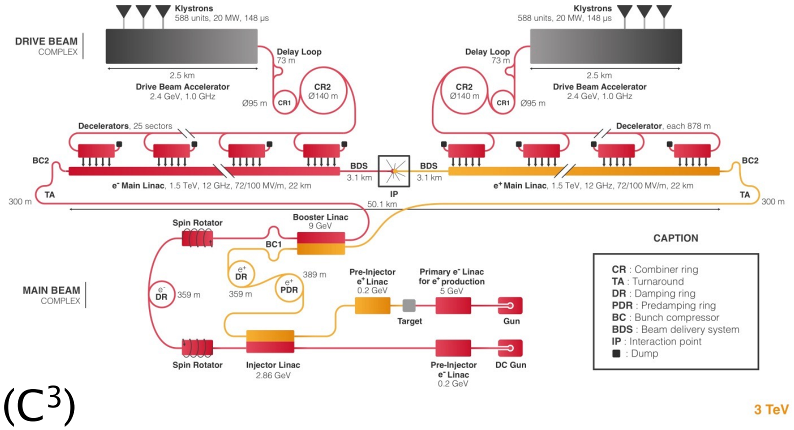
- Tracking and vertex requirements for future e+e- colliders
- Existing detector concepts
- Technology roadmap
- Discussion on opportunities for the UK

Future e$^+$e$^-$ colliders

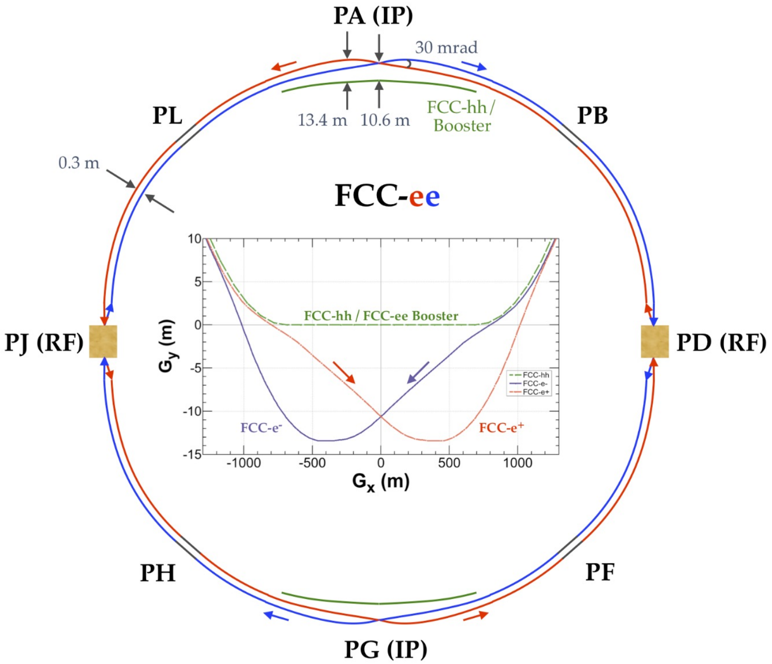
ILC

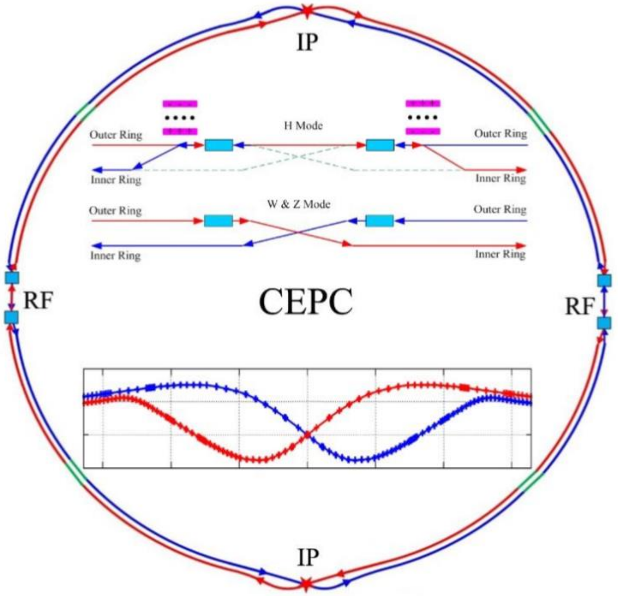


CLIC



Cool Copper Collider (C^3)





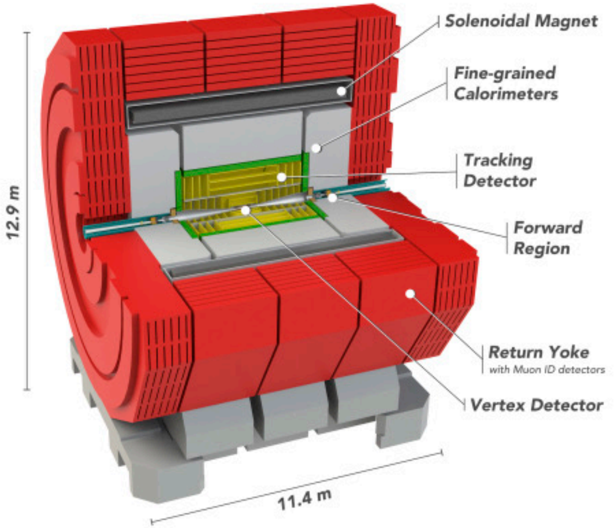
Requirements for Vertex and Tracking Detectors

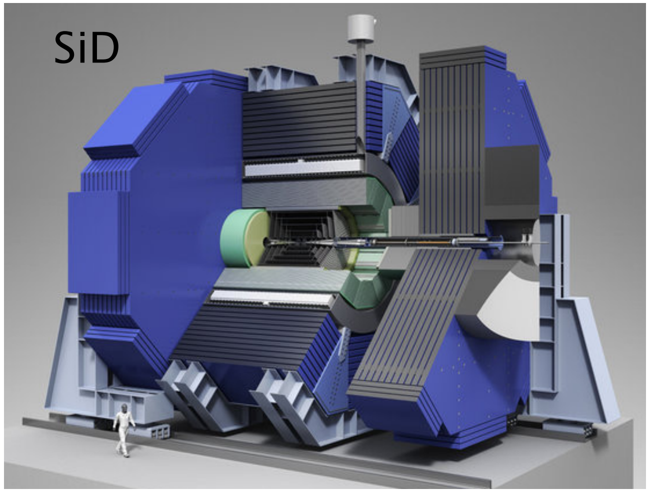
"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				< 2030					2030-2035					2035 - 2040	2040-2045		> 2045		
				Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 [1]	ALICE 3	LHCb ($\gtrsim$LS4) [1]	ATLAS/CMS ($\gtrsim$ LS4) [1]	EIC	LHeC	ILC [2]	FCC-ee	CLIC [2]	FCC-hh	FCC-eh	Muon Collider
Vertex Detector [3]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)		≃ 5		≲ 5	≃ 3	≲ 3	≲ 10	≲ 15	≲ 3	≃ 5	≲ 3	≲ 3	≲ 3	≃ 7	≃ 5	≲ 5
			X/X$_0$ (%/layer)	≲ 0.1	≃ 0.5	≃ 0.5	≲ 0.1	≃ 0.05	≃ 0.05	≃ 1		≃ 0.05	≲ 0.1	≃ 0.05	≃ 0.05	≲ 0.2	≃ 1	≲ 0.1	≲ 0.2
			Power (mW/cm^2)		≃ 60			≃ 20	≃ 20			≃ 20		≃ 20	≃ 20	≃ 50			
			Rates (GHz/cm^2)		≃ 0.1	≃ 1	≲ 0.1		≲ 0.1	≃ 6		≲ 0.1	≃ 0.1	≃ 0.05	≃ 0.05	≃ 5	≃ 30	≃ 0.1	
			Wafers area (") [4]					12	12			12			12		12		12
		DRDT 3.2	Timing precision σ_t (ns) [5]	10		≲ 0.05	100		25	≲ 0.05	≲ 0.05	25	25	500	25	≃ 5	≲ 0.02	25	≲ 0.02
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							≃ 6	≃ 2						≃ 10^2		
			Radiation tolerance TID (Grad)							≃ 1	≃ 0.5						≃ 30		
Tracker [6]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)						≃ 6	≃ 5		≃ 6	≃ 6	≃ 6	≃ 6	≃ 7	≃ 10	≃ 6	
			X/X$_0$ (%/layer)						≃ 1	≃ 1		≃ 1	≃ 1	≃ 1	≃ 1	≃ 1	≲ 2	≃ 1	
			Power (mW/cm^2)						≲ 100	≃ 100		≲ 100		≲ 100	≲ 100	≲ 150			
			Rates (GHz/cm^2)							≃ 0.16									
			Wafers area (") [4]						12			12		12	12	12	12		12
		DRDT 3.2	Timing precision σ_t (ns) [5]						25	≲ 25		25	25	≲ 0.1	≲ 0.1	≲ 0.1	≲ 0.02	25	≲ 0.02
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							≃ 0.3							≲ 1		
			Radiation tolerance TID (Grad)							≃ 0.25							≲ 1		

https://cds.cern.ch/record/2784893

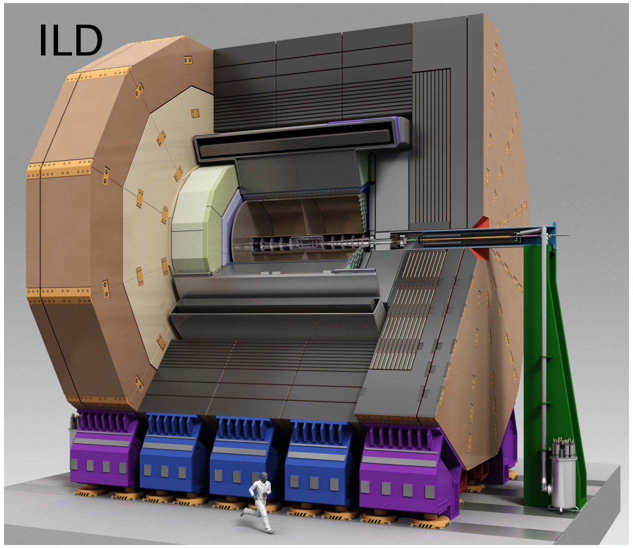
Existing detector concepts for e+e- colliders

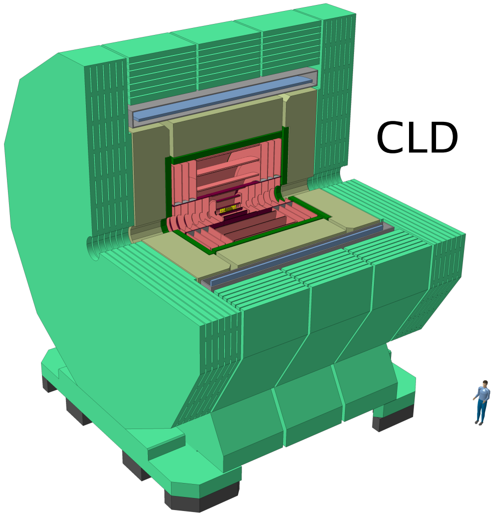
CLIC concept



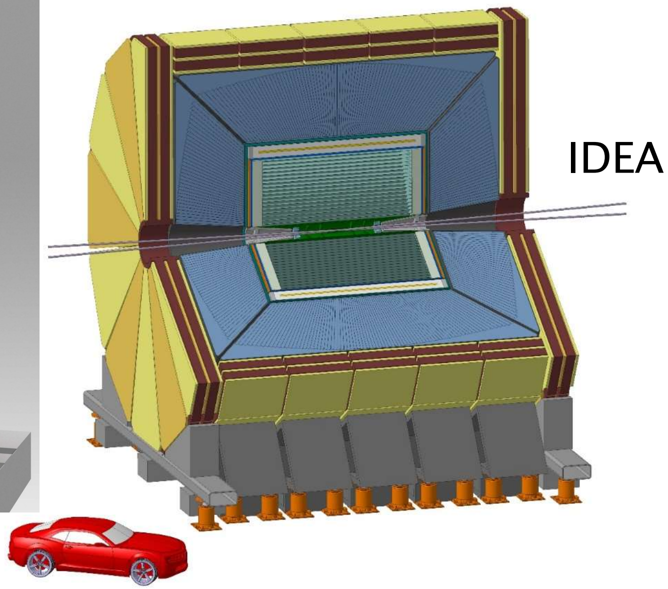


ILC concepts





FCC-ee concepts



Existing detector concepts for e+e- colliders

- Large-volume solenoid, enclosing calorimeters and tracking.
  - Only exception IDEA concept.
  - Smaller B-field, larger tracker outer radius at FCC-ee to retain momentum resolution.

- Highest precision, lowest mass, smaller radius vertex detector.
  - Silicon pixel detectors (MAPS, hybrids).

	ILD	**SiD**	**CLICdet**	**CLD**	**IDEA**	**CEPC**
Vertex technology	Si	Si	Si	Si	Si	Si
Vertex inner radius [cm]	1.6	1.4	3.1	1.75	1.7	1.6
Tracker technology	TPC + Si	Si	Si	Si	Drift chamber + Si	Si
Tracker outer radius [m]	1.77/1.43	1.22	1.5	2.1	2.0	1.8
Calorimeter	PFA	PFA	PFA	PFA	Dual readout	PFA
Solenoid field [T]	3.5/4	5	4	2	2	3
Solenoid length [m]	7.9	6.1	8.3	7.4	6.0	8.0
Solenoid inner radius [m]	3.42/3.08	2.6	3.5	3.7	2.1	3.4

Existing detector concepts for e+e- colliders

- Large area, low mass tracking detector.
  - Cost and ease of construction are key drivers for technological development.
  - All silicon (pixel/strip detectors) or silicon + gaseous detectors (TPC, drift chamber).
  - Gas detectors provide low mass, low cost large lever arm coverage with added PID.

	ILD	SiD	CLICdet	CLD	IDEA	CEPC
Vertex technology	Si	Si	Si	Si	Si	Si
Vertex inner radius [cm]	1.6	1.4	3.1	1.75	1.7	1.6
Tracker technology	TPC + Si	Si	Si	Si	Drift chamber + Si	Si
Tracker outer radius [m]	1.77/1.43	1.22	1.5	2.1	2.0	1.8
Calorimeter	PFA	PFA	PFA	PFA	Dual readout	PFA
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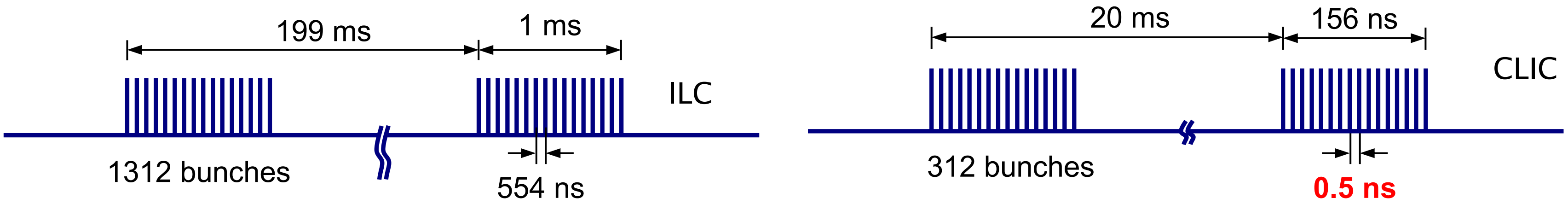
Solenoid inner radius [m]	3.42/3.08	2.6	3.5	3.7	2.1	3.4

Existing detector concepts for e+e- colliders

- Bunch trains (linear) vs. continuous beam (circular).
  - Power pulsing of FE electronics at linear colliders, no need for active cooling (i.e. air cooling can be used) → reduced material.
  - Bunch spacing down to 20 ns at FCC-ee, active cooling required → challenging to meet power management within low mass requirements, cooling studies for low mass, new technology nodes for low power electronics.



	ILD	SiD	CLICdet	CLD	IDEA	CEPC
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Vertex inner radius [cm]	1.6	1.4	3.1	1.75	1.7	1.6
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Calorimeter	PFA	PFA	PFA	PFA	Dual readout	PFA
Solenoid field [T]	3.5/4	5	4	2	2	3
Solenoid length [m]	7.9	6.1	8.3	7.4	6.0	8.0
Solenoid inner radius [m]	3.42/3.08	2.6	3.5	3.7	2.1	3.4

Existing detector concepts for e+e- colliders

- Beam-induced backgrounds more challenging at linear colliders.
  - CLIC 3TeV worse case: largest vertex detector inner radius; up to 8.8 hits/mm^2/train; 0.5 ns bunch spacing results in out-of-time pile-up, ns-level timing needed.

- Extremely high luminosities at FCC-ee (Z pole).
  - High statistical precision requires control of systematics down to 10^{-5} level → significant implications for the design of a stable and lightweight mechanical support.

	ILD	SiD	CLICdet	CLD	IDEA	CEPC
Vertex technology	Si	Si	Si	Si	Si	Si
Vertex inner radius [cm]	1.6	1.4	3.1	1.75	1.7	1.6
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Tracker outer radius [m]	1.77/1.43	1.22	1.5	2.1	2.0	1.8
Calorimeter	PFA	PFA	PFA	PFA	Dual readout	PFA
Solenoid field [T]	3.5/4	5	4	2	2	3
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Solenoid inner radius [m]	3.42/3.08	2.6	3.5	3.7	2.1	3.4

Technology development

- The existing vertex and tracking detector concepts are based on R&D prototype technologies (or extrapolations from state-of-the-art detectors).
- Many years of development of detector technologies for e+e- colliders provide solutions that meet some but not all key requirements.
- R&D (following the ECFA roadmap) is needed to meet all requirements and to further improve performance.
- For solid state detectors:

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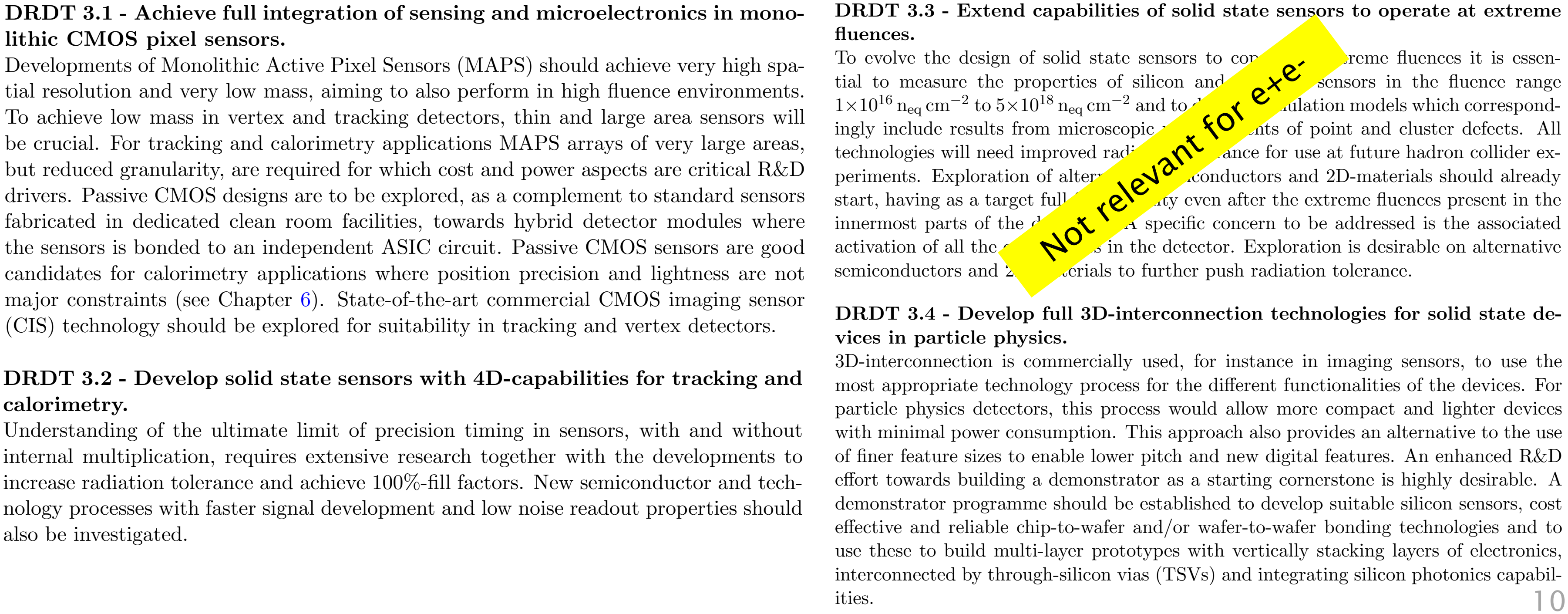

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass, aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity, are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors fabricated in dedicated clean room facilities, towards hybrid detector modules where the sensors is bonded to an independent ASIC circuit. Passive CMOS sensors are good candidates for calorimetry applications where position precision and lightness are not major constraints (see Chapter 6). State-of-the-art commercial CMOS imaging sensor (CIS) technology should be explored for suitability in tracking and vertex detectors.

DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
Understanding of the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research together with the developments to increase radiation tolerance and achieve 100%-fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.

DRDT 3.3 - Extend capabilities of solid state sensors to operate at extreme fluences.
To evolve the design of solid state sensors to co[illegible]reme fluences it is essential to measure the properties of silicon and [illegible] sensors in the fluence range $1{\times}10^{16}\,\mathrm{n_{eq}\,cm^{-2}}$ to $5{\times}10^{18}\,\mathrm{n_{eq}\,cm^{-2}}$ and to [illegible]ulation models which correspondingly include results from microscopic [illegible]nts of point and cluster defects. All technologies will need improved radi[illegible]ance for use at future hadron collider experiments. Exploration of alter[illegible]conductors and 2D-materials should already start, having as a target full [illegible]ty even after the extreme fluences present in the innermost parts of the d[illegible] A specific concern to be addressed is the associated activation of all the [illegible]s in the detector. Exploration is desirable on alternative semiconductors and 2[illegible]terials to further push radiation tolerance.

Not relevant for e+e-

DRDT 3.4 - Develop full 3D-interconnection technologies for solid state devices in particle physics.
3D-interconnection is commercially used, for instance in imaging sensors, to use the most appropriate technology process for the different functionalities of the devices. For particle physics detectors, this process would allow more compact and lighter devices with minimal power consumption. This approach also provides an alternative to the use of finer feature sizes to enable lower pitch and new digital features. An enhanced R&D effort towards building a demonstrator as a starting cornerstone is highly desirable. A demonstrator programme should be established to develop suitable silicon sensors, cost effective and reliable chip-to-wafer and/or wafer-to-wafer bonding technologies and to use these to build multi-layer prototypes with vertically stacking layers of electronics, interconnected by through-silicon vias (TSVs) and integrating silicon photonics capabilities.

Technology impact on physics programme

Figure 3.1: Schematic timeline of categories of experiments employing solid state sensors together with DRDTs and R&D tasks. The colour coding is linked not to the intensity of the required effort but to the potential impact on the physics programme of the experiment: Must happen or main physics goals cannot be met (red, largest dot); Important to meet several physics goals (orange, large dot); Desirable to enhance physics reach (yellow, medium dot); R&D needs being met (green, small dot); No further R&D required or not applicable (blank).

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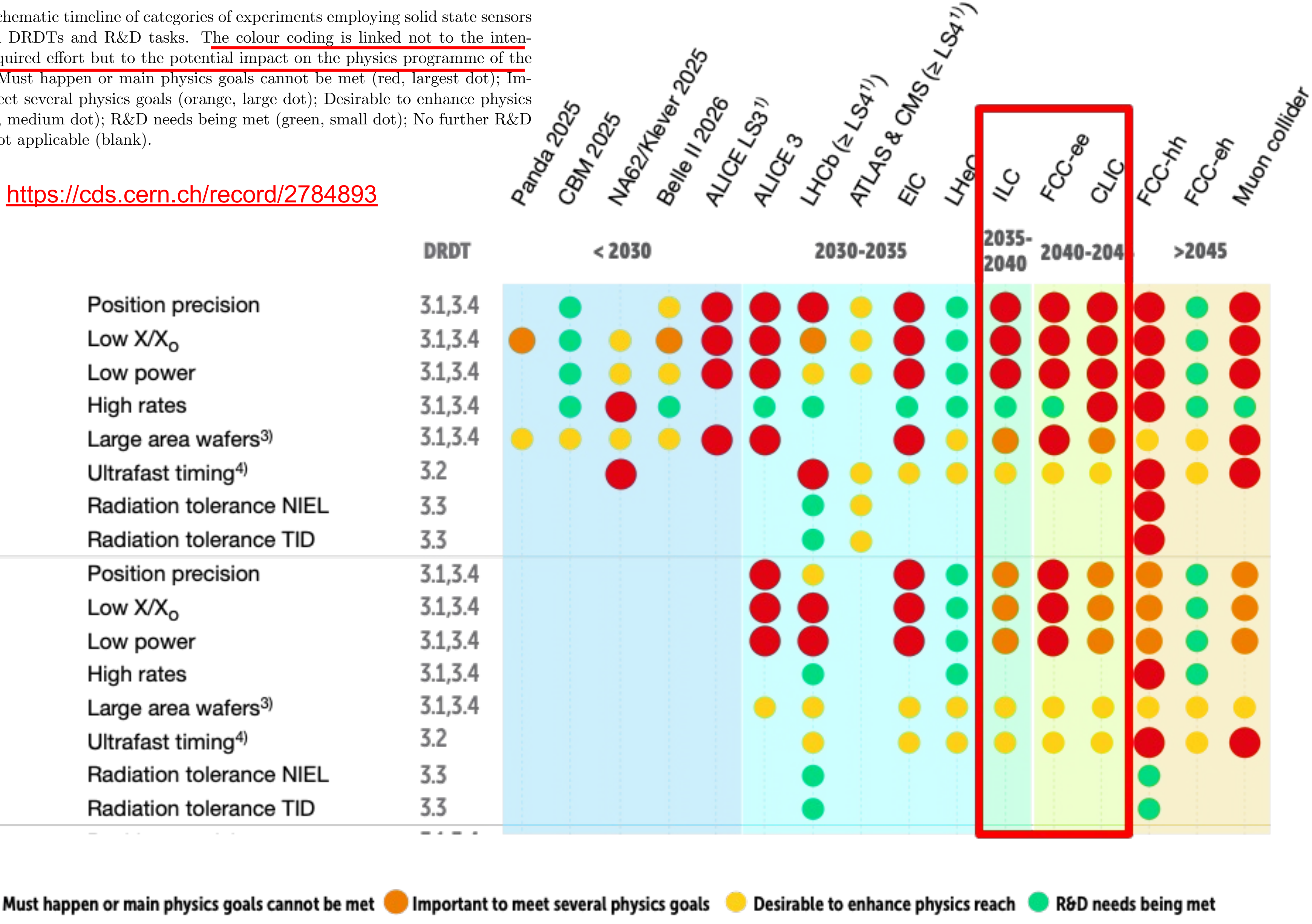
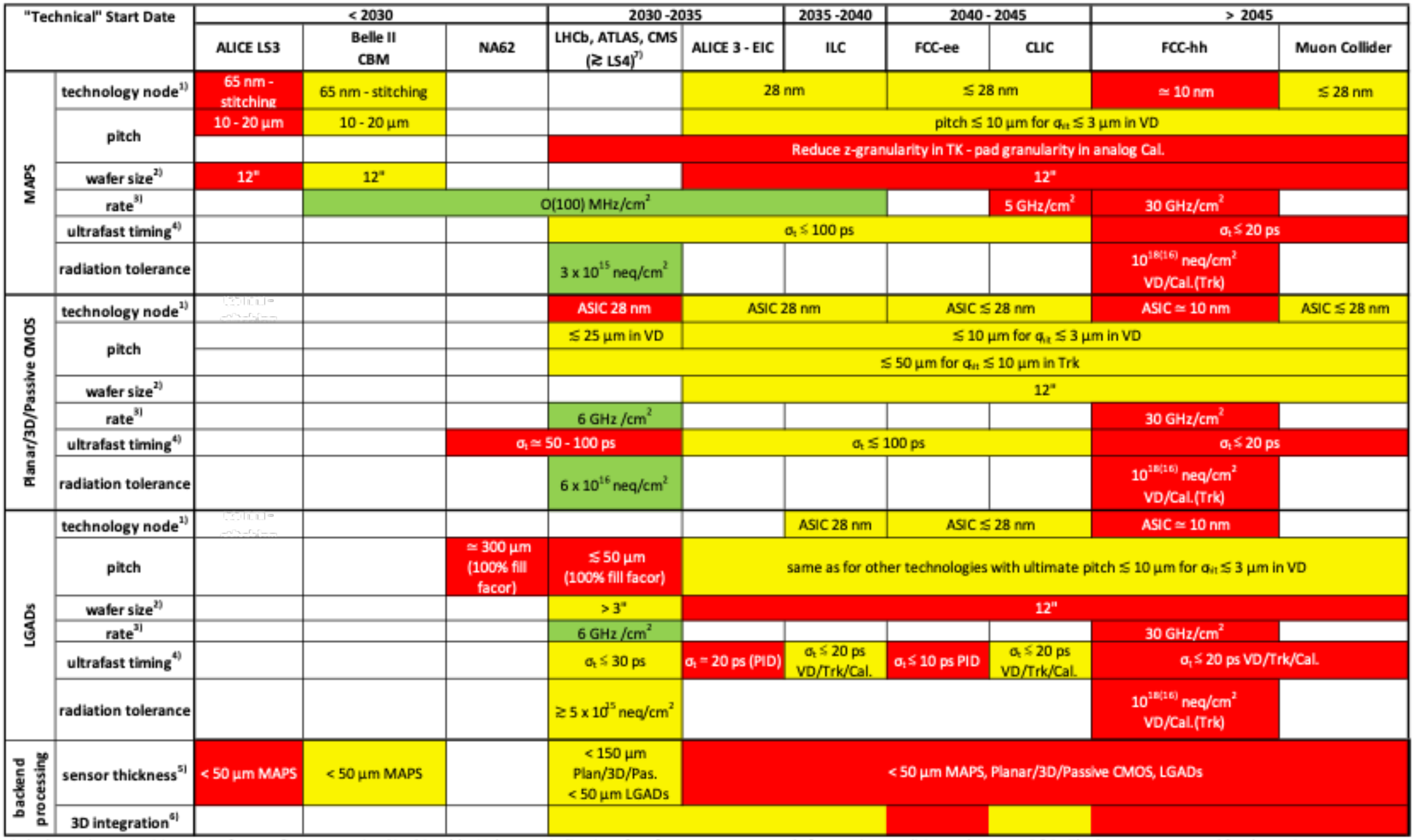


		DRDT	< 2030					2030-2035				2035-2040	2040-2045		>2045		
			Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 1)	ALICE 3	LHCb (≥ LS4 1))	ATLAS & CMS (≥ LS4 1))	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
Vertex detector2)	Position precision	3.1,3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X$_0$	3.1,3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1,3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1,3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers3)	3.1,3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing4)	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker5)	Position precision	3.1,3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X$_0$	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1,3.4							🟢			🟢				🔴	🟢	
	Large area wafers3)	3.1,3.4						🟡	🟡		🟡	🟡	🟡	🟡	🟡	🟡	🟡	🟡
	Ultrafast timing4)	3.2							🟡		🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		

🔴 Must happen or main physics goals cannot be met 🟠 Important to meet several physics goals 🟡 Desirable to enhance physics reach 🟢 R&D needs being met

Emerging/future technologies



"Technical" Start Date		< 2030			2030 -2035		2035 -2040	2040 - 2045		> 2045	
		ALICE LS3	Belle II CBM	NA62	LHCb, ATLAS, CMS (≳ LS4)7)	ALICE 3 - EIC	ILC	FCC-ee	CLIC	FCC-hh	Muon Collider
MAPS	technology node1)	🟥 65 nm - stitching	🟨 65 nm - stitching			🟨 28 nm	🟨	🟨 ≲ 28 nm	🟨	🟥 ≃ 10 nm	🟨 ≲ 28 nm
	pitch	🟥 10 - 20 µm	🟨 10 - 20 µm			🟨 pitch ≲ 10 µm for σ_{hit} ≲ 3 µm in VD	🟨	🟨	🟨	🟨	🟨
					🟥 Reduce z-granularity in TK - pad granularity in analog Cal.	🟥	🟥	🟥	🟥	🟥	🟥
	wafer size2)	🟥 12"	🟨 12"			🟥 12"	🟥	🟥	🟥	🟥	🟥
	rate3)		🟩 O(100) MHz/cm^2	🟩	🟩	🟩	🟩		🟥 5 GHz/cm^2	🟥 30 GHz/cm^2	
	ultrafast timing4)				🟨 σ_t ≲ 100 ps	🟨	🟨	🟨	🟨	🟥 σ_t ≲ 20 ps	🟥
	radiation tolerance				🟩 3 x 10^{15} neq/cm^2					🟥 $10^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
Planar/3D/Passive CMOS	technology node1)				🟥 ASIC 28 nm	🟨 ASIC 28 nm	🟨	🟨 ASIC ≲ 28 nm	🟨	🟥 ASIC ≃ 10 nm	🟨 ASIC ≲ 28 nm
	pitch				🟨 ≲ 25 µm in VD	🟨 ≲ 10 µm for σ_{hit} ≲ 3 µm in VD	🟨	🟨	🟨	🟨	🟨
					🟨 ≲ 50 µm for σ_{hit} ≲ 10 µm in Trk	🟨	🟨	🟨	🟨	🟨	🟨
	wafer size2)					🟨 12"	🟨	🟨	🟨	🟨	🟨
	rate3)				🟩 6 GHz /cm^2					🟥 30 GHz/cm^2	
	ultrafast timing4)			🟥 σ_t ≃ 50 - 100 ps	🟥	🟨 σ_t ≲ 100 ps	🟨	🟨	🟨	🟥 σ_t ≲ 20 ps	🟥
	radiation tolerance				🟩 6 x 10^{16} neq/cm^2					🟥 $10^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
LGADs	technology node1)						🟨 ASIC 28 nm	🟨 ASIC ≲ 28 nm	🟨	🟥 ASIC ≃ 10 nm	
	pitch			🟥 ≃ 300 µm (100% fill facor)	🟥 ≲ 50 µm (100% fill facor)	🟨 same as for other technologies with ultimate pitch ≲ 10 µm for σ_{hit} ≲ 3 µm in VD	🟨	🟨	🟨	🟨	🟨
	wafer size2)				🟨 > 3"	🟥 12"	🟥	🟥	🟥	🟥	🟥
	rate3)				🟩 6 GHz /cm^2					🟥 30 GHz/cm^2	
	ultrafast timing4)				🟨 σ_t ≲ 30 ps	🟥 σ_t = 20 ps (PID)	🟨 σ_t ≲ 20 ps VD/Trk/Cal.	🟥 σ_t ≲ 10 ps PID	🟨 σ_t ≲ 20 ps VD/Trk/Cal.	🟥 σ_t ≲ 20 ps VD/Trk/Cal.	🟥
	radiation tolerance				🟨 ≥ 5 x 10^{15} neq/cm^2					🟥 $10^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
backend processing	sensor thickness5)	🟥 < 50 µm MAPS	🟨 < 50 µm MAPS		🟨 < 150 µm Plan/3D/Pas. < 50 µm LGADs	🟥 < 50 µm MAPS, Planar/3D/Passive CMOS, LGADs	🟥	🟥	🟥	🟥	🟥
	3D integration6)				🟨	🟨	🟨	🟥	🟨	🟥	🟥

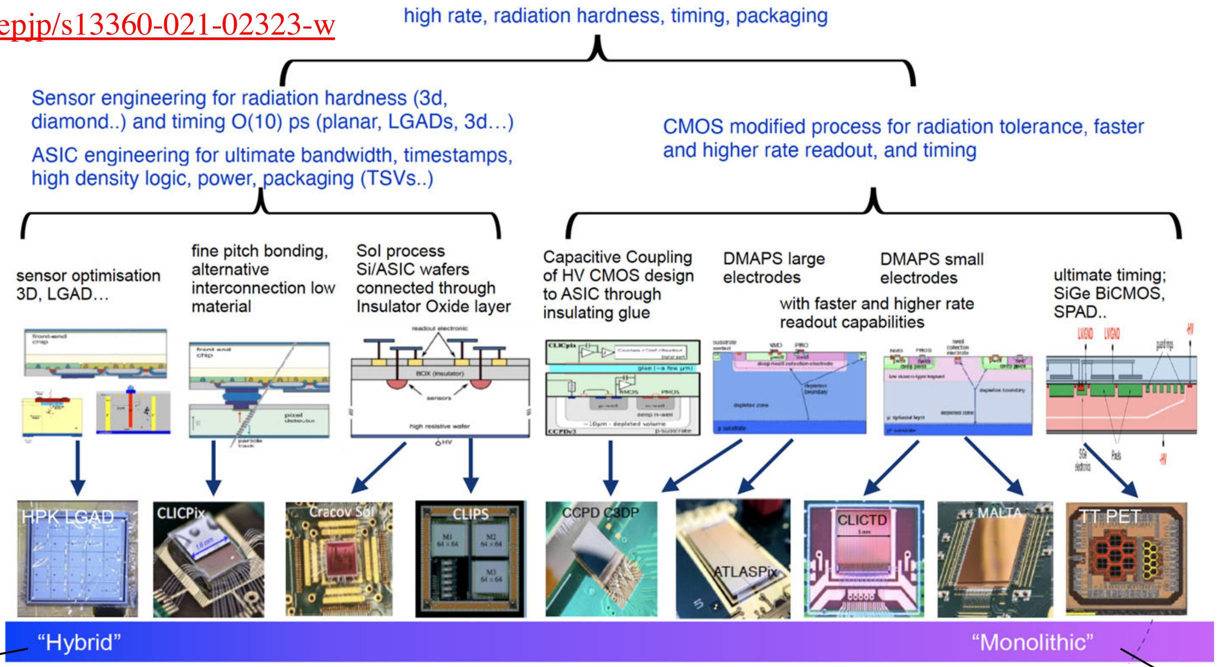
Figure 3.3: Compilation of the technology R&D needs and timeline for future solid state detectors. The colour coding is linked not to the intensity of the required effort but indicates what key progress would be need for a technology to enter a project (red), when it would be desirable (yellow), or when it is being met (green).

Smaller feature size technologies to further improve granularity, power consumption, rate, radiation hardness, …

https://cds.cern.ch/record/2784893

Silicon detector technologies

https://doi.org/10.1140/epjp/s13360-021-02323-w



high rate, radiation hardness, timing, packaging

Sensor engineering for radiation hardness (3d, diamond..) and timing O(10) ps (planar, LGADs, 3d…)

ASIC engineering for ultimate bandwidth, timestamps, high density logic, power, packaging (TSVs..)

CMOS modified process for radiation tolerance, faster and higher rate readout, and timing

sensor optimisation 3D, LGAD…

fine pitch bonding, alternative interconnection low material

SoI process Si/ASIC wafers connected through Insulator Oxide layer

Capacitive Coupling of HV CMOS design to ASIC through insulating glue

DMAPS large electrodes

DMAPS small electrodes

with faster and higher rate readout capabilities

ultimate timing; SiGe BiCMOS, SPAD..

“Hybrid”

“Monolithic”

There are many more prototypes!!!

Hybrid pixel detectors

- Sensor optimisation (3D, LGAD, passive CMOS, …)
- 65 → 28 nm ASICs
- New interconnection technologies (fine pitch bump-bonding, ACF, …)

MAPS

- Improved charge collection via full depletion (HV/HR-CMOS), driven by high rate, high radiation experiments.
- Higher granularity, lower mass with smaller feature size CMOS.

SiGe BiCMOS, SPAD: Ultimate timing.

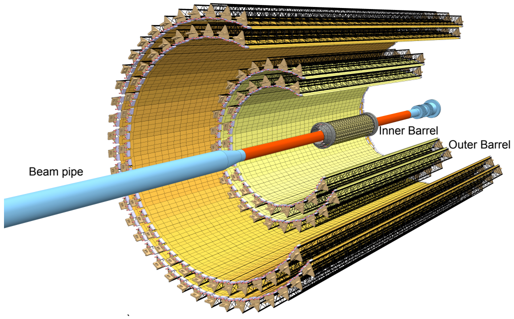
CCD (various types): Ultimate pixel size.

SOI, 3D integration,
capacitively coupled devices.

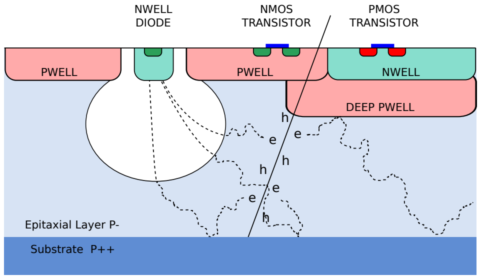
DRDT 3.1 - Monolithic CMOS

- Monolithic Active Pixel Sensors (MAPS) in commercial CMOS imaging technology could provide solutions for both vertex and tracking layers at e+e- colliders.
  - High granularity and low power consumption demonstrated by state-of-the art, further improved by the use of smaller technology nodes (see next slide).
  - Low cost, large volume production and ease of assembly would favour use in trackers wrt. strips.
    - Tracking detectors is an area where there is a lot of UK expertise.
    - Also consider overlapping requirements with calorimeters, and UK work on that → possible synergies?

ALPIDE @ ALICE ITS2
Example state-of-the-art MAPS detector



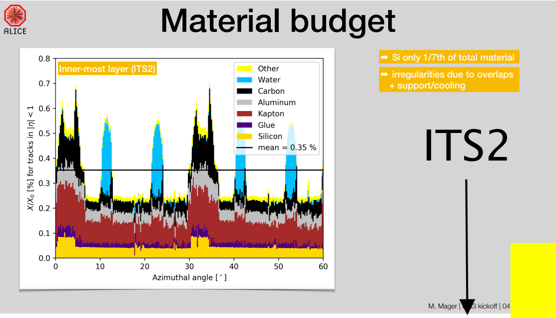
10m^2 surface
Inner Barrel = 0.3% X/X0 per layer
Outer Barrel = 0.8% X/X0 per layer
50 kHz interaction rate (Pb-Pb)
400 kHz interaction rate (pp)



180 nm CMOS TowerJazz
27 x 29 µm^2 pixel pitch
5 µs integration time
40 mW/cm^2

Stitched wafer scale sensors for cylindrical layers

- Exploration of 65 nm CMOS imaging processes for MAPS driven by CERN EP R&D WP1.2 and ALICE ITS3 upgrade.
  - 12” wafers, higher logic density, smaller pixels, faster read-out, lower power consumption.
- Wafer-scale, low power sensor design for truly cylindrical minimal material budget layers → New technology node & new detector concept
  - Mechanical support, power distribution and data lines outside acceptance, air cooling.



Material budget

- ➡ Si only 1/7th of total material
- ➡ irregularities due to overlaps + support/cooling

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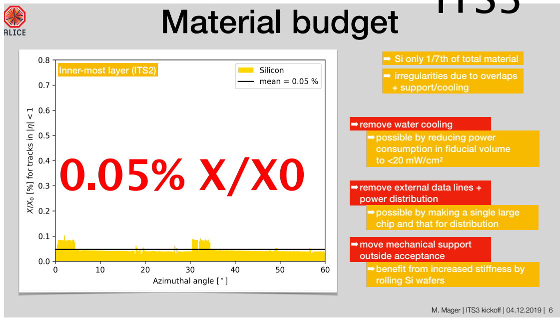
ITS2

ITS3



Material budget

0.05% X/X0

- ➡ Si only 1/7th of total material
- ➡ irregularities due to overlaps + support/cooling
- ➡ remove water cooling
  - ➡ possible by reducing power consumption in fiducial volume to <20 mW/cm²
- ➡ remove external data lines + power distribution
  - ➡ possible by making a single large chip and that for distribution
- ➡ move mechanical support outside acceptance
  - ➡ benefit from increased stiffness by rolling Si wafers

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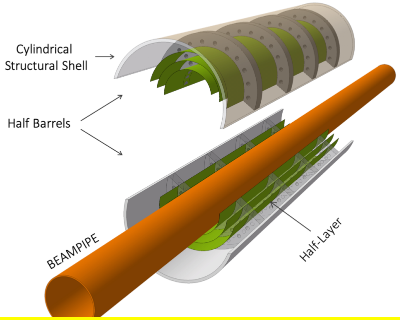
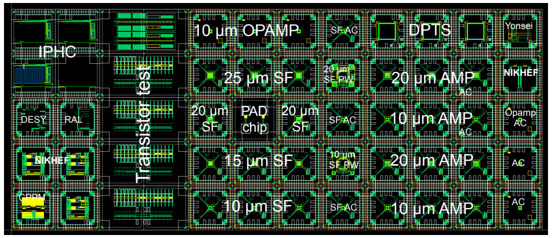
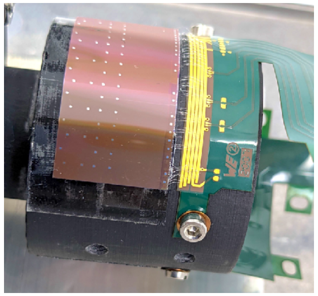


MLR1 submission

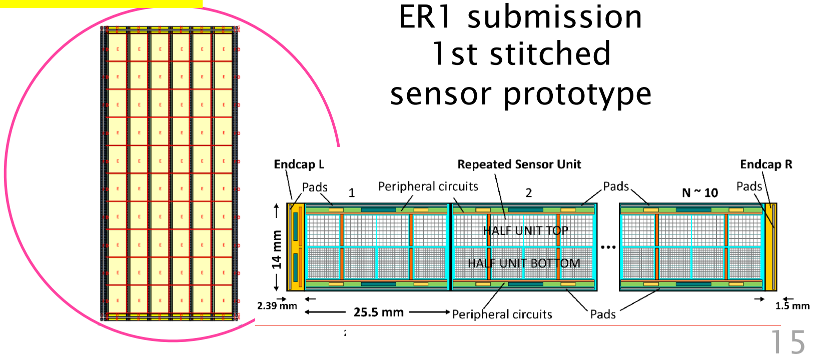


Example of emerging new technology relevant for e+e- colliders.

Bent ALPIDE



ER1 submission
1st stitched
sensor prototype



DRDT 3.4 - 3D integration

- Industrial developments of heterogeneous integration technologies to achieve further reductions in cost and power.
- 3D stacking is being studied for future HEP applications → potential for increased functionality and performance of silicon trackers.
- Pursuing this path would require large scale of investment and establishing a privileged relation with industrial partner(s), but it is a field where there isn't a clear leadership now.
  - Dependent on availability of process for R&D.
- There is expertise in the UK to work on each layer in the stack and on the interconnection technologies.

Electronics (beyond sensors) (Chapter 7)

(See Figure 7.1, R&D Roadmap for an overview)

- Under DRDT 7.2: High-granularity pixel readout chip with 10–100ps timing and charge measurement capability in 28nm CMOS, and highly programmable features
    - An opportunity to hang on to our involvement from RD53? A lot of this is chip design in IP blocks that can be useful elsewhere, but do we think it's worth the investment?
- DRDT 7.5 - Evaluate and adapt to emerging electronics and data processing technologies
    - Silicon photonics as the successor to actively modulated VCSEL-based links, facilitating full-custom photonic integrated circuits (PICs) for HEP
        - So far as I am aware this could be a wide open field with possible contributions from the UK - can significantly reduce optics power, expertise doesn't exist, but not sure it does elsewhere?
    - 3D integration and high density interconnects
        - We already have people working on some of these
- Under DRDT 7.1: Power and readout efficiency:
    - High conversion factor DC-DC converters based on new processes and materials, and associated power management circuit blocks
        - Long history of testing powering schemes, GaN HV switches fully developed through the UK now being looked at for higher efficiency DCDC at CERN

Mechanics & cooling (Chapter 8)

(Have a look at Figure 8.1)

- DRDT 8.1 - Develop novel magnet systems
- DRDT 8.2 - Develop improved technologies and systems for cooling
  - Experience with microchannel cooling, but are we happy? Other approaches?
- DRDT 8.3 - Adapt novel materials to achieve ultralight, stable and high precision mechanical structures. Develop Machine Detector Interfaces
  - Lots of carbon fibre experience in the UK, but lack of industry backing can be a problem
  - Work on detectors without support structures ongoing…

Working with UK industry

- Developments that involve UK industrial partners would be beneficial for funding situation.

- Involvement of existing infrastructure for large scale assembly also to be considered (for example national labs/SRF).

- Some examples of UK company for sensor production and interconnections: Alter Technology, Custom Interconnect Ltd, ElementSix, Micron, Micross, Nordson, Te2v.
  - There is certainly more.

- We are already working with some of these industrial partners.
  - Interest from some of these companies to work with us but small-ish R&D budgets and long development cycles not attractive for their business model.

Opportunities for the UK - Thoughts for discussion

- The UK community interested in e+e- colliders should identify opportunities where it can engage with the international efforts in a leading role.
- There is a large community in the UK working on many aspects of vertex and tracking detectors development, construction and operation (sensors, ASICs, mechanics, readout, cooling, DAQ, …) → a lot of expertise.
- At this early stage it would be good to identify technologies that are agnostic to the specific collider implementation, rather then splitting the community (and the resources) into groups working on detector R&D for different e+e- collider.
- The community should aim at a unified and coordinated vision.
    - Devise a common generic R&D programme that then can branch off for specific/targeted implementations required by different facilities.
- What we really need is a Workshop on Tracking and Vertexing for e+e- colliders, where the UK community comes together, presents their developments and identifies strengths that can culminate in a funded route for development and ultimately leadership in a section of the field.
    - What developments/expertise/links with industry can we leverage on?

Backup