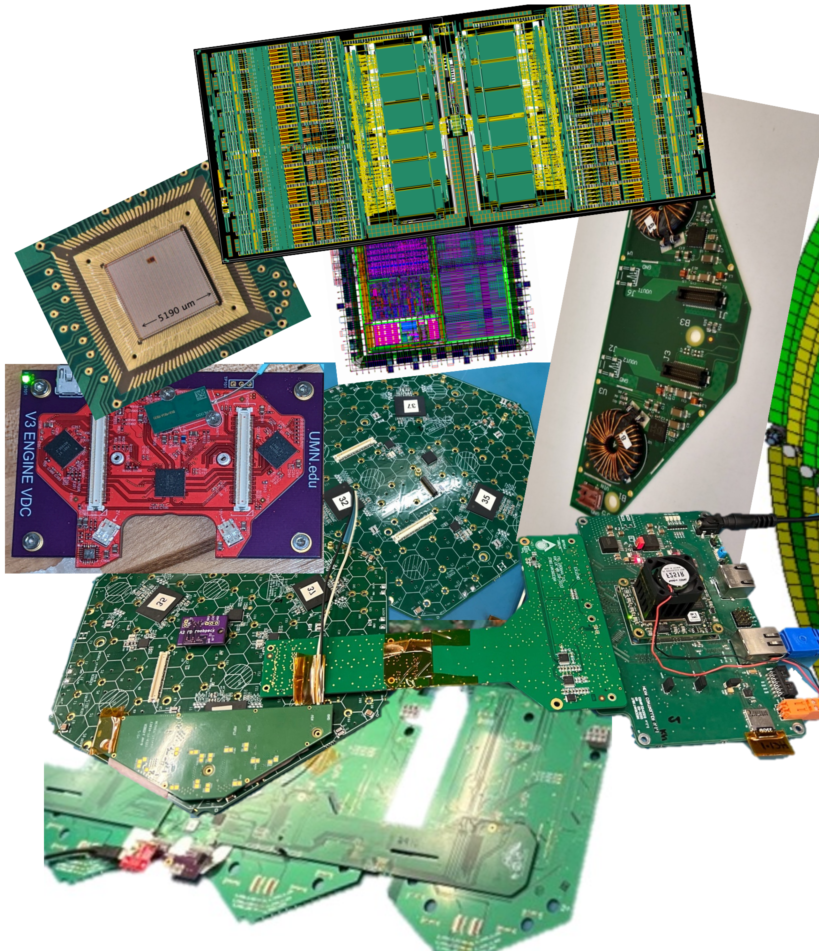
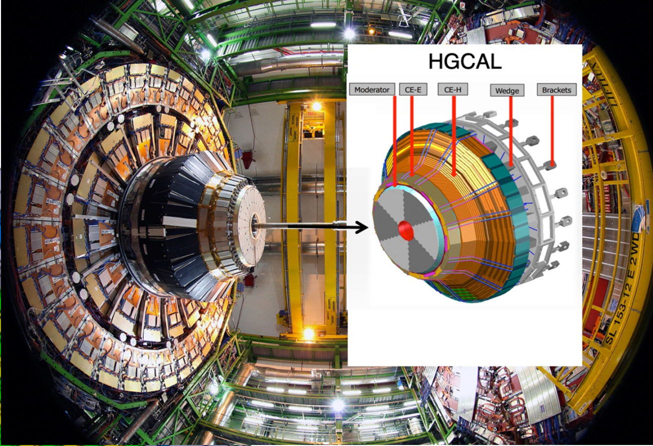
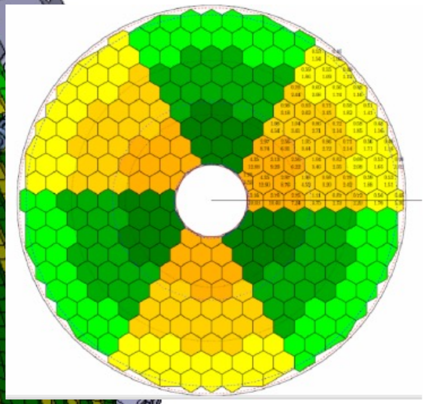
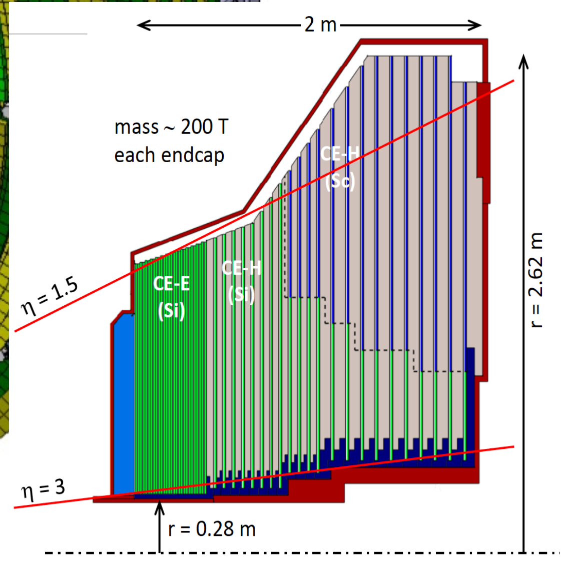
CMS High Granularity Calorimeter







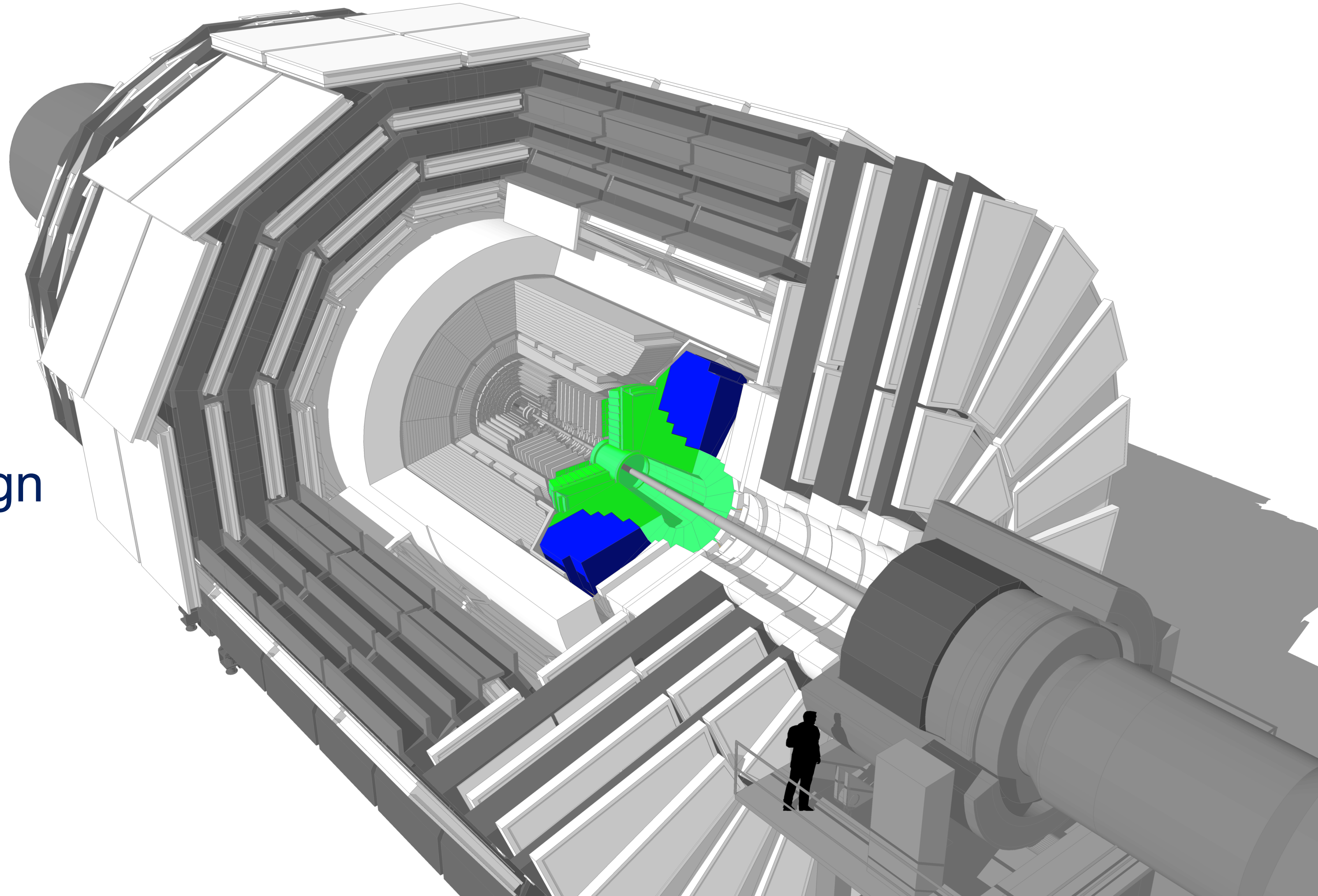


CMS HGCAL
An Electronics Perspective
UZH November 2022

Paul Aspell
CERN

Presentation structure:

- Introduction
- The HGCAL Upgrade
- Key challenges
- The Electronics System Design
- Validation
- Moving forward



A little personal background

I joined CERN in 1988.

I joined a small team working on the (at the time) brand new field of microelectronics for HEP.

Initially development of ASIC concepts for future HEP super colliders ; low noise front-ends, analog memories, triggering, pixels …

CMS Preshower – PACE

TOTEM – VFAT2

ILC - SALTRO

CMS GEMs Electronics Coordination – VFAT3 chip & GE11

CMS HGCAL Electronics Coordination from 2019

CMS HGCAL

Project timeline

Higgs discovery 2012

HL-LHC well underway

2013 …. Conception
2015 …. Technical Proposal (TP)
2017 …. Technical Design Report (TDR)

Design & prototyping phase

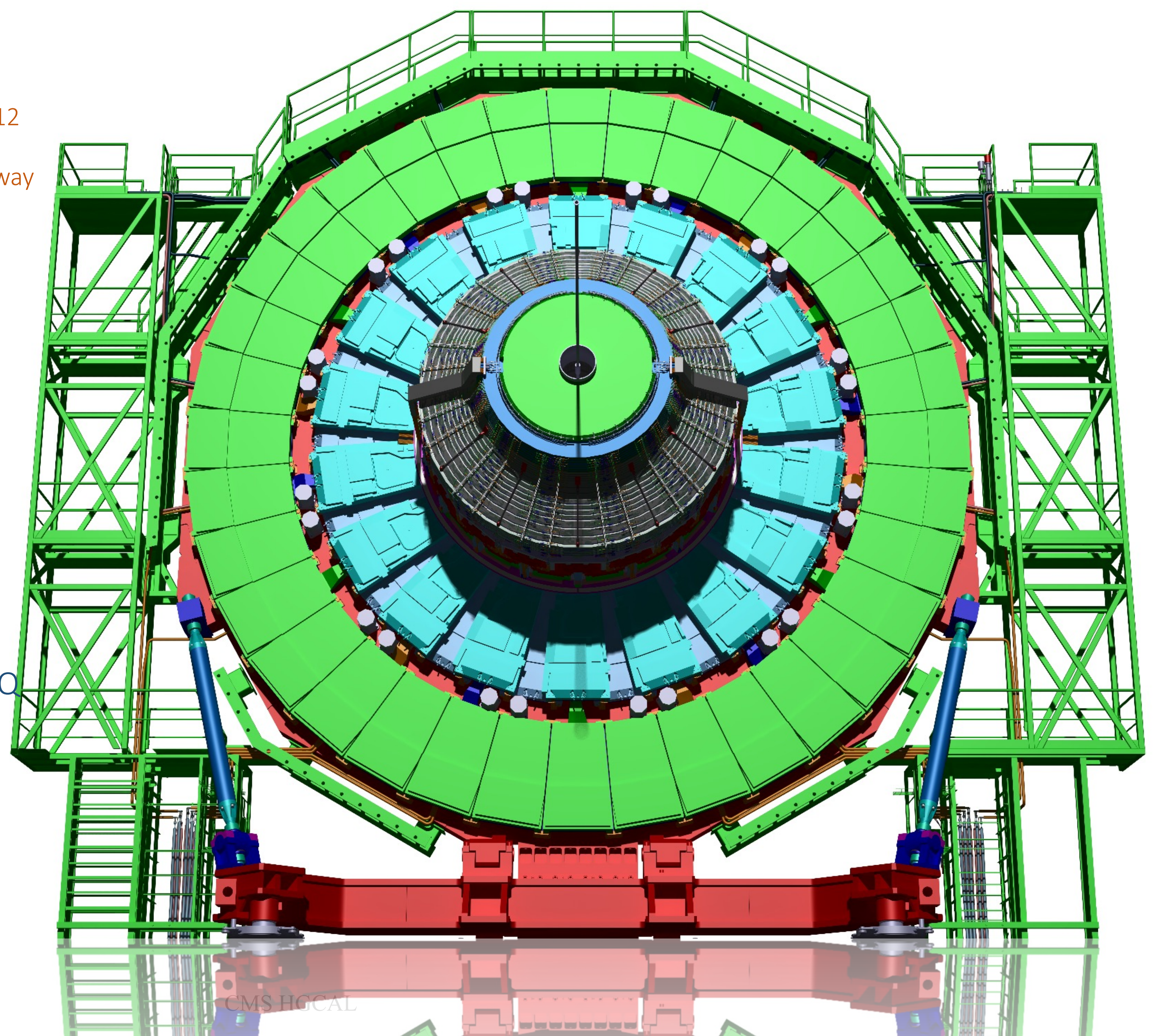
I joined in 2019 as Electronics Coordinator

2023 …. Electrical System Review (ESR)

Production

2027 …. Lowering
Installation & commissioning
2028 …. Integrated with CMS Central DAQ
2029 …. Run 4 starts

We are currently coming to the end of the design and prototyping phase and gearing up for production



CMS HGCAL

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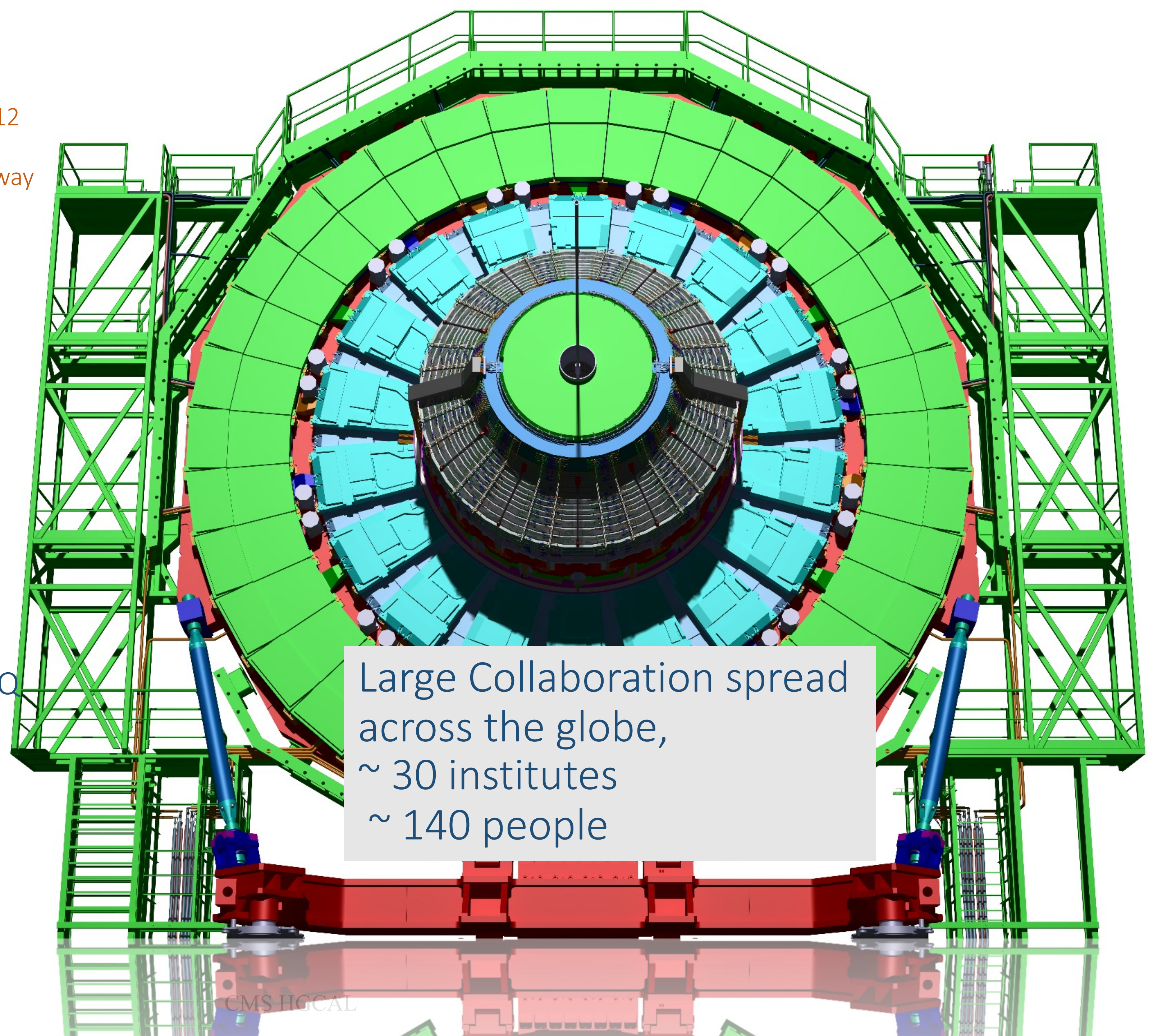


Large Collaboration spread across the globe,
~ 30 institutes
~ 140 people

Moving to the HL-LHC

The HL-LHC aims to operate with instantaneous luminosities of ~ factor 5 times the LHC nominal vlaue.

The mean number of events per bunch crossing (pileup) will increase from around 40 to 140-200.

This requires sensors and electronics to be able to with-stand the much increased radiation environments.

In addition, the performance needs to be greatly improved to cope with higher event rates and intermingled pileup events. This requires higher granularity as well as precision time measurement.
Leading to much more selective triggering.

CMS is therefore undergoing an extensive upgrade program.

The existing endcap calorimeters (ECAL & HCAL) would not survive and need to be replaced.

CMS High Granularity Calorimeter (HGCAL)

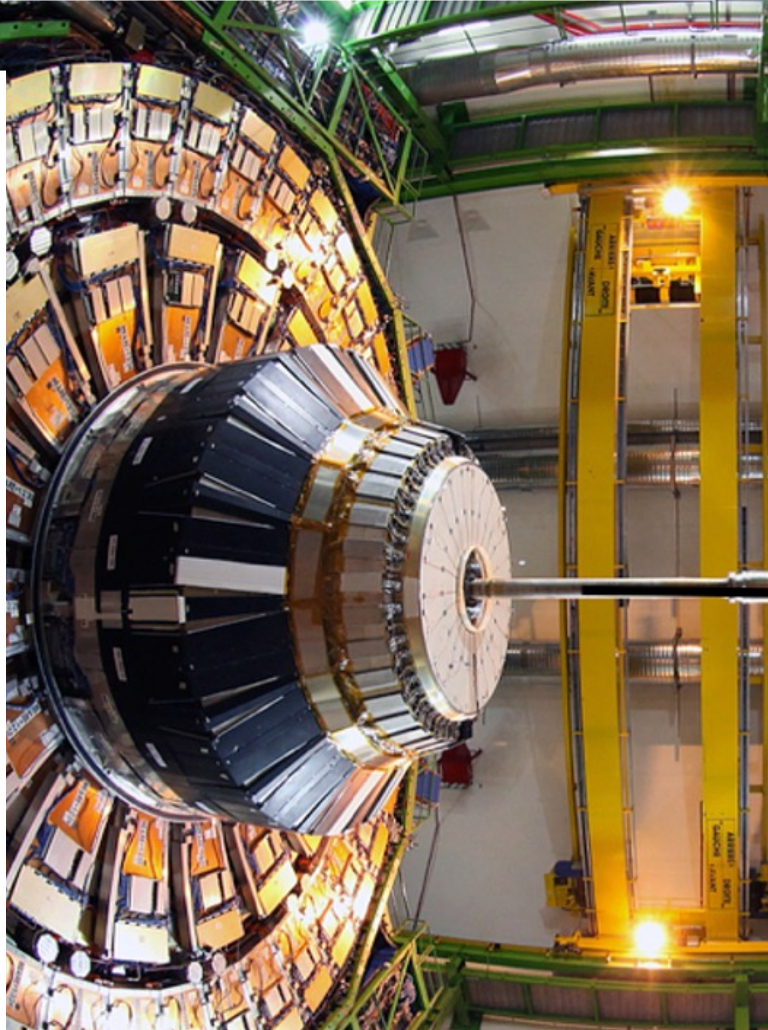
"Upgrade" ? That's an understatement.

Completely replaces the existing endcap Preshower + ECAL + HCAL.

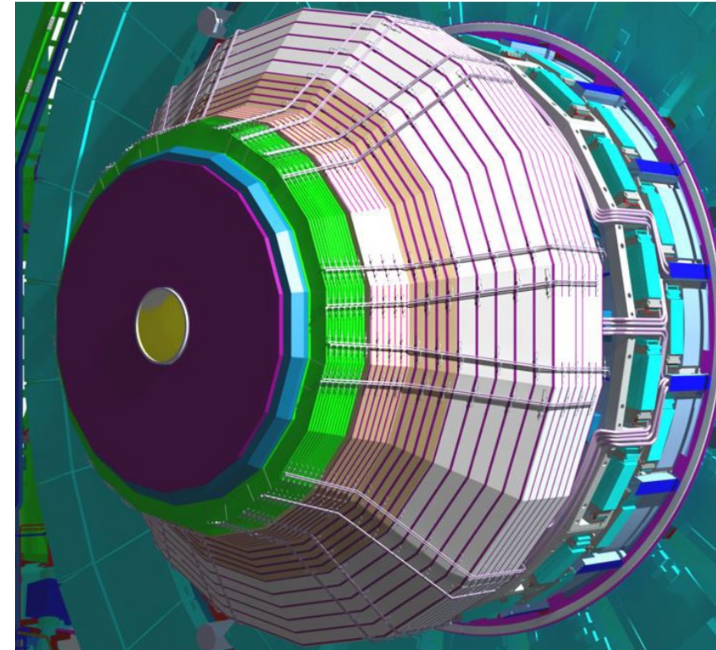
The detector concept :

Sampling calorimeter of many layers.

Will measure precisely
Energy
Spatial precision in 3D
Time



HGCAL



CMS HGCAL

47 layer Sampling calorimeter

HGCAL covers 1.5 < η < 3.0

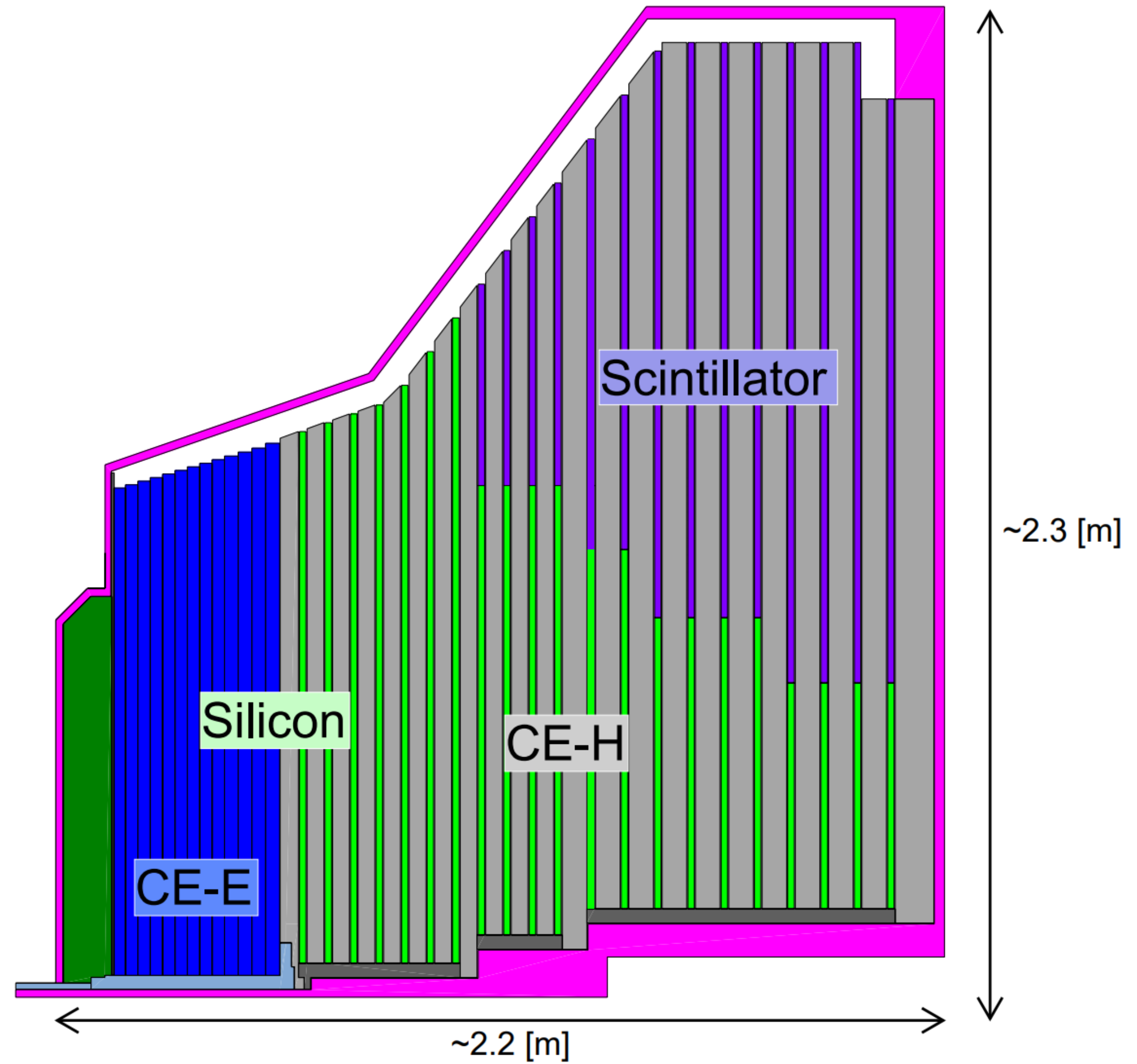
CE-E has all silicon sensors

CE-H has silicon sensors in the more demanding radiation regions and Scintillating tiles in the more outer regions

~620m2 Si sensors in ~27000 silicon modules
~ 6M Si Channels [0.5 or 1cm2 cell size]

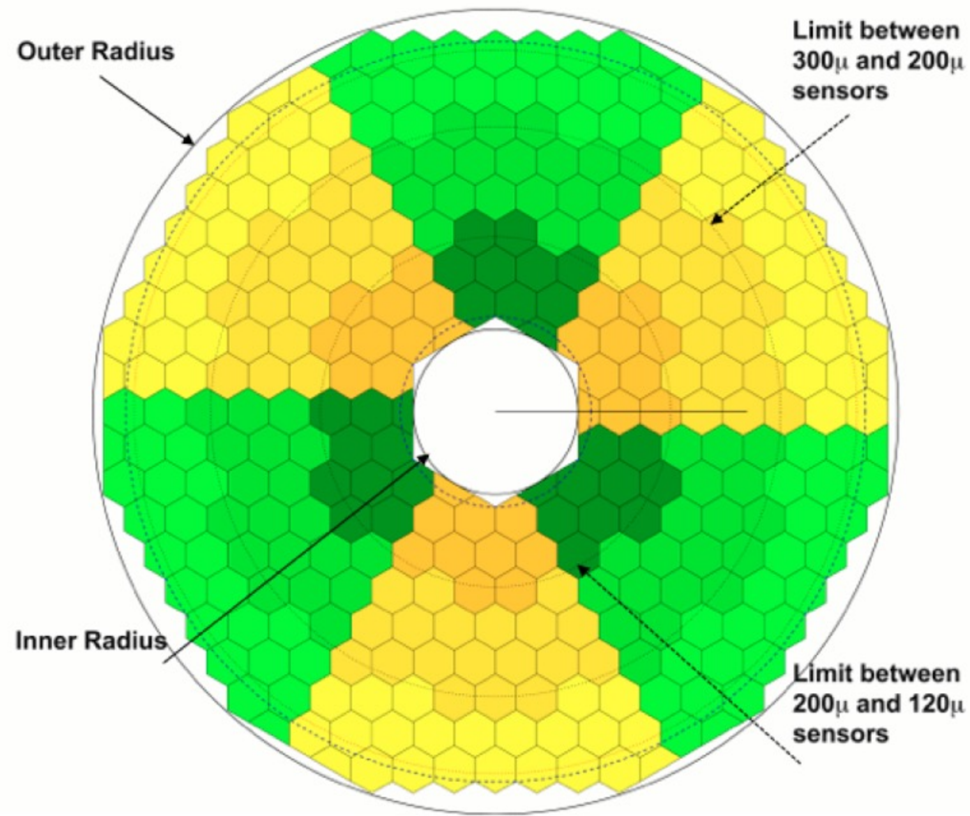
~400m2 of scintillators
~240000 scintillating channels [4-10cm2 cell size]

215 tonnes per endcap
~125kW per endcap
Cooled to -30°C

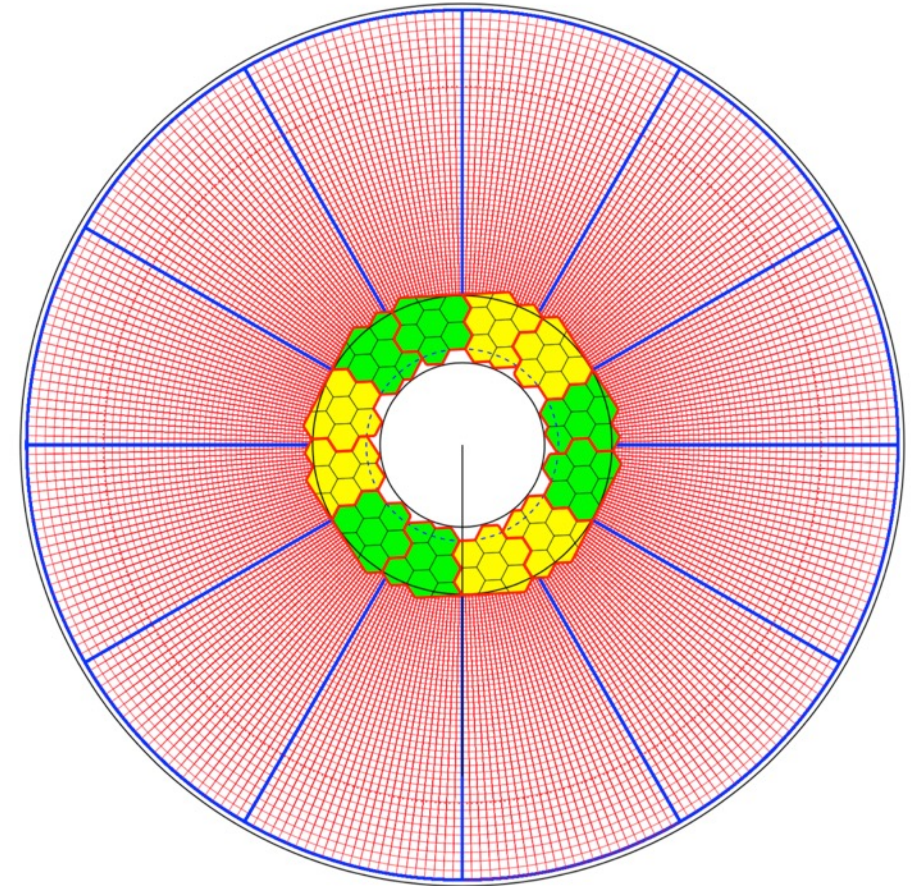


47 layer sampling calorimeter
Electromagnetic calorimeter (**CE-E**): **Si**, Cu/CuW/Pb absorbers, 26 layers
Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 21 layers

HGCAL, CE-E and CE-H



Silicon-only layer (in CE-E) showing “cassettes” and different sensor thicknesses



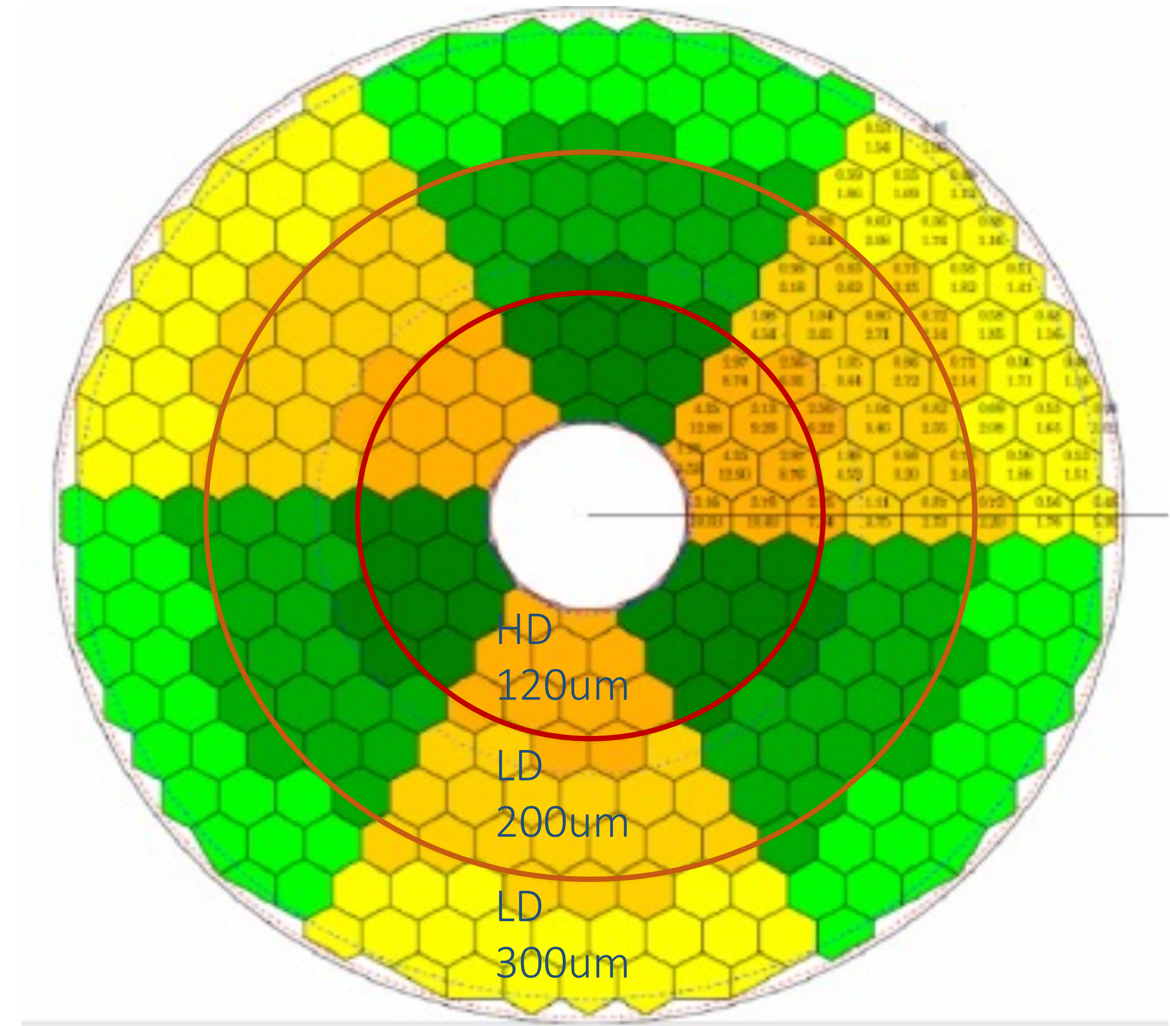
Mixed layer (in CE-H) with silicon at high η and scintillator+SiPM at low η

Silicon Sensors

Hexagonal form to maximise the silicon area from 8” wafers

N-on-P (P-Type) … tolerates the radiation levels and maintains adequate signal charge collection efficiency after $1.5x10^{16} n/cm^2$.

3 different sensor thicknesses 300um, 200um and 120um, (thinner sensors have better CCE w.r.t. fluence).



2 different pad sizes:
~$1cm^2$ for the Low Density (LD) 300um and 200um thick sensors
~$0.5cm^2$ for the High Density (HD) 120um thick sensors

HD sensors in the inner high radiation and high occupancy region

DC coupled

Silicon Sensors

Hexagonal form to maximise the silicon area from 8” wafers

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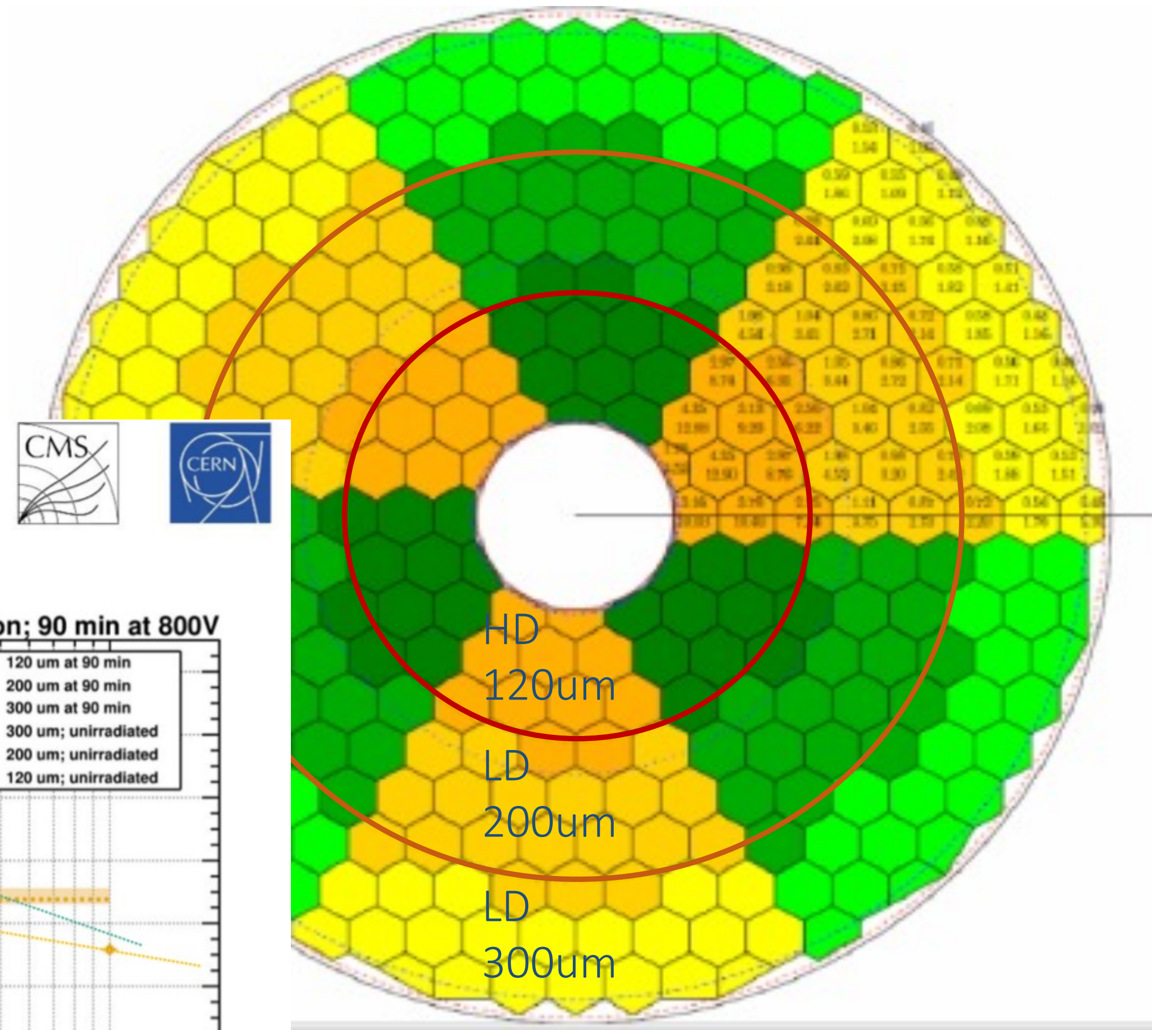
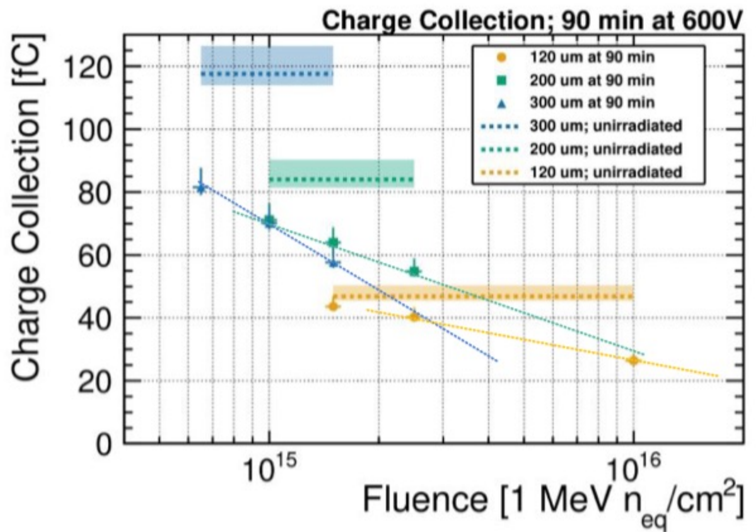
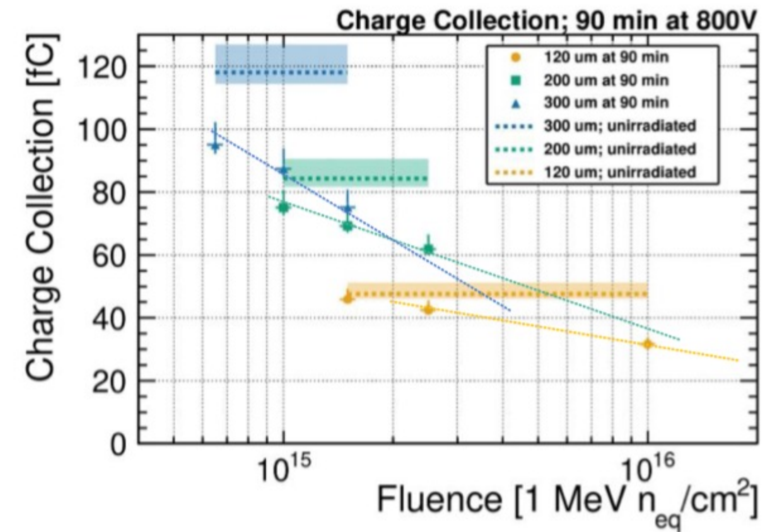


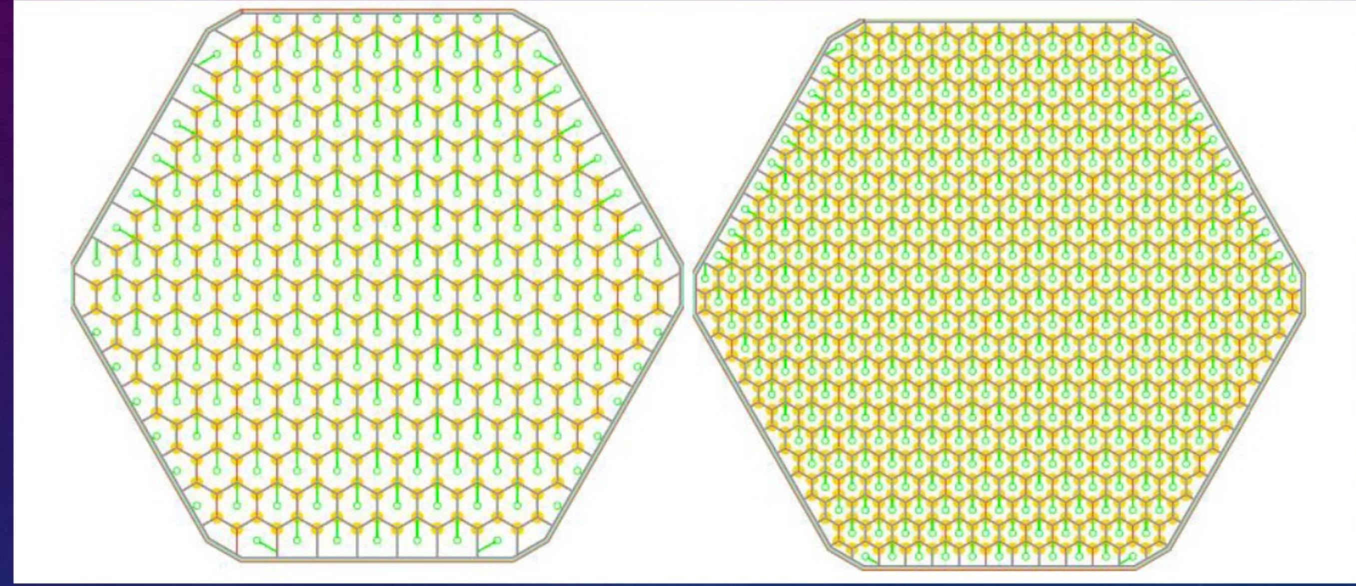
Charge Collection vs. Fluence, 90min

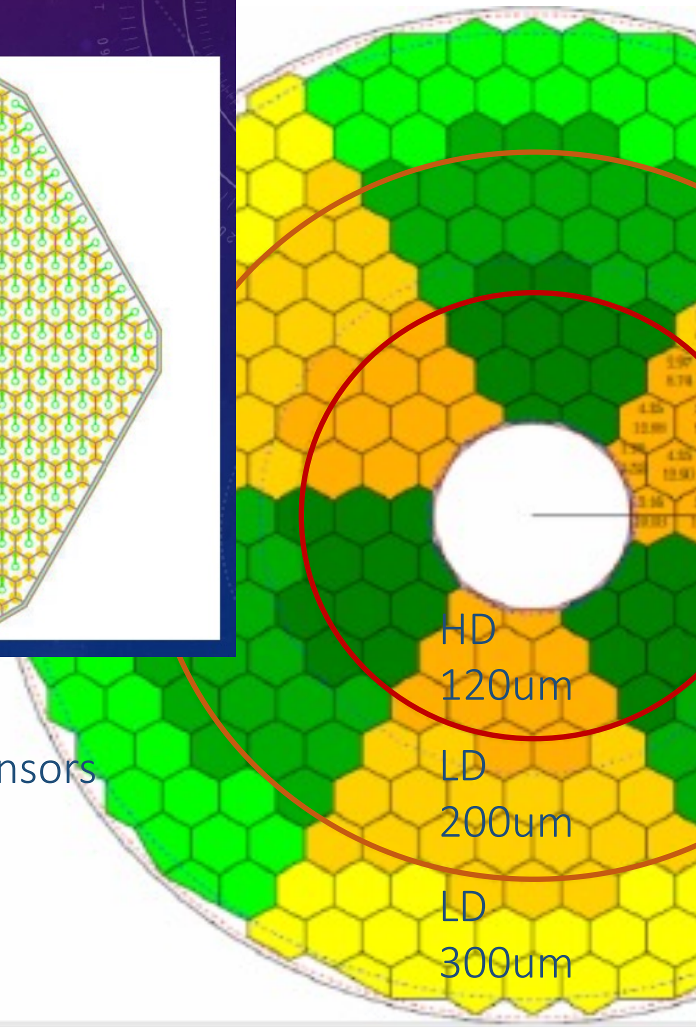




- Similar charge collection for the 200 and 300 µm at 10^{15} and 1.5×10^{15} n_{eq}/cm^2

Silicon Sensors

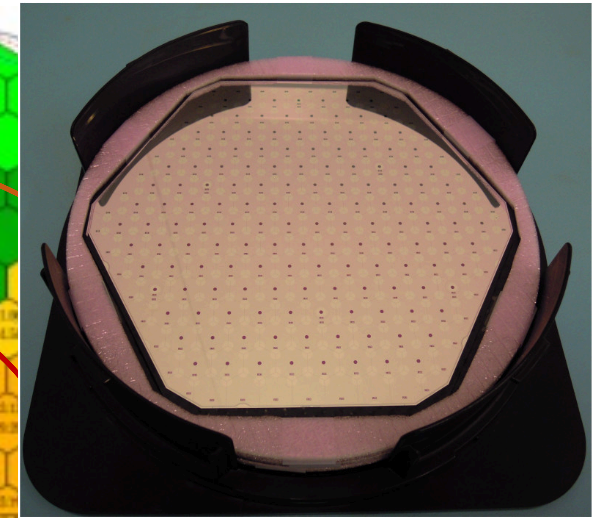




Low-Density sensor

$\sim$ 200 cells of 1.1 cm^2 size,

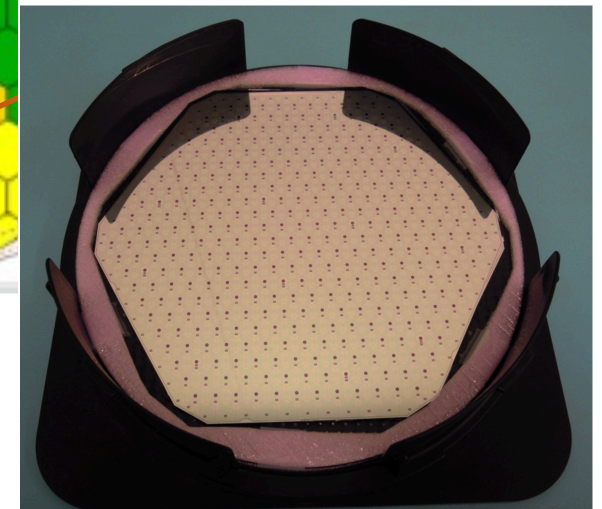
300 & 200 μm active thickness (FZ)



High-Density sensor

$\sim$ 450 cells of 0.5 cm^2 size

120 μm active thickness (epitaxial)



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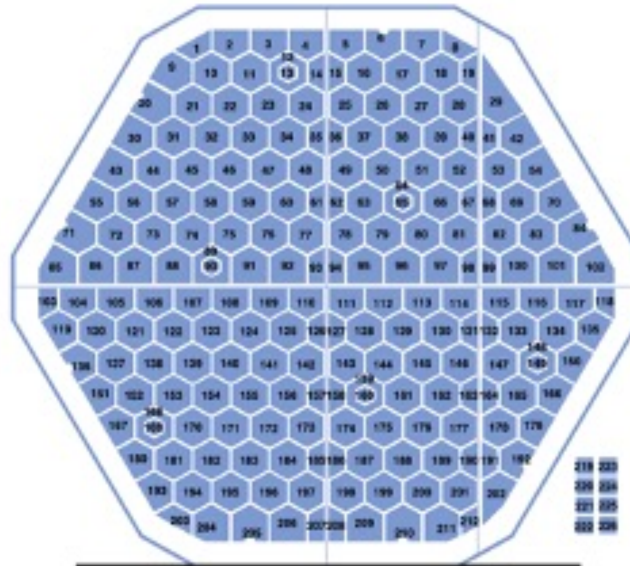
HD sensors in the inner high radiation and high occupancy region

DC coupled

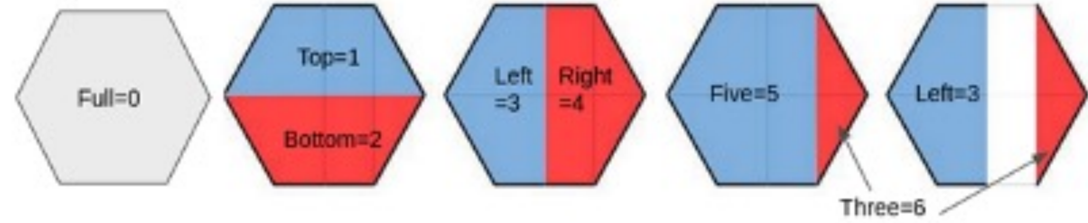
Silicon Sensors

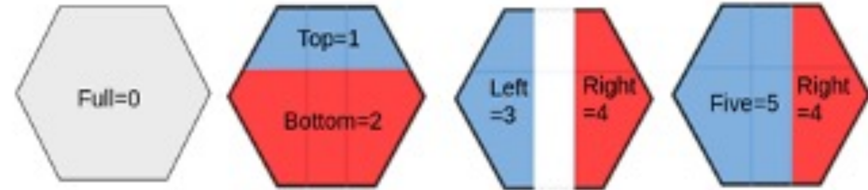
Multi-Geometry Wafers

To provide coverage on the inner and outer boundrkys

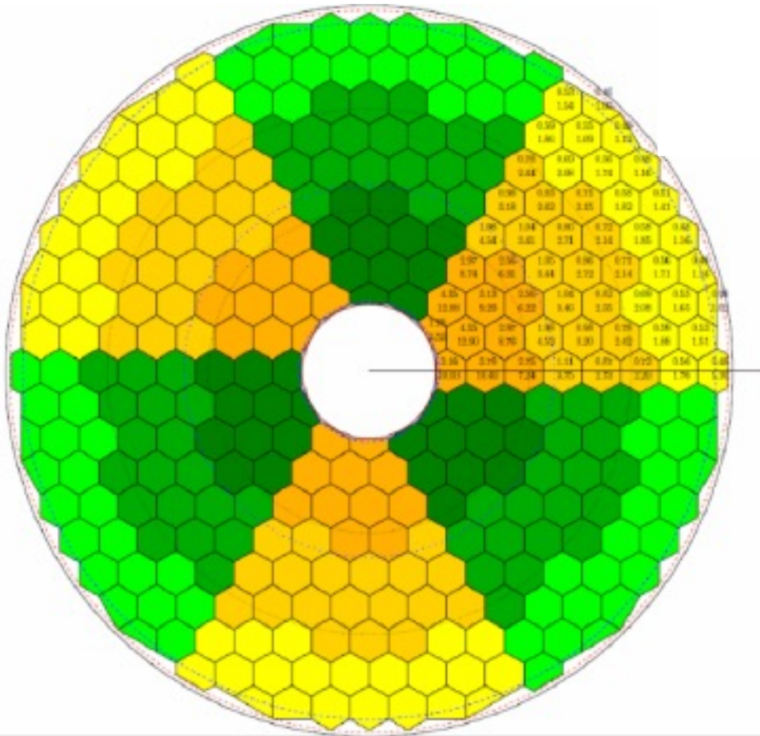


LD MGW sensor layout



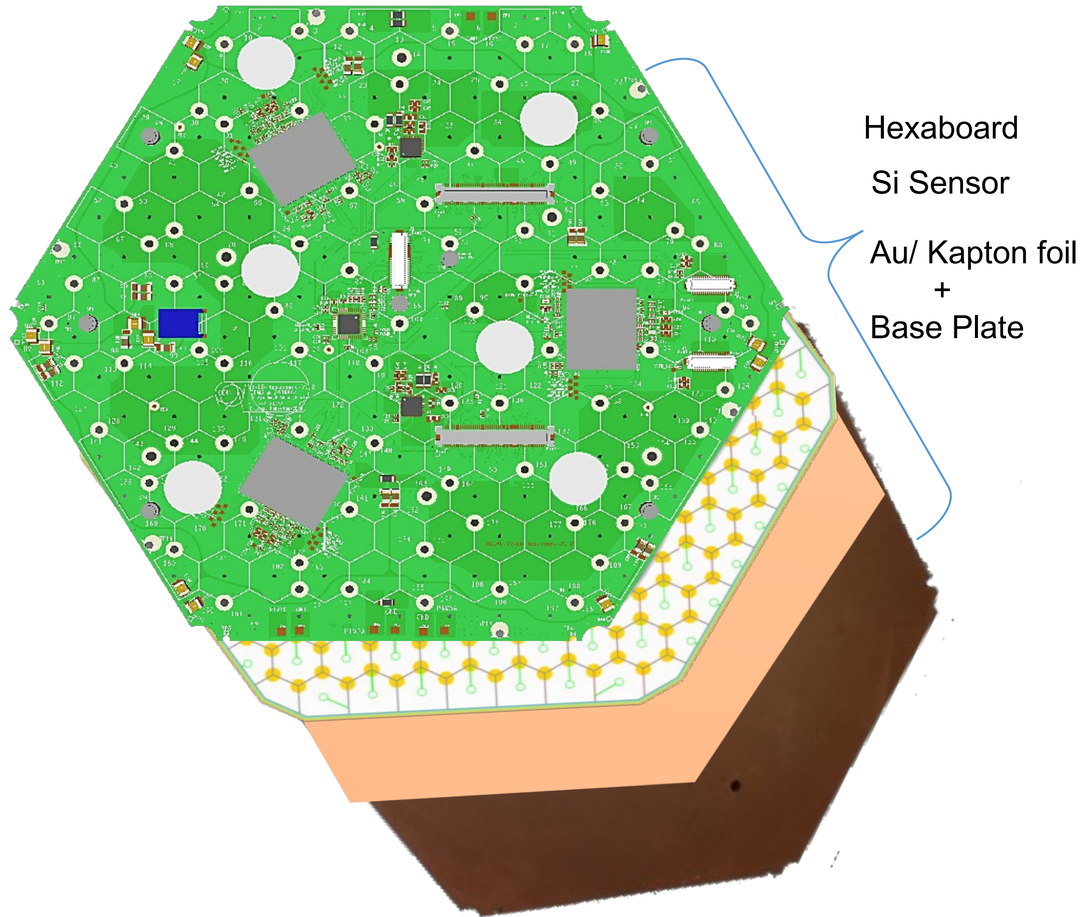


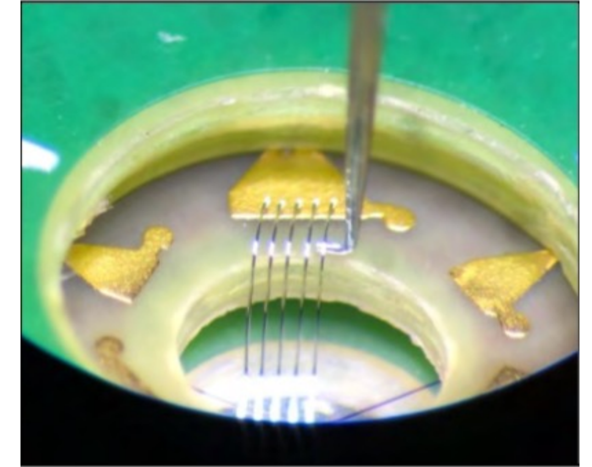
3-4 dicing types

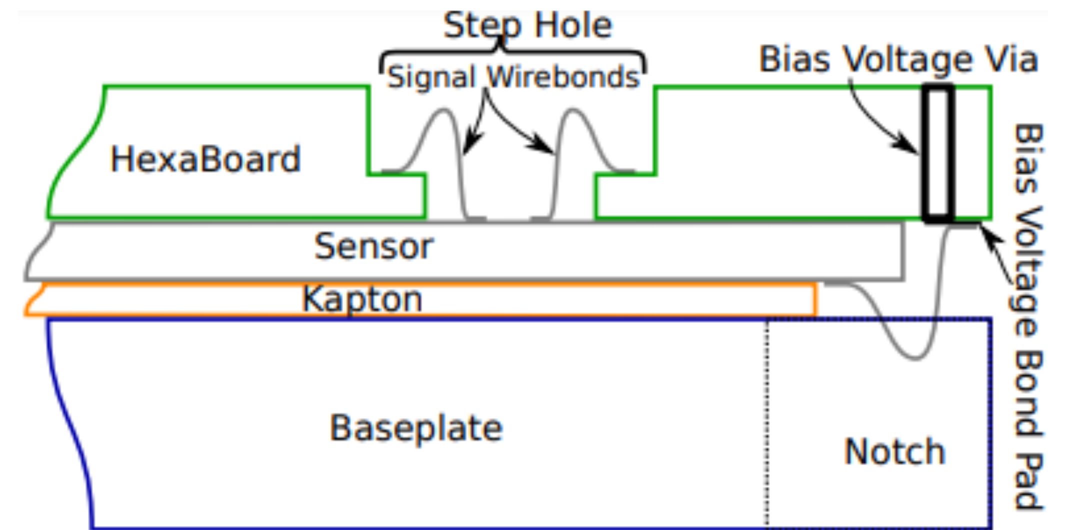


Silicon Modules

The silicon sensor is mounted on one side to a baseplate.
On the other side a front-end electronics board is mounted called the Hexaboard.
The Hexaboard contains the front-end readout ASICs (HGCROCs).
Each sensor cell is wire bonded to the HGCROC inputs through holes (stepped holes) in the Hexaboard.





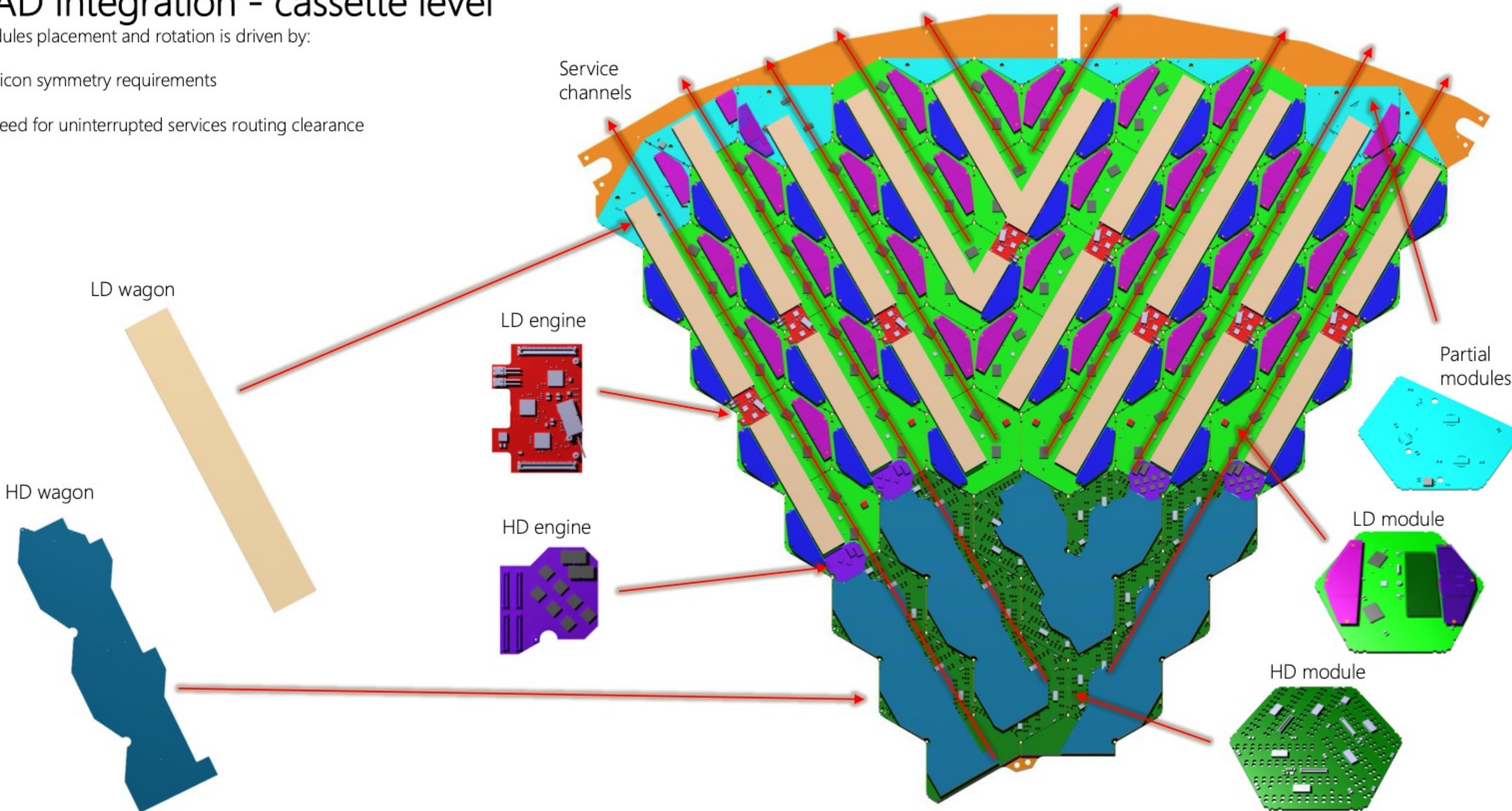


CAD Integration - cassette level

Modules placement and rotation is driven by:

1) Silicon symmetry requirements

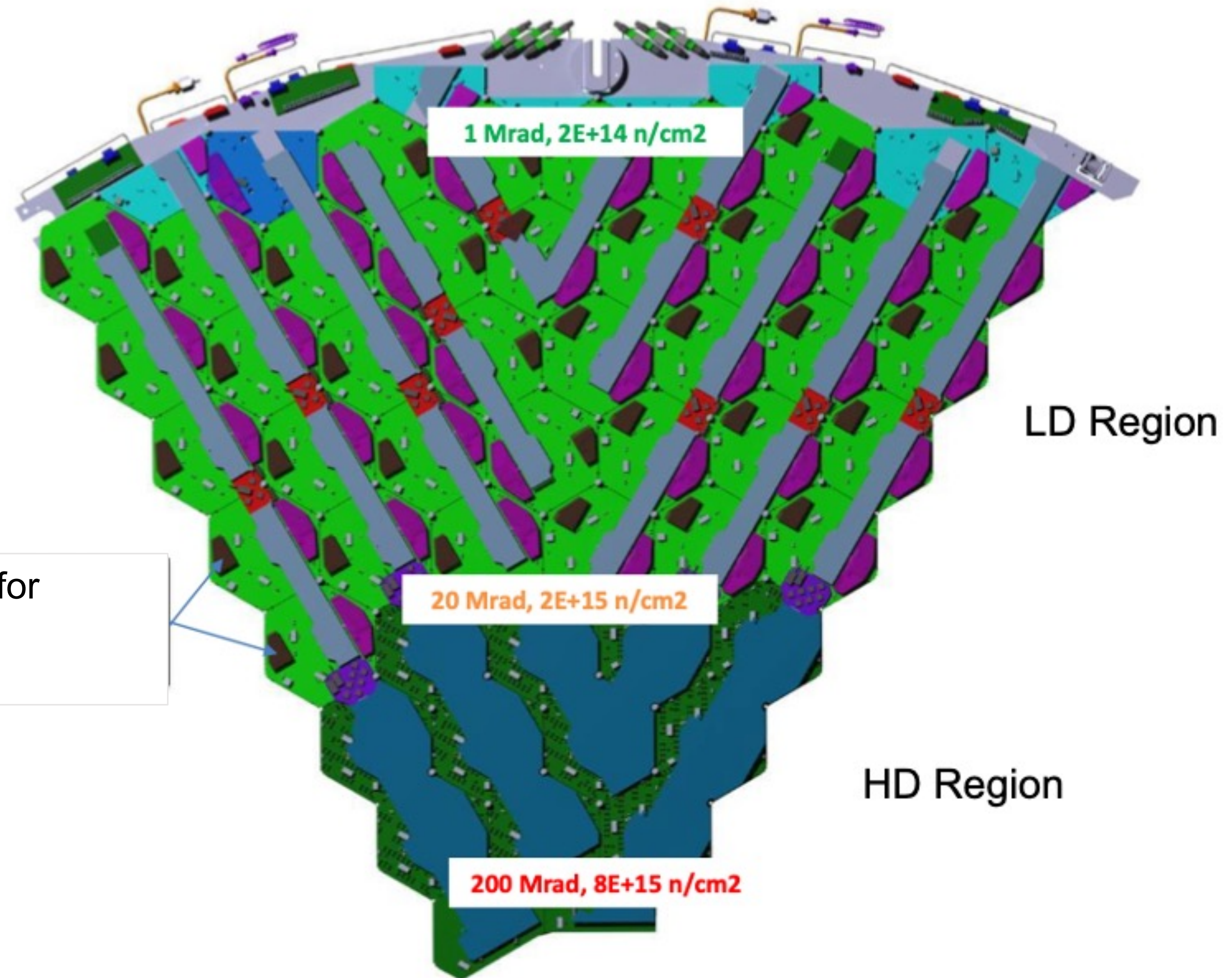
2) Need for uninterrupted services routing clearance



Radiation Environment

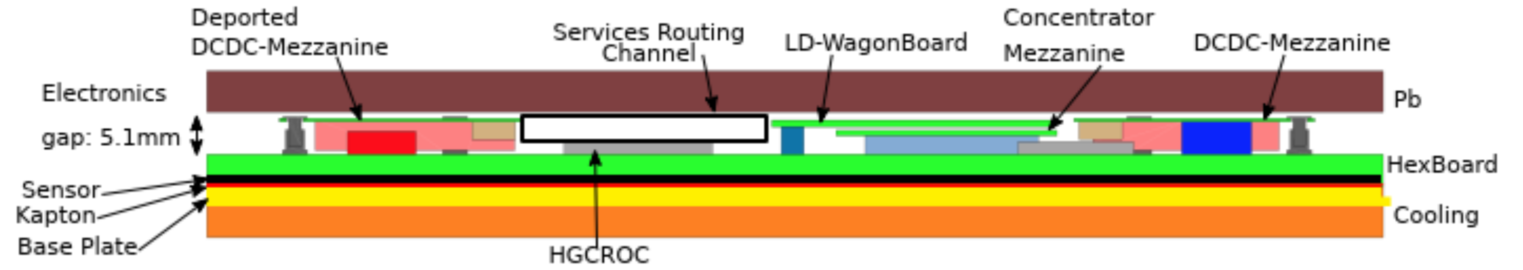
Affects the placement of certain components; VTRx+ and DCDC converters

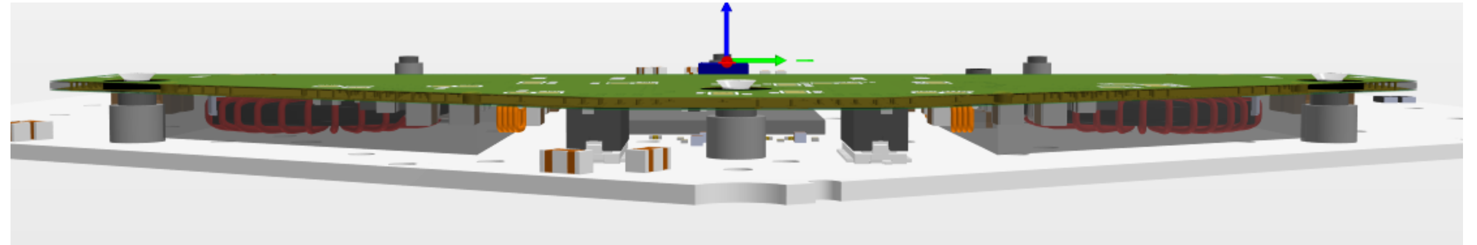
Deported DCDC modules for powering the HD region



Very demanding physical integration

Only 5.1mm to put all electronics (components, boards, services and optical fibres etc.).





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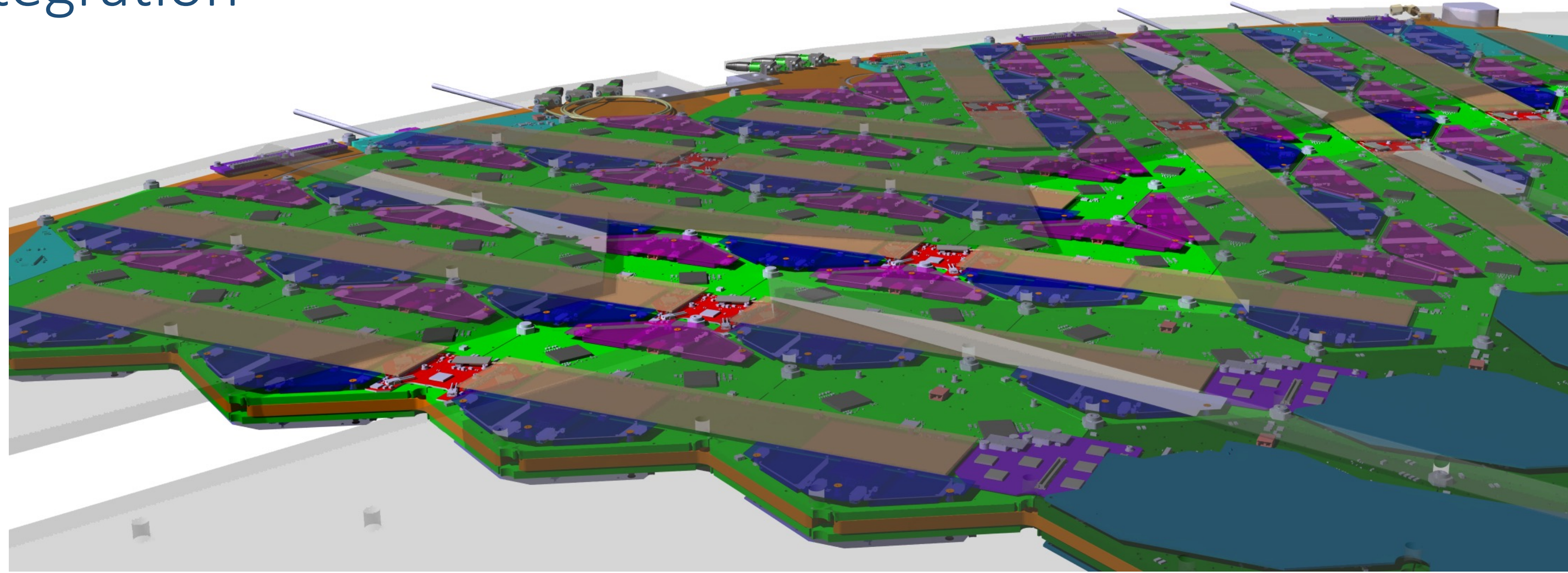

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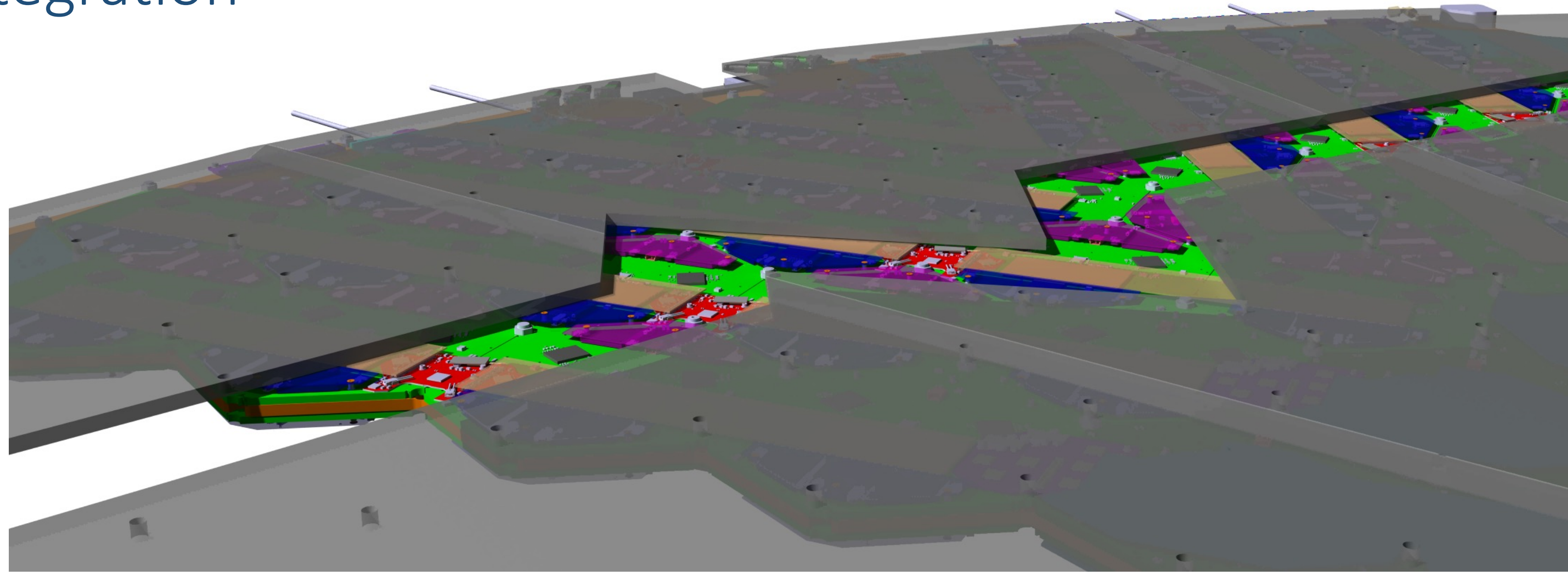
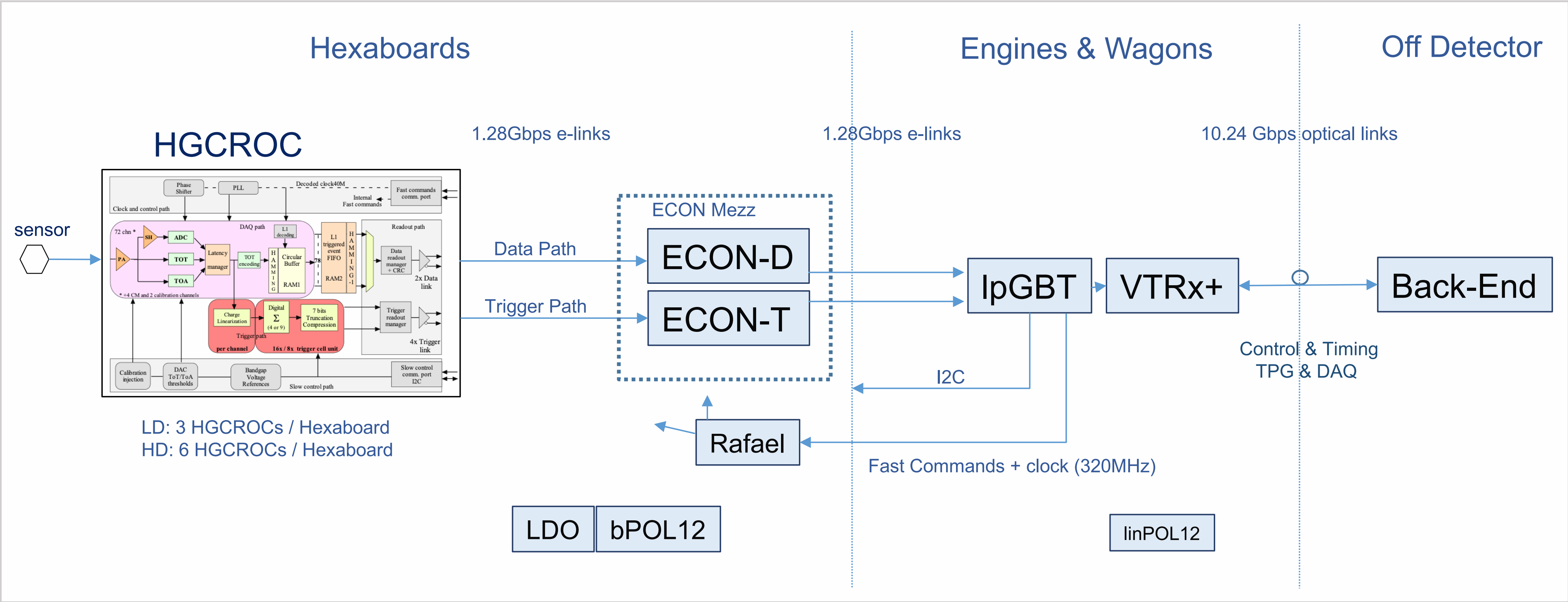


HGCAL Electronics – Main components and signal flow.



ASIC developments: HGCROC, ECON-T/D, LDO & Rafael

Generic components: lpGBT, VTRx+, DCDCs

These are hosted on pcbs: Hexaboards, Engines & Wagons (CE-E/H) & Tileboards (CE-H)

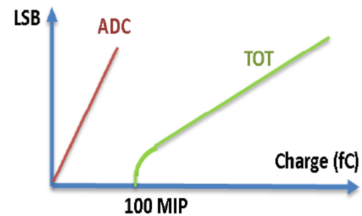
Note: The figure above is for the Si region.
The scintillator region is very similar. It uses a different version of HGCROC ie. HGC2ROCv3 and also uses the SCA for Slow Control and ALDO for SiPM biasing.

HGCROC Architecture specifications (TDR)

Analog
72 active channels
+2 for calibration
+4 for Common Mode

Dynamic Range ~0.2fC to 10pC
ENC < 2500e (Cd=65pF)
Peaking Time ~20ns
Linearity <1%
Pos. & Neg input charge

Energy Measurement
ADC 10b SAR
range 0 > 100fC (150fC)
TOT range 100fC > 10pC
TOT bin size 2.5fC



Time Of Arrival (TOA)
10b TDC , >12fC
lsb 25ps, 25ns full range

2 HGCROC versions:
Different preamps optimised for Si & SiPM readout

Phase Shifter
PLL
Clk 40M
Fast commands comm. port
L1
BxRst
Clock and control path
72x
SH
ADC
PA
TOT
TOA
Latency manager
TOT encoding
L1 decoding
Circular Buffer
L1 triggered event FIFO
72x
Readout path
Data readout manager
2x Data link
DAQ path
Charge Linearization
Digital Σ (4 or 9)
7 bits Truncation Compression
Trigger path
16x / 8x trigger cell unit
Trigger readout manager
4x Trigger link
Calibration injection
DAC ToT/ToA thresholds
Bandgap Voltage References
Slow control path
Slow control comm. port

Monitoring
Monitoring of DACs and essential bias voltages to SCA

Comm port
320MHz clock
Reception of T1 fast commands
From lpGBT

Data Readout Path
Data packets after LV1A
LV1A latency up to 12.5us
2 slvs outputs @ 1.28Gbps

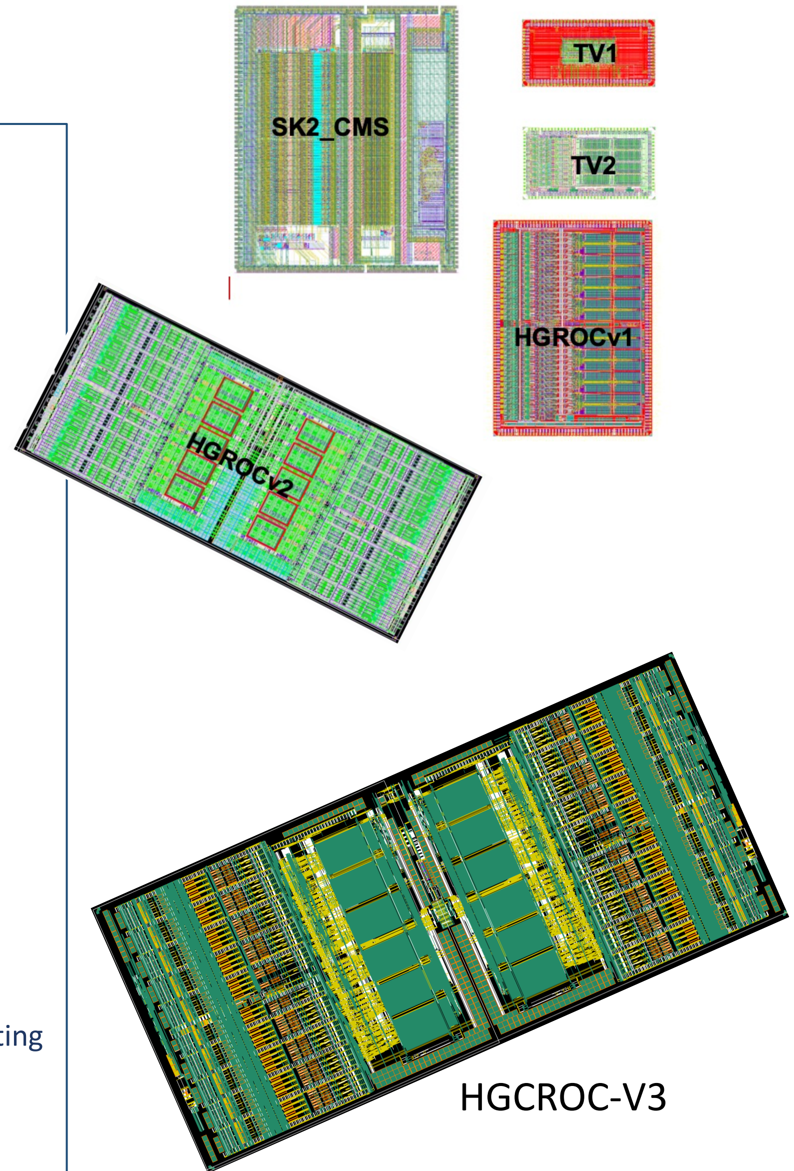
Trigger readout Path
Trigger primitives
max latency of 36bx
4 slvs outputs @ 1.28Gbps

Slow Control
Programmable registers
I2C protocol
Connected to SCA

HGCROC

HGCROC Prototyping history

SKIROC2_CMS …	ASIC for initial system prototypes & test-beam SiGe, analog with TOT Tape-out Jan. 2016, TWEPP 2016
TV1 & 2 … Test vehicles	130nm CMOS, TV1 preamplifier studies, TV2 analog channel Tape-out 2016, TV2 in TWEPP 2017
HGCROC-V1 …	Designed, fabricated & tested 130nm CMOS, Tape-out July 2017, TWEPP 2018
HGCROC-V2 …	Designed, fabricated & being tested TSMC 130nm CMOS Tape-out Feb. 2019 Naked and packaged chip characterisation done Extensive TID and SEE tests performed
HGCROC-V3 …	TDR Architecture Design submitted for fabrication in Dec 2020 TSMC 130nm CMOS Received May 2021 Packaging issues leading to modifications before testing could begin. Characterisation done on modified packages Mounted on V3 Hexaboards
HGCROC-V3b ….	Design in progress, expected to be production version. PRR in Nov 2022 followed by Eng Run for production.



HGCROC3 is the Full TDR Architecture

Fully functional,
Excellent analog performance

A few issues currently being worked on to arrive at HGCROC3b – production.

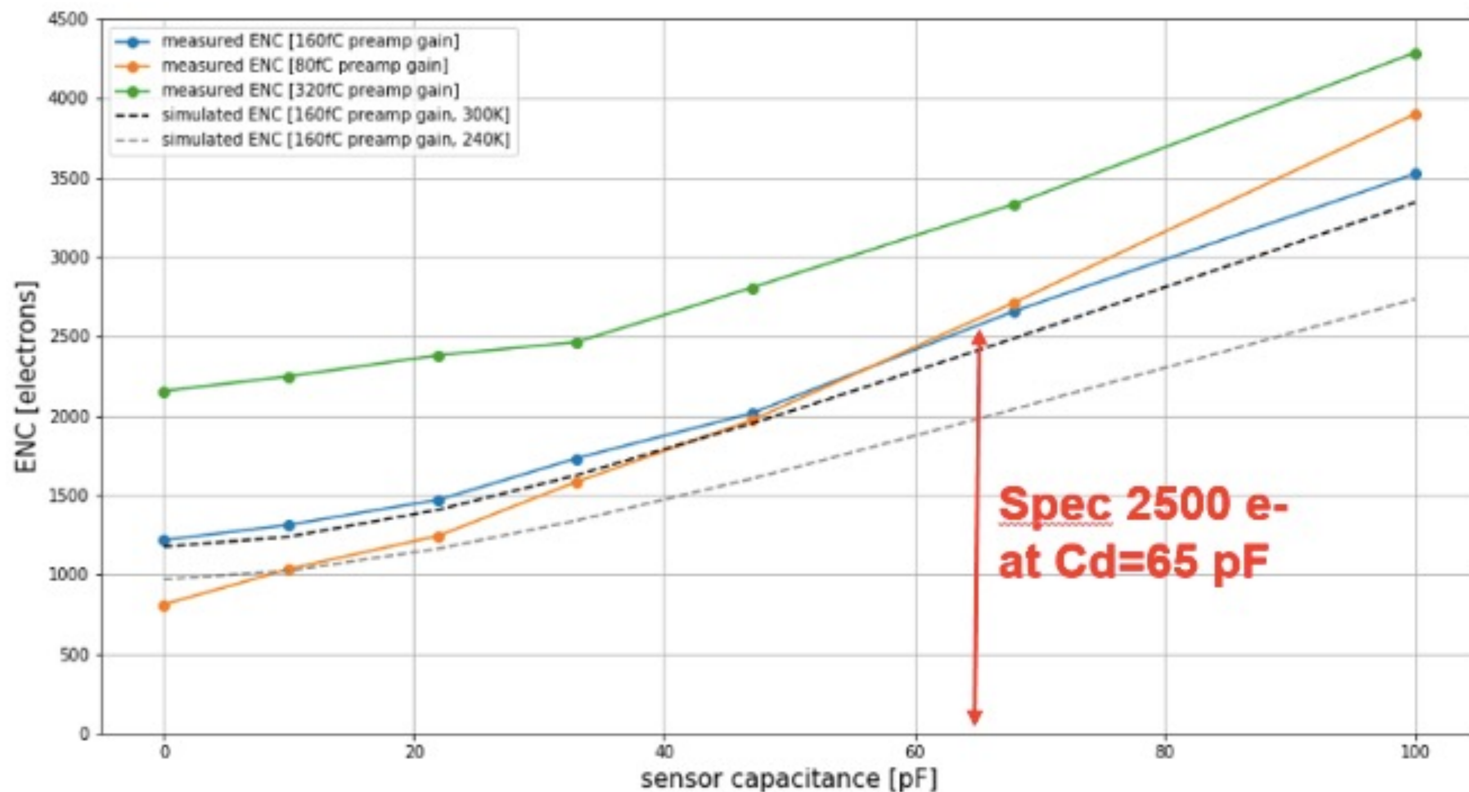
HGCROC3

HGCROC3 received in May 2021
Packaging
Semi-conductor crisis has led to very long turn around times in packaging.
1st round - HD HGCROC3 received July 2021, bug on package substrate, bump shorting VDD to GND.
– 2000 drilled packages, > 90% successful in removing short circuit. Used for characterization. *HGCROC drilling slide*
2nd round - LD HGCROC3new –Feb 2022 with bug corrected
3rd round - HGCROC3LDb package (separated returns (an & dig)).

HGCROC3 measurements
Analog and digital characterization,
The chip works very well
Analog performance excellent
Digital coupling degrades the analog performance at board level,
A few minor issues found on the digital side.
DRAM bit flips: 0>1 mechanism understood, reproduced by simulation, re-design strategy understood.
Statistically rare ADC sampling errors, studied, fixed and prototyped in an MPW.

HGCROC3b :
Expectation to submit the next version as HGCROC3b in January 2023 which will be the production version of the chip.

HGCROC3 ENC

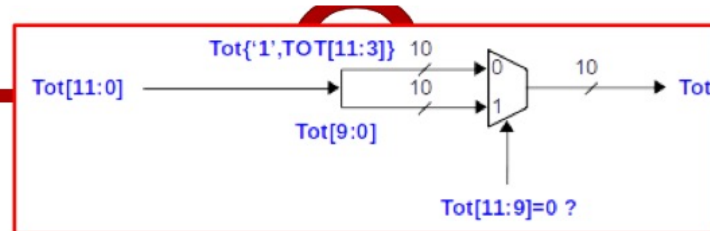


Signal ~22ke for 300um Silicon Sensor

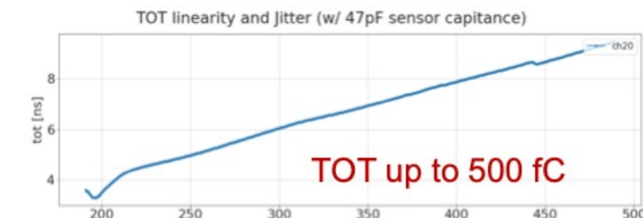
	0 pF Cdet	47 pF Cdet	68 pF Cdet
High gain ENC	900 electrons	2000 electrons	2750 electrons
Typical gain ENC	1250 electrons	2000 electrons	2700 electrons
Low gain ENC	2200 electrons	2800 electrons	3400 electrons
TOA FOM (1)	NA	2.5 ns/fC (FlipChip) 3 ns/fC (BGA)	3 ns/fC (FlipChip)
TOA noise floor (1)	20 ps	25 ps (FlipChip) 25 ps (BGA)	25 ps (FlipChip)
TOA Time-Walk	0.8 ns (FlipChip) 4 ns (BGA)	2.5 ns (FlipChip) 6.5 ns (BGA)	4 ns (FlipChip)

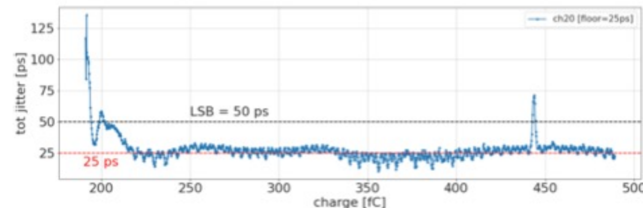
HGCROC3 Linearity

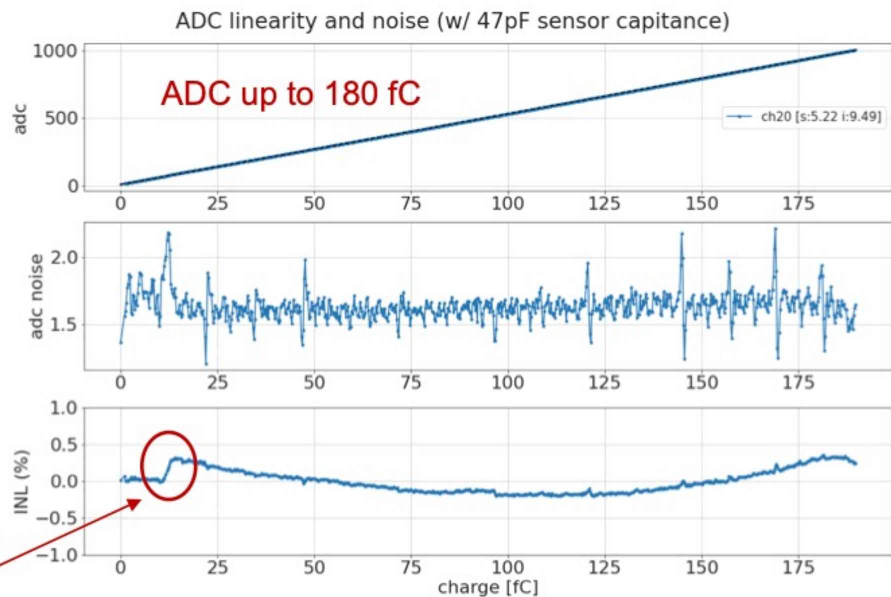
Charge

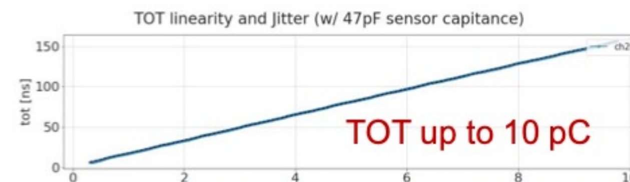


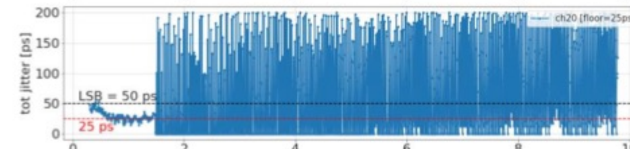
- ADC range
  - Linearity in +/- 0.5 %
- TOT range
  - Linearity in +/- 0.5 %
  - Jitter around 25 ps (50 ps binning)
  - TOT 12-to-10 compression visible on the jitter

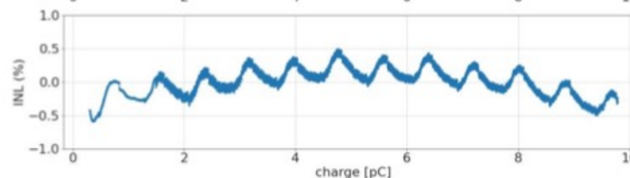






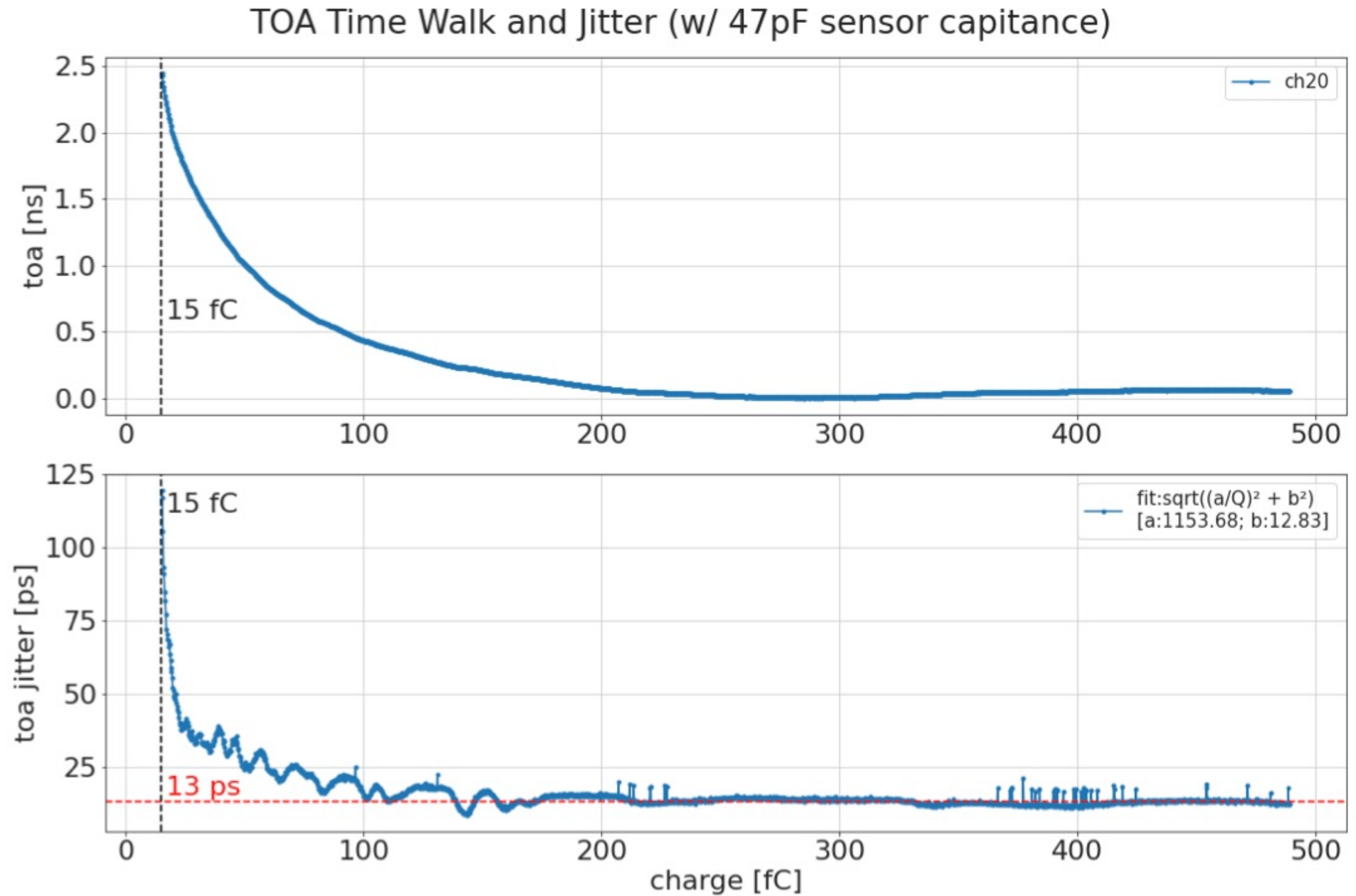




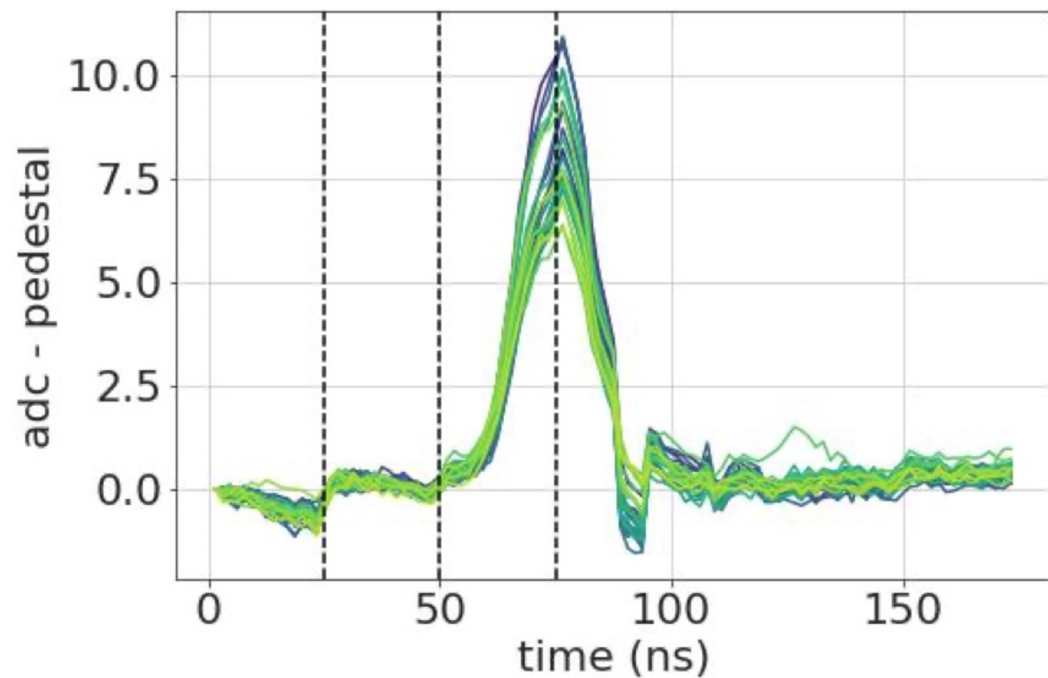


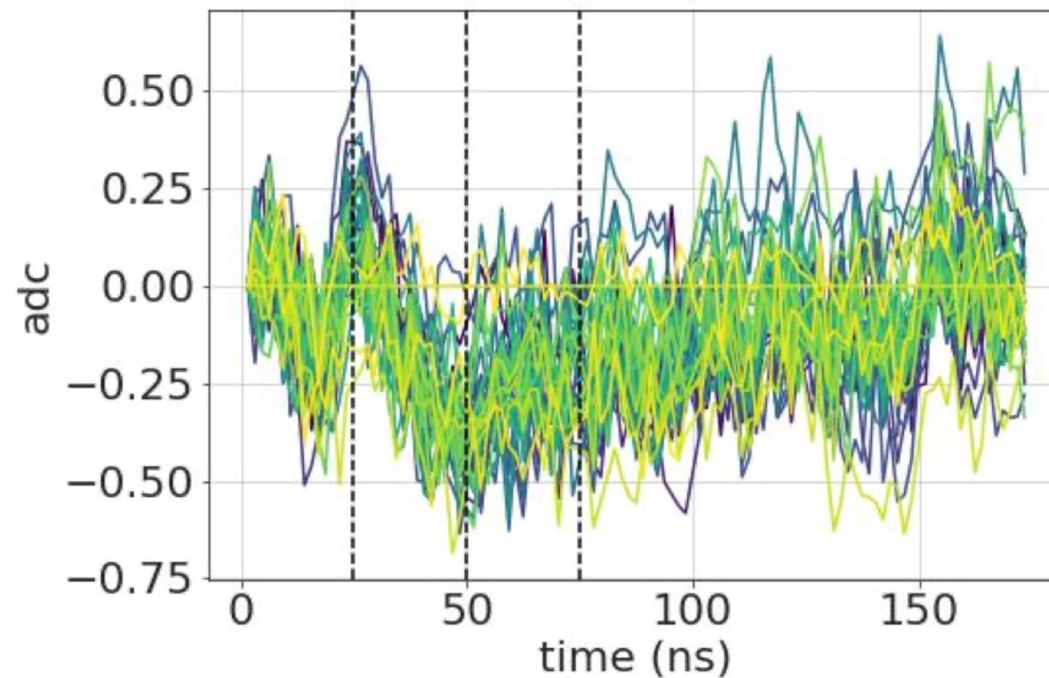
HGCROC3 Timing Resolution

- Threshold set to 15 fC
- Time walk
  - 2.5 ns
- Jitter
  - 1.8 ns/Q(fC)
  - 13 ps floor



HGCROC3 Crosstalk

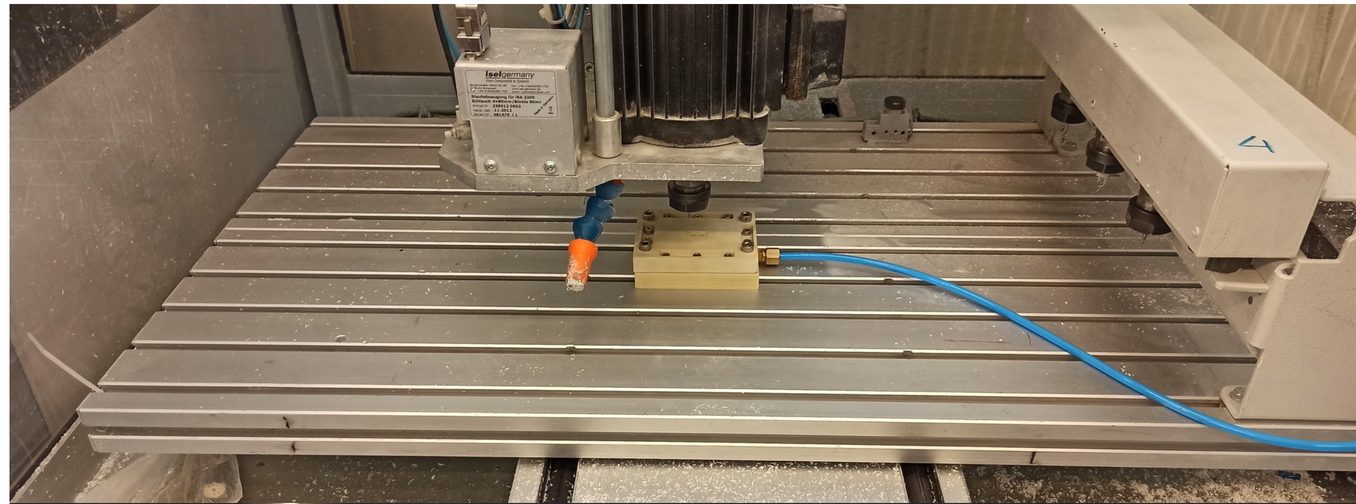


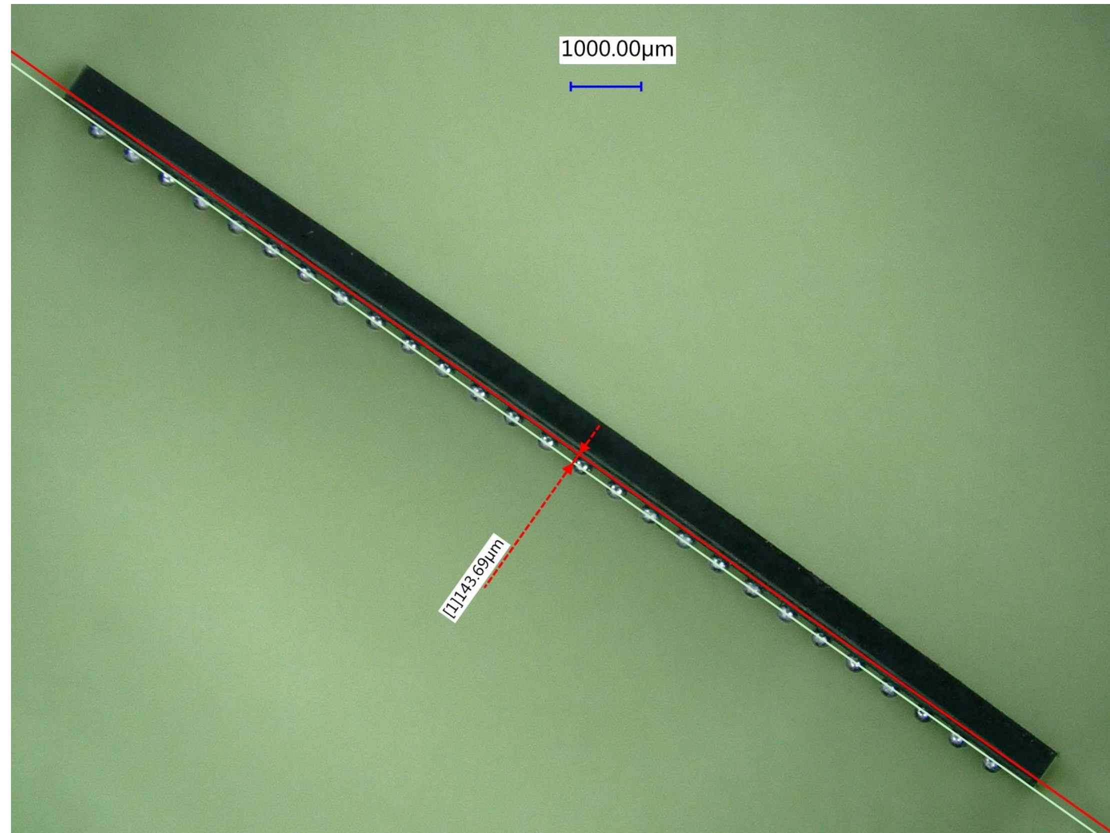


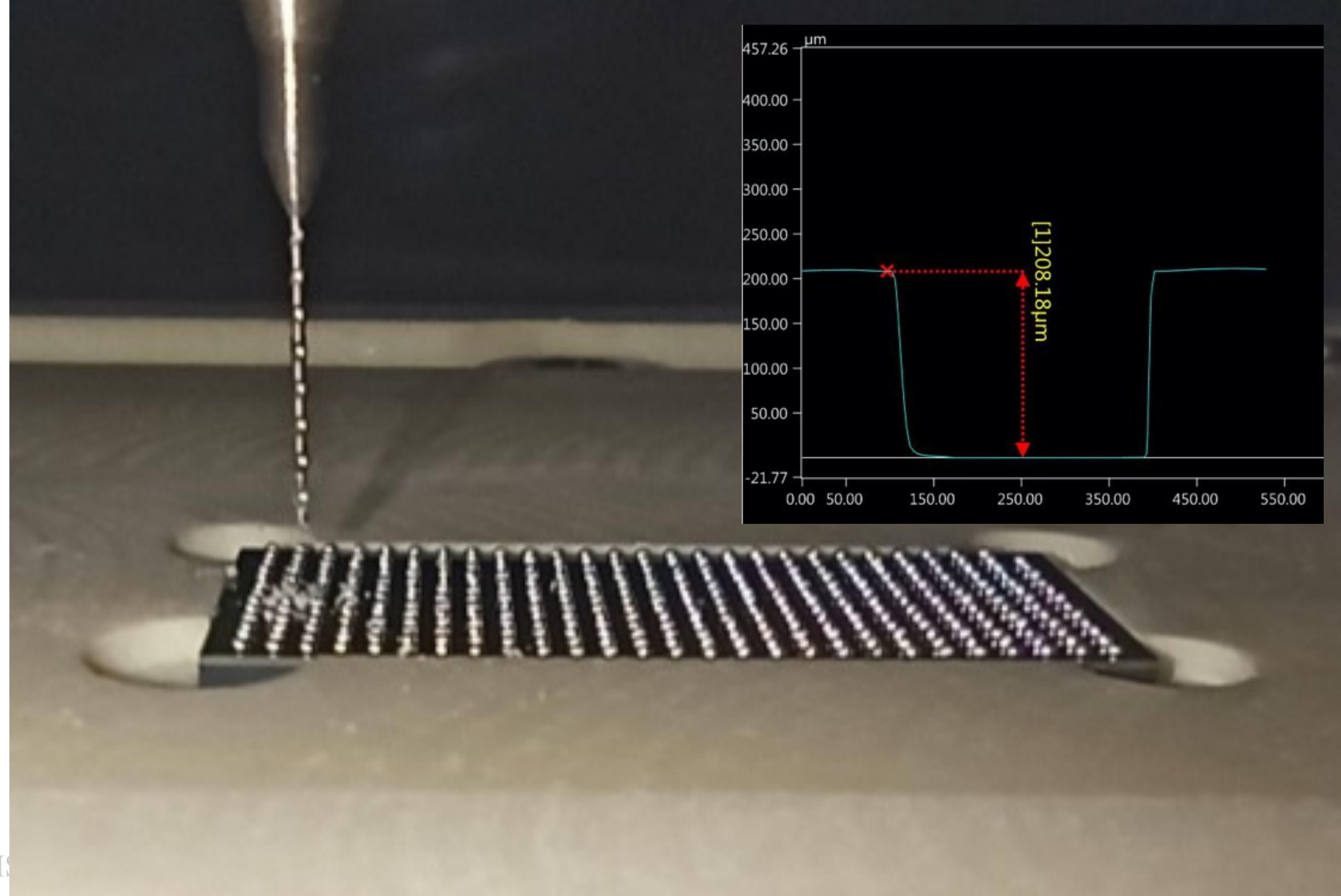
HGCROC3 Packaging – Precision Drilling

- Drilling to remove internal short circuit during summer.
- ESE.
- Jig with vacuum
- CNC milling machine
- Mill = 0.3mm
- Depth ~200um
- Difficult with arc in package

- Omega then subcontracted the process to industry.

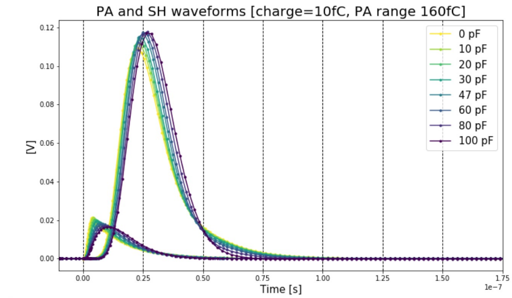






CMS

HGCROC3 - why minimising digital coupling is important



100 fF, 200 fF
20K to 100K
100 fF, 200 fF, 400 fF, 800 fF
PREAMPLIFIER NMOS input T
Calibration Circuit
TOT DISCRIMINATOR
Vth_tot
500 fF
5K
700 fF
RtR ampli
Vref_sk
TOA DISCRIMINATOR
Vth_toa
TDC (24 - 12 ps) CEA-IRFU
TDC (50 ps)
7K
500 fF
14K
Vref_inv
3K
1.16 pF
Vref_noinv
2.33K
SAR ADC (10b) Krakow

The ADC samples synchronously. So digital modulation with phase does not add to noise here.

HGCROC3 – digital coupling affects TOA and TOT

Critical node for digital coupling,

100 fF, 200 fF
20K to 100K
100 fF, 200 fF, 400 fF, 800 fF
PREAMPLIFIER NMOS input T
Calibration Circuit
5K 5K 700 fF 500 fF
RtR ampli
5K 5K
Vref_sk
TOT DISCRIMINATOR
Vth_tot
Vth_toa
TOA DISCRIMINATOR
TDC (24 - 12 ps) CEA-IRFU
TDC (50 ps)
7K 500 fF
RtR ampli
14K 7K
Vref_inv
3K 1.16 pF
RtR ampli
SAR ADC (10b) Krakow
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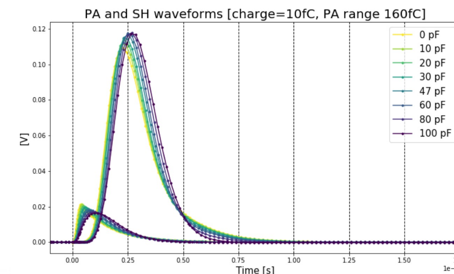
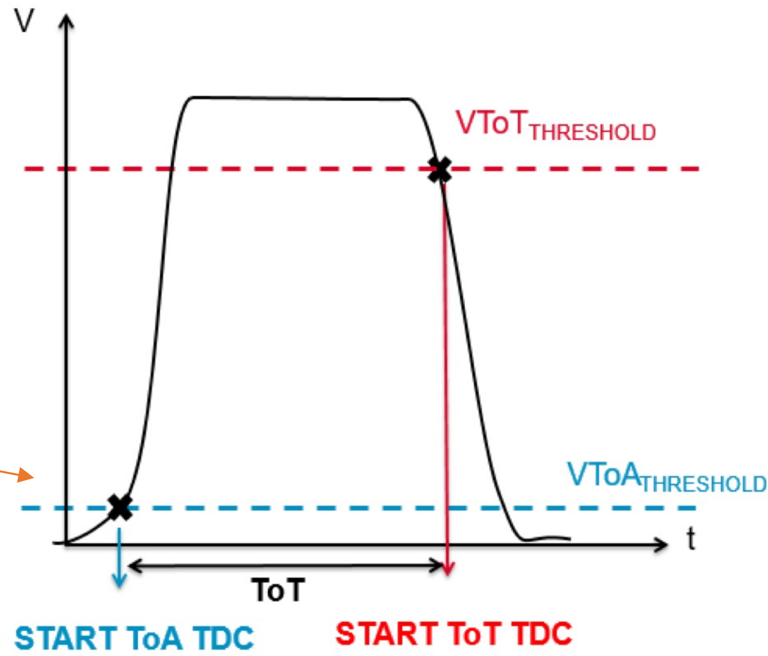
2.33K
RtR ampli
500 fF 7K
3K 1.16 pF
RtR ampli



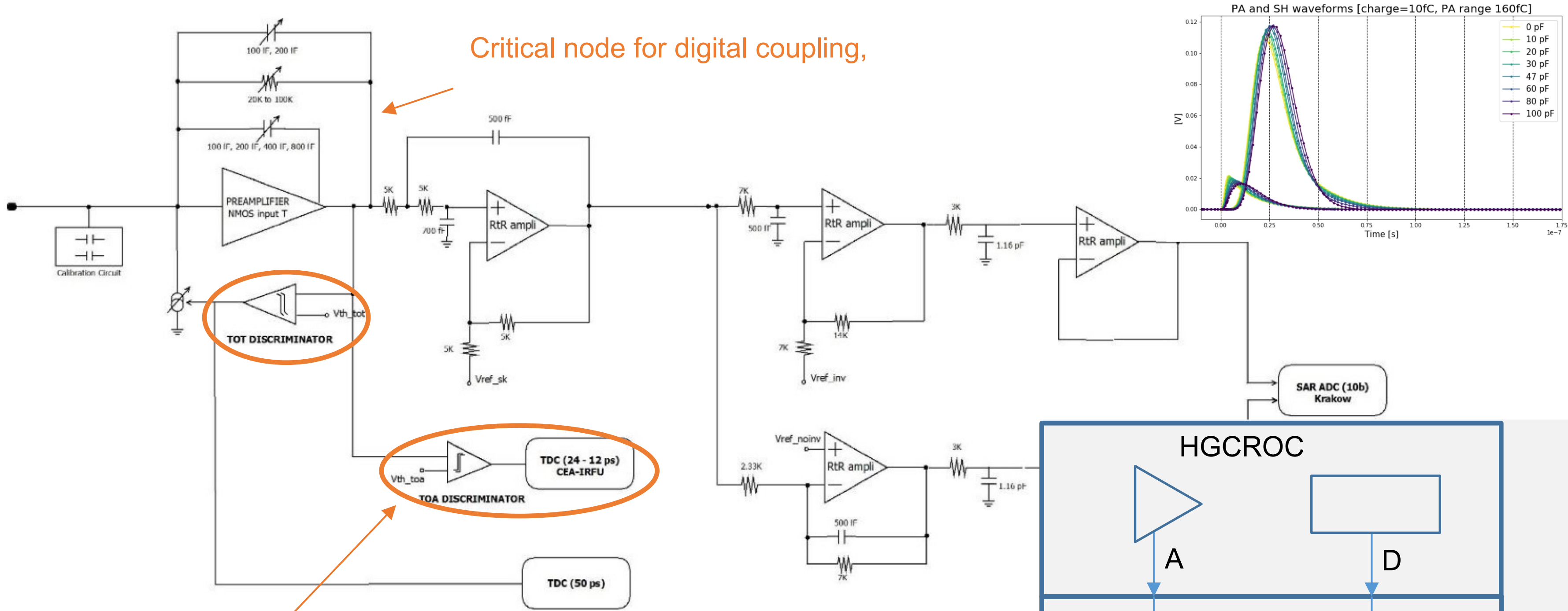
Asynchronous comparators for TOA and TOT are sensitive to digital pickup with respect to phase.
The digital coupling was initially a problem for the use of the TOA.

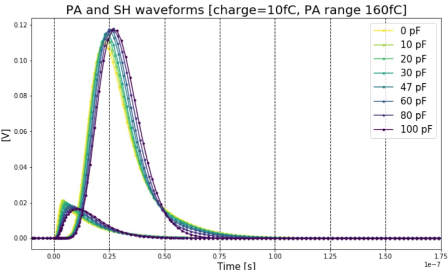
Digital coupling drastically reduced with package and Hexaboard optimization.



HGCROC3 – digital coupling affects TOA and TOT

Critical node for digital coupling,





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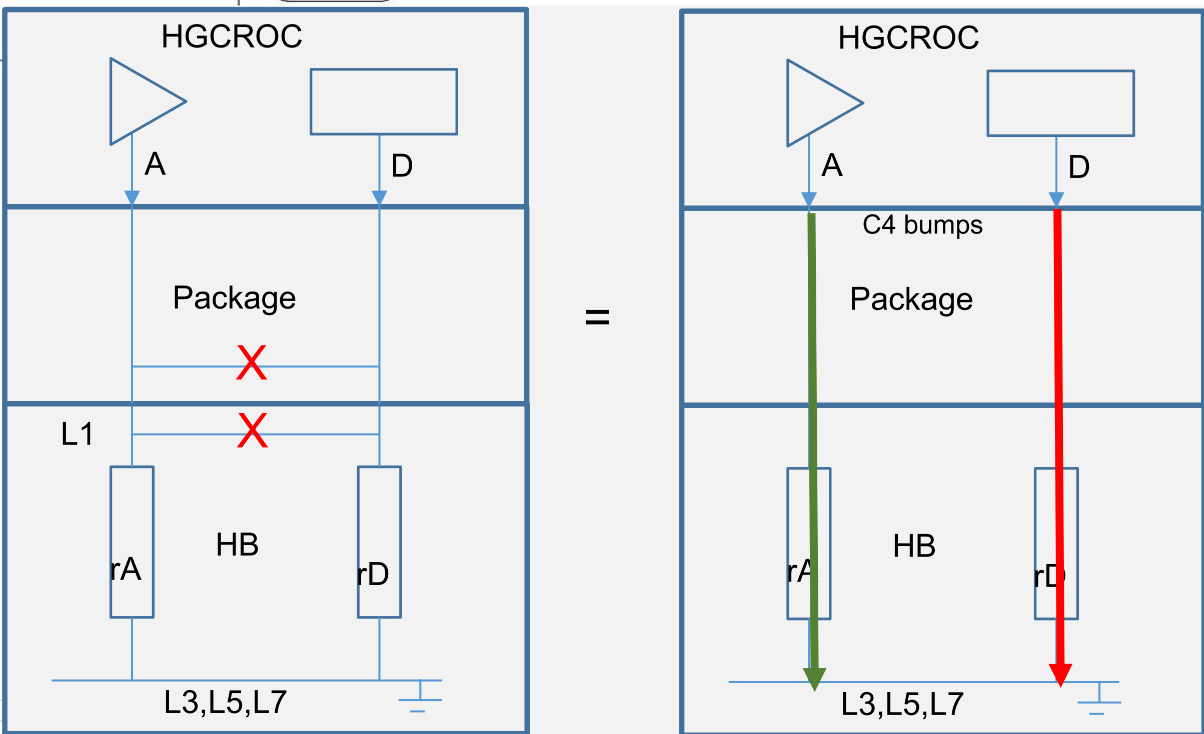
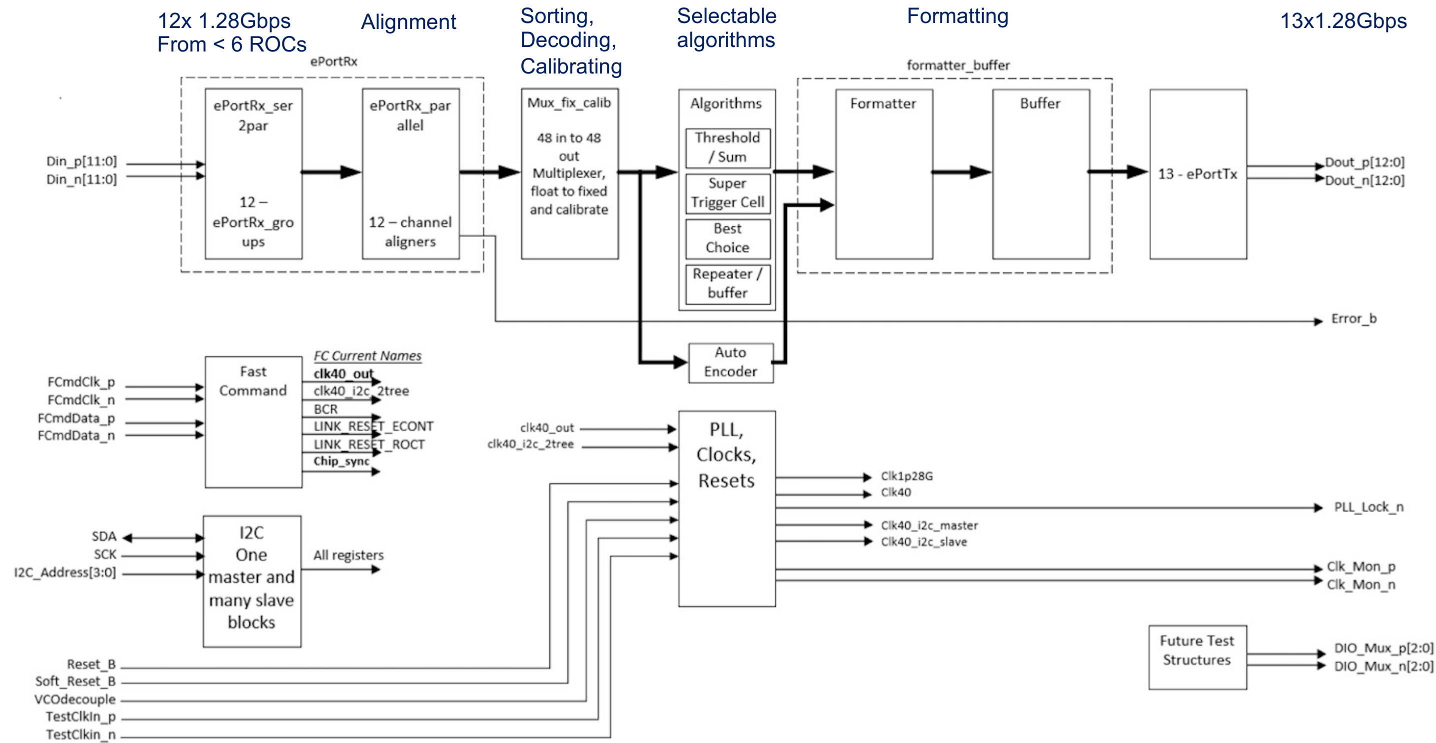


ECON-T



ECON-T: Select & compress interesting HGCROC trigger data for transmission off detector for every bunch crossing (40MHz).

ECON T/D
TSMC 65nm

Trigger data transmission 40MHz
DAQ data transmission at 750kHz

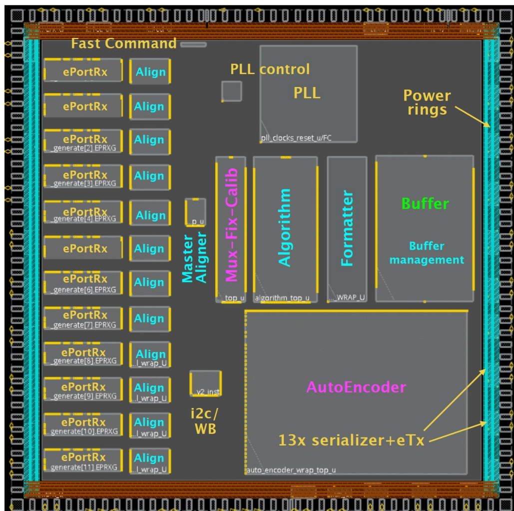
12 inputs (1.28Gbps)
13 Outputs (1.28Gbps)

lpGBT IP used for ePortRxGroup, PLL, eTx

Fast Command Block (6b8b inspired).

Power = 563mW

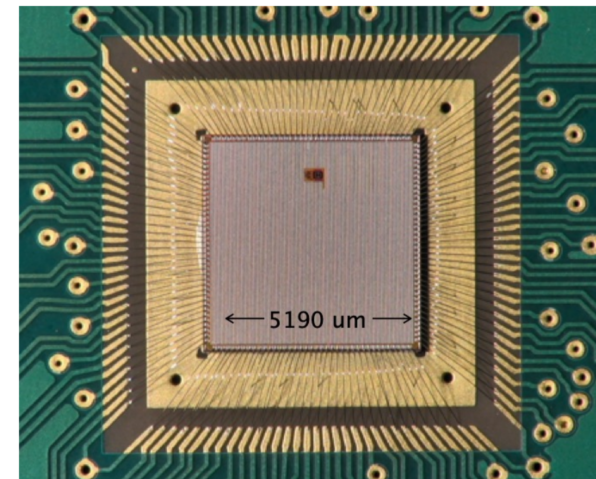
Latency: Threshold 19Bx
STC:...............8Bx
BC: 9Bx



ECON-Tp1 prototype without full triplication
Submitted for fabrication …. End of June 2021
Naked chip testing from end of Nov 2021

Functional and radiation tests done

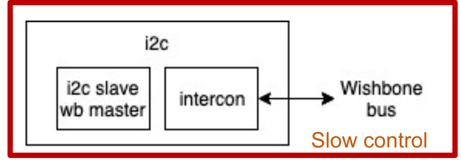
ECON-Tp2 will be the design with full triplication

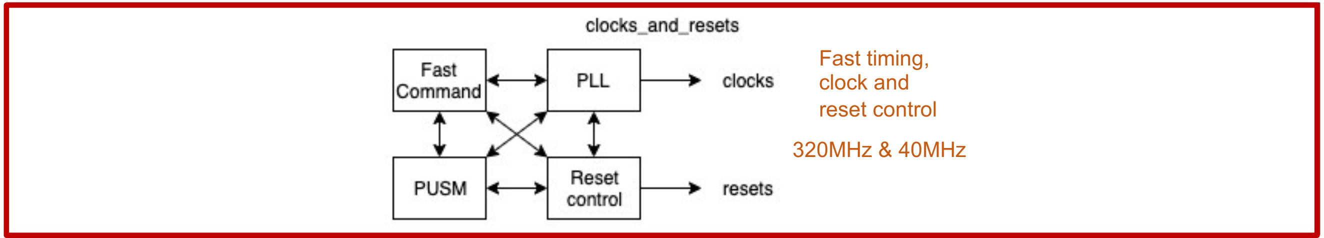


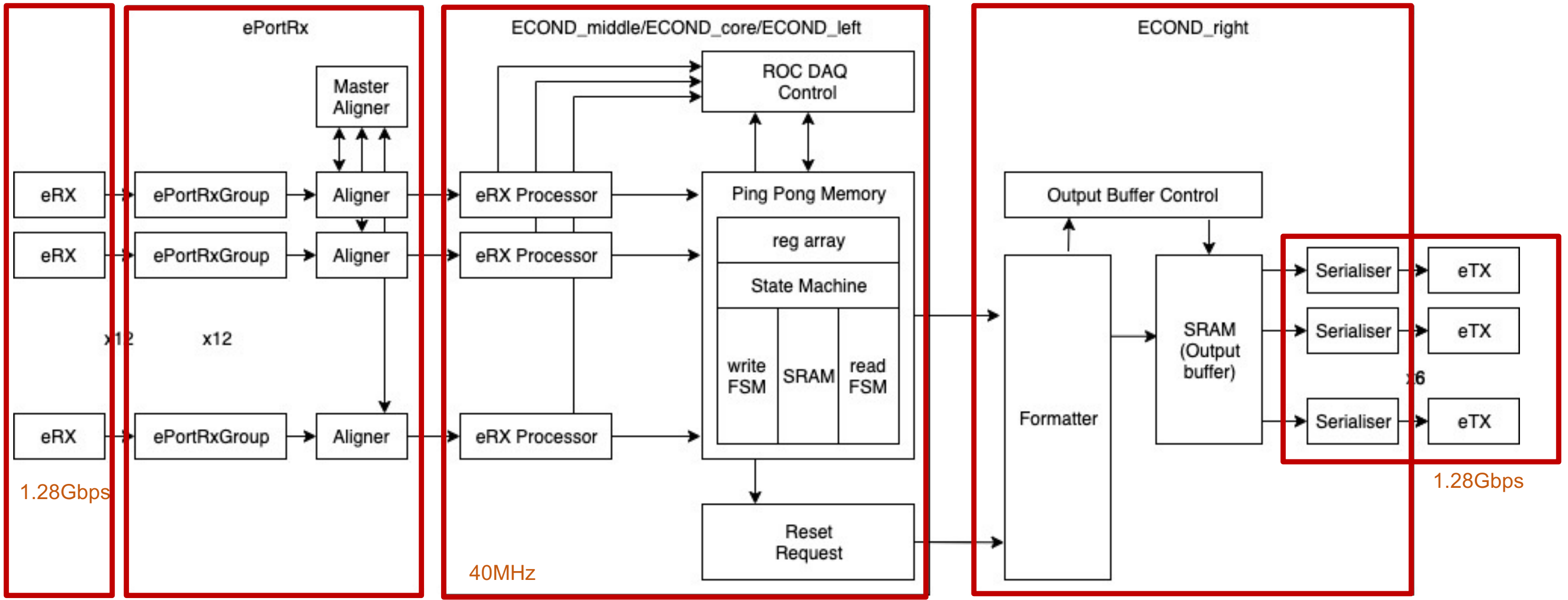
Fermilab

ECON-D

ECON-D: Receives HGCROC data packets after LV1A. Performs zero suppression and concentration of data up to L1 trigger rates of 750kHz.







Zero suppression
done here

Data formatting and
readout control

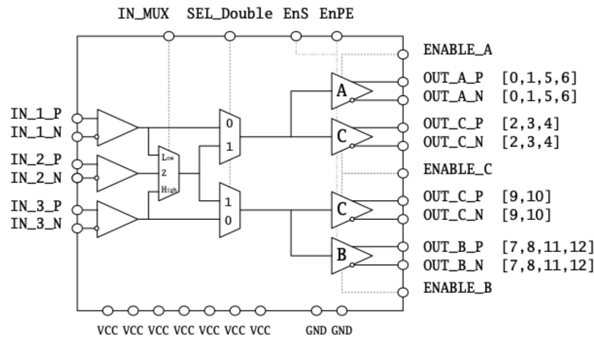
ECON-D design team
This year FNAL is complimented by 3 CERN microelectronics engineers via the CHIPs program.

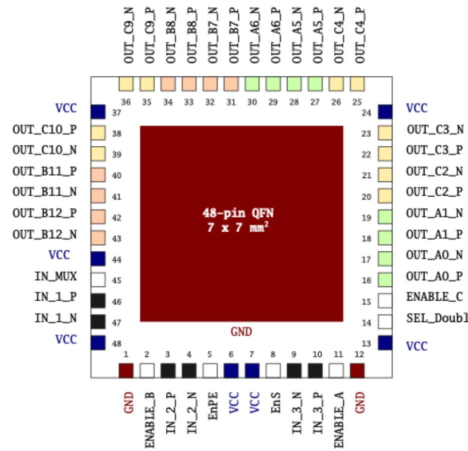
Aim to submit ECON-D as a final design, ie. Full functionality, fully triplicated and confident verification level.

ECON-D prototyped first on an FPGA as an emulator. Currently being tested within the system.

RAFAEL

A simple fan-out ASIC





- TSMC 130 nm
- 3 CLPS Inputs (compatible LVDS)
- 13 CLPS Outputs
  - *Signal strength : 2 mA or 1 mA (Differential : 400 mV or 200mV) or OFF (per bank A/B/C)*
  - *Pre-Emphasis : +2 mA or +1 mA or OFF*

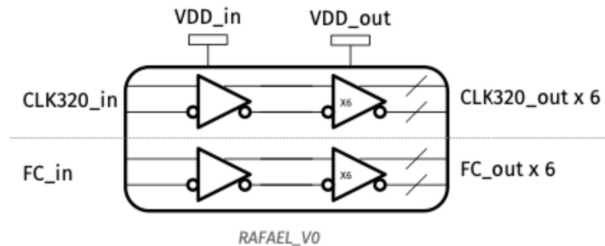
Double buffer mode:

- IN_1 → Outputs [0:6]
- IN_2 → Outputs [7:12]

Single buffer mode

- IN_1 or IN_2 or IN_3 → Outputs [0:12]

Used for FC and 320MHz clock fanout



RAFAEL_V0

Summary

- 130nm TSMC
- 7x7mm package
- Jitter = 9.6ps (double buffer mode)
- Power = 109 mW

History:

- Rafael v0, MPWs Dec2019, Dec2020 & ER Jul2021
- Functional test good but jitter 9.6ps in double buffer mode (high)
- TID tests to 390MRad ok

- Rafael v1 ER Jan 2021
- Jitter = 1.6ps in double buffer mode (much better).
- TID to 300 Mrad ok
- Neutron irradiation verified
- SET (some SET but not necessarily critical)

- Rafaelv2 MPW Dec2022
- Design to improve SEU robustness & improve packaging yield (larger pad openings).

- Packaging
- SERMA prototypes v1 very low yield (25%)
- Roodmicrotec 1100 Rafael v1 in packaging, available in Jul2022.
- Investigating Roodmicrotec for production packaging and test.

- Rafael PRR Q4 2022 followed by production.

LDO

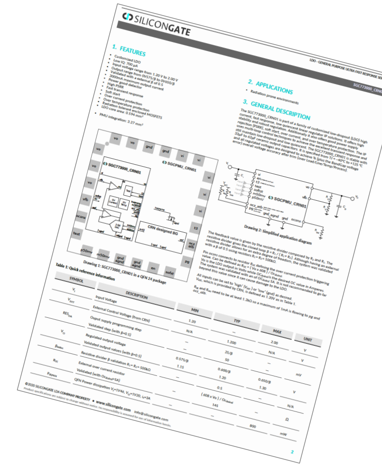
For low voltage conditioning of the HGCROC power supply.

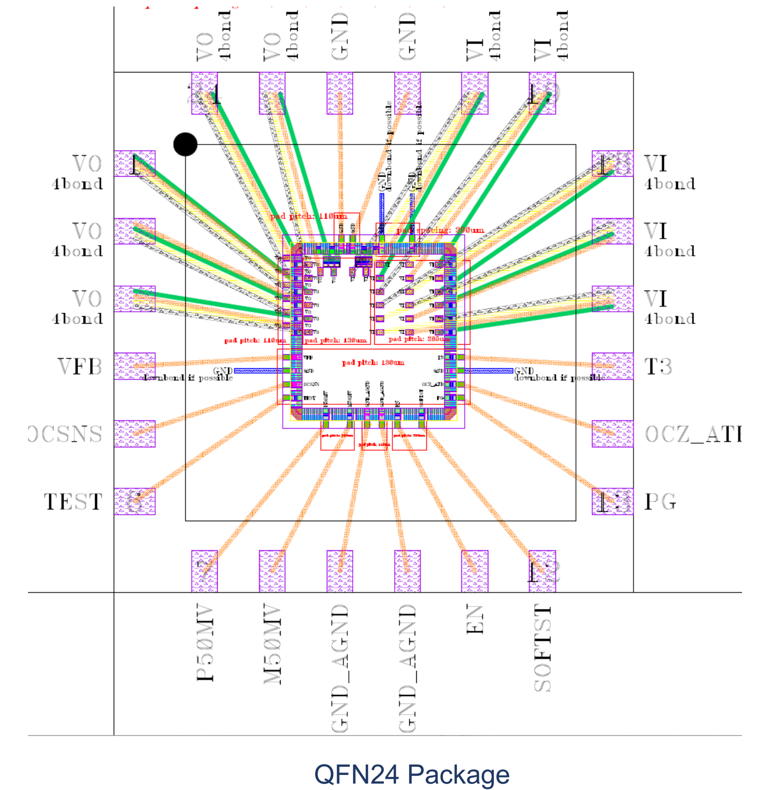
Design: with SiGate in Portugal under contract with CERN.

- TSMC 130nm, CRN01 LDO
- MPW submissions in 2020 and 2021
- Electrical characterization done at SiGate
- Very detailed characterization report delivered.
- Excellent results shown by A.Marchioro at TWEPP 2020
- Data Sheet available.
- 4 prototype versions made

Radiation tests at CERN

PRR expected in Q4 2022

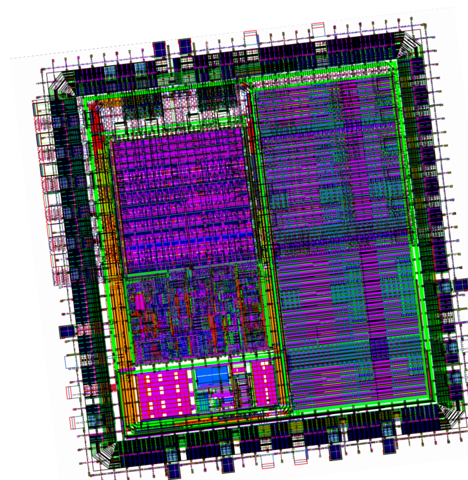


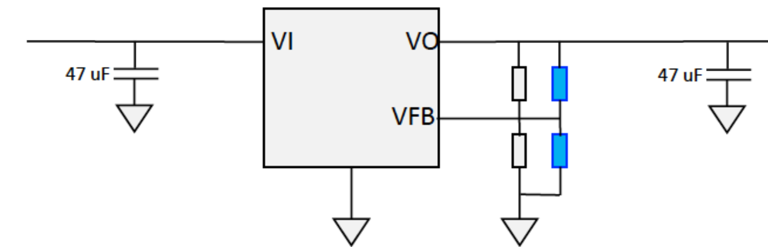


QFN24 Package

Summary Specifications

- Tech : 130nm CMOS
- I_{max} : 3A
- Vin_{max} : 2 V
- Adjustable V_{out} : 1.0 - 1.5 V
- V_{out}-V_{in} : 175 mV @ I_{max}
- OverTemp, overI protection
- Digital adjust : +/- 50 mV control
- Digital enable
- Max dissipation : 500 mW**
- Small form factor





Binning into 2 or 3 types for voltage adjustment using resistors mounted on the boards

DCDC Module Design

LD bPOL12 module

Hexaboards

The Hexaboards host the front-end HGCROC chips.

They provide the interface between the HGCROC channels and the sensor cells.

Also hosted are the Rafael and LDO ASICs.

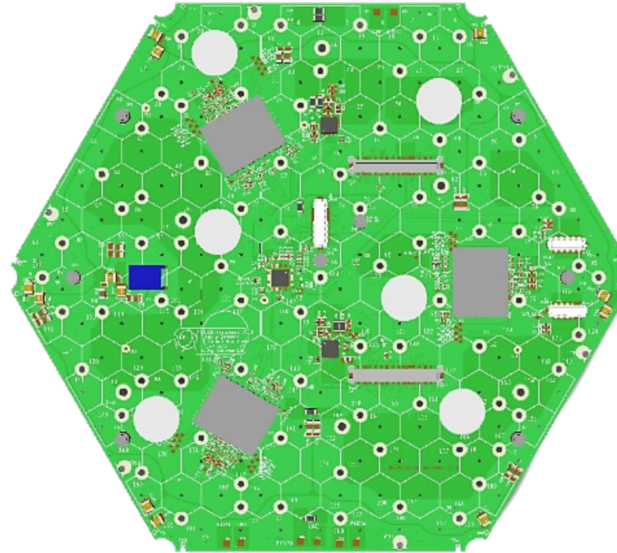
Very challenging pcb design to achieve low noise behaviour.

Prototype evolution leading to our V3 Hexaboard designs, (our production versions).

The V3LD has been prototyped, characterized, assembled into modules and used in beam tests.

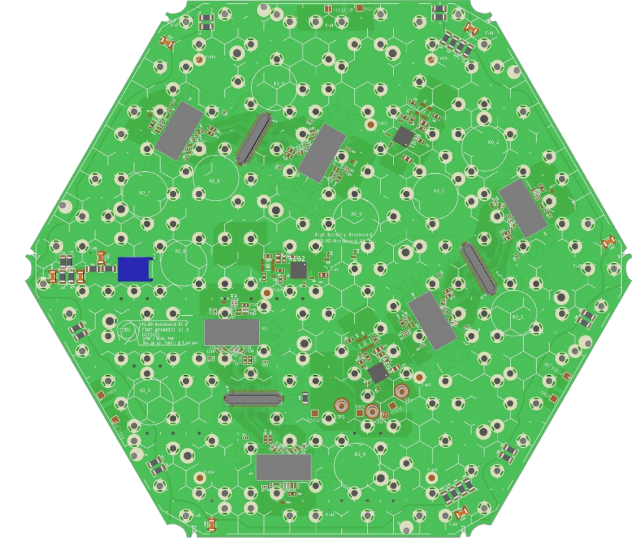
The V3HD has just been prototyped and now in characterization.

Low Density

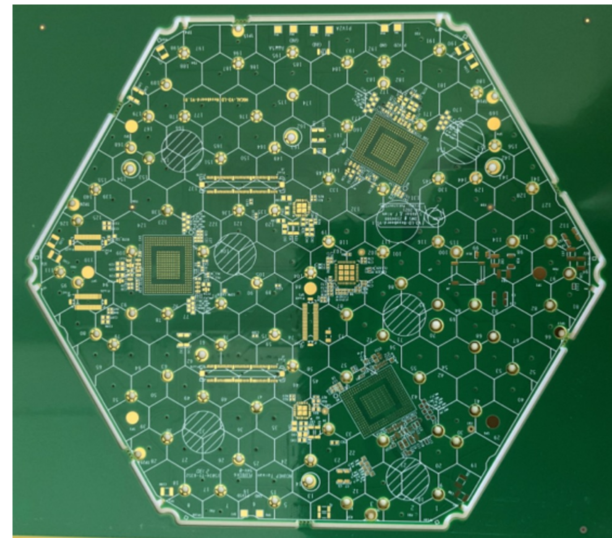


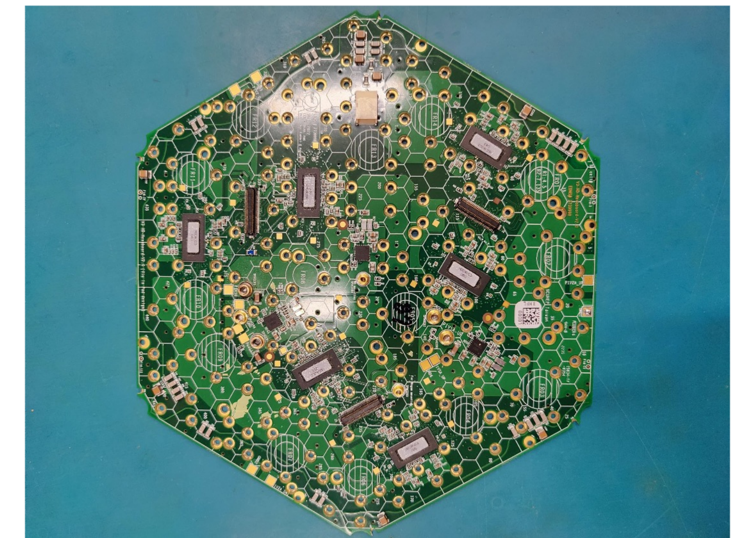
V3-LD-Hexaboard
3 x HGCROC-V3(LD-package)
Reads 192 Si cells(1.1cm^2)

High Density

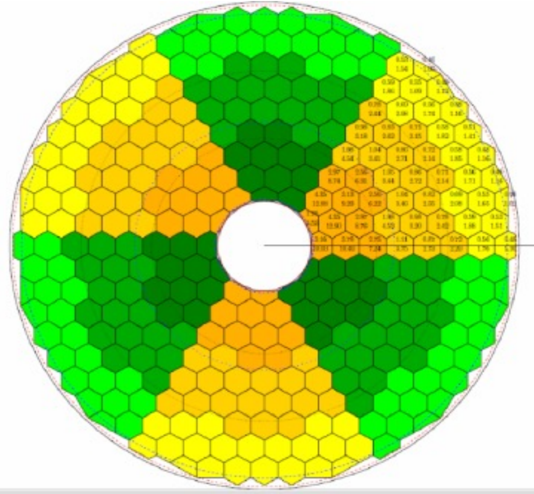


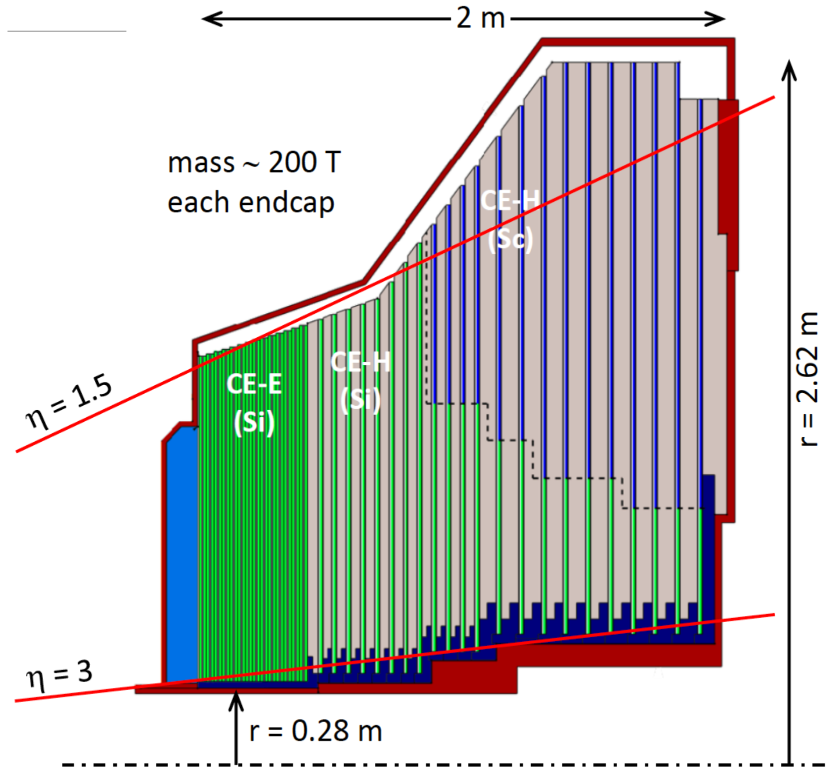
V3-HD-Hexaboard-V2
6 x HGCROC-V3(HD-package),
Reads 432 Si cells (0.5 cm^2)

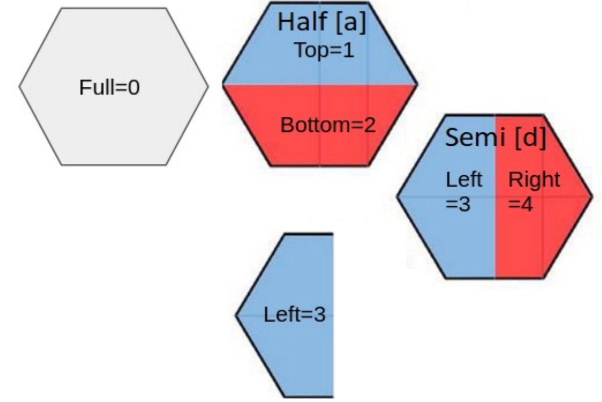


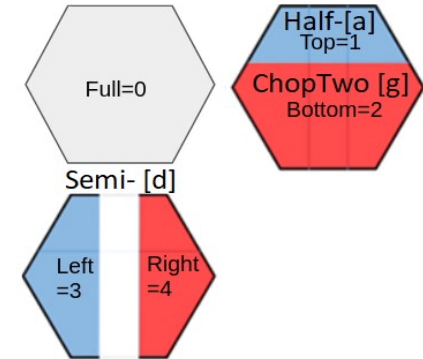


Hexaboard Variants









For maximum coverage of inner and outer radius
Each layer is different requiring different combinations of HBs and wagons

2 types of Full HB
8 types of partial HBs each with multiple variations
~12 variants in total

Each variant is applicable in many different physical locations
Hence each HB design has to consider:

- Compatibility with its own sensor type
- Cell mapping
- Electrical performance (crucial)
- Electrical inter-connectivity.
- Integration aspects using CAD 3D models
- Its own connector and component placements to avoid physical conflicts with other local boards.
- Physical support
- Thermal “cooling” properties
- Allowing space for other integration items such as service routing.

On Detector Powering System

- Uses bPOL12 + LDO (for regulating 1.2V)

- linPOL12V introduced for VTRx 2.5V

Note :
- Flexible voltage regulation.
- The LDO preforms voltage regulation for the ROCs.
- Point of load regulation; 4 adjustment values of 50mV increments is possible as the system ages.
- Powerful excel based tool developed including power trees, dcdc/LDO current dependent efficiencies, cable size, lengths etc. Calculating voltage drops everywhere.

PP0
Cassette Periphery
EngineBoard
WagonBoard
HexModule
Concentrator Mezzanine
ECON-T
ECON-D
VDDD = 1.2V
RAFAEL
10V
linPOL12V
2.5V
VTRx+
1.5V
LDO
1.2V
EN
lpGBT
x3
DCDC Module
bPOL12V
Low Density Regions
DCDCModule
HGCROC-D x3
VDDA = 1.2V
HGCROC-A x3
High Density Regions
x6
RAFAEL 1:13
VDDD=1.2V
HGCROC-D x6

- Deported DCDC modules : Located in the LD region but powering the HD region.
- A recent update is the addition of a 3rd bPOL12 on the deported DCDC module

bPOL12V modules

- HGCROC
- ECON
- Hexaboards
- Motherboards
- LDO & DCDC
- Tile-boards
- Test Systems
- System Baseline
- Cassette Integration
- Powering
- Timing
- Back-end

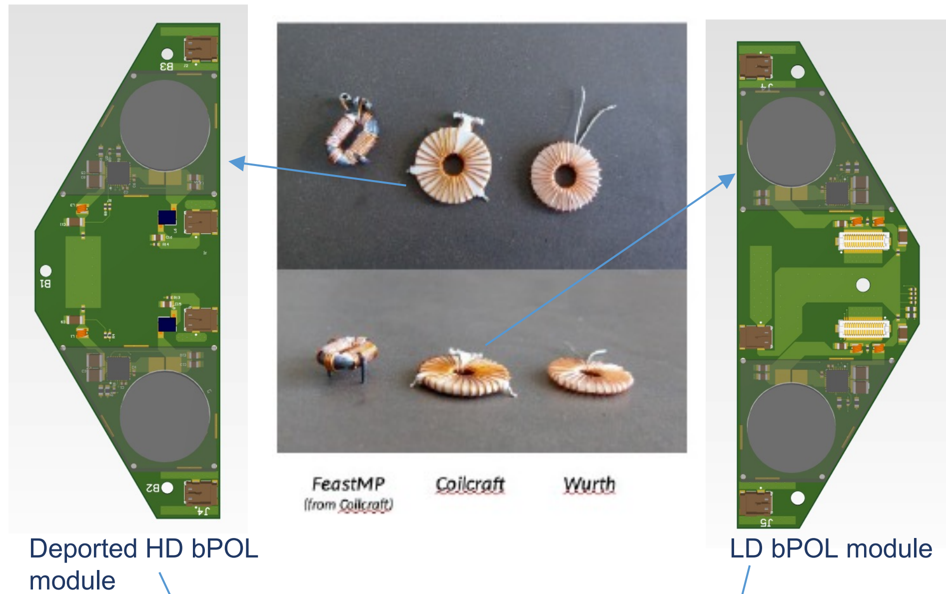
2 bPOL12V modules (LD and deported HD)
Custom coils, L~470nH, d~20mm, t~3mm

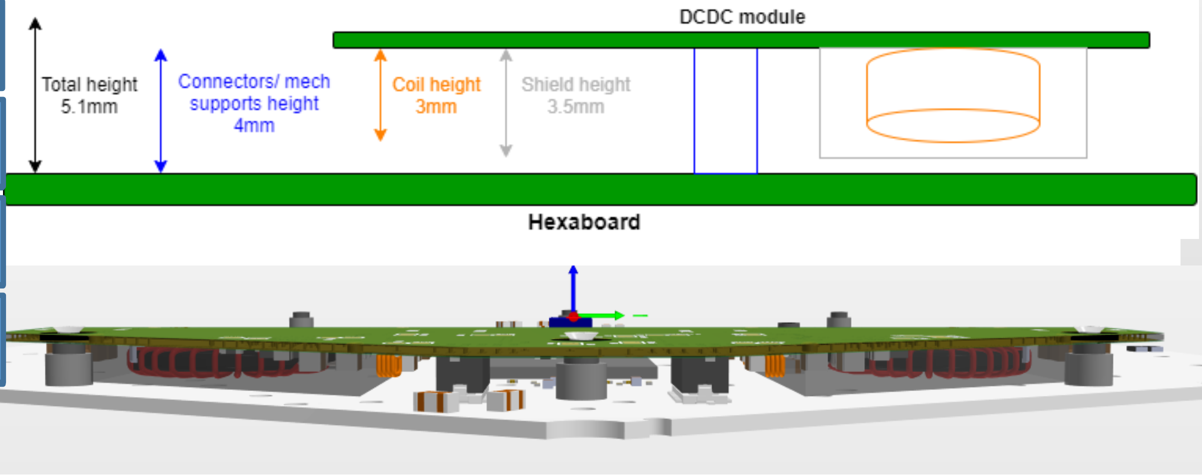
Mechanical models : for CAD
Very limited space (Vertically 5.1mm total)

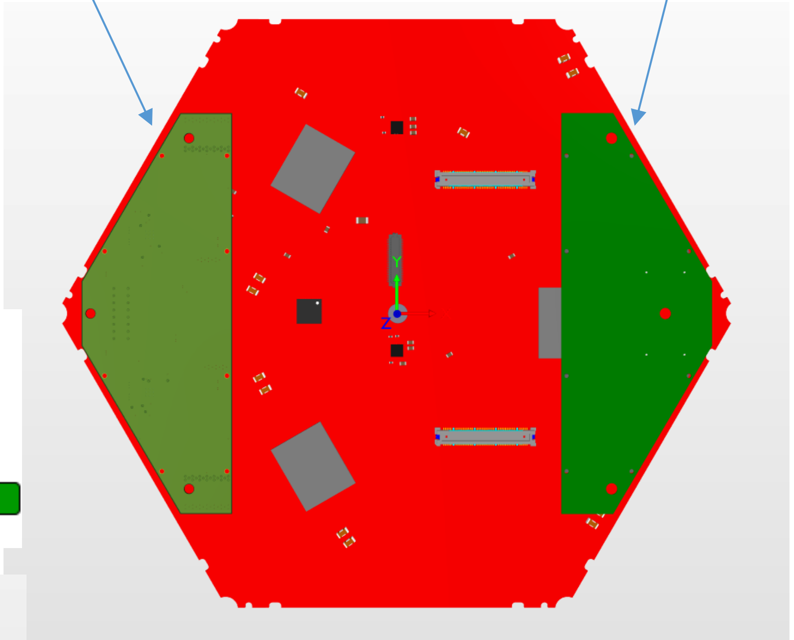
Thermal simulations done.
Initial dummy modules for mechanical tests

Electrical prototypes made with bPOLv4 and custom toroidal coils and shields.
Tests done for :
Efficiency, Thermal, Noise

A 3rd bPOL12V added to deported module for HGCROC analog load in the HD region initiating a study to reduce coil size.







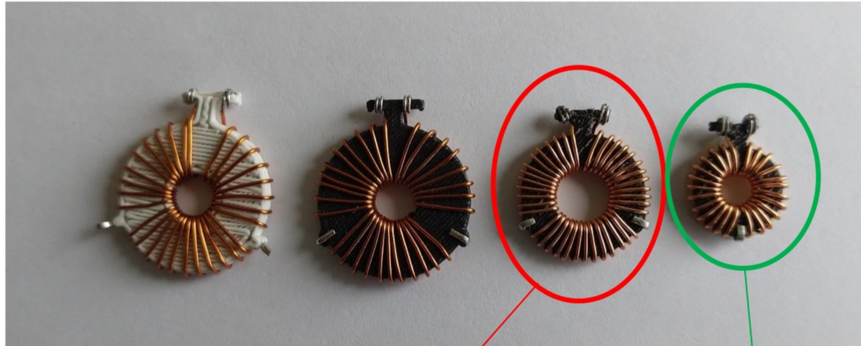
DCDC Module Design

LD bPOL12 module

Coil Studies

Efficiency vs physical size, inductance, DC-DC switching frequency

Coils prototypes

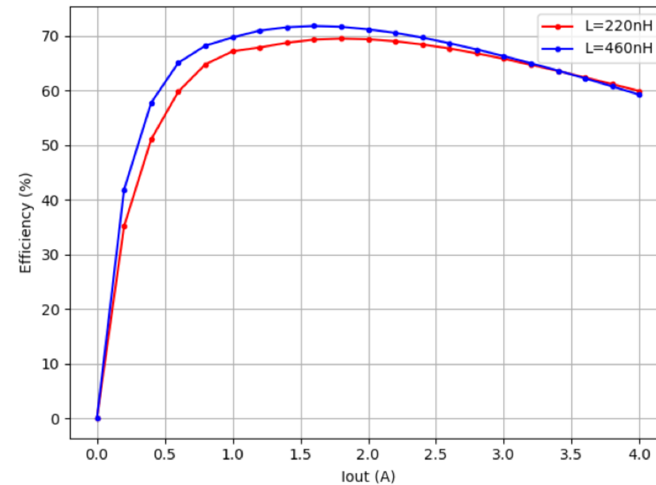


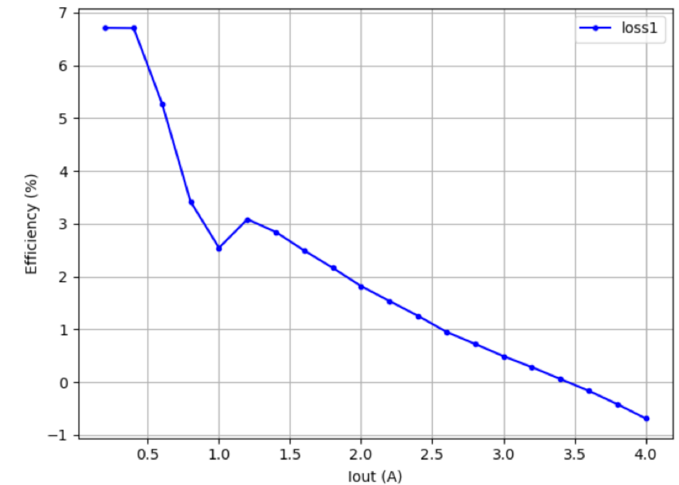
L = 460nH
fswitch = 1,7MHz
DCR = 60mΩ
Outer diameter = 16mm

L = 220nH
fswitch = 2,5MHz
DCR = 35mΩ
Outer diameter = 12m

Very little change in efficiency @ 2A load between the 2 coils measured.

Coil choice: impact on efficiency





Using the smaller coil will induce an efficiency drop that depends on the load current.
At smaller loads the drop is larger since the switching losses dominate,
while at higher loads conduction losses dominate, and the efficiency drop vanishes (the smaller coil has lower DCR)

Coil/Shield Studies

Noise emissions vs shield type

EMC measuring setup

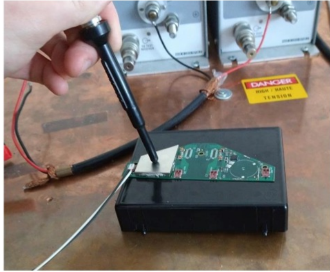
The near field probe set is designed as a diagnostic aid for locating and characterizing sources of E and H-Field emissions.

It is useful to compare measurements done with different coils/shields.

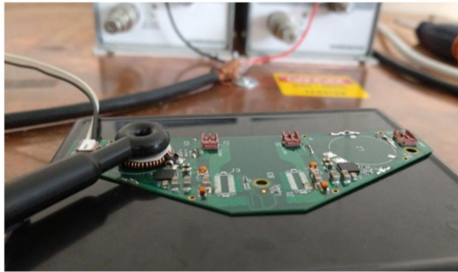
Spectrum analyzer

PC for data acquisition

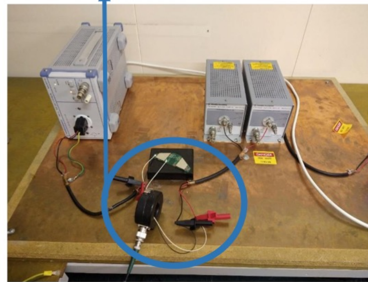
E near field probe



H near field probe



Current probe

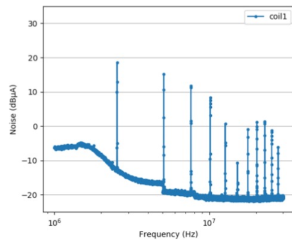


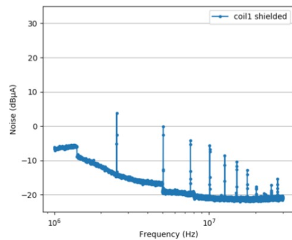
EMC tests: conducted noise

The results gathered show that the shield has a strong beneficial effect on conducted Common Mode noise.

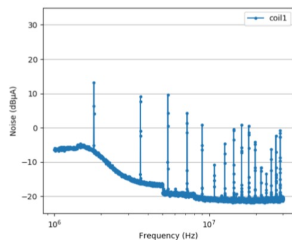
The measured noise levels show significant variations from coil to coil.

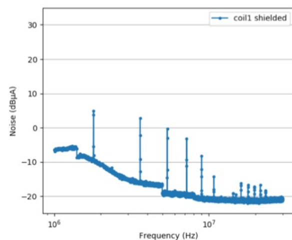
L = 220nH





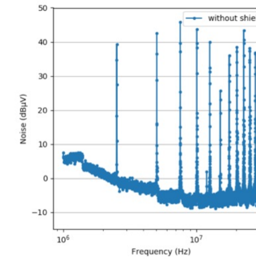
L = 460nH

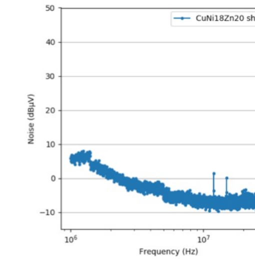


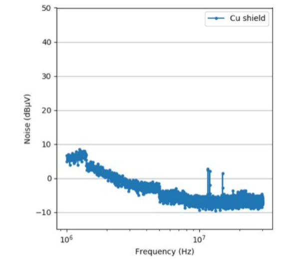


EMC tests: radiated noise (E)

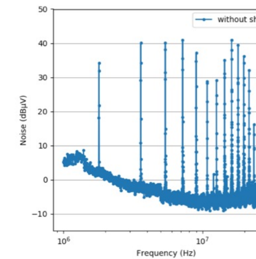
L = 220nH

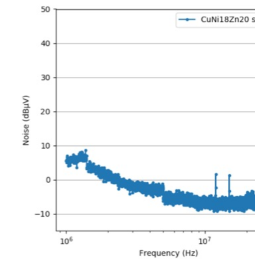


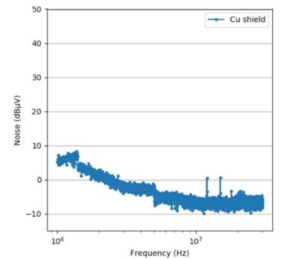




L = 460nH





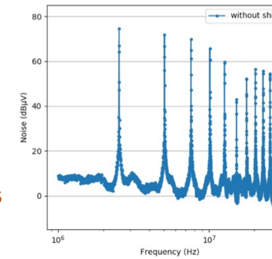


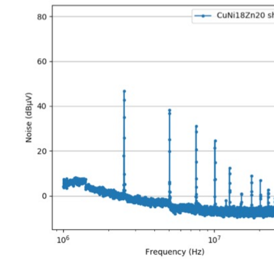
EMC tests: radiated noise (H)

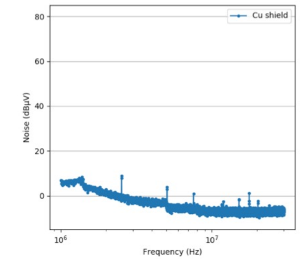
Very similar noise results between the 2 coil sizes.

Copper shield much better for radiated noise using the magnetic field probe.

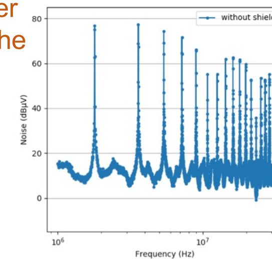
L = 220nH

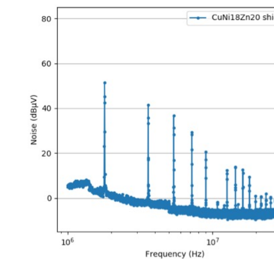


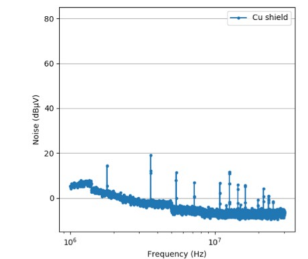




L = 460nH







bPOL12V module prototypes with custom coils and shields

Custom shield prototyped using a CuNi18Zn20 foil,
which was provided by a shield manufacturer

LD bPOL12V module prototype with custom coils

The prototype has been tested for : Efficiency, Thermal aspects, noise emissions with different shield types.

S. Caregari,
NCU Taiwan

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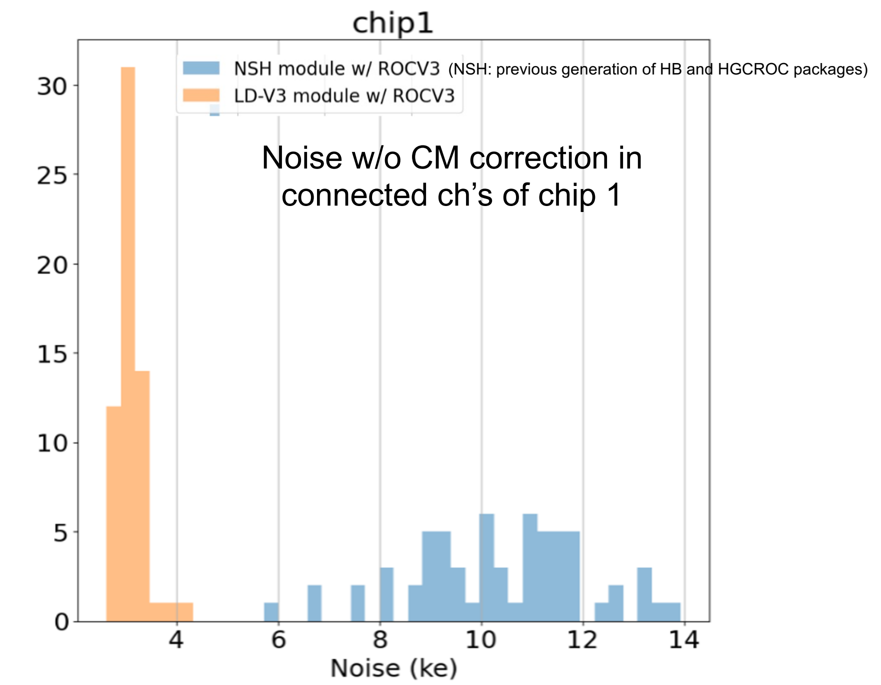
Hexaboardv3-LD Assembled

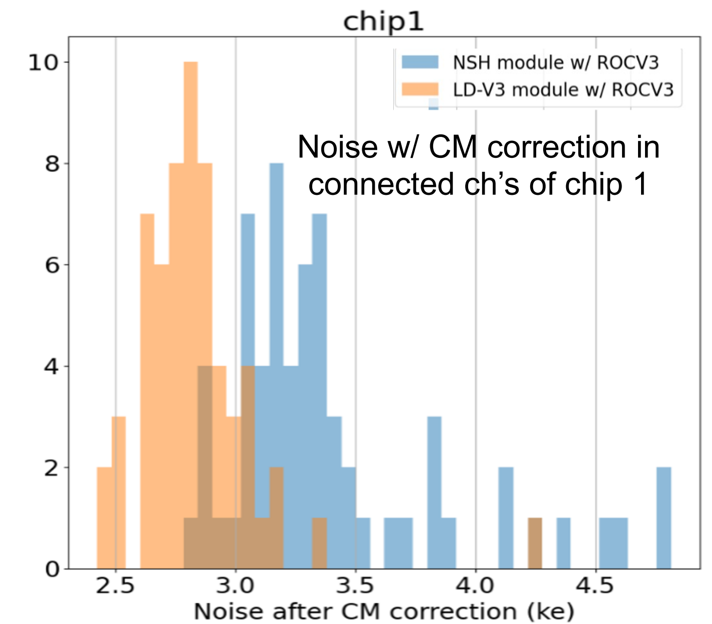
Noise measurements

Gain setting (320fC range).
CM channels facilitate CM correction.

Comparing the previous generation (NSH module) with the current V3 module.

Improvements in Hexaboard and HGCROC package design have greatly improved the noise performance.

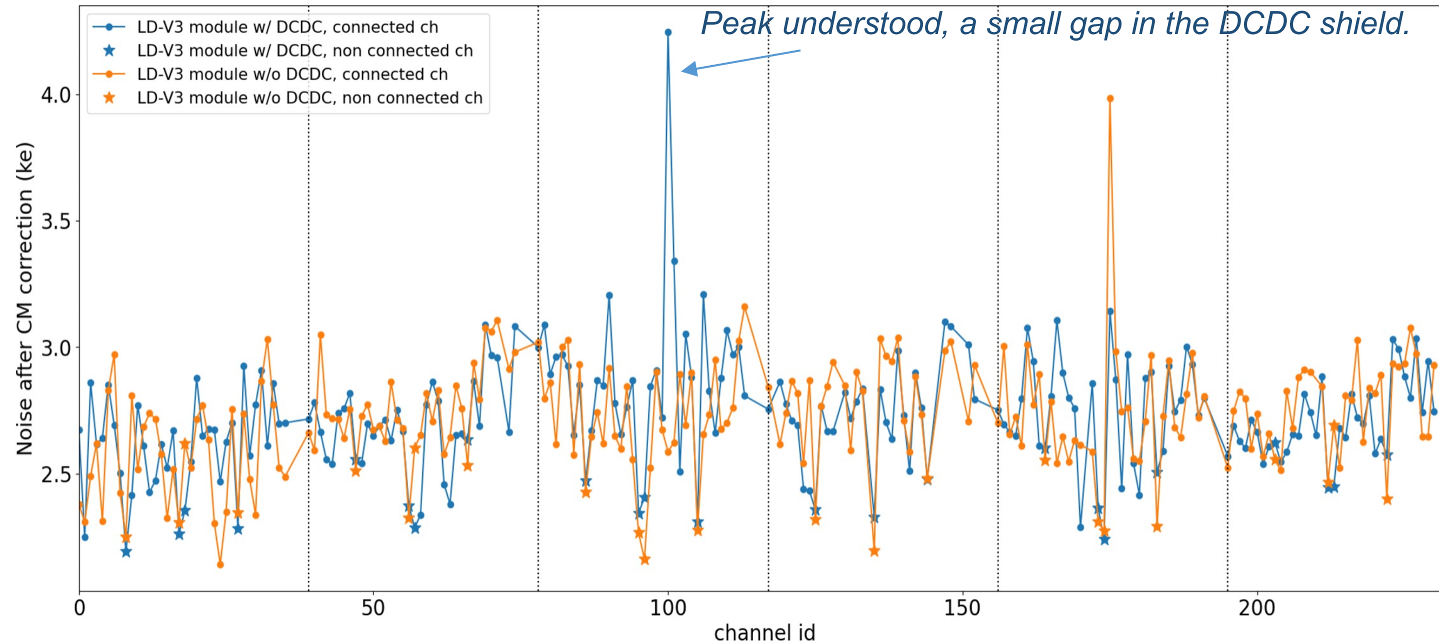




Module Noise Performance

Gain setting (320fC range).
CM channels facilitate CM correction.

Comparing noise with and without the DCDC mezzanine.

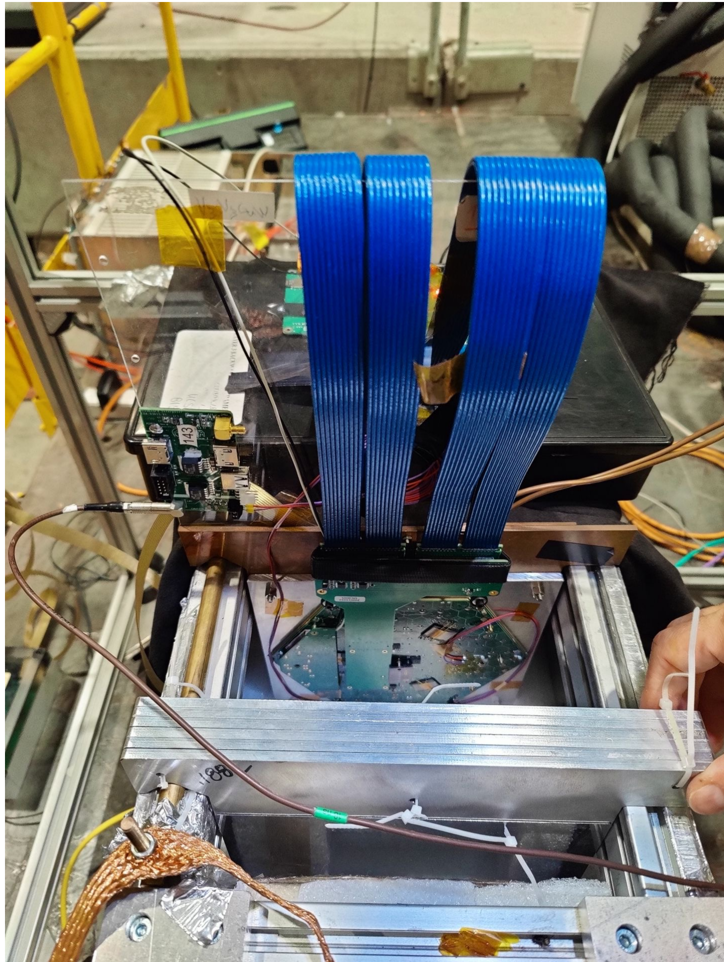


	Noise w/o CM corr.	Noise w/ CM corr.
LD-V3 module (with DCDC)	3.0 ke	2.7 ke
LD-V3 module (no DCDC)	2.9 ke	2.7 ke

Very little effect from the very close proximity of the DCDC converter.
A huge sigh of relief.

Module v3-LD

Module preparation for 2022 beam test



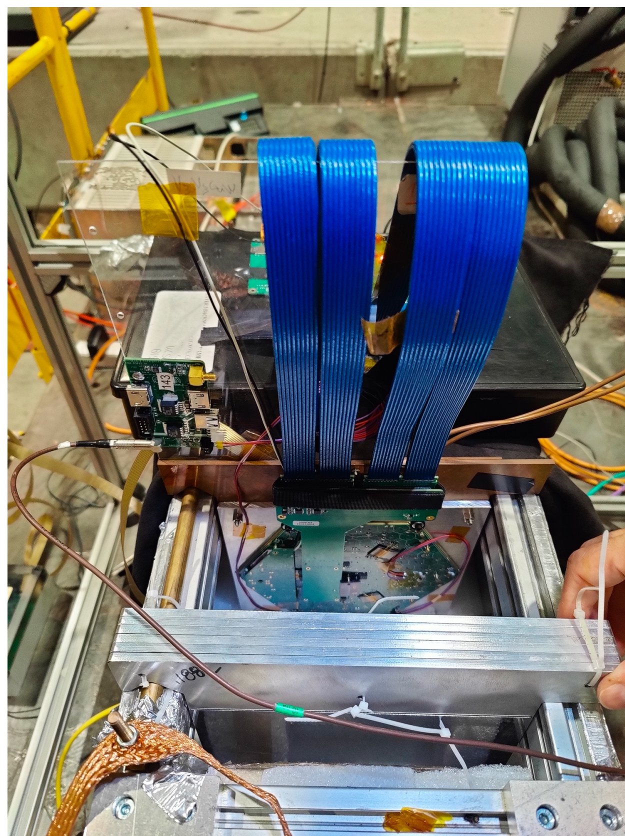
Test bean with V3 Silicon Module

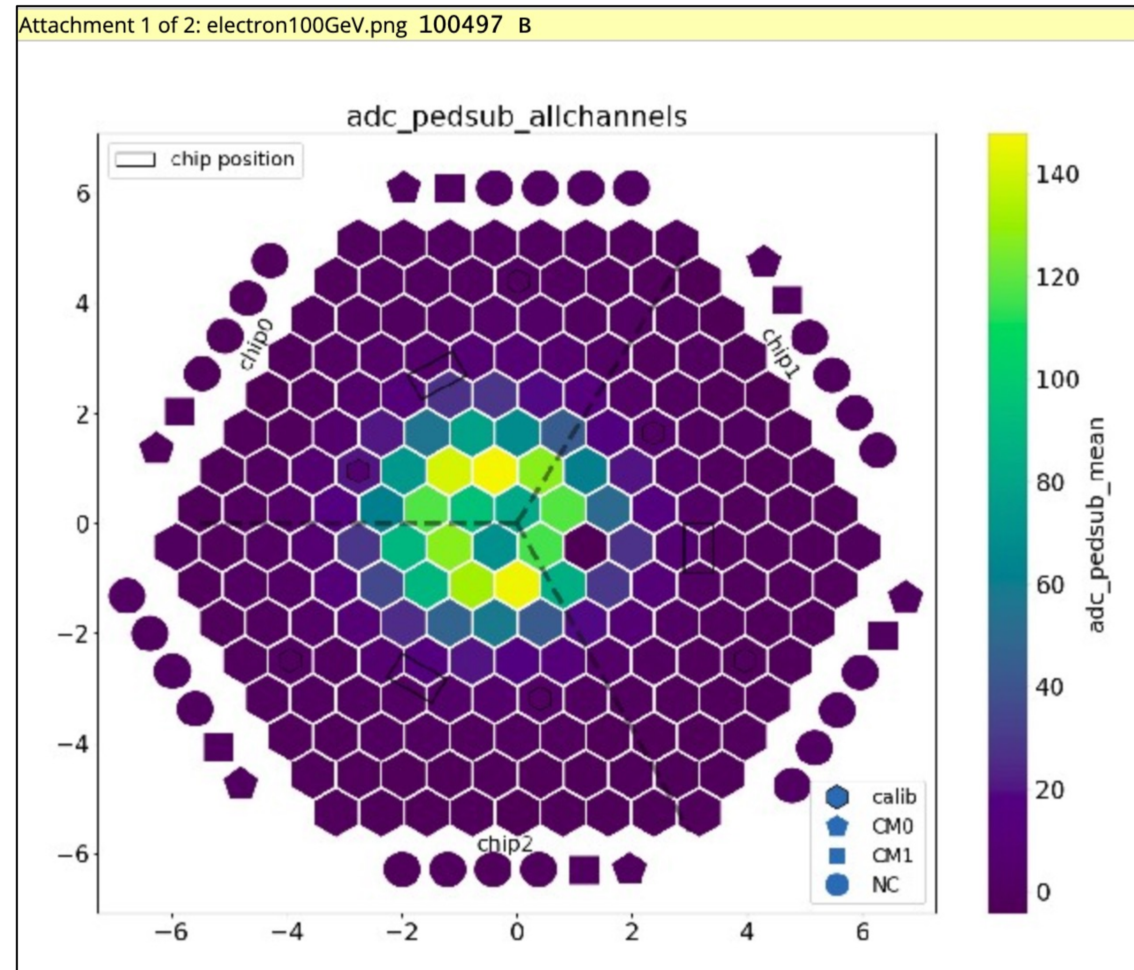
3 full size LD silicon module tested in SPS in October 2022

* V3 LD hexaboard
* 300 µm LD Si sensor, 270V bias
* Includes LDO on analog supply of HGCROC and local DCDC converter

Data acquired with:

* 150 GeV pion beam without absorber plates
  For all HGCROC gain settings
* Electron beam from 20 to 250 GeV with absorber
* Muon beam



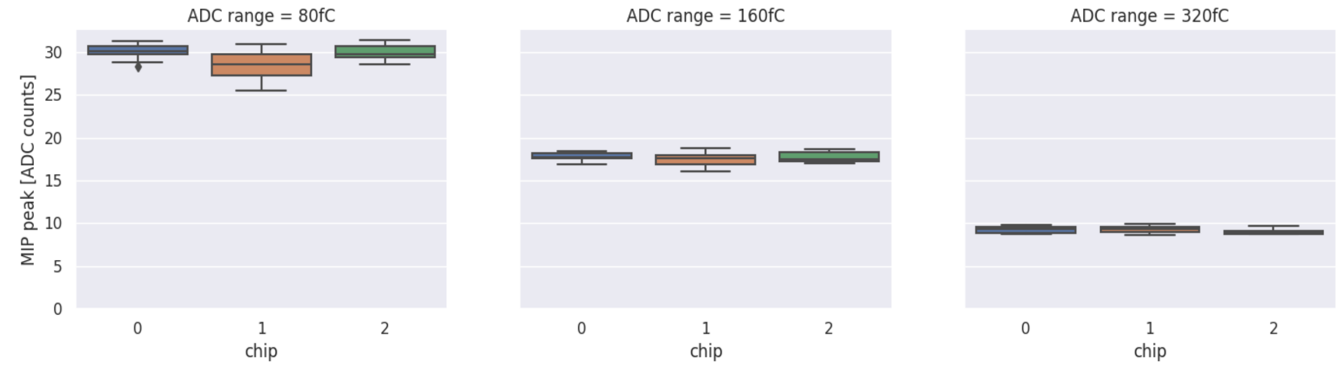


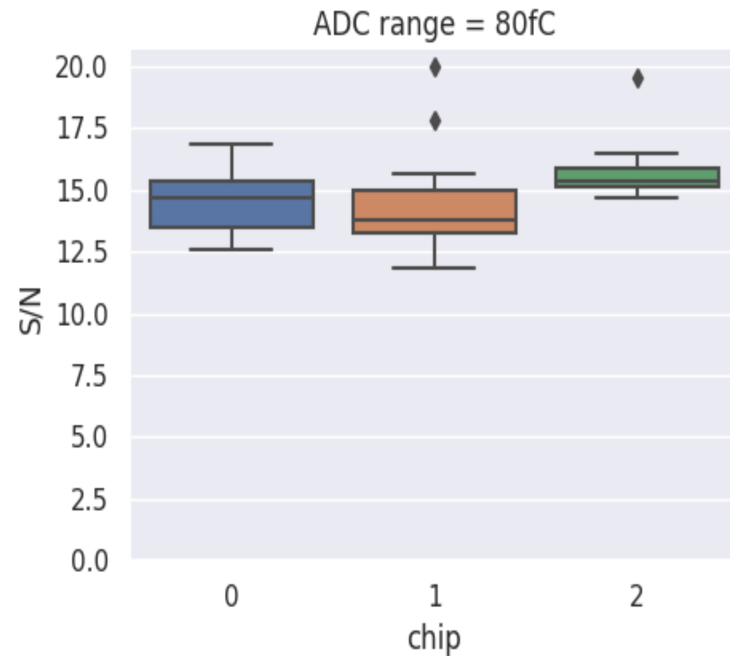
Test beam with V3 Silicon Module

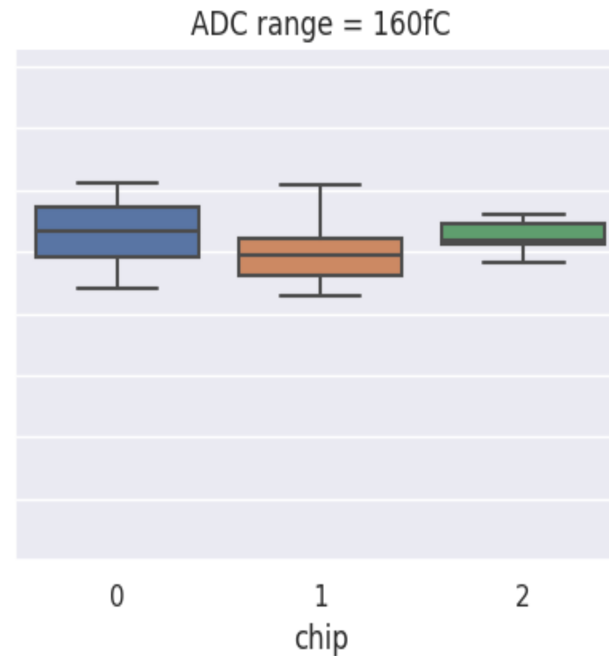
3 full size LD

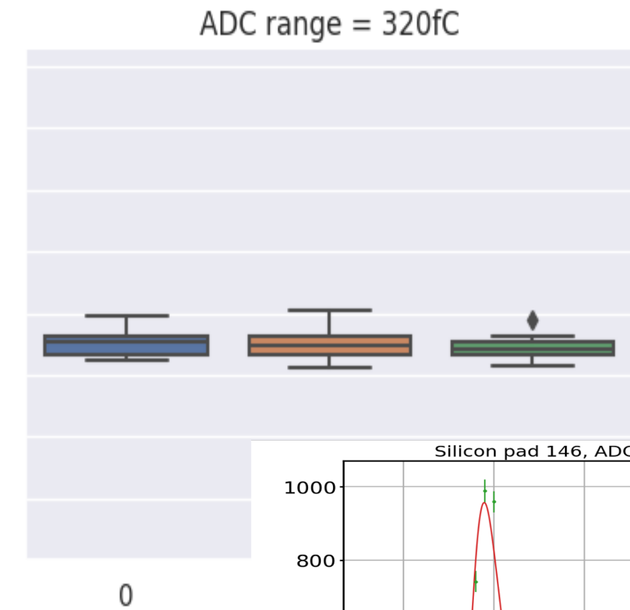
- Very encouraging results from the preliminary analysis of the 150 GeV pion data

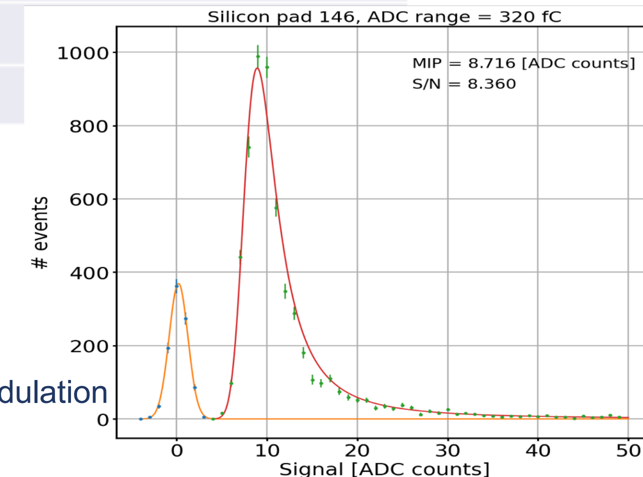
- S/N consistent with expectations











Small print:
Test beam data here collected from the ~40 channels exposed to the beam
Full offline common mode subtraction done. To be repeated using dedicated CM channels
"MIP peak" plotted here is 9% more signal than a real MIP. i.e. 22ke + 9% = 23.9ke
This larger signal size was used to calculate the noise and digital modulation values in the respective plots of noise and digital modulation

Signal to Noise Evolution and confirmation from Test Beam

	300um	200um	120um
Area cm2	1.26	1.26	0.56
Capacitance (pF)	48	69	54
Signal at start of life (SOL)	22 ke	15 ke	9ke
Charge at SOL (fC)	3.52	2.4	1.45
Preamp Gain (=full scale) at start	160 fC	160 fC	160 fC
Noise (e-)	2000	2700	2250
Expected S/N	11	5.55	4.0
TDR value	11	6	4.5
Max Fluence	1E15	2E15	8E15
CCE at End Of Life (EOL)	60%	70%	62%
Charge at EOL	13.2 ke	10.5 ke	5.6 ke
Leakage current 600V (uA) EOL	9	12	13
Additional noise (to be added in quadrature)	1346 e-	1554 e-	1617 e-
Preamp gain EOL	160 fC	160 fC	80 fC
Base noise with this gain	2000 e-	2700 e-	2250 e-
Total noise	2410 e-	3115 e-	2770 e-
S/N EOL	5.5	3.37	2.02
S/N EOL TDR	4.7	2.3	2.2

Start of life performance confirmed at test beam

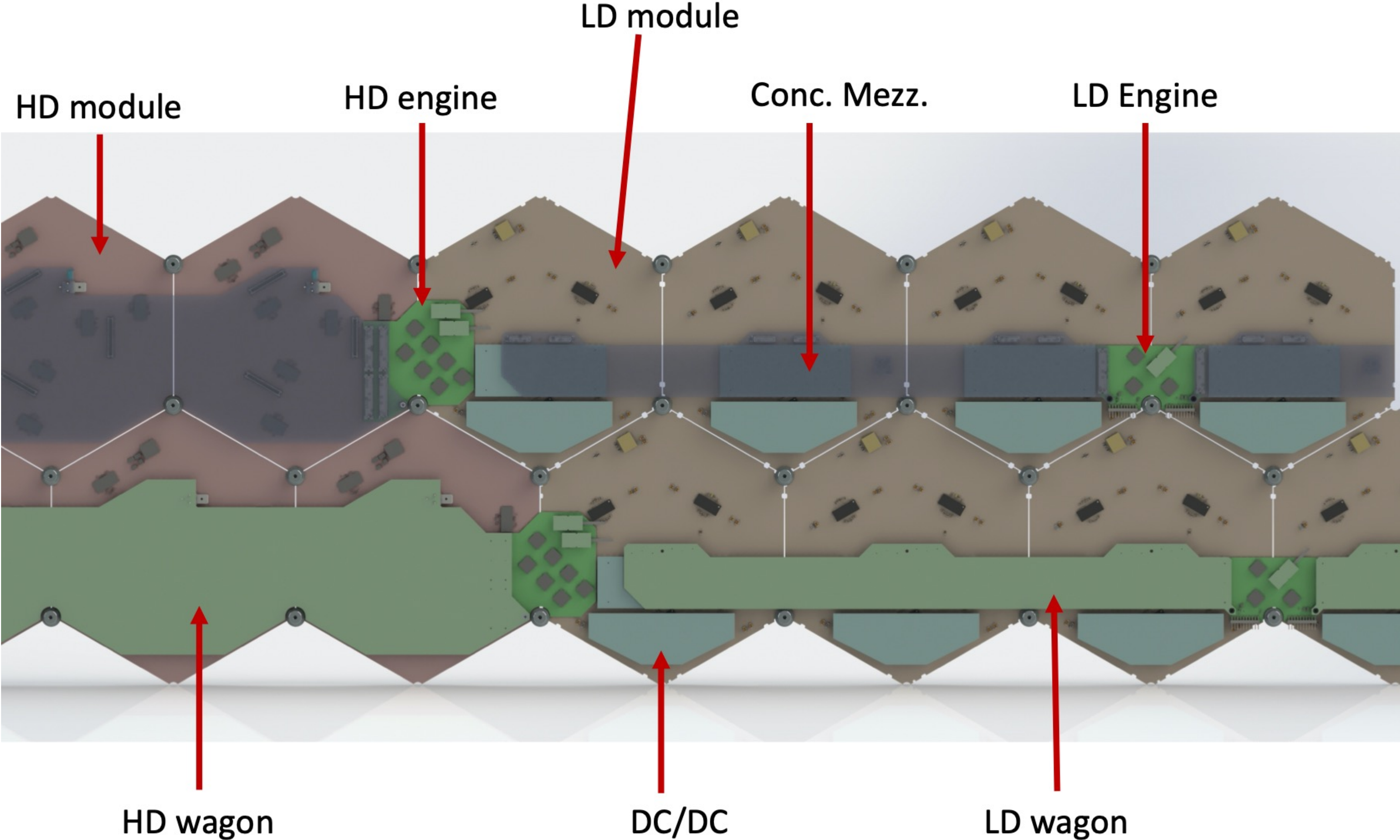
Expected End of life performance

Notes:

Test beam 2022
300um Sensor, full cell
Gain = 320 , Expected S/N = 7.85. observed 8.66
Gain = 160 , Expected S/N = 11.0. observed 12.8
Gain = 80. , Expected S/N = 11.0. observed 14.6

However
Note: 150GeV Pion beam generates 9% more charge in 300um silicon than true MIP signals ie. 23.9ke signal rather than 22ke.

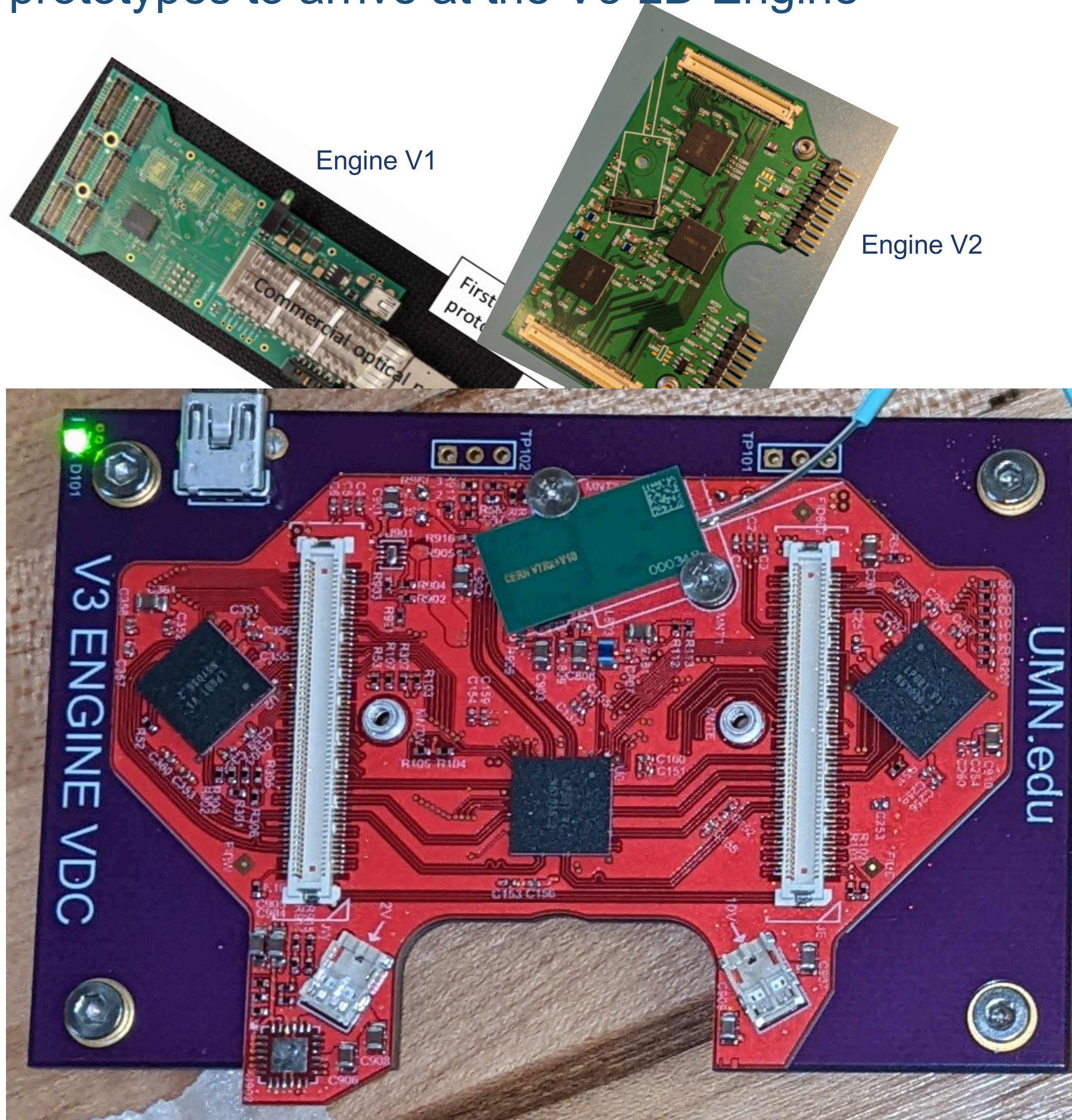
HGCAL Electronics – Engines & Wagons



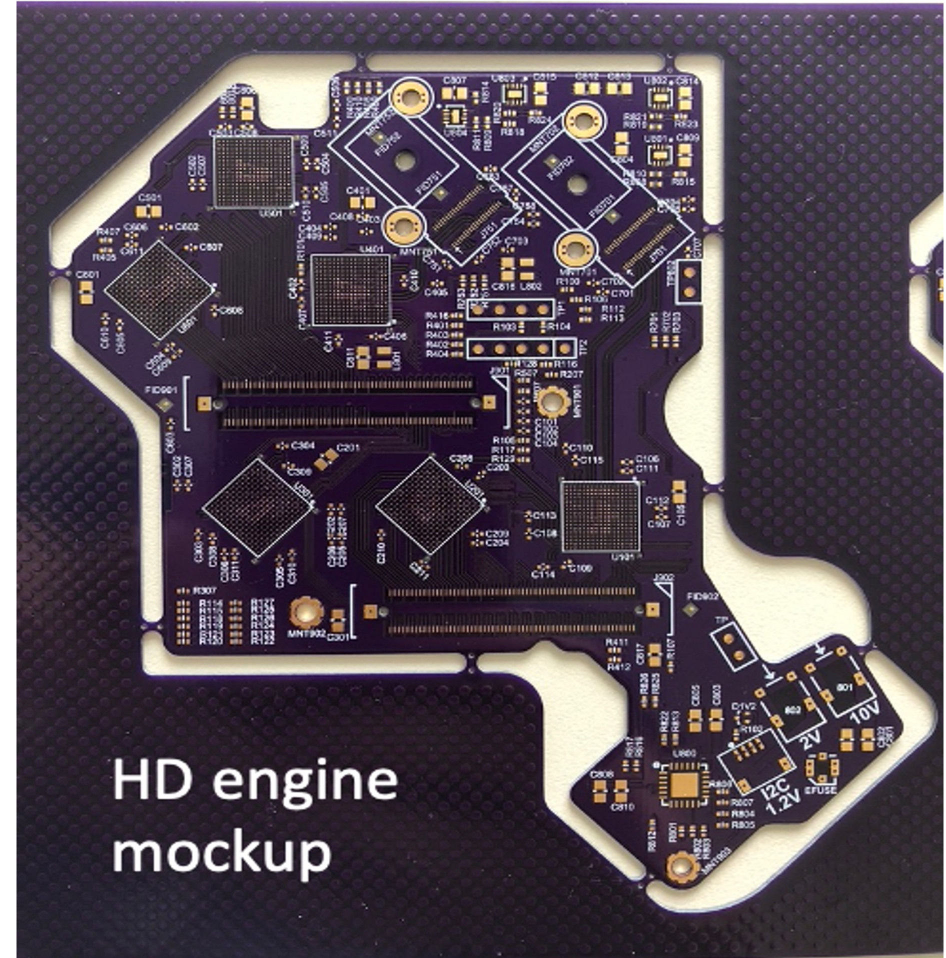
Engines

LD Engine prototype through a series of prototypes to arrive at the V3 LD Engine

LD Engine contains 3 lpGBT chips and 1 VTRX+ & fibre
LD Engine contains 6 lpGBT chips and 2 VTRX+ & fibre



Engine V3 LD

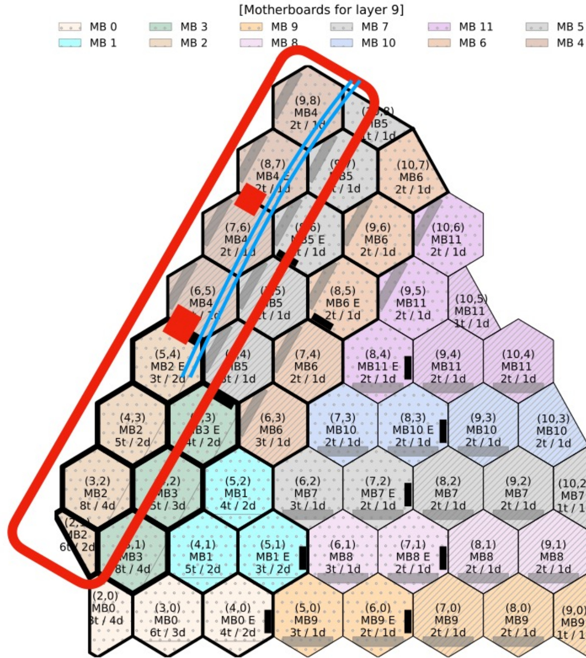


Engine V3 HD (in fabrication)

Engine & Wagon Varieties

Engine varieties

- We expect to produce 2 LD engine varieties and at least 2 HD engine varieties
- The 2nd variety is to be used when the LD train is rotated by 180°, with service channel on the “right”
- LD: 2nd variety needed to ensure VTRX+ fiber points to the outside of the cassette
- HD: 2nd variety needed to avoid overlap with ROC on 180° rotated LD module that the HD engine overlaps with



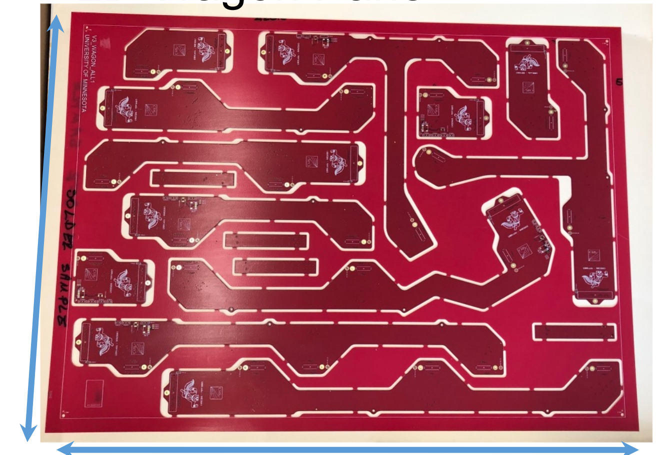
2 main types (LD & HD)

2 variants of each.

Wagon varieties

Many varieties needed to cover all layers
Wagon identification tool referencing a mapping file : 86 different varieties identified
Most are LD variants which are uncomplicated and simply for connectivity.

LD Wagon Panel



Scripting assisted layout procedure to:
1. Determine location of wagon components
2. Define board outline
3. Convert to text file readable by Altium with correct footprints
4. Minimal routing remaining, possibly by hand.

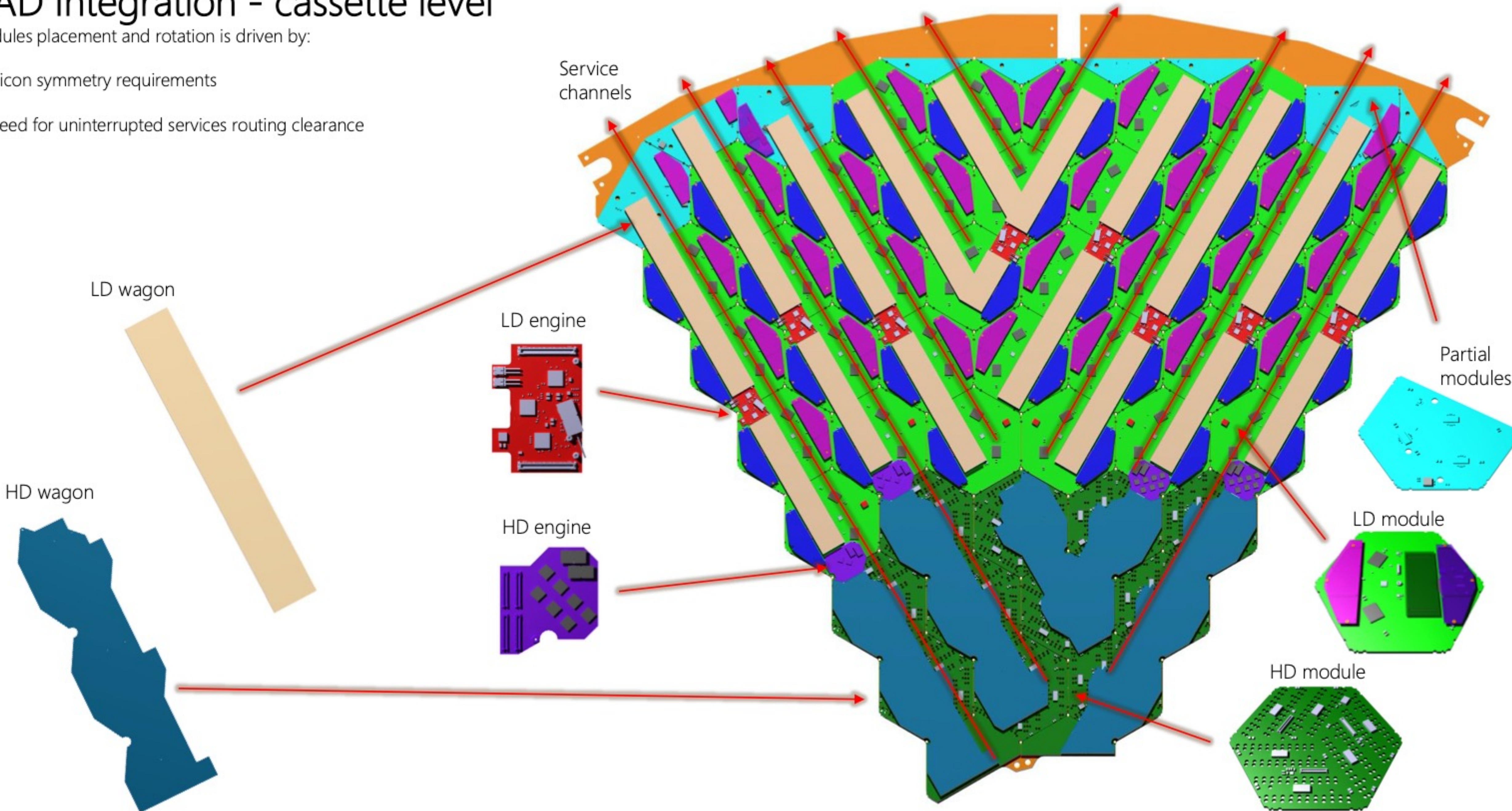
First run through expected in a few weeks.

CAD Integration - cassette level

Modules placement and rotation is driven by:

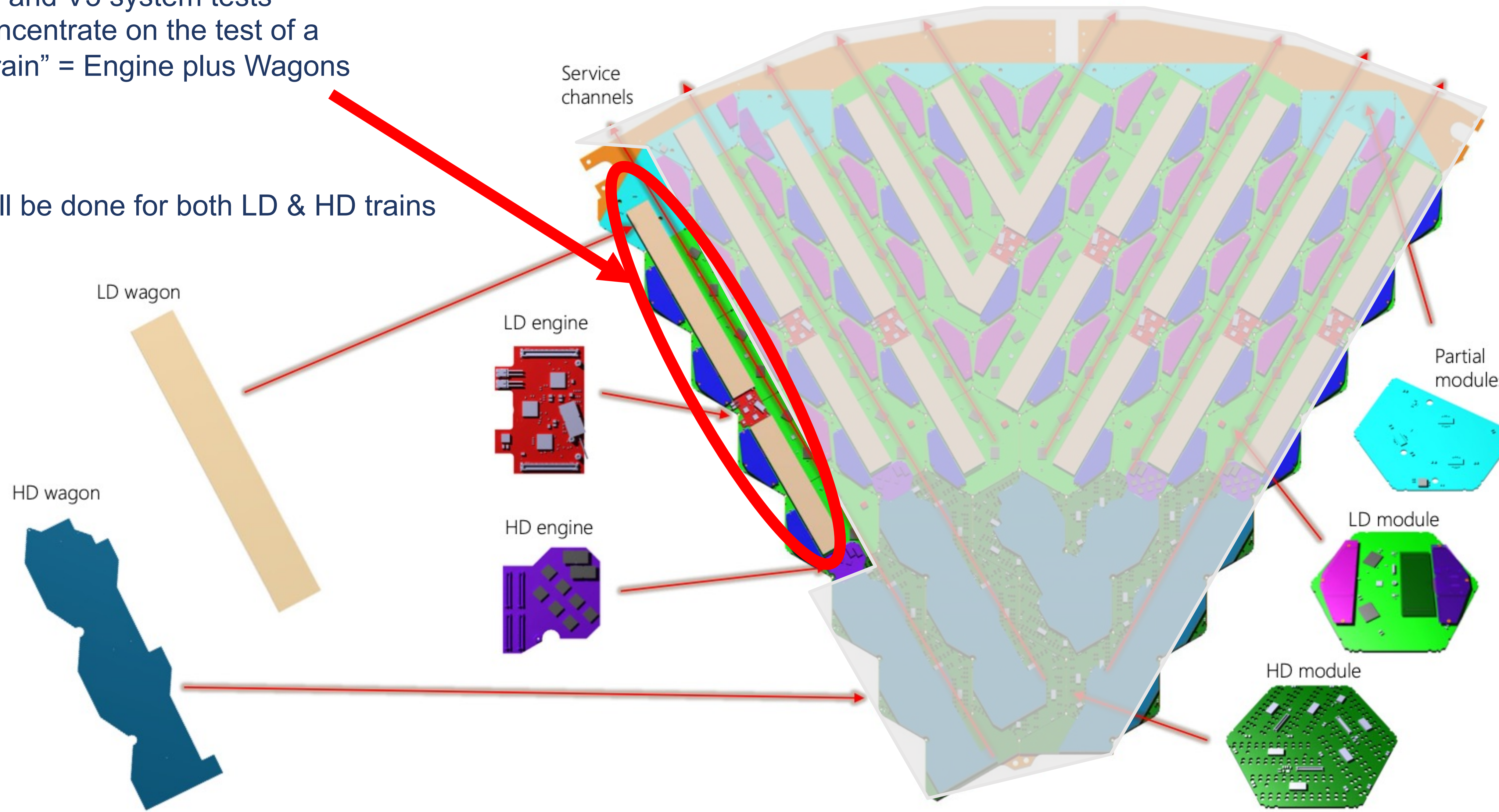
1) Silicon symmetry requirements

2) Need for uninterrupted services routing clearance



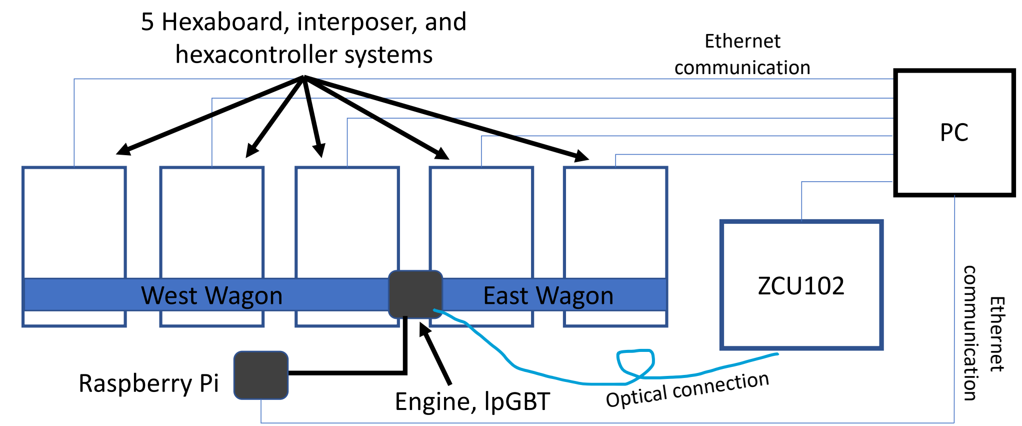
V2 and V3 system tests concentrate on the test of a "Train" = Engine plus Wagons

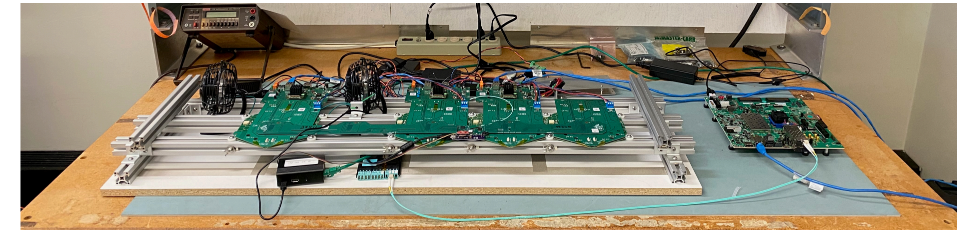
Will be done for both LD & HD trains



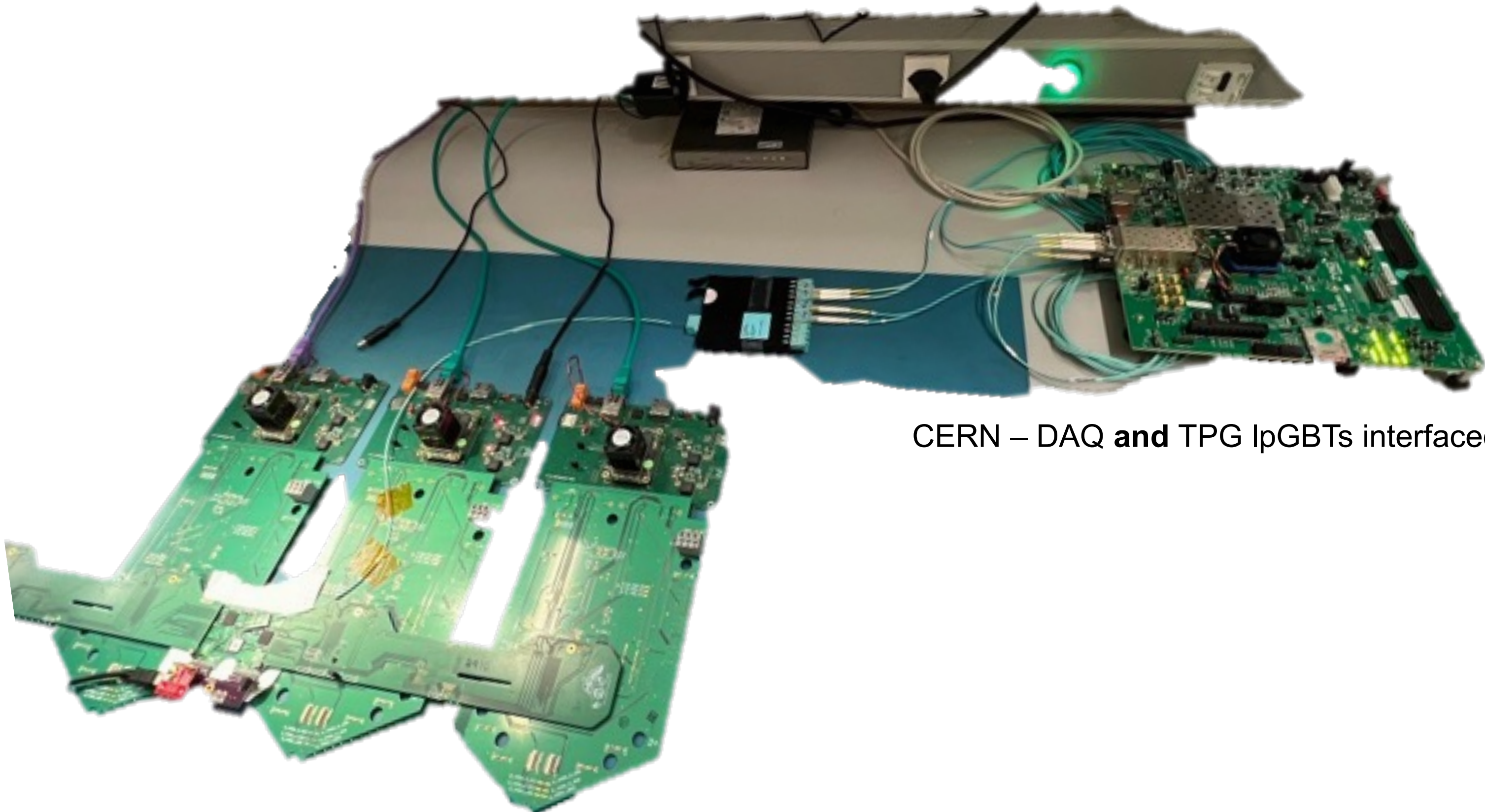
V2 System Tests

- UMN focus: commissioning
  - lpGBT and GBT-SCA communication
- FNAL ⇔ focus: in-cassette module performance
  - ROC readout through Hexacontroller
  - Four modules arriving from IHEP MAC





FNAL – DAQ lpGBT interfaced



CERN – DAQ **and** TPG lpGBTs interfaced

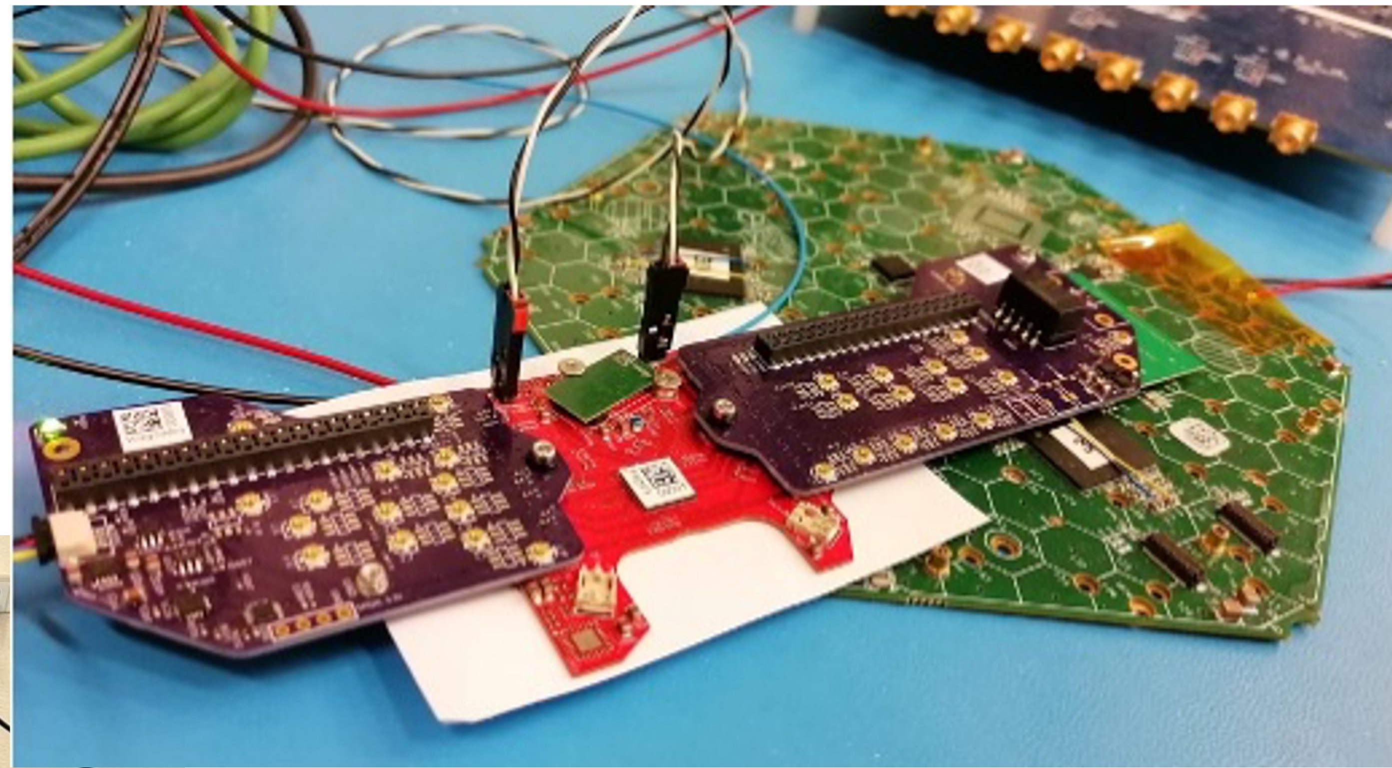
- CERN ⇳ focus: towards BE DAQ and TPG integration
  - Slow and fast control from ZCU102 via lpGBT and GBT-SCA
  - ECON-T-P1 emulator read out
  - Trigger lpGBTs read out
- Common software and firmware tools
  - Evolution towards final ATCA BE firmware

V3 System Tests

V3 system tests ramping up and will evolve throughout 2023.

Different test benches evolving in different labs.

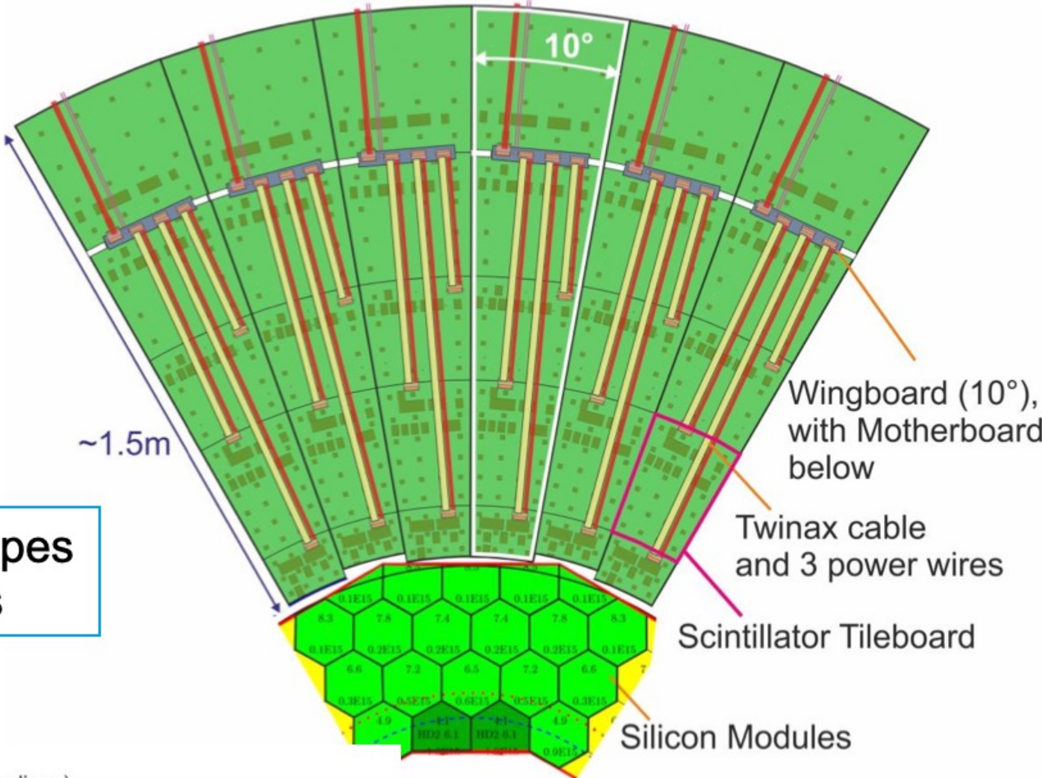
Path will go to full “train” readout
Then a full cassette.



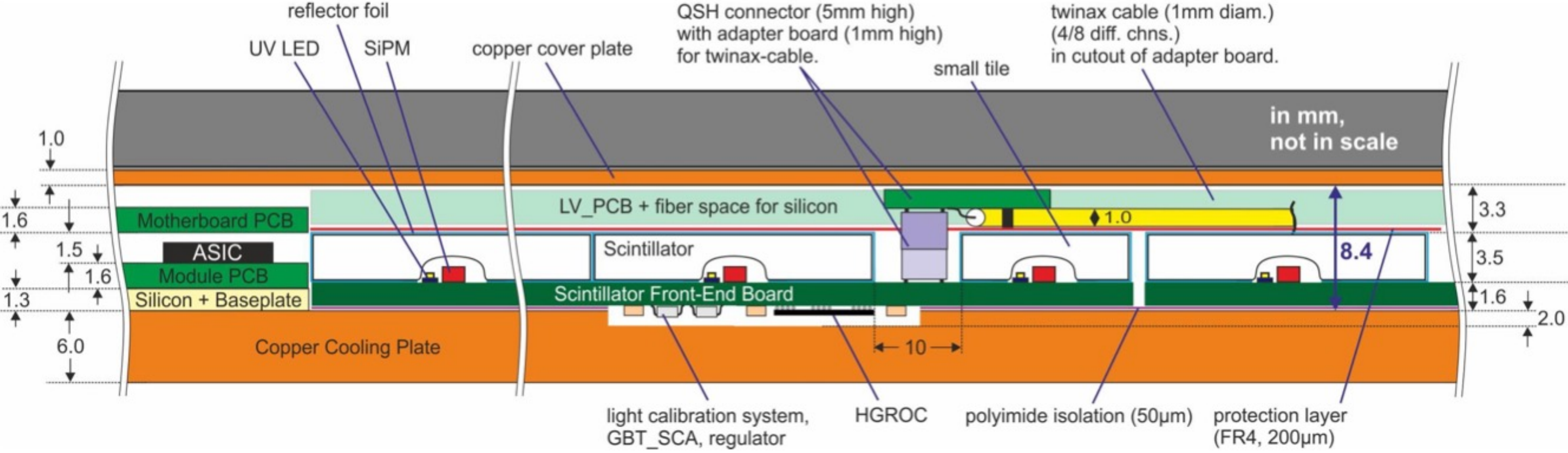
Currently:
CERN: ECON-Tp1 > Backend
UMN: HGCROC3 > ECON-Tp1
HGCROC3 > ECON-D Emulator
FNAL: Cassette Tests

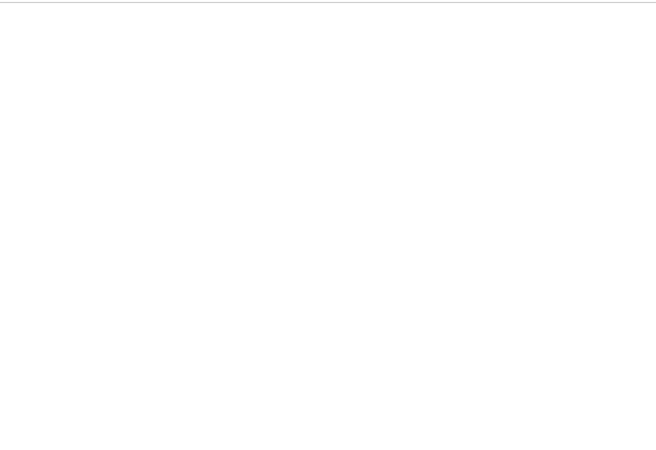
SiPM-on-Tile Region

Parallel development to the silicon
Very similar electronics chain



8 tileboards types + sub-variants

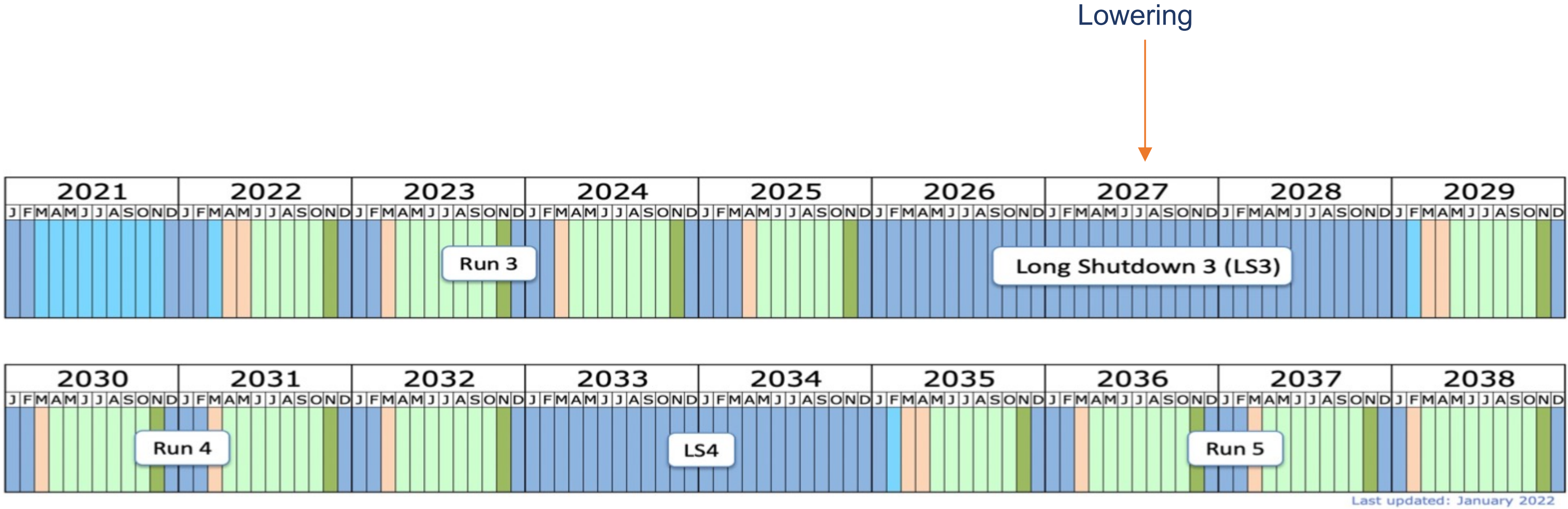




Moving forward

Lowering

LHC Schedule



Moving forward

2022	2023	2024	2025	2026	2027	2028	2029

Electronics Prototyping

System Testing

Production Tenders

ASIC Production

Board Production

Module Assembly

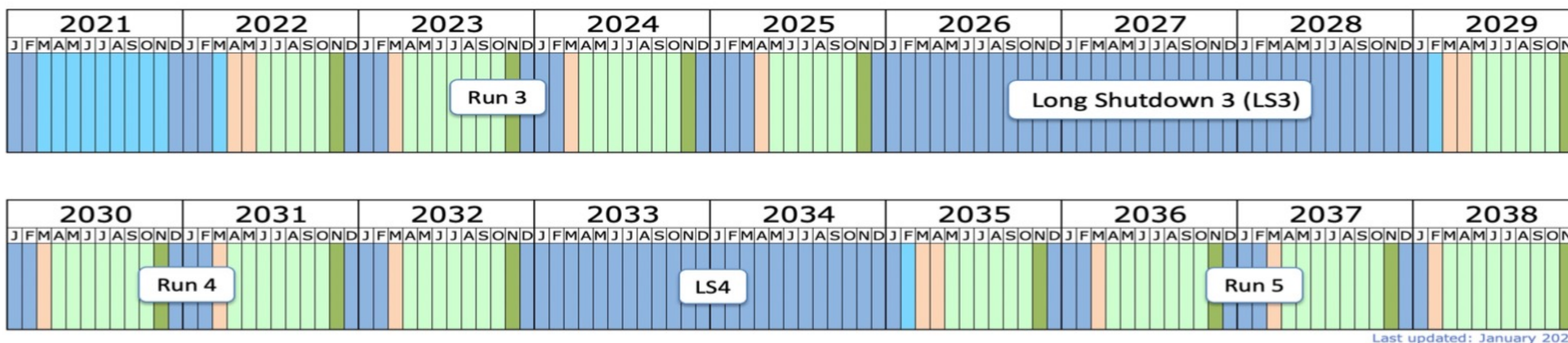
Casette Assembly

Lowering

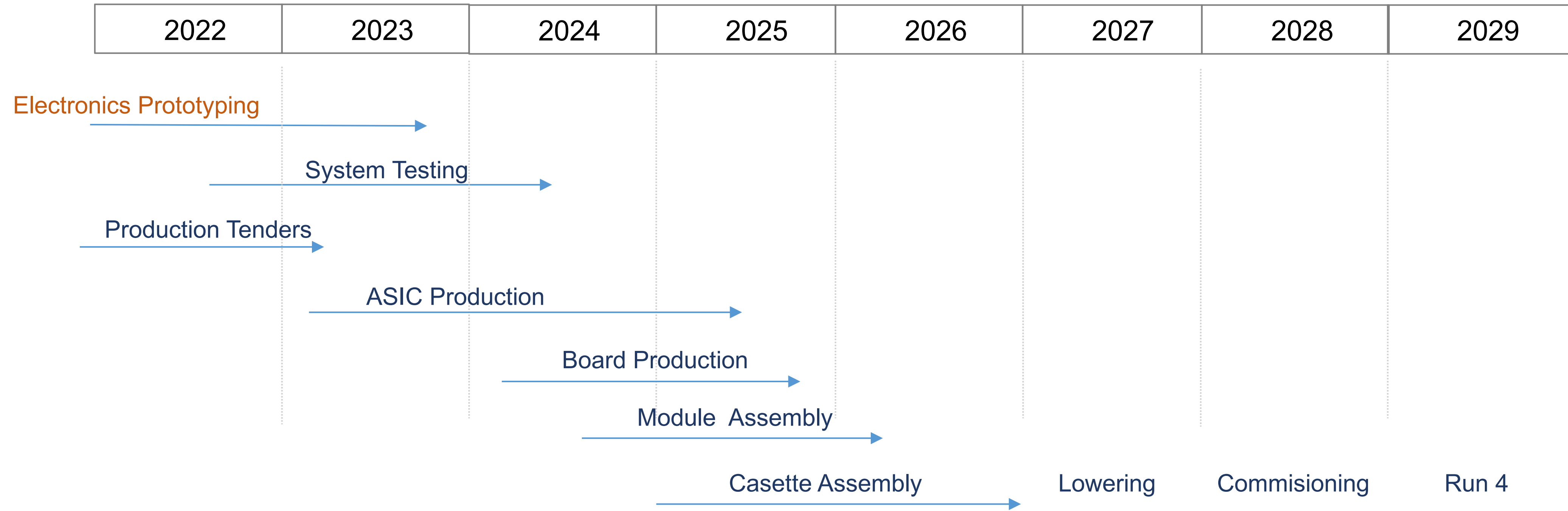
Commisioning

Run 4

LHC Schedule



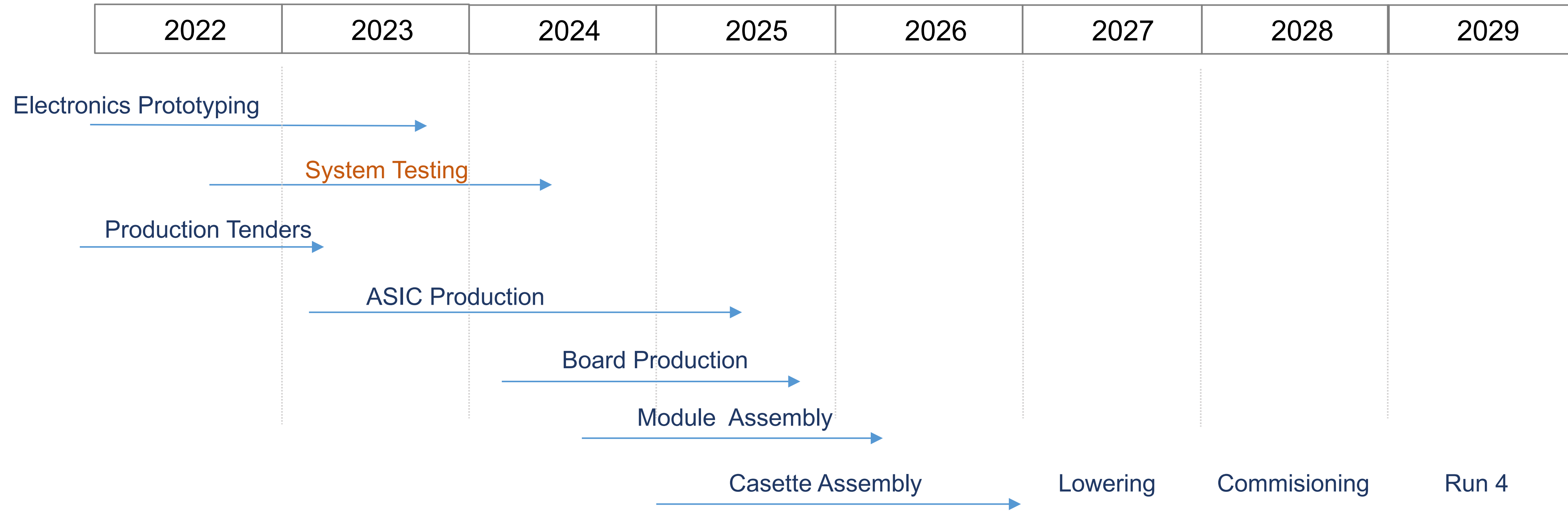
Moving forward



Electronics prototyping phase nearing it's completion

HGCROC, LDO, Rafael ready to launch engineering runs
ECONs will be ready in 2023
Hexaboards, Engines & Wagons, Tileboards on final prototypes

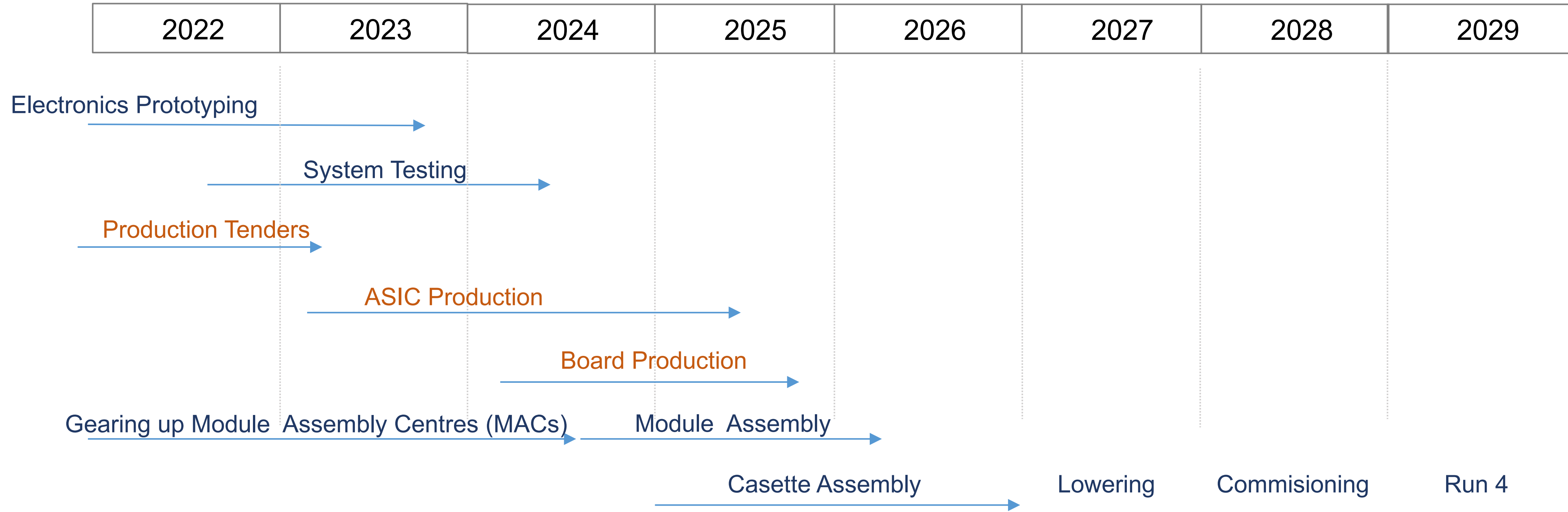
Moving forward



In 2023 we will prototype the system in steps as follows:

1, The full ”train level”
2, The Cassette Level with multiple trains
3, Multiple Cassette Level with a cosmic stack.

Moving forward



Production Phase
This is a huge planning and logistics task:
Production, assembly and QA/QC across the globe, Europe, US and Asia

All ASICs, boards, modules and eventually cassettes need their own production & QA/QC procedures.

Tenders for company selection in 2022

2023 – 2024 ASIC production
HGCROCs x 100 000
ECONs x 30 000 of each type
LDOs x 100 000
Rafael x 30 000
bPOLs x. 70 000
….
2024 – 2025 Board production & Module assembly
Hexaboards x 30 000
Modules x 30 000

Moving forward

2022	2023	2024	2025	2026	2027	2028	2029

Electronics Prototyping

System Testing

Production Tenders

ASIC Production

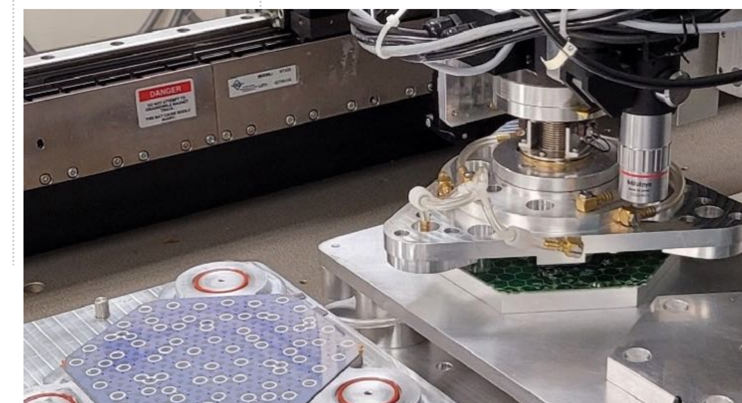
Board Production

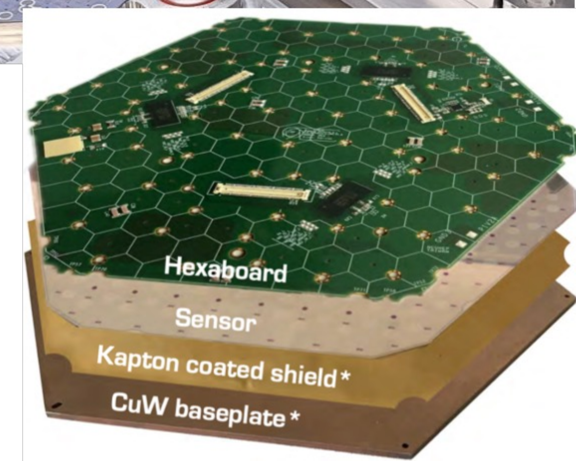
MACs/TACs Gearing Up

Module Assembly

Casette Assembly

Lowering





* In CE-H, PCB baseplate with laminated Kapton™

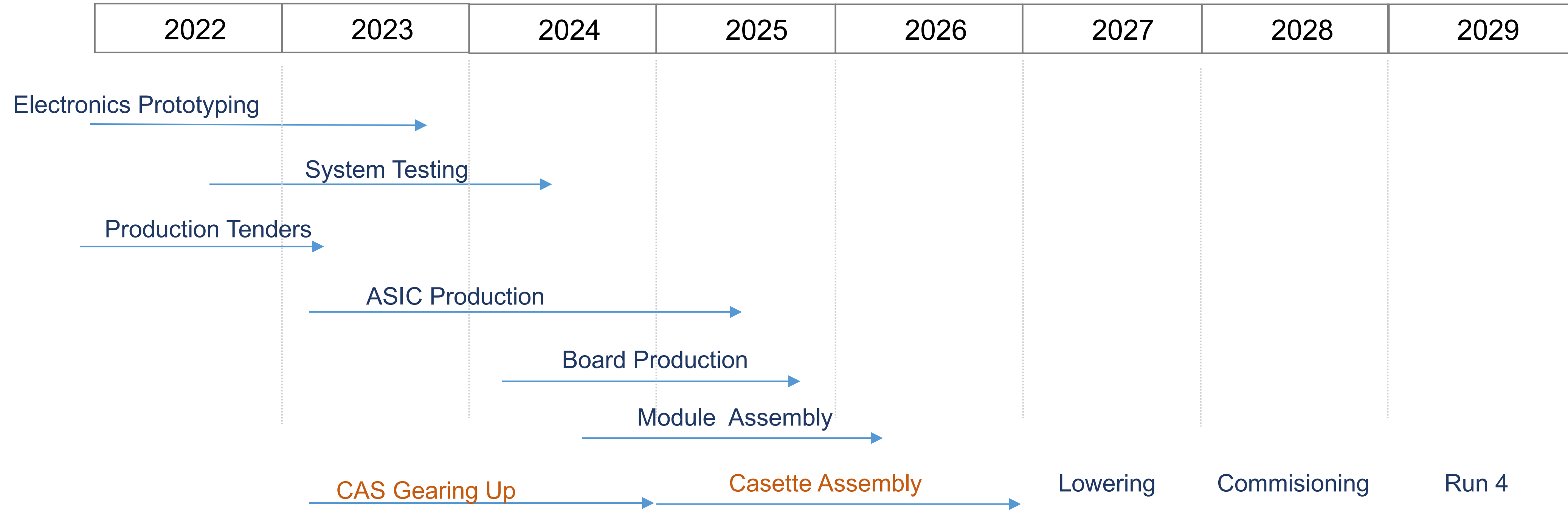
Module Assembly Centres (MACs)

5 MACs (3 in US, China, Taiwan + possible 6th in India)

Tileboard Assembly Centres (TACs)

Germany & US

Moving forward



Cassette Assembly Centres (CAS)

CERN
US (FNAL)

Headwinds

We have all the usual headwinds such as challenging spec.s, low staffing levels and aggressive schedules

However, there have also been the exceptional un-expected headwinds too:

Covid
Impact : Lab work, travel, design teams

Electronics Crisis
Silicon
Packaging
FPGAs

The terrible war on Ukraine
HGCAL has relatively large exposure

- Funding
- Machined cast scintillators manufactured in Kharkiv
- Sanctions affecting mechanics and scintillator manufacturing in Protvino, Minsk and Dubna
- Collaboration staffing

Cost - Inflation
All costs increasing

Moving forward

2022	2023	2024	2025	2026	2027	2028	2029

Electronics Prototyping

System Testing

Production Tenders

ASIC Production

Board Production

Module Assembly

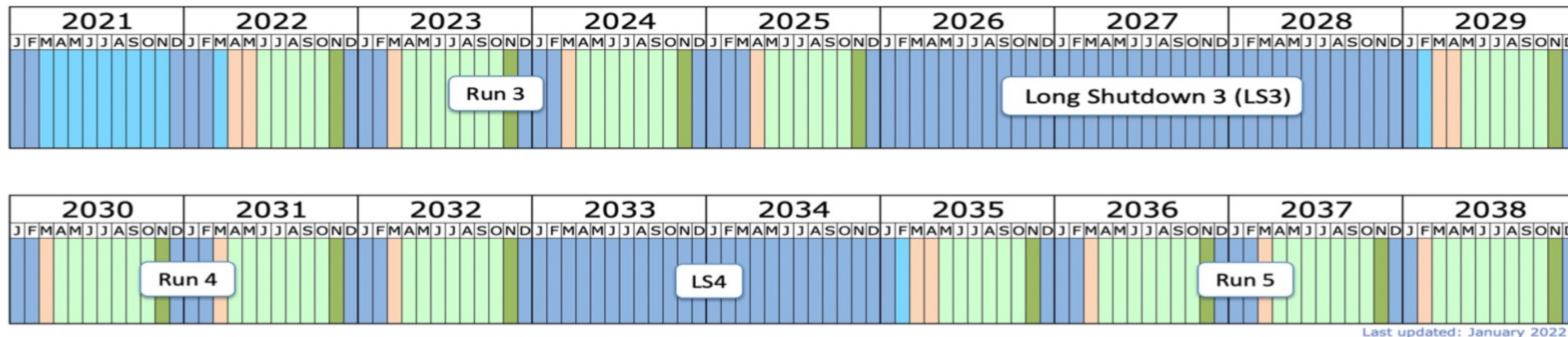
Casette Assembly

Lowering

Commisioning

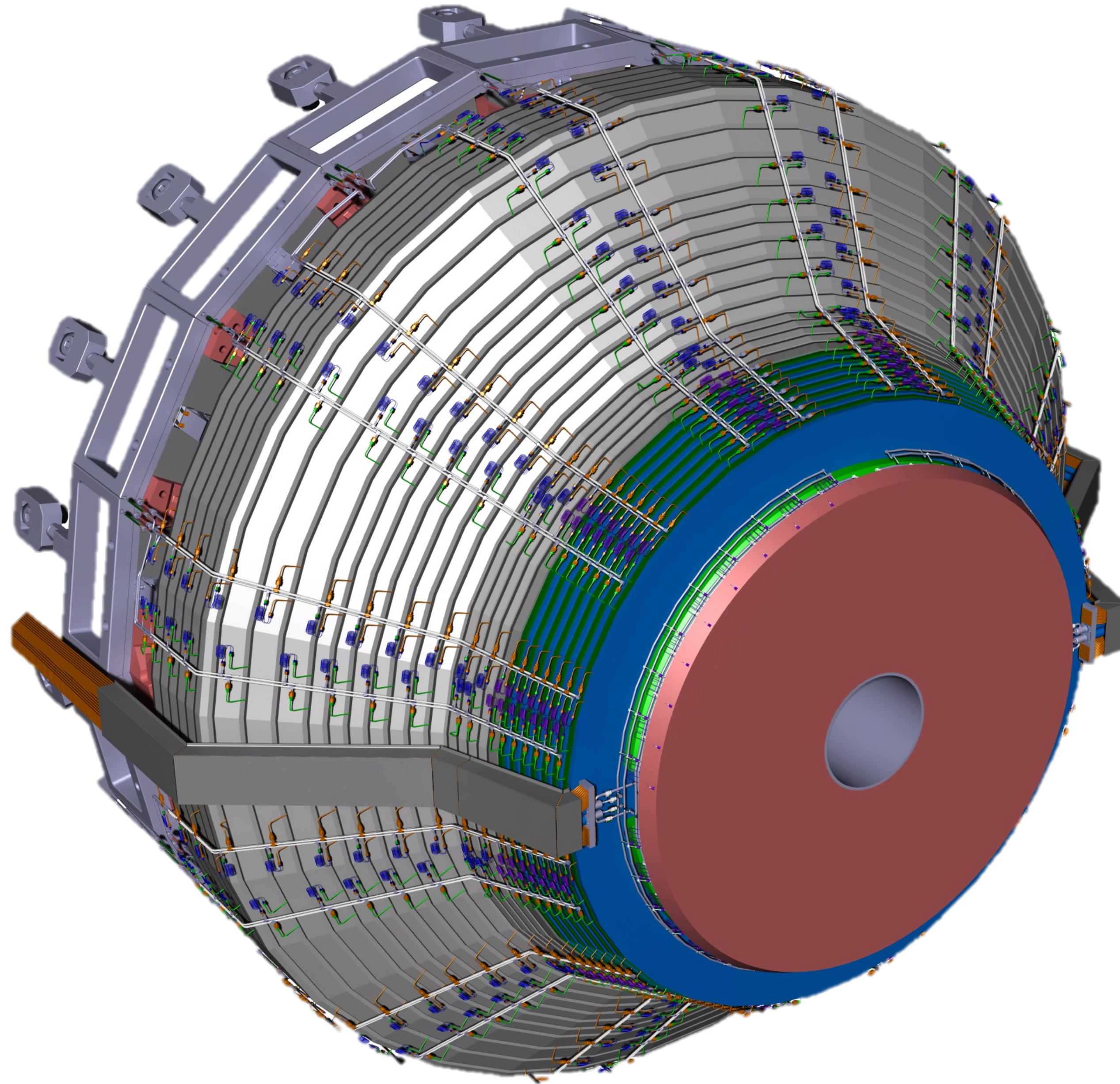
Run 4

LHC Schedule

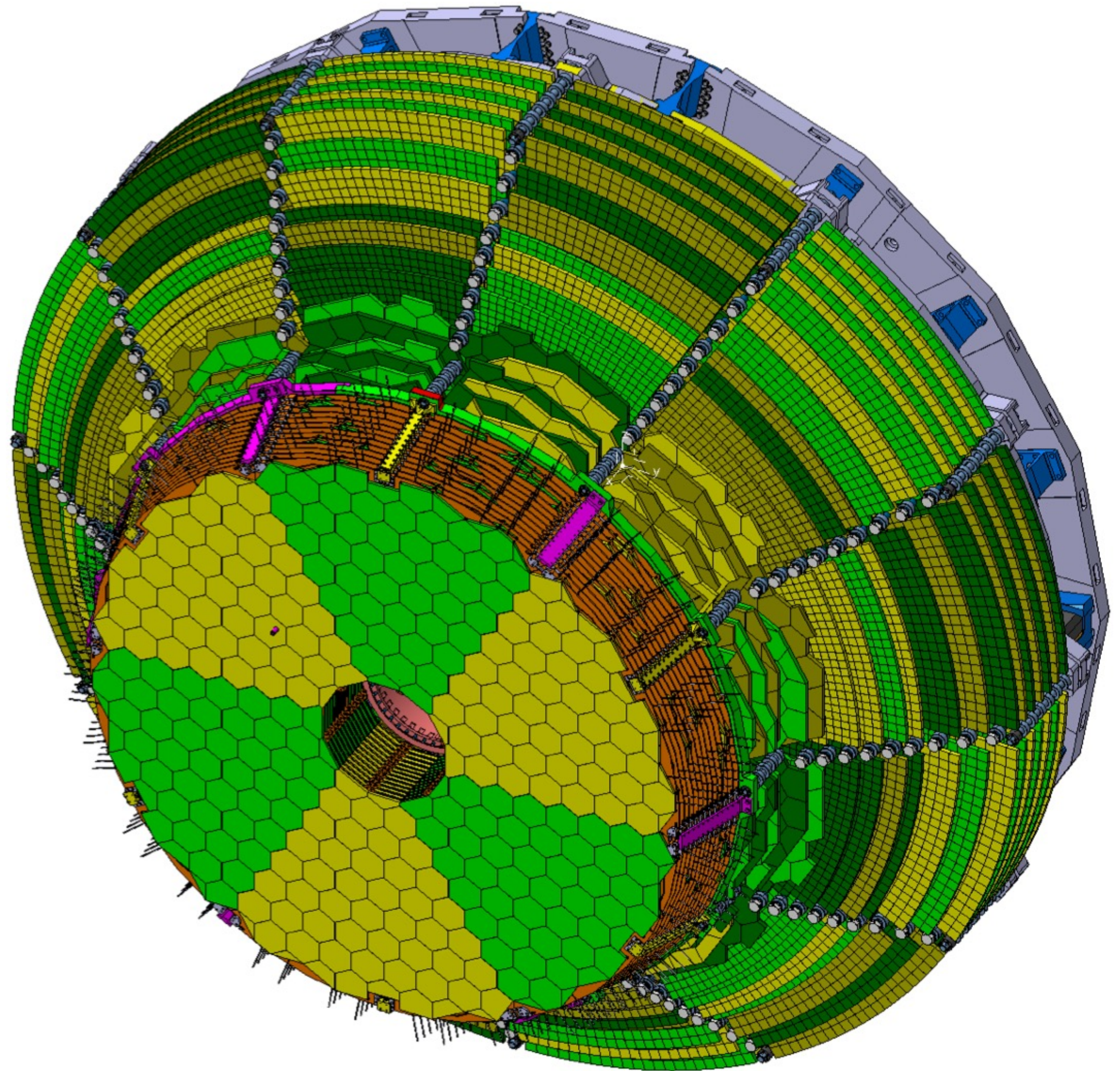


Shutdown/Technical stop
Protons physics
Ions
Commissioning with beam
Hardware commissioning/magnet training

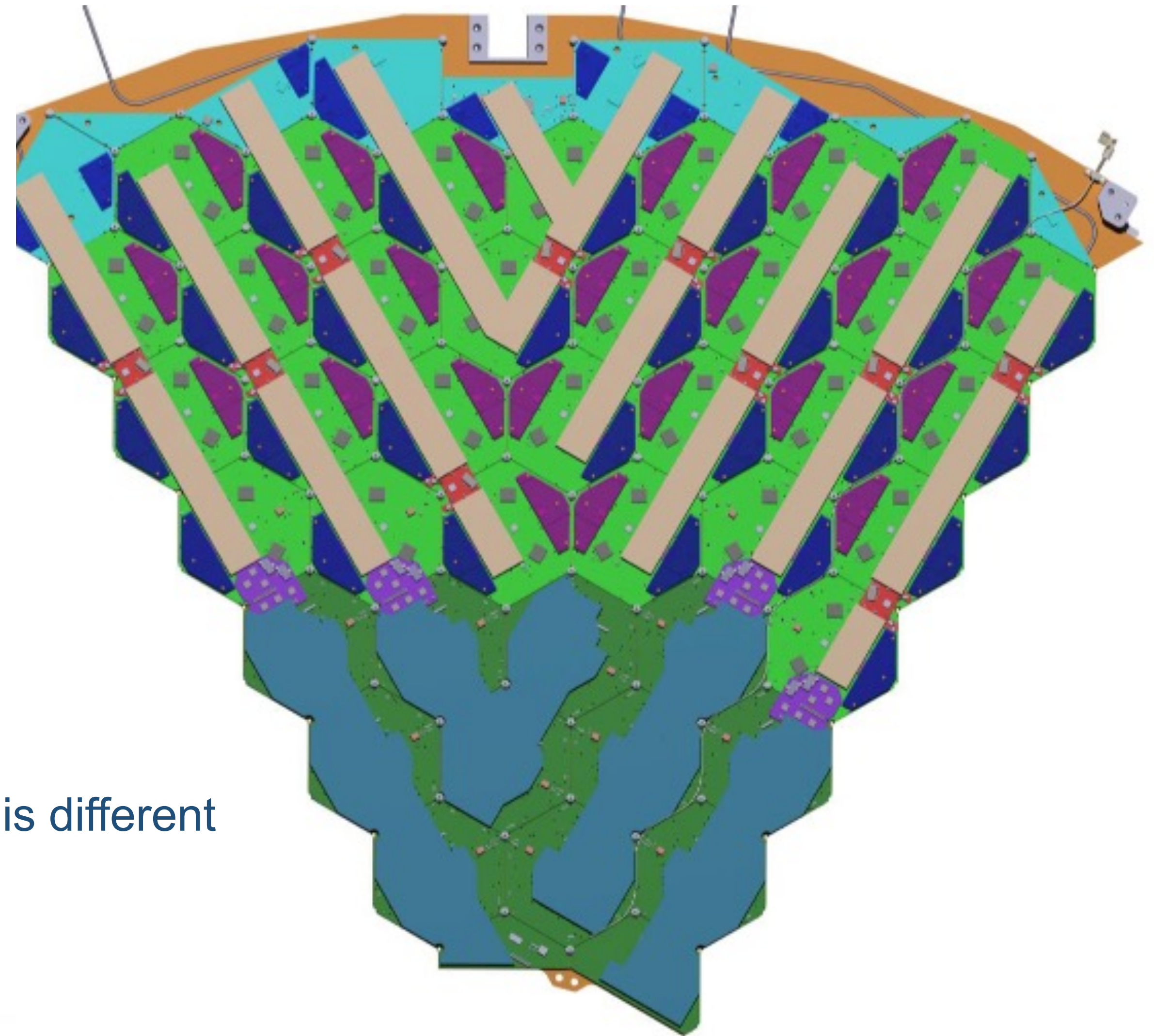
Thanks very much



Additional slides

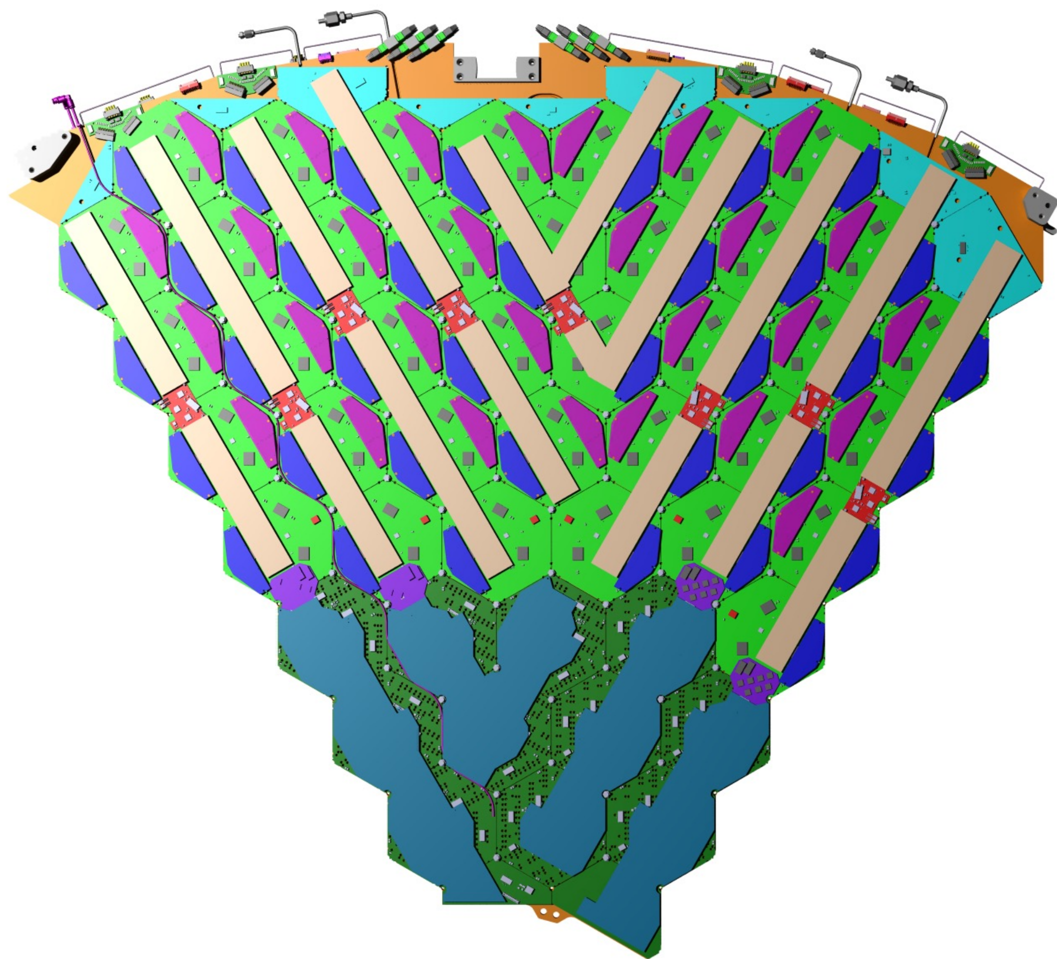


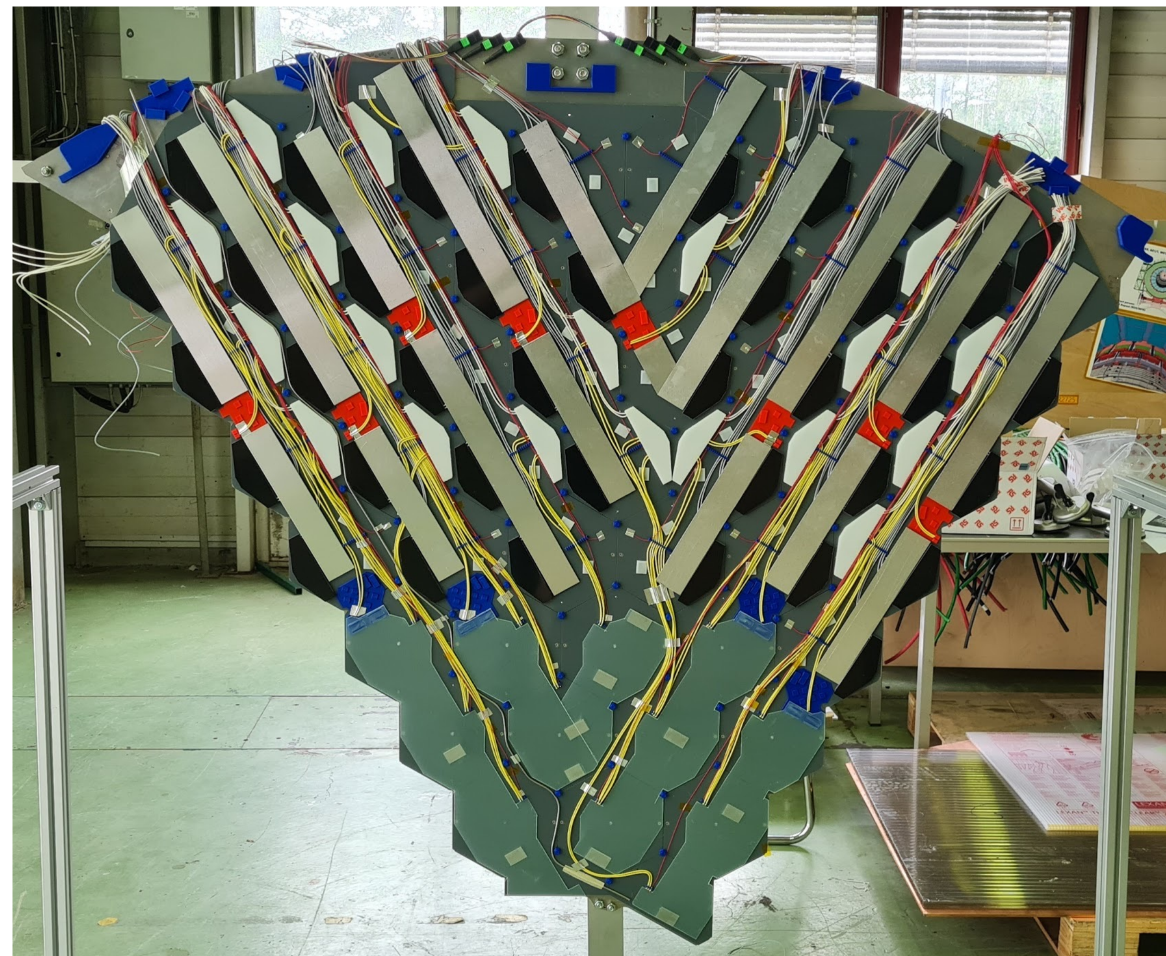
A few CAD images



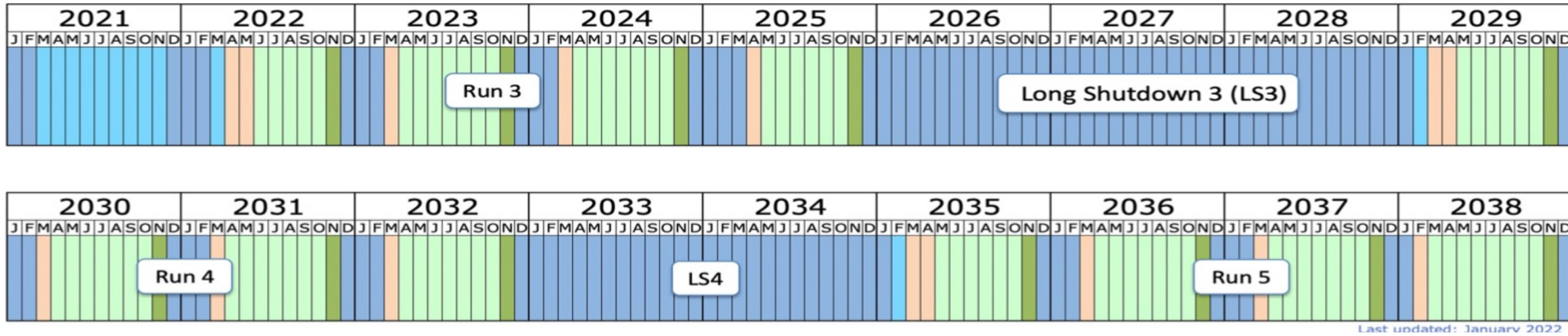
Every layer is different

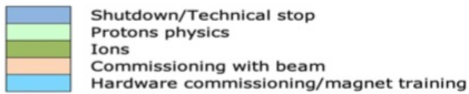
Mockups





LHC & CMS Re-baselined Schedules



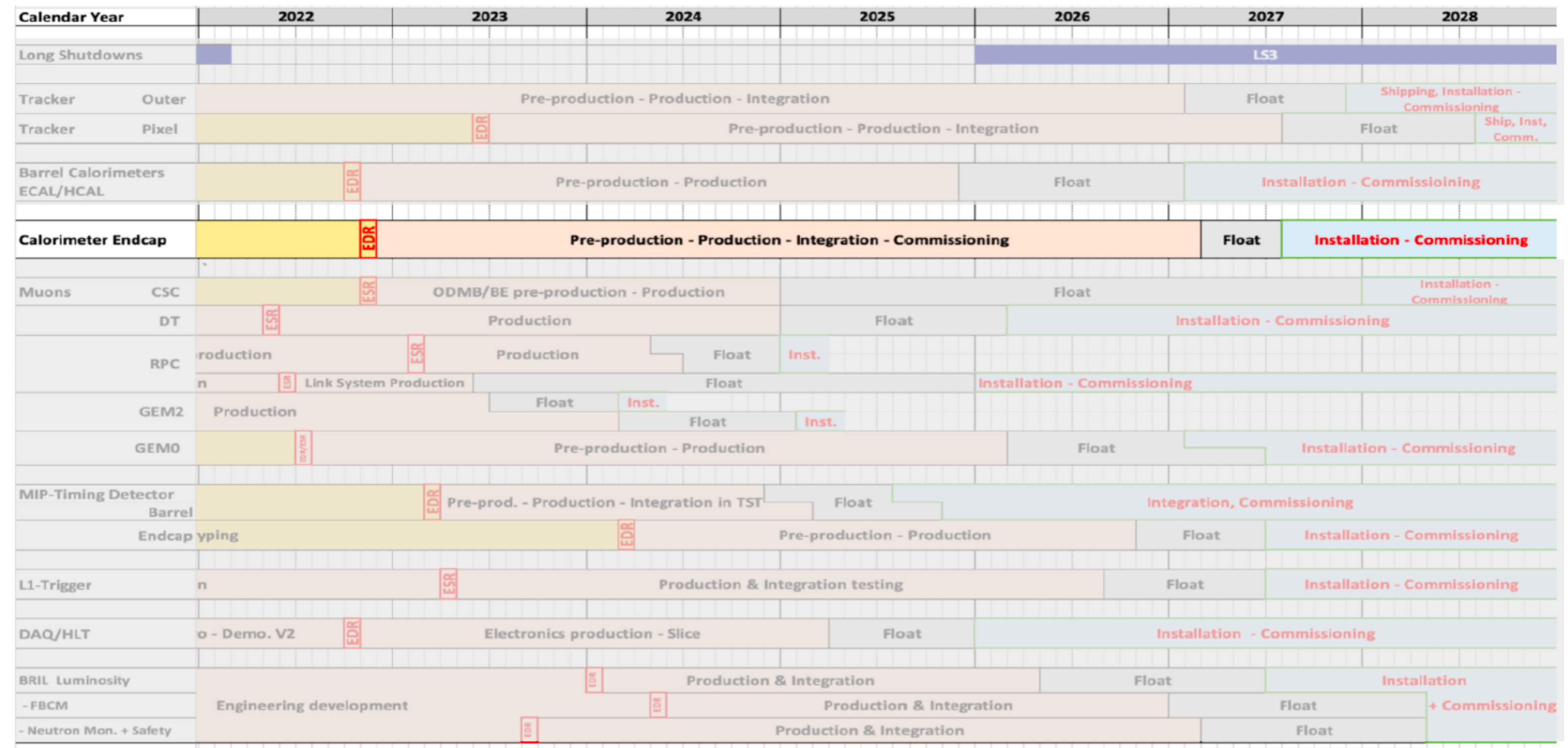


This follows an adjustment of:

- Run 3 extension by one year
- LS3 extended by 6 months

As reported at the May 2022 P2UG

CMS Master Schedule after re-baseline



Invasion to Ukraine impact not factored in

LHC / HL-LHC Plan

LHC

HL-LHC

Run 1 | Run 2 | Run 3 | Run 4 - 5...

LS1 | EYETS | LS2 | EYETS | LS3

7 TeV | 8 TeV | 13 TeV | 13.6 TeV | 13.6 - 14 TeV | energy

splice consolidation
button collimators
R2E project

cryolimit
interaction
regions

Diodes Consolidation
LIU Installation

Civil Eng. P1-P5

pilot beam

inner triplet
radiation limit

HL-LHC
installation

2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2040

experiment
beam pipes

ATLAS - CMS
upgrade *phase 1*

ALICE - LHCb
upgrade

ATLAS - CMS
HL upgrade

75% nominal Lumi

nominal Lumi

2 x nominal Lumi

2 x nominal Lumi

5 to 7.5 x nominal Lumi

30 fb^{-1}

190 fb^{-1}

450 fb^{-1}

integrated
luminosity

3000 fb^{-1}
4000 fb^{-1}

HL-LHC TECHNICAL EQUIPMENT:

HL-LHC CIVIL ENGINEERING: