Run Plan Session - Cherenkov

- Inspections in fall 2010 show hardware in stable/ready condition.
- Online monitoring software should be updated.
  - V1734(100 MHz fadc) -> V1731(500 MHz fadc) transition issues.
  - Peter Sonnek at UM looking at Online and Reco Code.
- Ckov may require special led pulser and cosmic run during beam off periods.
  - Sonnek, Cremaldi will schedule time to visit RAL in Mar /Apr.
- Would like access to Run Control Software to review V1731 DAQ setup.
  - Programmable DC Offsets, LVDS setup, Event size pre-post trigger adj, etc.
- Fast Access to Data for Offline monitoring.

L. Cremaldi, CM29, Feb 15, 2011.

V1731

4/8 Ch. 8 bit 1000/500 MS/s Digitizer

+ Image

- 8/4 channel
- 8 bit 500 MS/s - 1 GS/s (interleaved) ADC
- 1 Vpp Input dynamics (single ended or differential).
- 16-bit programmable DC offset adjustment (±0.5V)
- External ADC clock input or PLL synthesis from internal/external reference
- Front panel clock In/Out available for multiboard synchronisation (direct feed through or PLL based synthesis)
- 16 programmable LVDS I/Os
- Trigger Time stamps
- Memory buffer: up to 4 MSample/ch
- FPGA for real-time data processing
- Zero Suppression and Data Reduction algorithms
- Programmable event size and pre-post trigger adjustment
- VME64X compliant interface
- Optical Link interface
- A2818 PCI controller available for handling up to 8 Modules daisy chained via Optical Link
- Firmware upgradeable via VME/Optical Link
- Libraries, Demos (C and LabView) and Software tools