

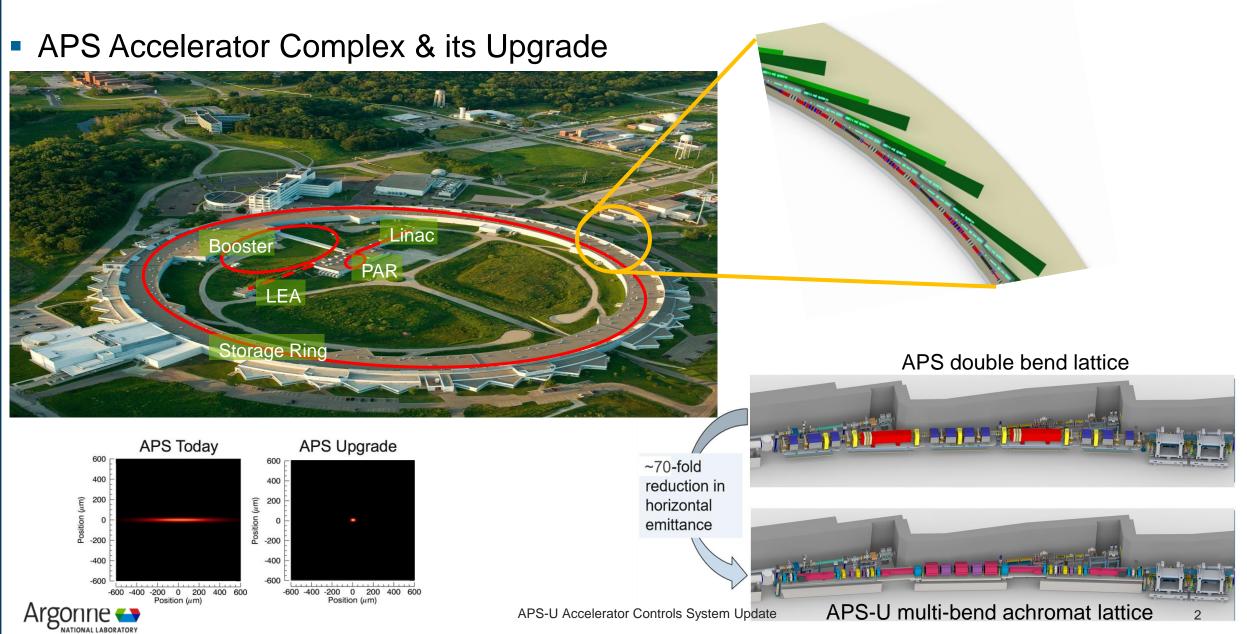
APS-U Accelerator Controls System Update

PRESENTED BY KAREN WHITE FOR APS-U CONTROLS

Advanced Photon Source Argonne National Laboratory

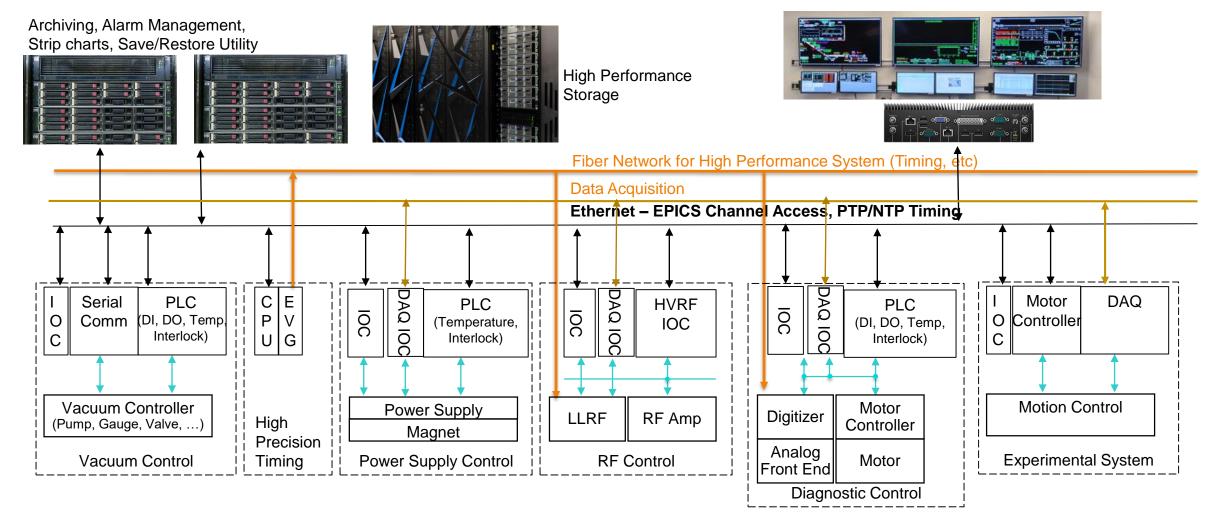
09-14-2022

APS & APS-U Overview



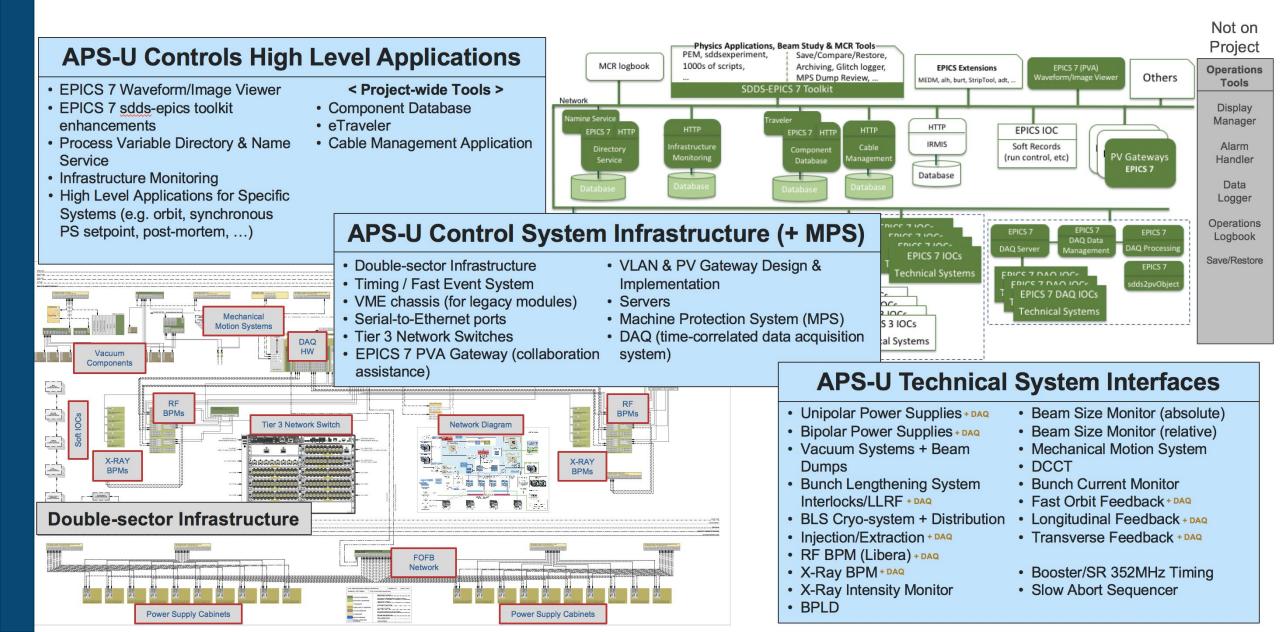
APS-U Controls System Architecture

Standard 3-tier distributed structure with EPICS7 as software framework





Overview of APS-U Controls System



Database Applications

- CDB, CDB/Cable, eTraveler are actively supporting project construction
 - CDB Mobile application provides sufficient flexibility to support in field work

341

2,706

33,841

- Some statistics of data entry
 - CDB:
 - Registered Users
 - Catalog Items
 - Inventory Items
 - Machine Elements 30,391
 - MAARC Items 163,063
 Inventory Item Tracking in CDB

- Cable:
 - Cable Catalog Items 17
 - Cable Inventory Items 2,365
 - Cable Design Items 11,8

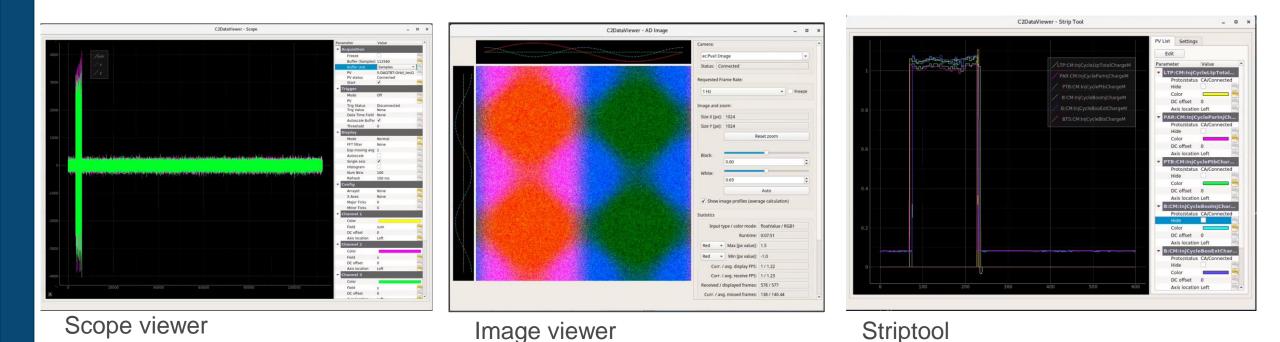
eTraveler

176 Registered Users: 287 2,365 Draft Forms: 703 11,875 **Released Forms:** 960 18,564 Active travelers: Finished travelers: 12,825 Archived travelers: 7.418 CDB Inventory Status Change by Month

		Inventory	y Item	Tracki	ng in C	DB		
Function Name	<u>Project</u> Name	Catalog Name	Tag	<u>QR ID</u>	Inventory Id		Inventory Hyperlink	Status
			Unit: 4	2852	3718	400	View Item	Installed
			Unit: 2	2850	3716	400	View Item	Installed
			Unit: 1	2213	2922	400	View Item	Installed
Controller - Motor	APS-U Production	Horizontal Collimator Controller Chassis	Unit: 0001	Null	196716	No Data	View Item	Planned
		MAXv	Unit: 0005	24691	250519	No Data	View Item	Planned
			Unit: 0004	24690	250518	No Data	View Item	Planned
			Unit: 0003	24689	250517	No Data	View Item	Planned
			Unit: 0002	24688	243383	No Data	View Item	Planned
СРИ	APS-U Production	MVME2500 CPU	Unit: 0027	33261	107989	L2109	View Item	Ready For Use
			Unit: 0028	33262	107990	L2109	View Item	Ready For Use

EPICS 7 Waveform/Image Data Viewer (C2DV)

- C2DV: A Python based data visualization tool for EPICS 7 high speed DAQ system
 - A scope viewer for plotting PVA waveforms
 - An image viewer for displaying streaming Area Detector image data over PVA
 - A striptool for monitoring CA and PVA scalar PVs



Argonne

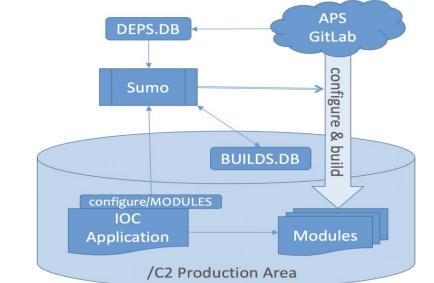
Other High-Level Applications

- A web-based naming system, which was developed originally at FRIB, has been introduced to manage the APS-U naming convention
 - 600+ name entries captured in the naming system
- OpenNMS was selected to monitor controls system infrastructure
- Olog is deployed as next logbook management system
 - Existing Controls logbook data has been migrated into this system now
- Logging as well as IOC console message to be logged into ElasticSearch using logstash, and browse it on Kibana



EPICS Module Configuration, Build, and Management

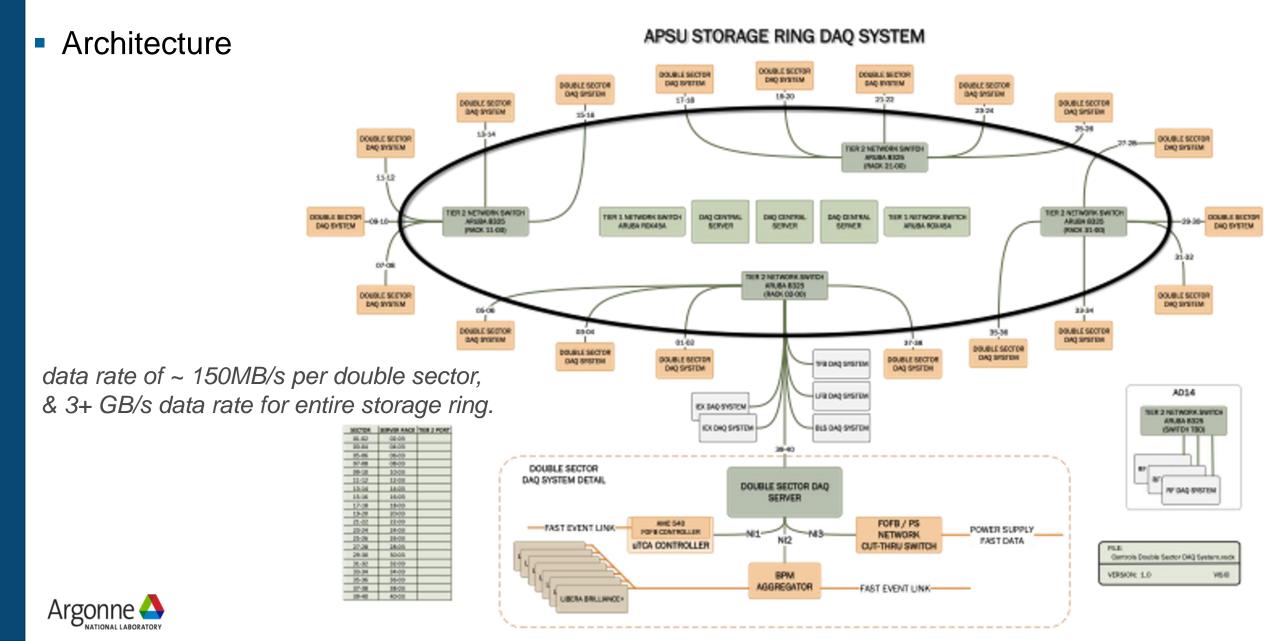
- Using Conda for software environment management including EPICS
- Adopted 'Sumo' package to automate IOC modules configure/build
 - Sumo (HZB/BESSY) to build IOC support modules from source on demand
 - All source comes from APS' GitLab server
 - IOC applications will specify needed support modules and versions
 - Sumo is used similarly to create private module build areas to assist development
 - Where appropriate we hope to include PLC, FPGA, and DSP code in the same environment
 - We are developing against an EPICS 7 release



0 0 X tosc ad	0 0 0 X rtbEvents.ad				
U:S27:BPSC2 Bipolar PS Controller	U:S28:BPSC2 Bipolar PS Controller				
FPGR Suster Info					
Sig ID: 040 0kg	RTFB Events and Timing	panatility trux 175+53			
Dup ID: 0+fffffffc 0+7	RIFB Event	angers and			
FPGA Build Date: 2017-07-03 14:41:40	Nux Events: 30 events				
Git Description: v0.2-13-gBal0dBe	Last Interval: 28,000 US (between events)	and the second sec			
Git Hach: 8a10dRa25ce04bebac0d4457482685eFFaa2dbd	flax Interval: 27,000 uS (between events)	******** Reboot Time : 2019-0	5-22 11:48:30 *******		
-Controller Texperatures	Min Interval: 23,000 uS (between events)	<pre><<<< Press any key to enter</pre>	manner of mahoot assas		
Reference: 124,00 degC TC short to VEC TC short to DE	FBC Clock Event	content of the stand of the sta			
Therecouple: 33,00 degC to teen	Nus Events: 31 events				
Bire	Last Interval: 34,000 uS (between events)	Please type in User Name [tfo			
0 0 X tost ad	Max Interval: 33,000 uS (between events)	Please type in reason for reb			
	Min Interval: 24,000 uS (between events)	Reboot time is recorded. # Show startup message			
U:S27:BPSC3 Bipolar PS Controller	and the second second second second second	stdPrtMessage			
FPGH System Info	UDP Packet RX (Internal FPGA Event)				
Sys ID: Oxfffffffd Oxfffffffb	Valid Packets: 26 events Invalid Packets: 36 events				
Dig ID: Oc Orffffffa	Last Interval: 18,000 US (between events)	^A d Detach screen			
PPGA Build Date: 2017-07-03 14:41:40	Nex Interval: 31.000 uS (between events)	^A ? Help			
Git Description: v0.2-13-g8a10dHe Git Hash: 3a10dHg25ce84bebac0d4457482685effax2bbd	Min Interval: 25,000 uS (between events)	#			
		## Start sequence programs			
-Controller Teaperatures	Latency	#seq bpscSeq, "IOC=\$(IOC_NAME			
Reference: 113,00 degC TC short to KC Thereocouple: 39,00 degC TC short to DB	Time From FBC Elock Event to the next valid	cd "/home/phoebus/TFORS/C2/io			
ingradoupte: 35,00 cag. It gas	UDP Packet RX event in the PS controller.	## Script st.cmd done. sioc2s27bpsc>			
Rev	Nun Ress: 35 events Last Latencu: 22,000 uS	2019-85-22 12:00 sioc2s27bp			
© © S bpsc.ad	Mer Latency: 22,000 uS	2019-05-22 13:00 stoc2s27bp			
	Min Latency: 37,000 uS				
U:S28:BPSC2 Bipolar PS Controller	Clear Datistics	Data: id=b'AMM' flags=0 pkN		reserved#0 length#4 ref	
- FPGR System Info	Live Restored	Command received on: 2019-05 RX: b'AMM\x00\x00\x04\xe1\			
Sys ID: 0.dffffffc 0.3		Data: id=b'AMM' flags=0 pkN			
FPGA Build Date: 2017-07-03 14:41:40		Command received on: 2019-05	-22 13:41:57.397021		
Sit Description: v0.2-13-e8a0069a					
Git Hash: 8a10d9a25ce94bebac0d4457482685effaa2dbd		Data: id=b'AMM' flags=0 pkN	m#408465 tac=0x10:read	reserved=0 length=4 ref	+0x382c
-Controllar Teaceratures		Command received on: 2019-05 RX: b'AMM\x00\x00\x84\xe1\			
Reference: 115,00 degC TC short to UC		Data: id=b'AMM' flags=0 pkN			
Thereaccupie: 24.00 degC To peer		Command received on: 2019-05	-22 13:41:57.397172		
Ree					
		Data: id=b'AMM' flags=0 pkN	m=319963 tac=0x10:read	reserved=0 length=4 ref	=0x382c
0 0 🖄 bpsc.adl		Command received on: 2019-05 RX: b'AMM\x00\x00\x04\xe1\	22 10:41:07:397320		
U:S28:BPSC3 Bipolar PS Controller		Data: id=b'AMM' flags=0 pkN			
FPB Sates Info		Command necetived on: 2019-05	-22 13:41:57.397400		
Sur ID: 0.0 0.4ffffff Mark					
Dip D: 0dfffffff 06		Data: id=b'AMM' flags=0 pkN		reserved=0 length=4 ref	=0x382c
PGA Build Date: 2017-07-03 14:41:40		Command received on: 2019-05 RX: b'AMM\x00\x00\x04\xe1\			
Sit Description: v0.2-13-gBa10d9a		Data: id=b'AMM' flags=6 pkN			
61t Hash: 8a10d9a25ca94bebac034457482655efFaa2dbd		Command received on: 2019-05	-22 13:41:57.397614		
-Controller Texperatures-		RX: b'AMM1x001x001x841xe11			
Reference: 113.00 degC TC short to VCC					=0x302c
Thereocouple: 28.00 deaC TC teen					

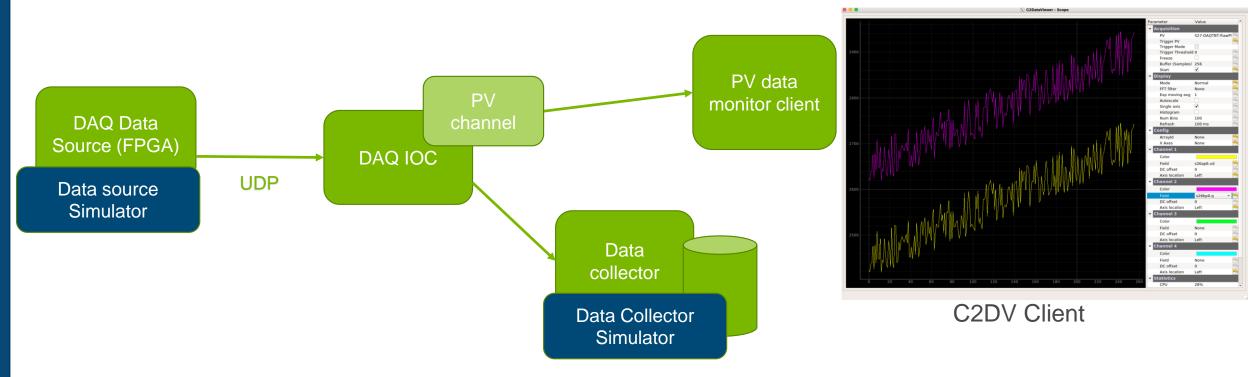
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APS-U Time-Corelated DAQ System



DAQ System Simulation Environment

- In order to run the DAQ system in different test environments, several simulation tools were developed including data source simulator and data collector simulator
 - Data source simulator: simulate the hardware that generates and sends data to a specific DAQ IOC. The simulation generates simple linear data with noise to easily verify that the data was processed correctly
 - Data collector simulator: captures PV objects published by the DAQ IOC, and save the data into a local file in desired format like HDF5, or other site-specific data format (e.g. Self-Describing Data Sets [SDDS] at APS)





APS-U Time-Corelated DAQ System

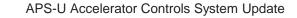
DAQ Hardware







TBT DAQ aggregator FPGA chassis







Example of DAQ Linux Servers installed



APS-U MRF Fast Event/Timing System

- New timing system with MRF 300-series hardware
 - Event Link distributed to 232 technical systems
 - 113 + Individual Triggers (TTL) to technical systems

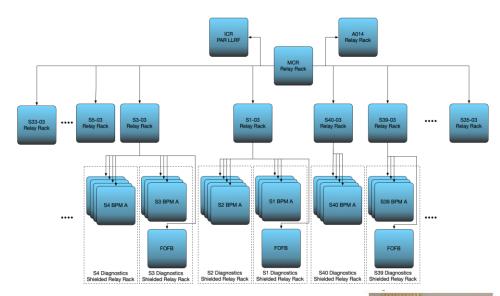
Generator	Receiver	Fanout	Rear Transition	TTL Input	TTL Output
33	41	45	9	31	162

Jitter measured relative to event clock reference at APS

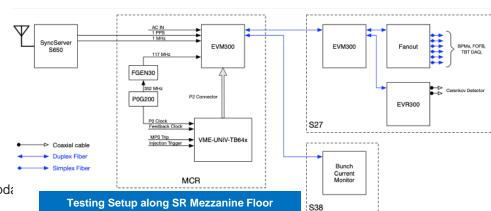
	UNIV Output		CML Output		
PLL Bandwidth	RMS	Pk-Pk	RMS	Pk-Pk	
MH (375 Hz)	16.15 ps	101.56 ps	8.70 ps	78.13 ps	

- Fully use delay compensation function to compensate the time delay in the fibers
- A few testing stands setting up
 - In Diagnostics lab, supporting RF BPM acceptance test
 - Along SR mezzanine floor
 - In installation preparation warehouse



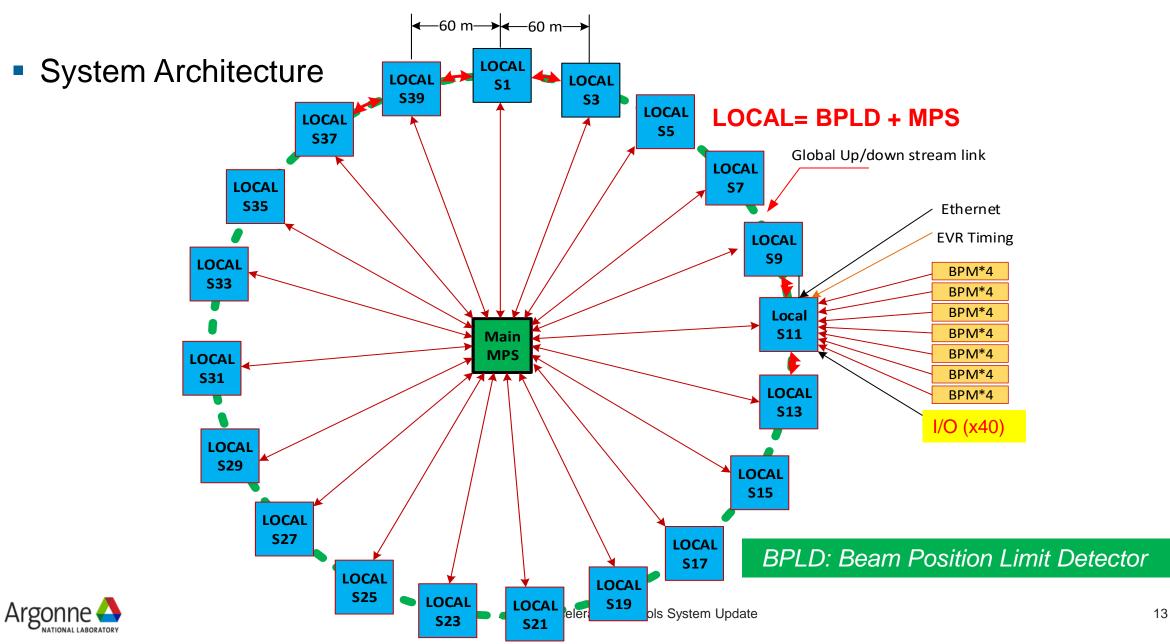






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APS-U MPS and BPLD System



APS-U MPS and BPLD System

System Hardware



Main MPS Chassis



Local MPS/BPLD Chassis



MPS Chassis Power Supply



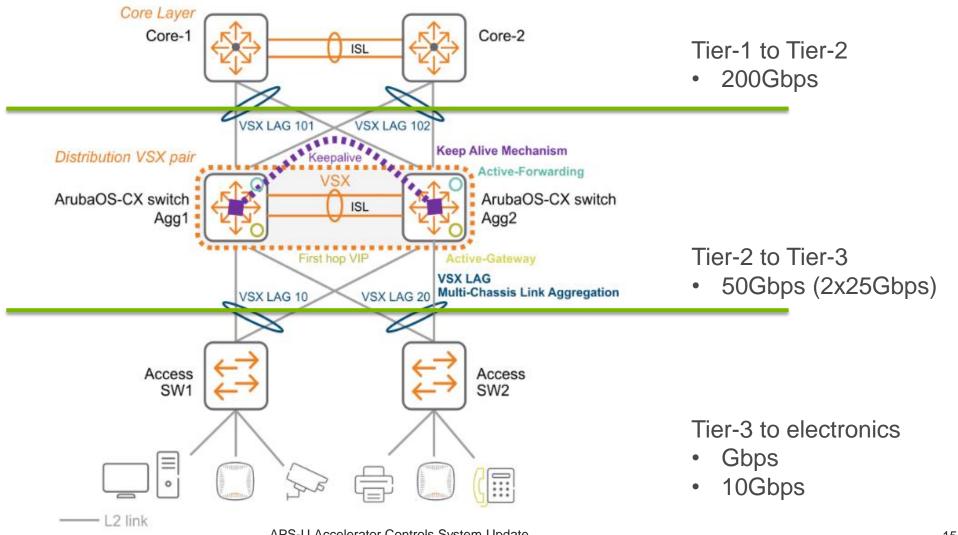
Fully populated MPS stand under integration testing Left to right:

- MPS chassis rack #1,
- *MPS chassis power supply rack,*
- electronics rack (BPM, MRF timing, network, etc),
- MPS chassis rack #2
- MPS chassis rack #3

APS-U Accelerator Controls System Upda

APS-U Accelerator Network

Architecture



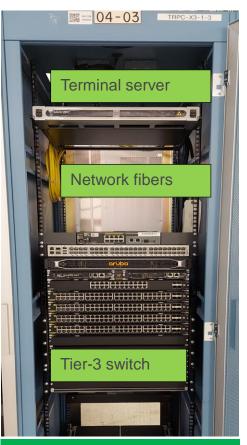


APS-U Accelerator Network

- Network Infrastructure Status
 - APS-U network installation finished, including its fibers
 - Network subnet/VLAN (total 31 VLAN) design finished, implemented, and ready to use

Vlan Name (32 max)	Max Hosts	DHCP
MCR-Workstations	250	yes
DAQ-Servers	64	yes
MPS	250	no
Accelerator-Timing	250	no
Injection-Extraction-System	125	no
Spark-BPM-DAQ-System	250	yes
RF-BPM-Libera-Brilliance	250	yes
RF-BPM-Spark	250	yes
BSM-Motion-XBPM	250	no

Example APS-U accelerator VLAN implemented and ready



Tier-3 Network installed



Summary

- APS-U is under active construction and preparation for its dark time starting from April 2023
- Database application like CDB, Cable, as well as eTraveler system plays critical role to support the project
- EPICS7 based time-corelated DAQ system capable to stream data over pvAccess with data rate higher than 3GB/s, which is gaining more and more interesting in supporting beam commissioning and future operation
- MRF 300-series based timing system, with lots of new functions enhanced to meet APS-U needs including full functional delay compensation capability
- The MPS/BPLD system starts with a star connection topology with future extendibility to a ring structure
- A high-performance network with 31 VLAN in place to meet various needs
- Installation started in the place where suitable including network as well as rack mounted DAQ computer server
 APS-U Accelerator Controls System Update