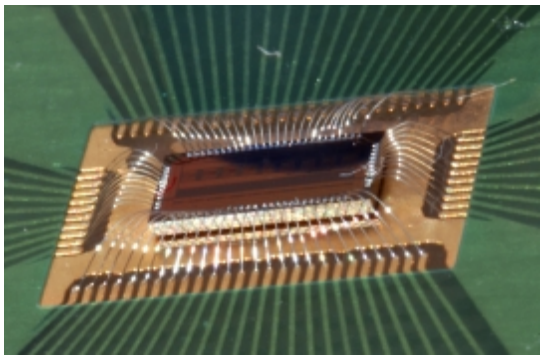
European Organization for Nuclear Research

NINO - An ultra fast low power front end amplifier discriminator chip



Abstract

CERN has available a low power front-end amplifier discriminator ASIC chip for use in applications based on electron and photon detecting in medical imaging, life science or material research. This so-called NINO ASIC allows for an 8-channel input signal charge measurement through encoding discriminator pulse width with excellent timing resolution at very high rate, while at the same time providing a very low noise performance and power consumption characteristics per channel.

Technology stage

Produced in 0.25µm CMOS technology, the NINO ASIC is available off the shelf for licensing or can be produced on short term. Upon request, CERN provides support and pre-configured solutions (data acquisition, chip boards, readout software) for the integration of such chips with user specific detectors and mechanical support structures.

Possible applications

- Photon and electron detection at very high rates in medical imaging, life science and material research.

Innovative features

- Compact packaging through 0.25µm CMOS technology (fits in a 2x4 mm2 area).
- Adjustable discriminator thresholds.
- Adjustable 50 ohm input resistance.
- 27mW power consumption per channel.
- Front end time jitter <10ps.
- Sustains very high rate (>>10MHz).

Specifications

- Channels: 8.
- Voltage supply: 2.5V.
- Peaking time: 1ns.
- Input signal range: 30fC - 2pC.
- Noise: <2500 e-.
- Discriminator threshold: 10fC - 100fC.
- Timing precision: <10ps jitter.
- Output: LVDS.

Contact

Bernard DENIS

Tel.: +41 22 767 5387

Fax: +41 22 767 3540

Email: bernard.denis@cern.ch