PETA2: A 36-CHANNEL TDC/ ADC ASIC

ABSTRACT

A self-triggered, multi-channel readout ASIC, PETA2, combining time and energy measurements has been developed. Each of the 36 channels is independently triggered by a leading edge discriminator. Upon a hit, the event time is registered and an integrator is started for a programmable period. After conversion of the integral by an on-chip ADC, the fully digital hit data is read out through shift registers. The ASIC is therefore perfectly suited to replace existing discrete readout electronics by a single chip.

Achieving low noise in the analog part was the most important design

goal. Current-mode logic with low swing and minimal supply bounce has therefore been used in critical parts, supplies have been separated for various digital and analogue blocks, and the tri-wells available in UMC's 0.18 um technology have been exploited. The lowest possible threshold setting with all channels running is about 2 mV, the threshold noise is ~0.2 mV (rms). To achieve a uniform threshold level in all channels a compensation circuit is included. The circuit compensates for a threshold dispersion caused by process mismatch. The measured timing resolution of 16 ps (single-channel rms) is very close to the theoretical expectation for the PLL-locked 50 ps bin width. The 8-bit energy resolution is sufficient for the main target application. The power consumption is 31 mW per channel.

TECHNOLOGY STAGE

- Prototypes of PETA2 available from a MPW
- Next generation of the ASIC (PETA3) is expected back from fabrication by the end of February 2011.

POSSIBLE APPLICATIONS

- medical imaging
- particle physics experiments
- range finding
- material science

SPECIFICATIONS PETA2

- Technology: 0.18 um standard mixed mode CMOS, 1P6M
- Power supply: 1.8 V
- Power consumption: ≅ 31 mW/ch
- Lowest threshold: ≅ 2 mV
- Single channel timing resolution: 16 ps rms

ADVANTAGES

- Self-triggering analog input-digital output solution
- 36 differential channels
- Leading-edge discriminator
- Integrator and ADC
- Time-to-digital converter

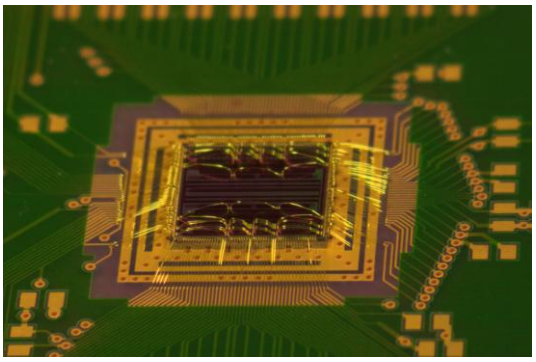

Figure 1. PETA2 die (5 mm x 5 mm) wire-bonded to a PCB

EXISTING APPLICATIONS

The first application of the ASIC is the EU-funded HYPERImage project (www.hybrid-pet-mr.eu) which has as a goal to build a PET system which can be operated inside of a MRI scanner. The detection of the scintillation light from the 511 keV gamma rays is done with novel silicon photo multiplier arrays which replace the large and magnetic field sensitive photo multiplier tubes. The cell size of one photo detector element of only 3 mm x 3 mm leads to a large number of readout channels. The readout electronics is therefore required to be compact, low-power and scalable. The PETA2 ASIC processes the analogue information in close proximity to the photo detectors, reducing both the noise interference on analog signals and the number of wires to be routed to the readout modules. A total of twelve ASICs is read out by a large FPGA located still in the MR bore. After first preprocessing steps, the event data is sent out by a single gigabit optical link. A first small system was currently built. The excellent timing resolution of PETA2 enables the use of time-of-flight information in a whole-body scanner.

Figure 2 shows the basic building unit of the HYPERImage scanner, a self-contained detector stack consisting of 3 interconnected PCBs. The 4x4 photo detector elements on the upper layer are connected to two PETA2 ASICs on the middle layer. The lowest PCB contains voltage regulation and data preprocessing in a small FPGA.

SPECIFICATIONS STACK

- SiPM channels: 64
- SiPM size: 2 x 2 monolithic array
- Fill factor: 85 %
- Power consumption: ≅ 3 W
- Dimensions: 33 mm x 33 mm x 25 mm

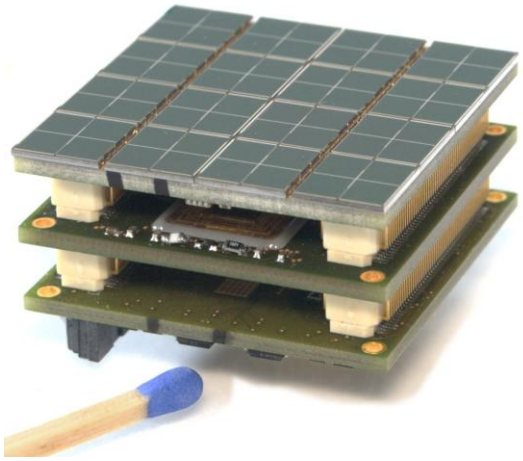

Figure 2. The basic building block of the HYPERImage PET/ MRI scanner (33 mm x 33 mm x 25 mm)

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ACKNOWLEDGEMENTS

This work is supported by the European FP7 Health project HYPERImage, Grant Agreement N° 201651.