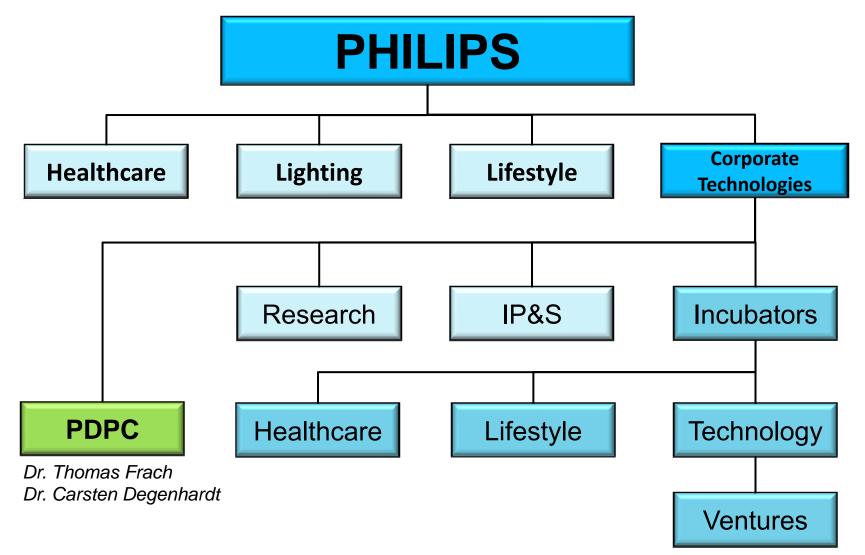
# **PHILIPS** sense and simplicity

# Photon Counting with arrays of Digital SiPM's

Philips Digital Photon Counting (PDPC) Dr. York Hämisch Anja Schmitz

SiPM event, CERN, February 17th, 2011

### **PDPC** in Philips



### **Digital Silicon Photomultipliers (dSiPM) -**The next solid state innovation

Transistor



Television

**Digital Camera** 

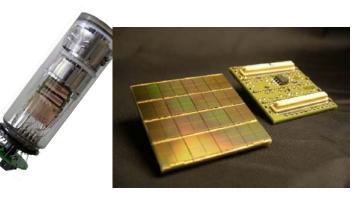




X-Ray imaging

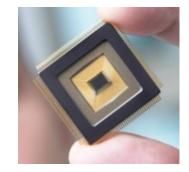


#### **Digital Photon Counting**

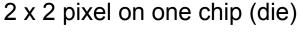


### How to replace old-fashioned PMT's?

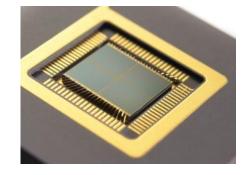
- Make the SiPM digital
  - 1 pixel

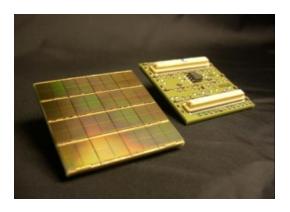


- Increase integration
  - $-2 \times 2$  pixel on one chip (die)



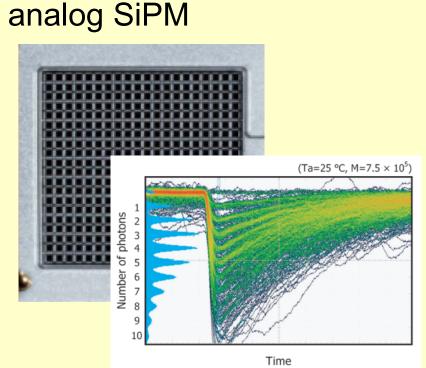
- Assemble arrays
  - 8 x 8 pixels on one PCB (tile)





# Digital Photon Counting – The concept

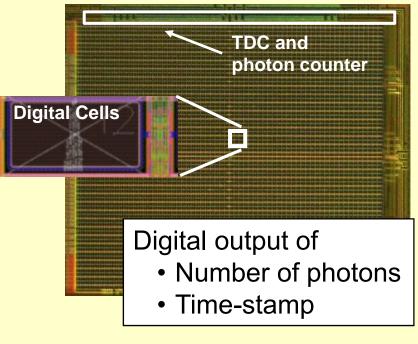
Intrinsically, the SiPM is a digital device: a single cell breaks down or not



www.hamamatsu.com

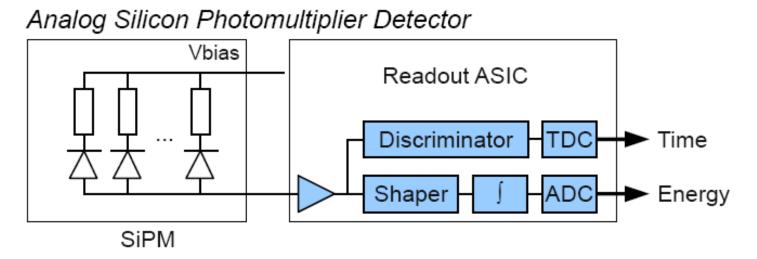
### Summing all cell outputs leads to an analog output signal and limited performance

### digital SiPM (dSiPM)

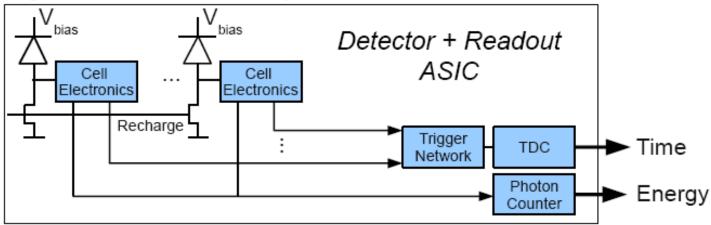


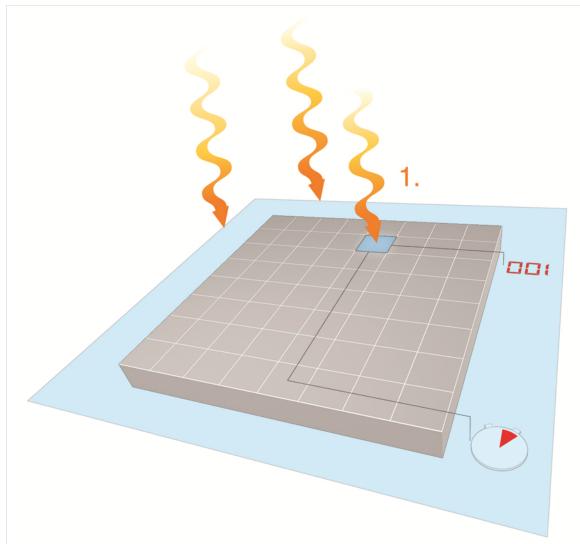
Integrated readout electronics is the key element to superior detector performance

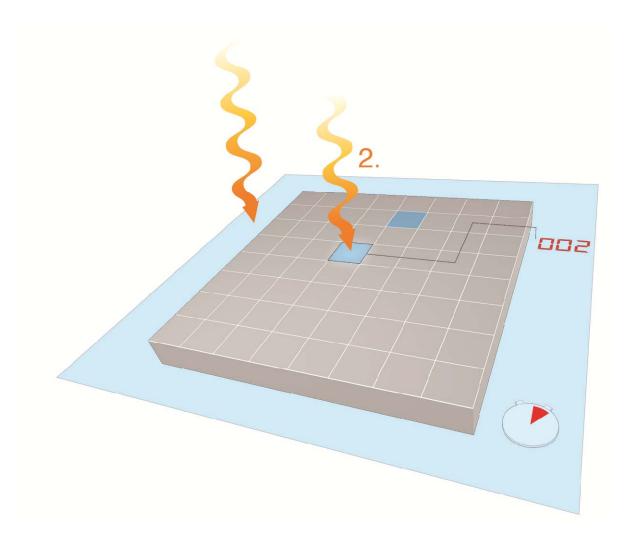
### Analog vs. Digital SiPM

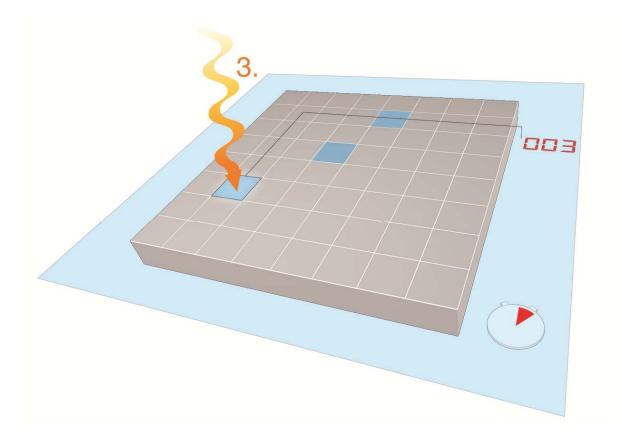


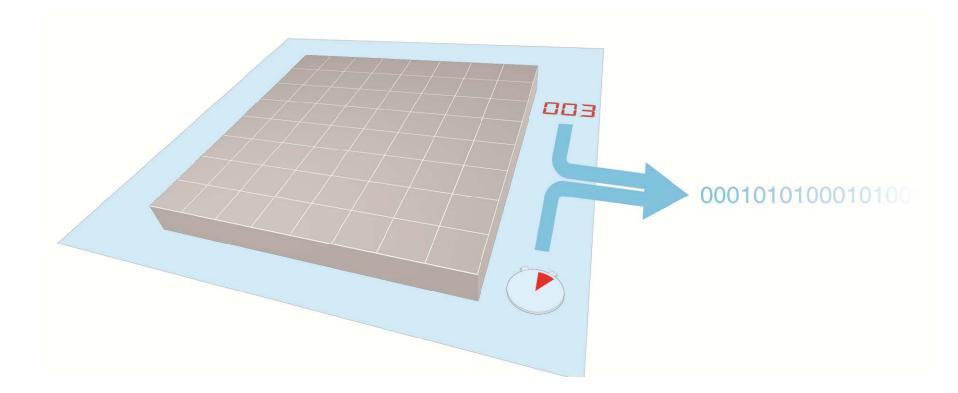
#### Digital Silicon Photomultiplier Detector



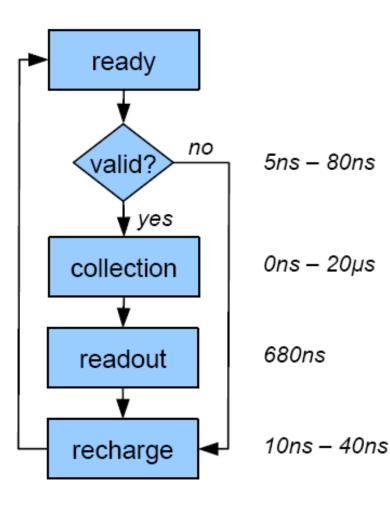








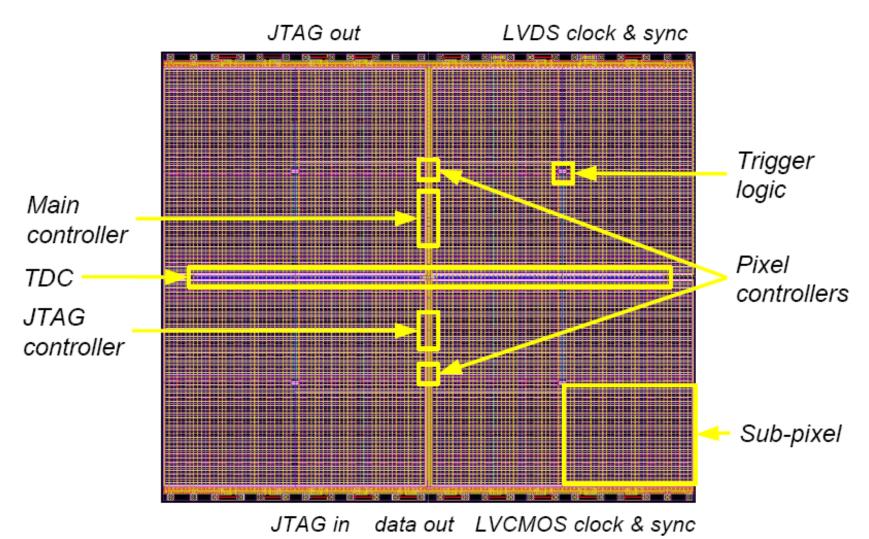
# **Digital SiPM: Acquisition sequence** (example)



- 200MHz (5ns) system clock
- Variable light collection time up to 20µs
- 20ns min. dark count recovery
- dark counts => sensor dead-time
- data output parallel to the acquisition of the next event (no dead time)
- Trigger at 1, ≥2, ≥3 and ≥4 photons
- Validate at ≥4 ... ≥64 photons (possible

to bypass event validation completely)

### PDPC Digital SiPM: architecture (die)

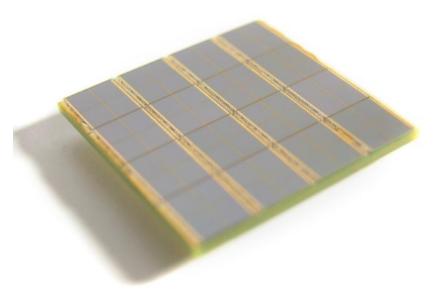


©Philips Digital Photon Counting, February 2011

# Digital SiPM array (tile)

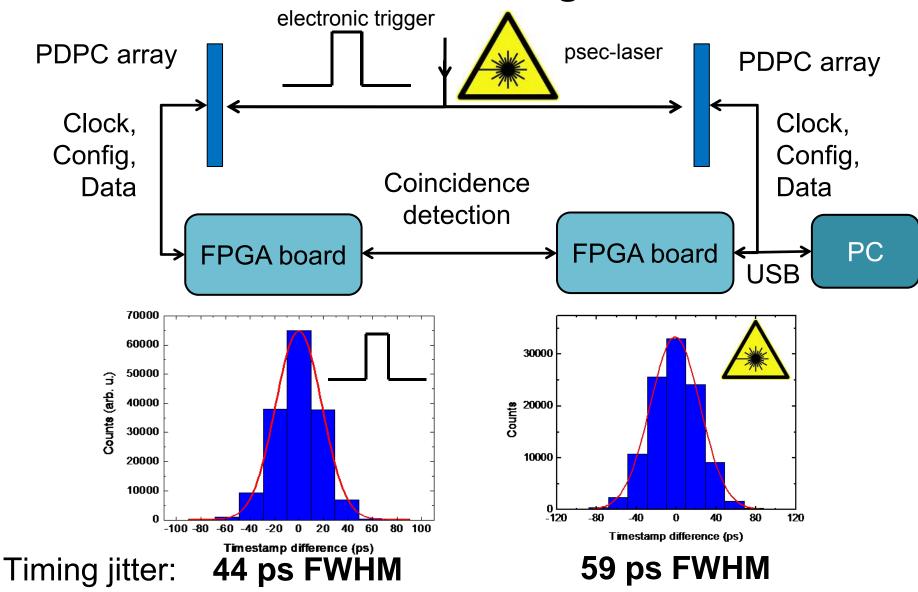
Features

- 8 x 8 digital SiPMs (on 4 x 4 chips)
- 6400 diodes (cells) per pixel
- ~ 11 cm<sup>2</sup>
- 4-side tiling possible
- Inputs
  - 1.8 V, 3.3 V, 30 V
  - JTAG (test and configuration)
  - 200 MHz reference clock
  - External trigger input
- Outputs
  - 100 MHz serial data (photon count, timestamp)
  - Event detect trigger

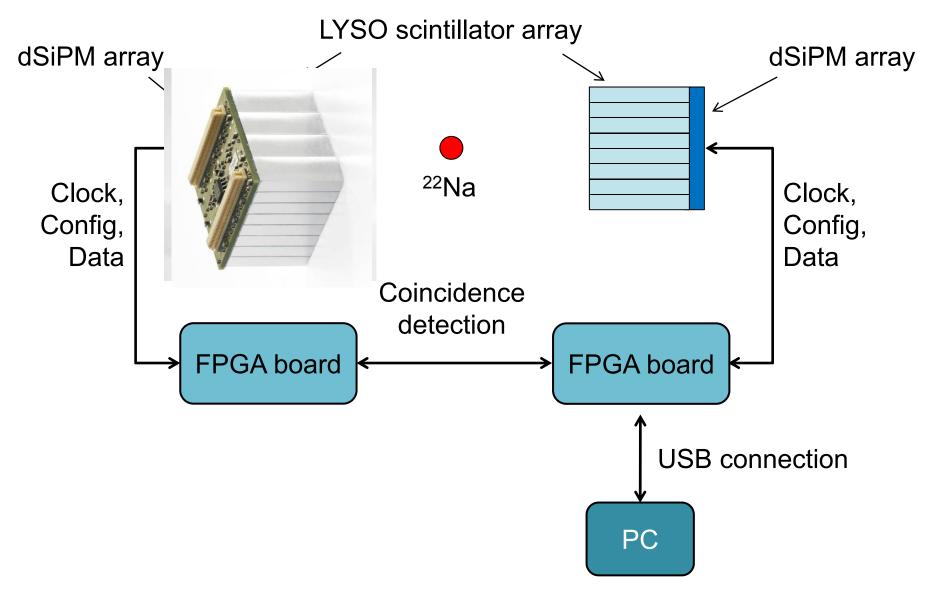


YΗ

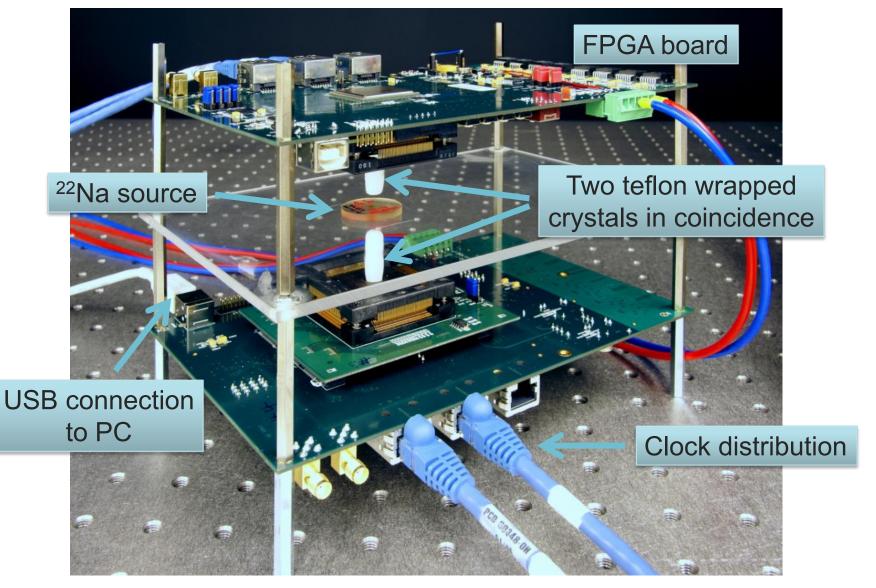
### PDPC dSiPM: intrinsic timing resolution



### PDPC scintillator coincidence setup

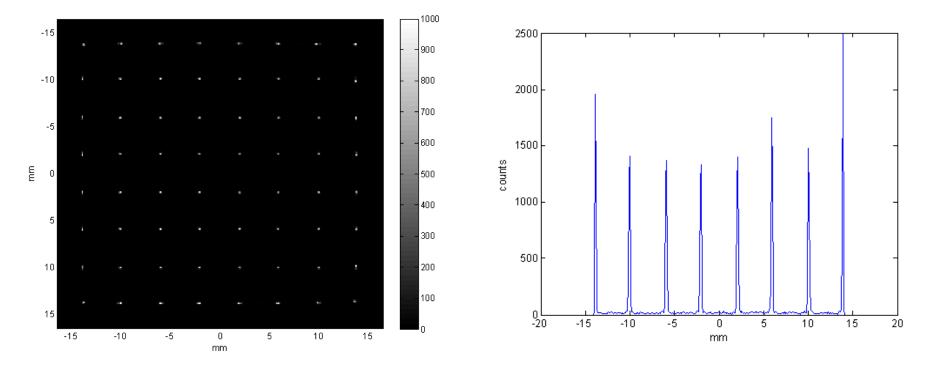


### PDPC test setup (available Q2-11)



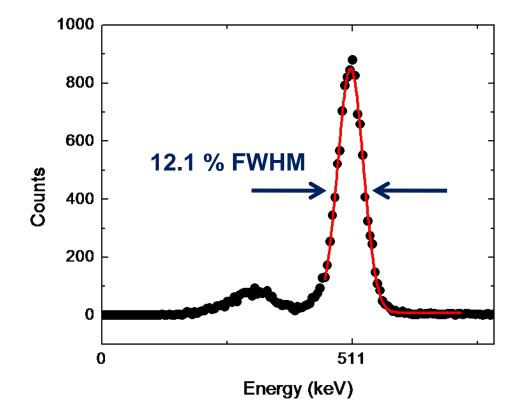
### **PDPC dSiPM: Scintillator readout** (1:1 coupling) Floodmap

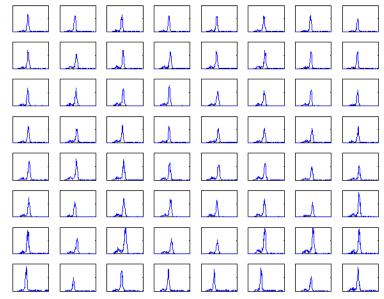
• LYSO array, 8 x 8 crystals, 4 mm x 4 mm pitch, 22 mm length



### **PDPC Digital SiPM**

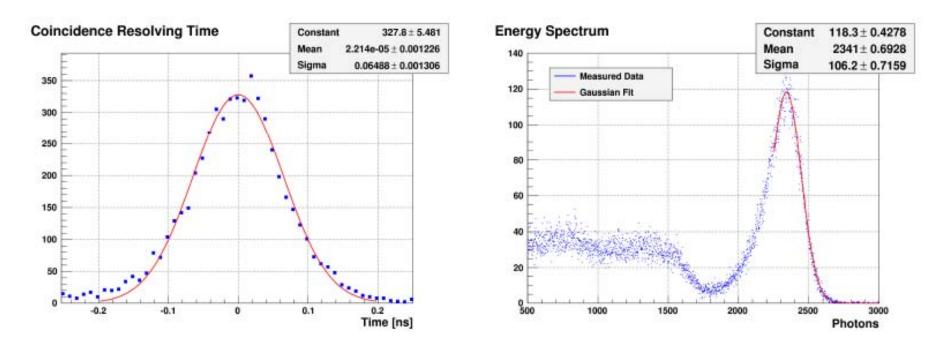
Energy resolution





- LYSO array, 8 x 8 crystals, 4 mm x 4 mm pitch, 22 mm length
- Saturation was corrected for

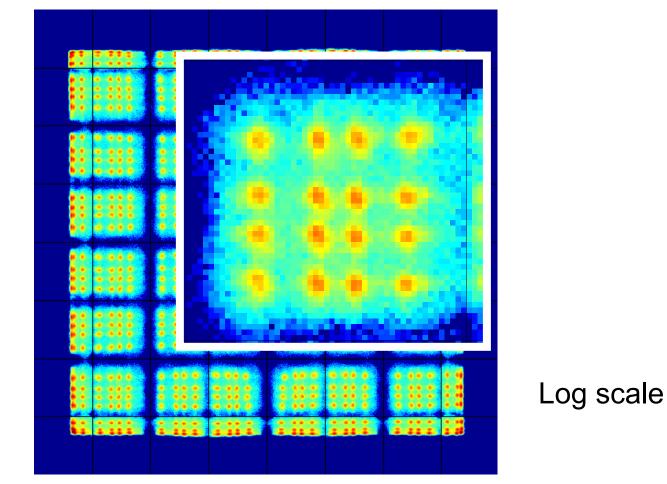
### PDPC dSiPM: Coincidence timing resolution



- 3X3x5 mm<sup>3</sup> LYSO in coincidence, <sup>22</sup>Na source
- Time resolution in coincidence: 153ps FWHM
- Energy resolution (excluding escape peak): 10.7%
- Excess voltage 3.3V, 98.5% active cells
- Room temperature (31°C board temperature, not stabilized)

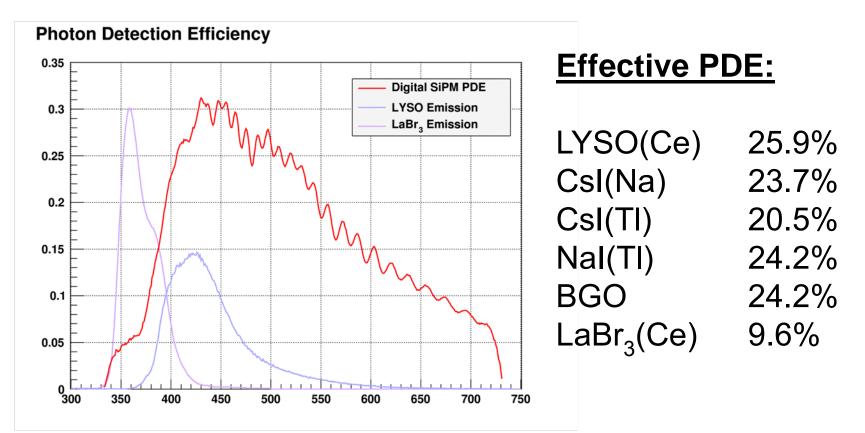
### PDPC dSiPM: Small crystal readout

LYSO array, 30 x 30 crystals, 1 mm x 1 mm pitch, 10 mm length



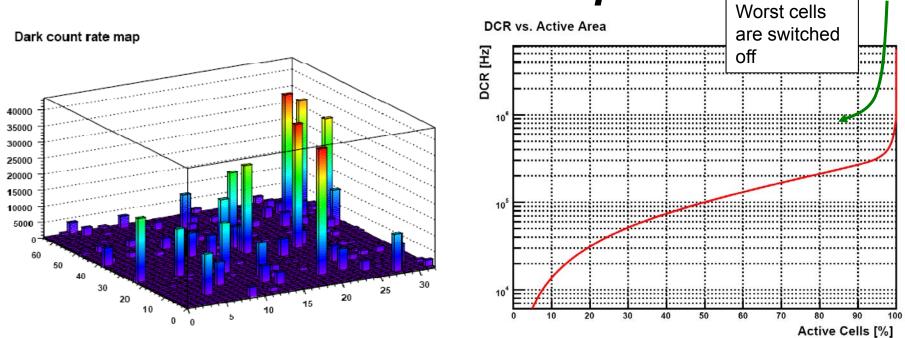
Data analysis by P. Düppenbecker, Philips Research

### PDPC dSiPM: Spectral sensitivity



- Peak PDE ~30% at 430nm and 3.3V excess voltage
- Conservative diode design (50 % fill-factor)
- No anti reflection coating used

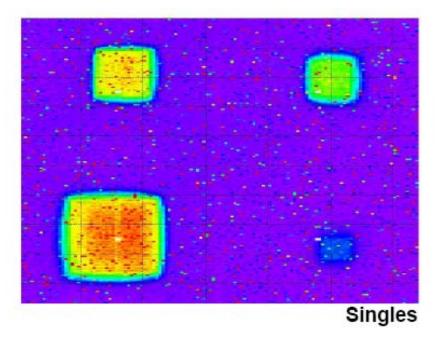
### PDPC dSiPM: Dark count map

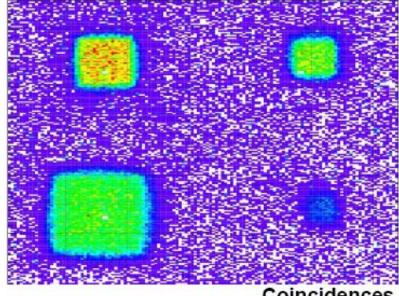


- Dark counts per second at 20°C and 3.3V excess voltage
- ~ 95% good diodes (dark count rate close to average)
- Typical dark count rate at 20°C and 3.3V excess voltage: ~150Hz / diode
- Dark count rate drops to ~1-2Hz per diode at -40°C

#### DHIIDS

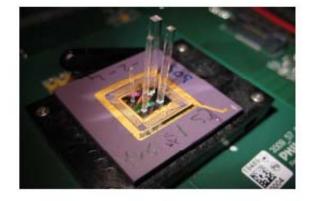
### PDPC dSiPM: slow scan imaging mode



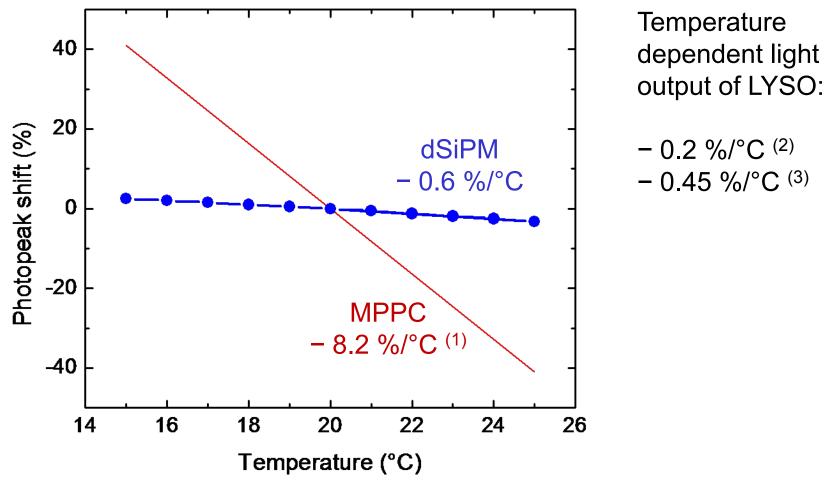


Coincidences

- Spatial sampling of the light distribution
- Similar to dark count map measurement
- Dark count map can be used for correction
- Alternatively, use coincidence to reduce noise
- Potentially useful for light guide design

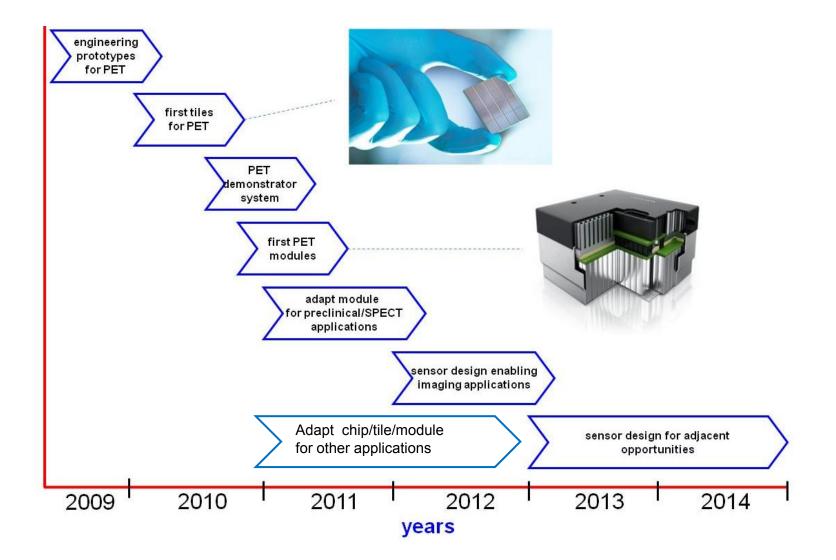


### **PDPC dSiPM: Temperature dependence**



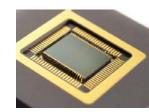
- <sup>1</sup> K. Burr et al, Nuclear Science Symposium Conference Record, N18-2, 2007
- <sup>2</sup> R. Mao et al, IEEE Transactions of Nuclear Science, vol. 55, 2008
- <sup>3</sup> C. Kim, Nuclear Science Symposium Conference Record, M07-113, 2005

### PDPC: Technology Roadmap



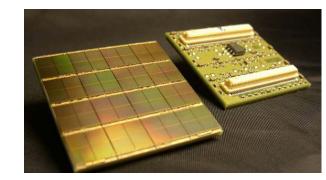
### PDPC sensors: simplified electronic design

die (2 x 2 pixel)



no. of photons/pixel

tile-PCB (16 dies + FPGA)



time stamping sorting, control

module PCB (n-tiles)

#### processing unit





tile power supply, clustering, Anger logic

e.g. coincidence processing

### **PDPC sensors: Benefits**

### Application

Speed

Outstanding timing resolution (e.g. for TOF)

Sensitivity

 Lower dark count level (background noise) than analogue systems

#### Robustness

- Low sensitivity to temperature variations
- Insensitive to electromagnetic interference

### System design

- Simplified system design (no HV, no analog processing)
- Reduced system costs
- Low voltage operation / Reduced power consumption





