An ASIC for Readout of SiPMs

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Abstract

We have developed an application specific integrated circuit (ASIC) suitable for the readout of up to 64 silicon photomultipliers (SiPM).

The ASIC can be used with SiPMs and scintillators for energy spectroscopy and timing of ionizing radiation. The ASIC provides important functionality for SiPMs: The preamplifier input potential can be programmed to set the bias voltage for the SiPMs connected to the input. The input dynamic range is relatively large (0 to 55 pC). The ASIC triggers, if any of the input signals exceeds a threshold. The trigger can be used to sample the signal amplitude and record the trigger time. The ASIC delivers both amplitude and time from all channels via an analog multiplexer. The ASIC has a programmable register which configures digital-to-analog converters for the preamplifier input potentials, the trigger thresholds, the internal bias setting and other functionality. Many ASICs can be combined for the readout of multiple arrays of SiPMs. The preamplifier input is designed for capacitive load of up to 300 pF and a dark current of up to 10 uA.

We have produced prototypes of the ASIC and tests are in progress. The article describes the functionality of the ASIC and its performance.

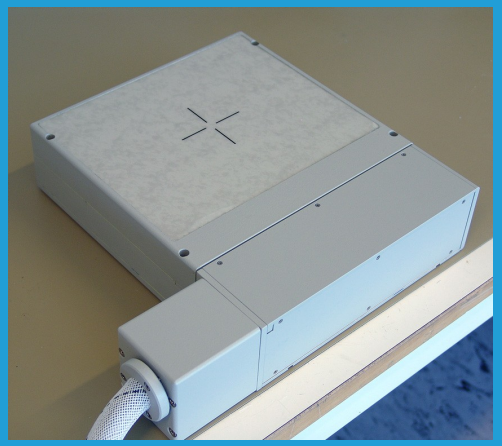
Motivation for the Development of ASIC for SiPM/MPPC

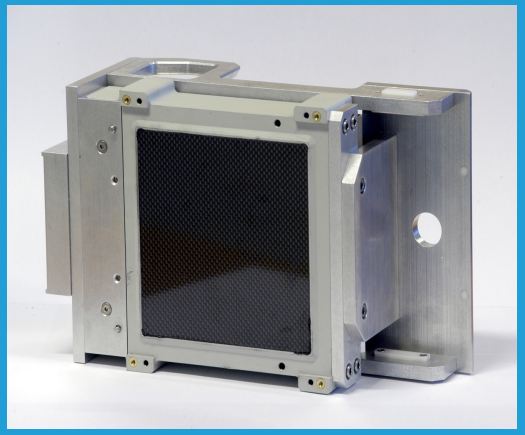
There is great interest in SiPMs / MPPCs,
since they provide an alternative to PMTs, and APDs.
SiPMs / MPPCs are photon counters, that offer a large effective gain, fast signal formation, good detector efficiency, small/compact, etc.

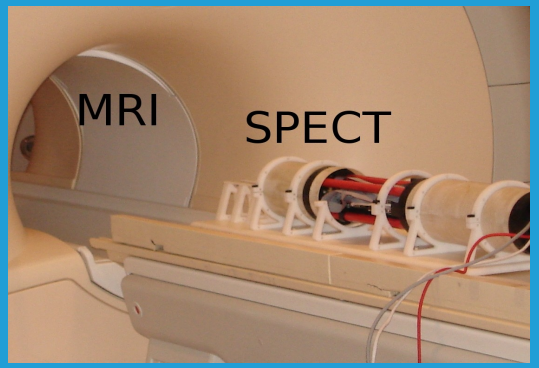
There is great interest in mixed-mode analog-digital integrated circuits (ICs) for readout of SiPMs / MPPCs
ICs can read many SiPMs/MPPCs, ICs can be designed for low noise, ICs provide many functions, and they are small/compact

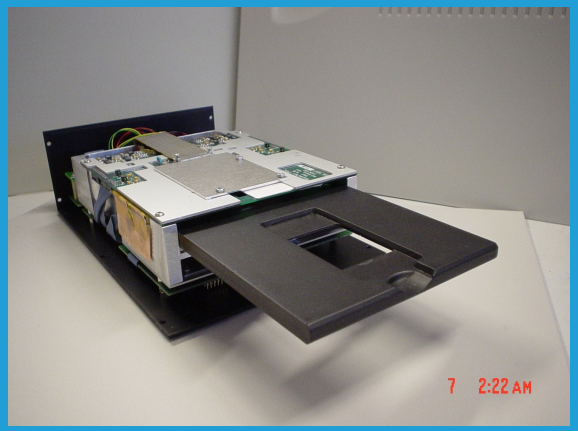
Many applications require specific ICs ----> ASICs
An ASIC provides a compact data acquisition system solution in a monolithic silicon chip.

GMI Gamma Camera Prototypes, Examples

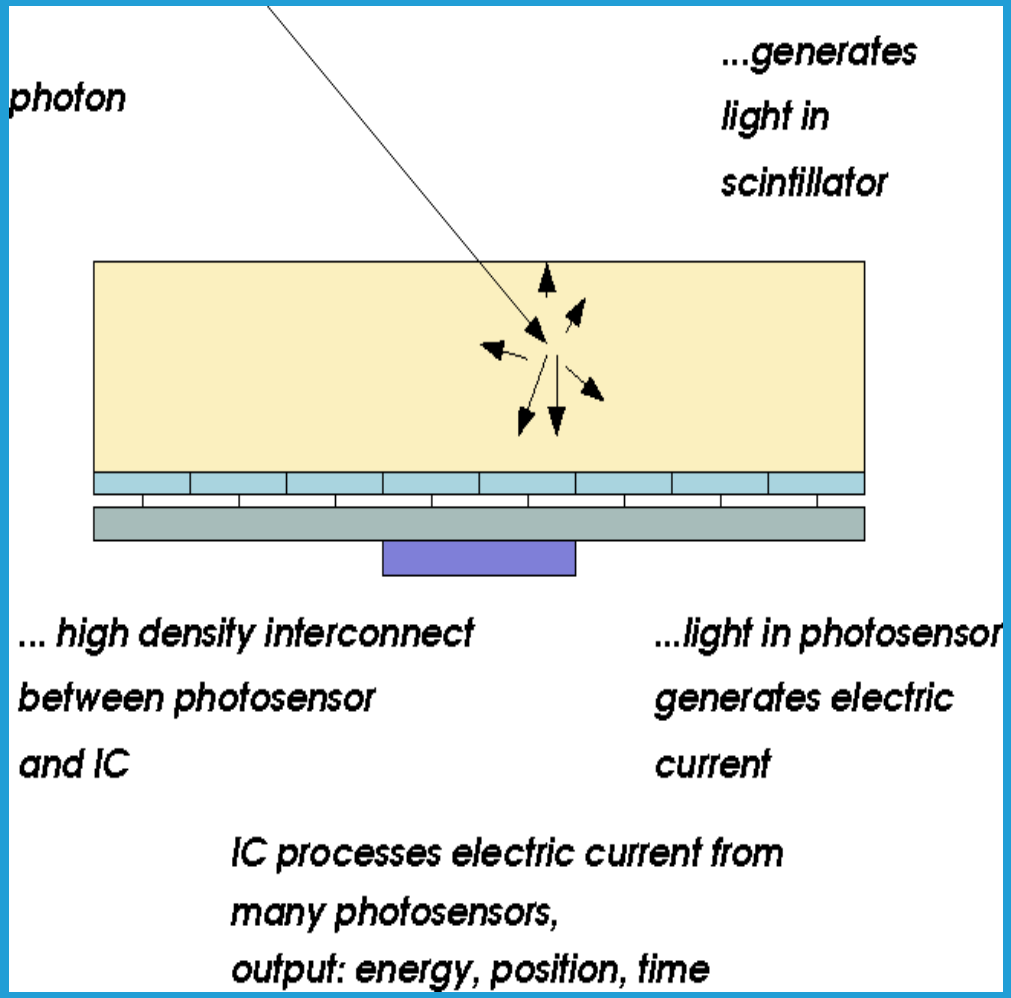


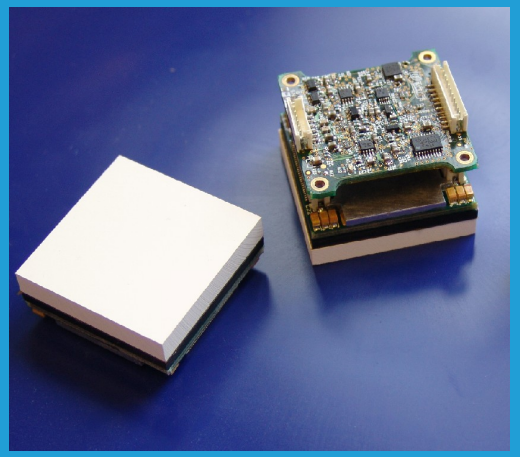


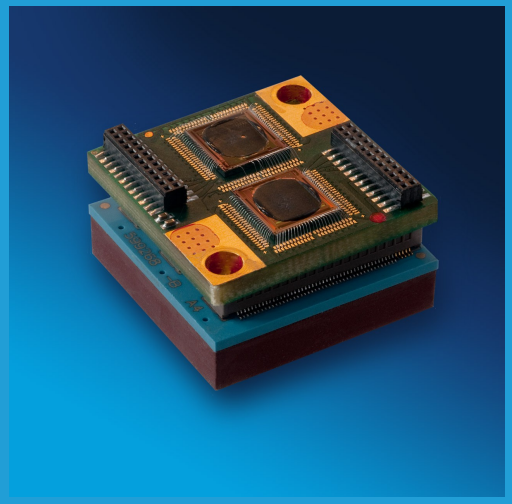




Technology Example: Radiation Detectors with Integrated Readout

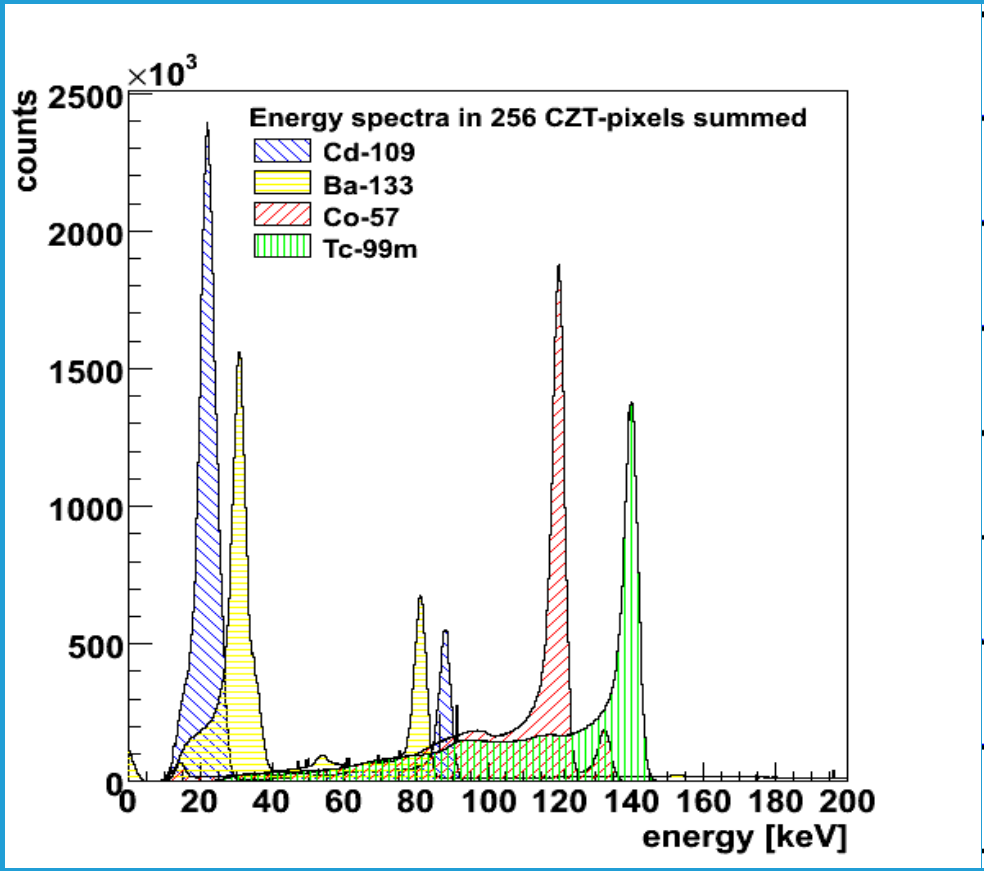


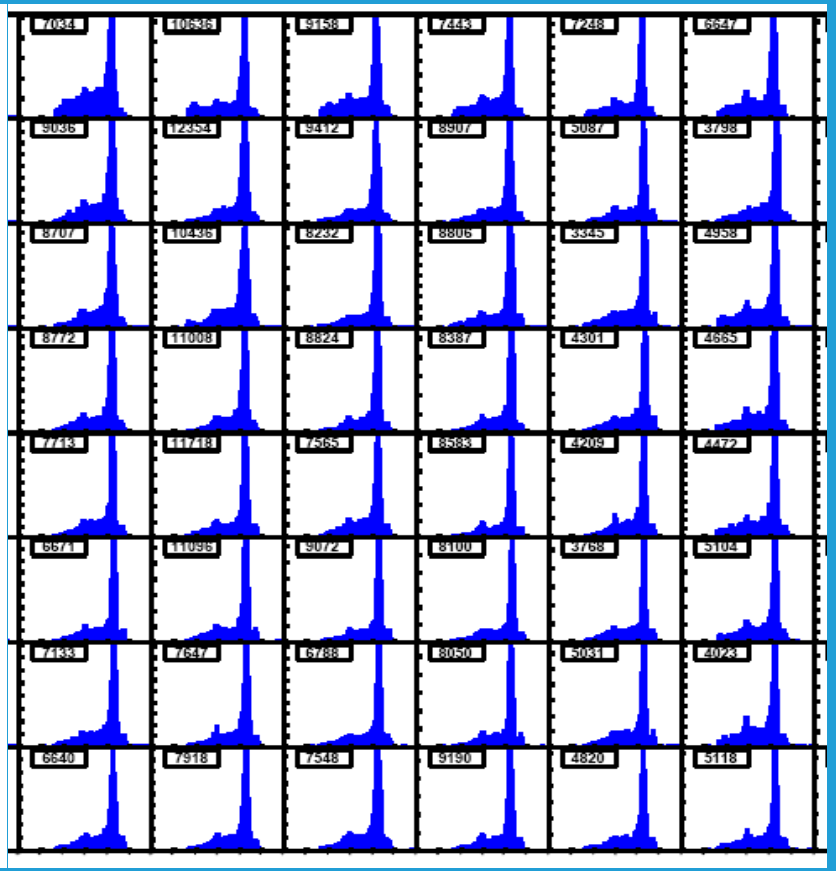




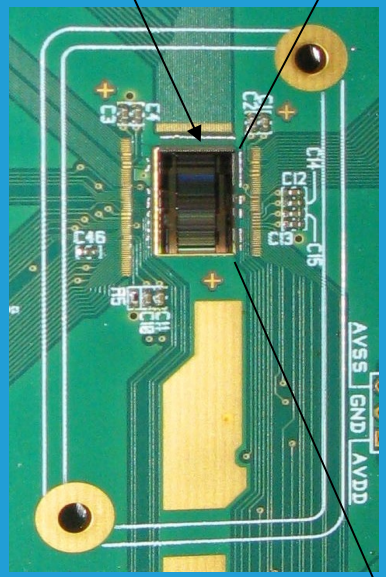
Modules with Integrated Readout

Energy spectroscopy in CZT Pixels

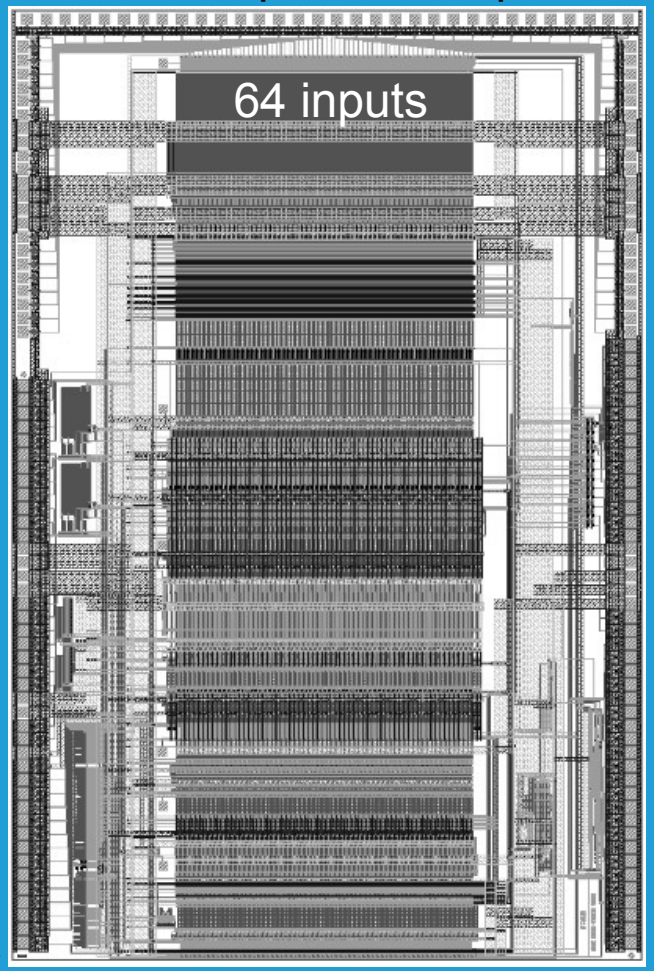


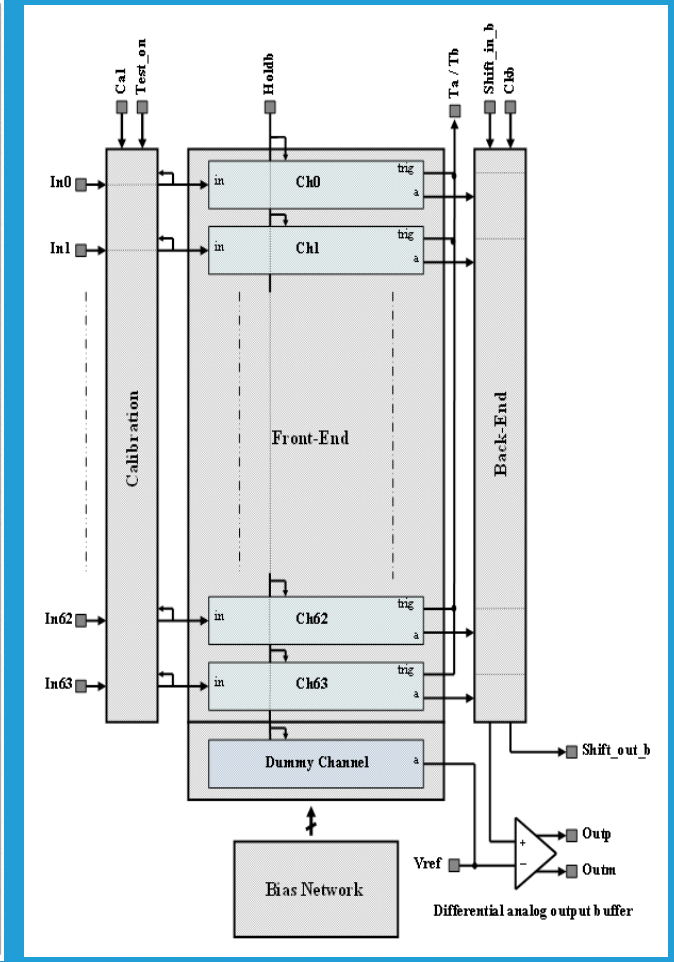


ASIC Floorplan, Padframe, Block Diagram



6500 µm x 9810 µm





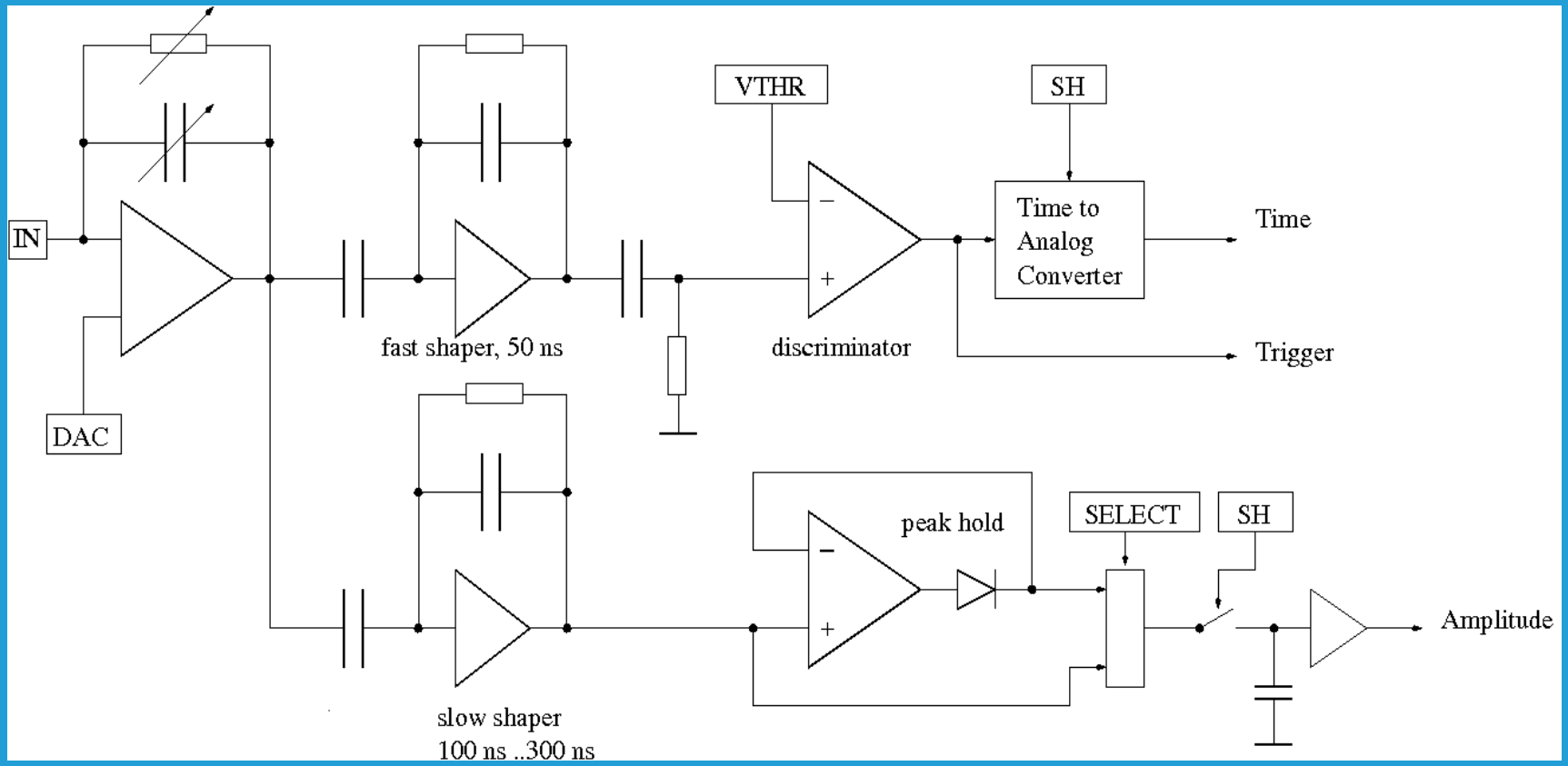
Preliminary Specifications

PRELIMINARY SPECIFICATIONS OF THE ASIC.

number of inputs	64
silicon die size	9810 μm $\times$ 6500 μm
input capacitive load	0..300 pF
input current load	0..10 μA
shaping time	programmable 50,100,150,300 ns
input dynamic range	programmable D_1=[-6,+7] pC, D_2=[-20,+55] pC optimized for positive charge
noise	$\approx$ 1 fC ENC at D_1, $\approx$ 8 fC ENC at D_2
supply voltages	-2.5 V, +2.5 V
power dissipation	$<$ 15 mW/channel

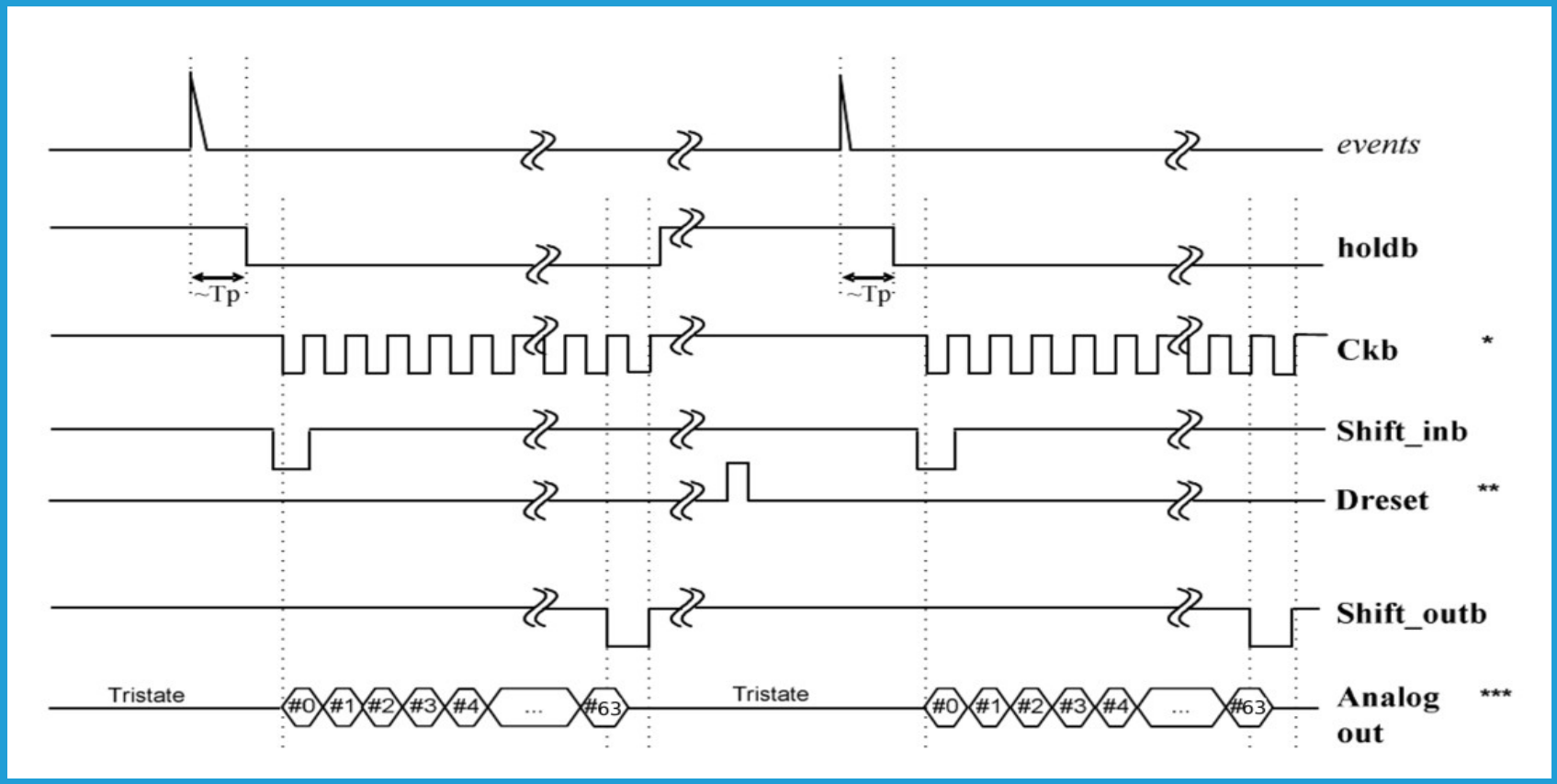
ASIC preliminary specifications, not yet optimized for a specific application.

Channel Architecture – 1 out of 64



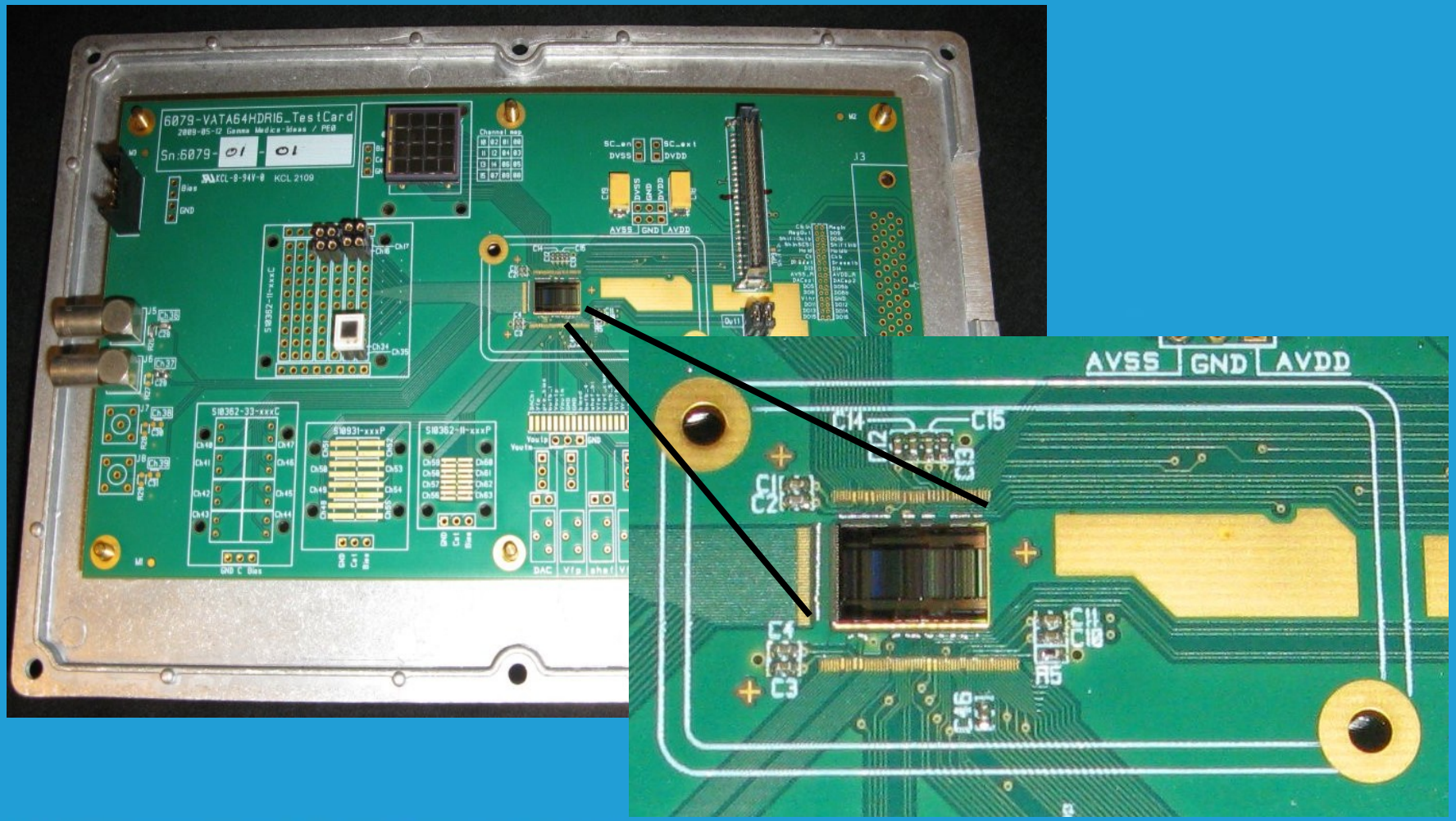
All features are programmable via DACs, or can be enabled/disabled

Readout Timing Diagram

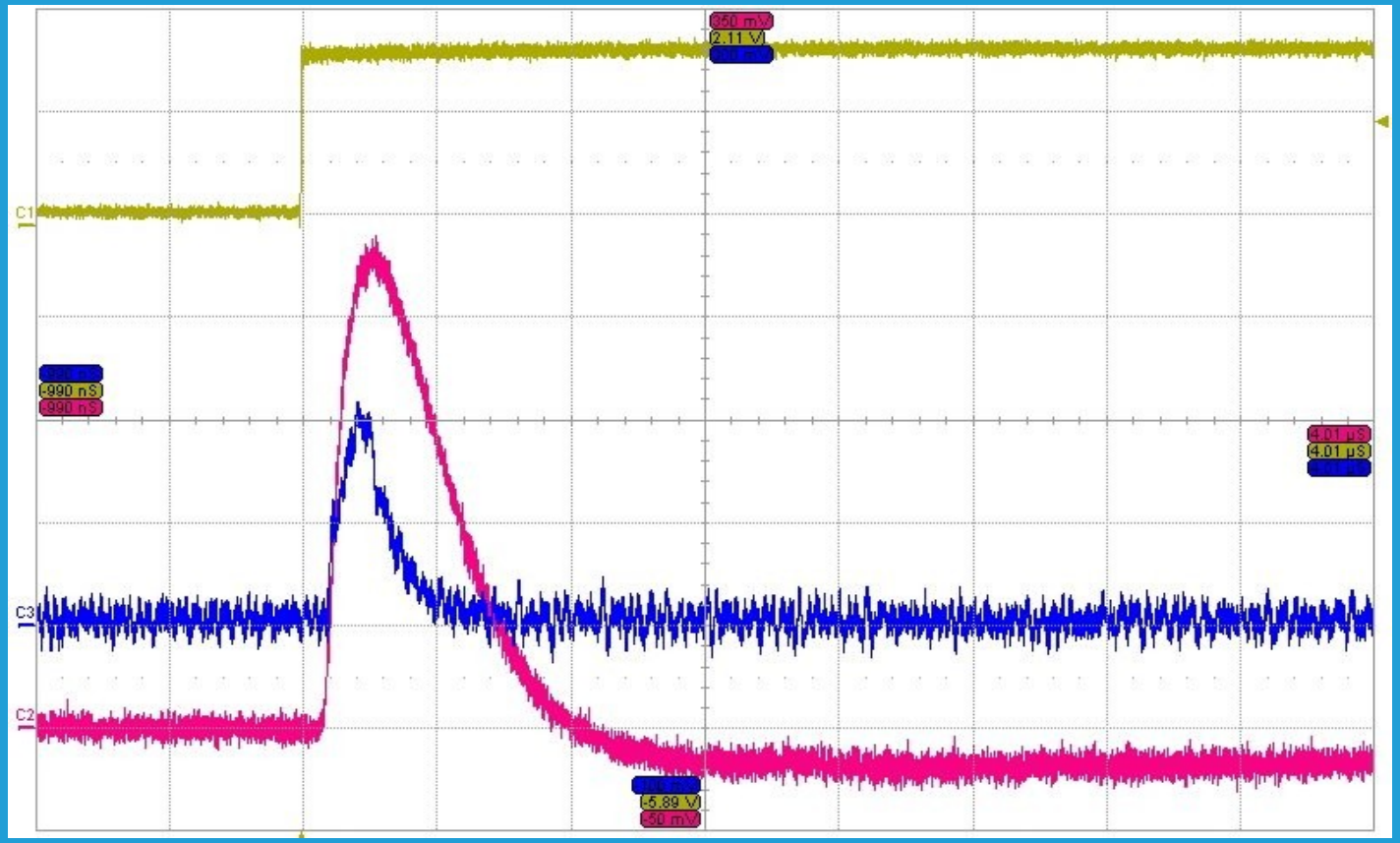


Sequential analog readout of the amplitude and TAC from all channels, SH can be generated internally, or applied externally

ASIC/MPPC/SiPM Assembly for the Experimental Tests



Test - Charge at Input



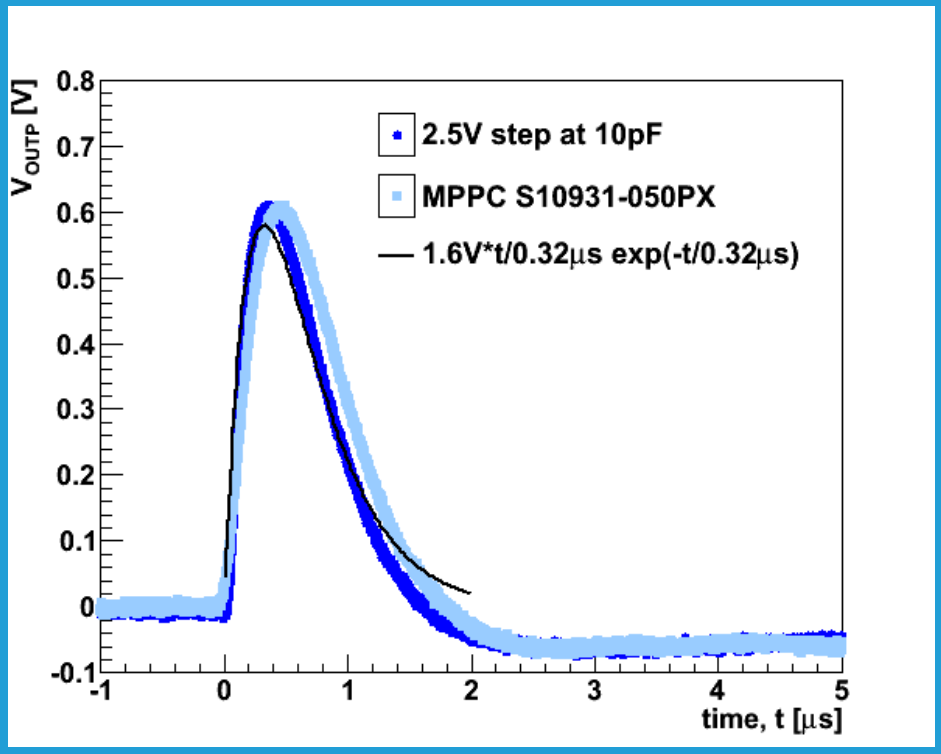
1 pC input charge

Trigger

200ns Semi-Gauss

GAMMAMEDICA

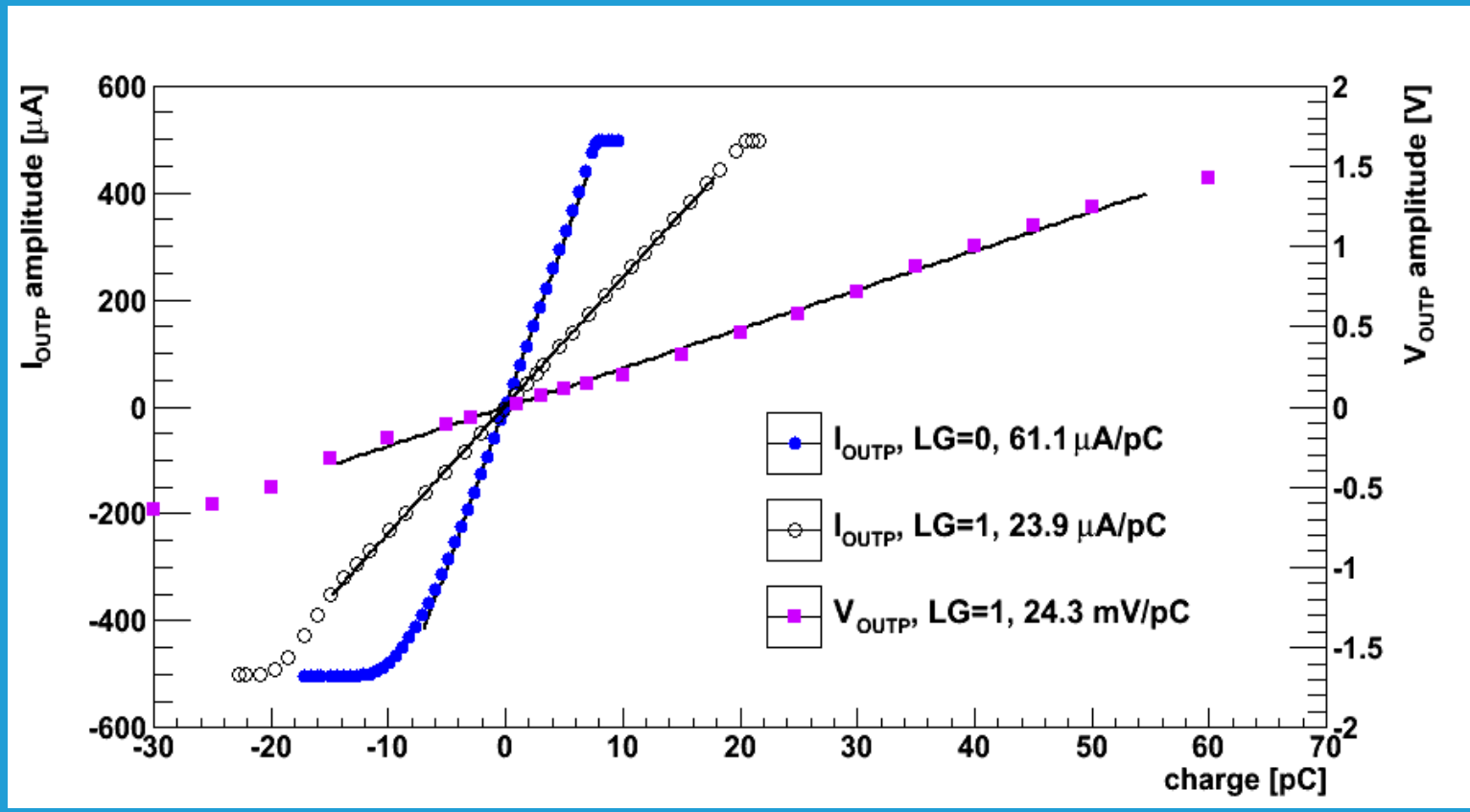
Test – Signal Shape under Capacitive Load



Signal shape fits a
- 1st order Gaussian shape, here about 200 ns peaking time.

MPPC capacitive load
- affects the pre-amp risetime but has negligible effect on the signal shape

Test - Input Charge Dynamic Range



Large dynamic input range, programmable range, up to +55 pC input charge

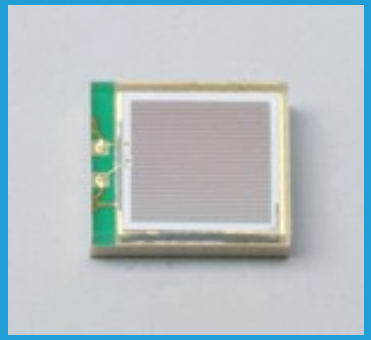
MPPC with LYSO

Specifications

Package	Plastic
Active Area	3 x 3 mm
Number of Elements	1
Pixel Size	50 x 50 um
Fill Factor	61.5 %
Spectral Response Range	320 to900 nm
Peak Wavelength	440 nm
Operating Voltage	70±10 V
Dark Count	6000 kcps
Terminal Capacitance	320 pF
Temperature Coefficience of Reverse Voltage	56 mV/deg. C
Gain	750000
Measurement Condition	Ta=25 °C
Note	

$$G = \frac{(V_{op} - V_{br})C_p}{e}$$

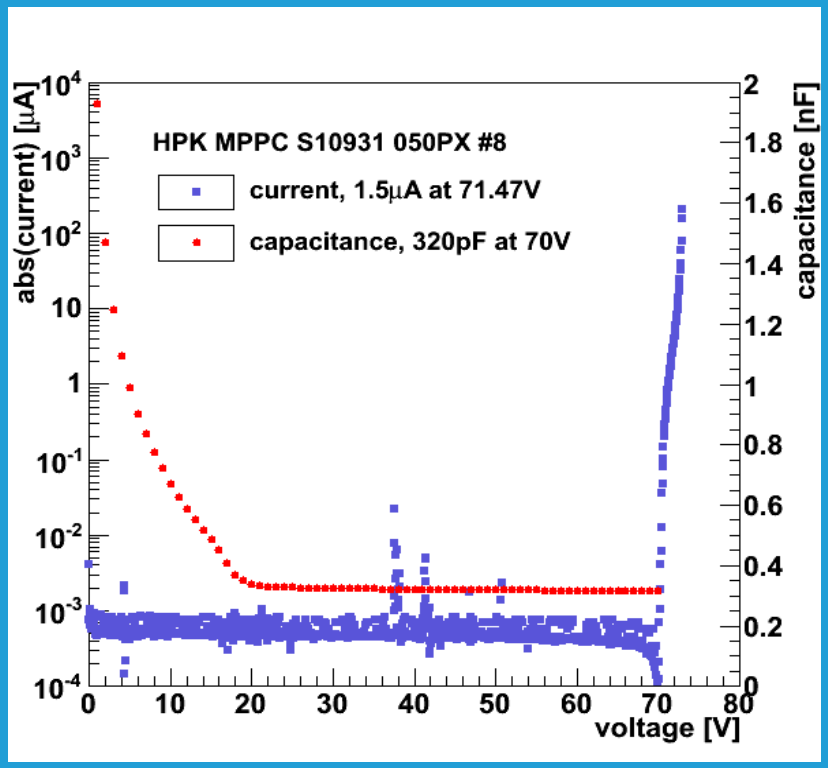
$$750000 = \frac{1.35V*320pF/3600pixels}{1.602e\text{-}19C}$$

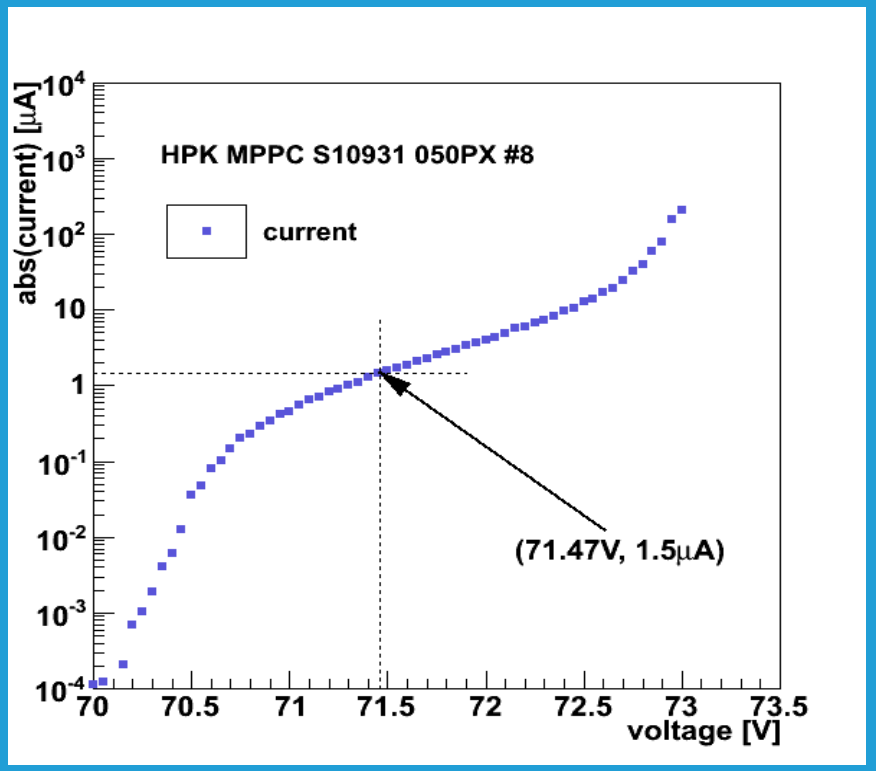


Assembly of LYSO and MPPC, thanks to A.Rudge, P.Weilhammer

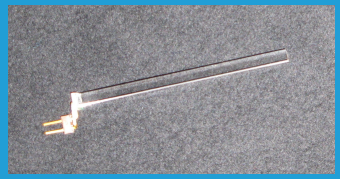
http://jp.hamamatsu.com/products/sensor-ssd/4010/S10931-050P

MPPC – Current and Capacitance

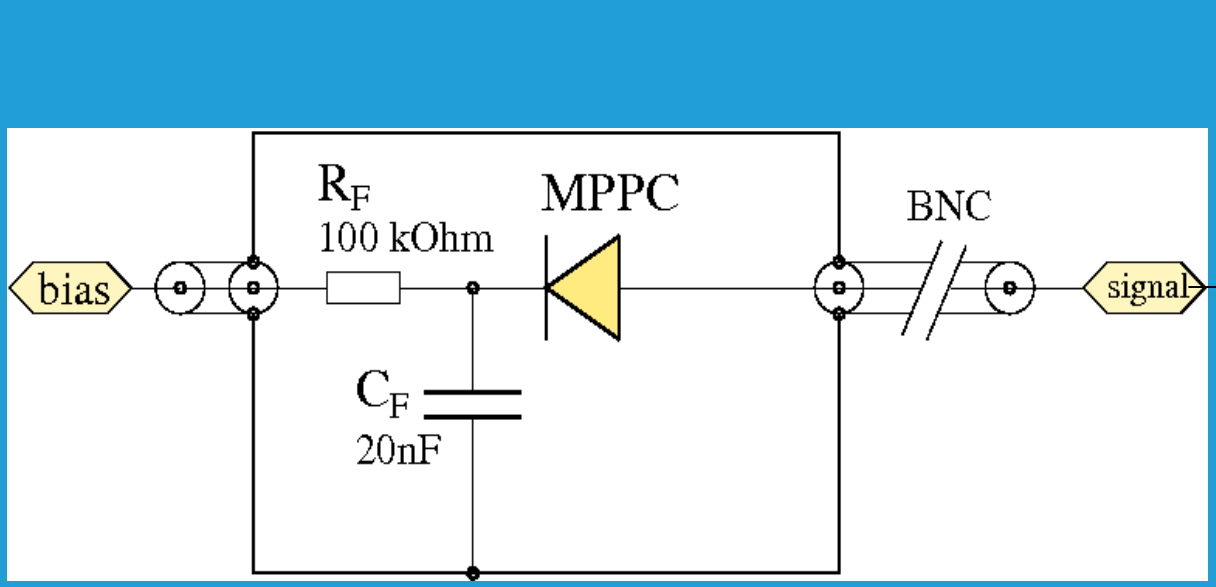


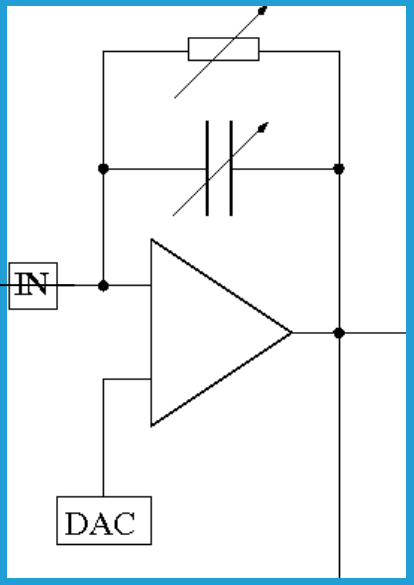


Measurements agree with Hamamatsu datasheet.



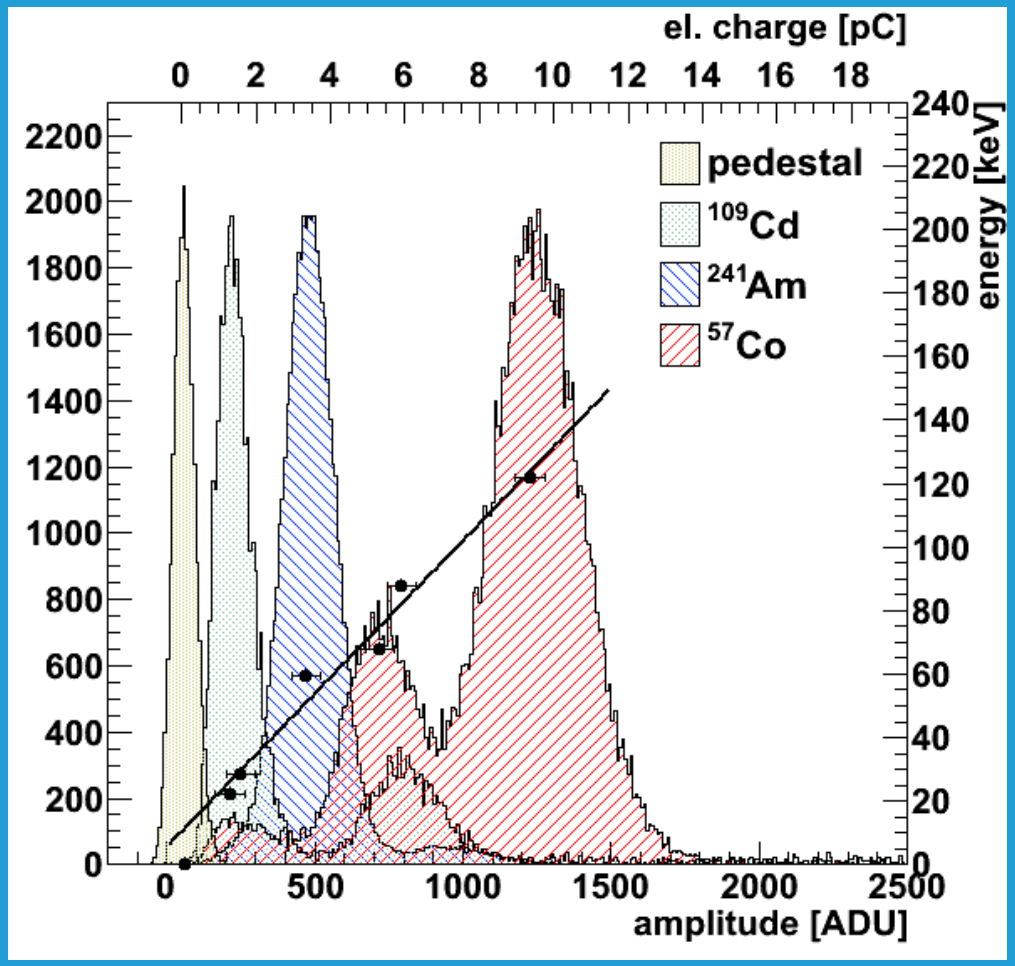
MPPC – Bias Voltage and Direct Coupling to Readout



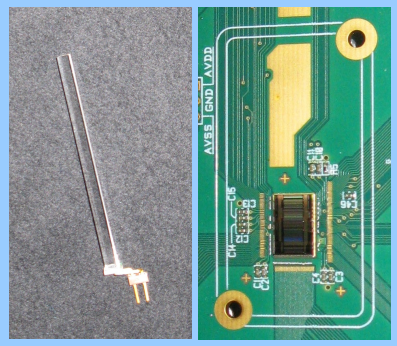


MPPC directly coupled to readout input
Input stage provides: variable gain and input voltage adjustment by DAC

MPPC/LYSO/ASIC - Energy Spectra from Radiation



Experimental setup

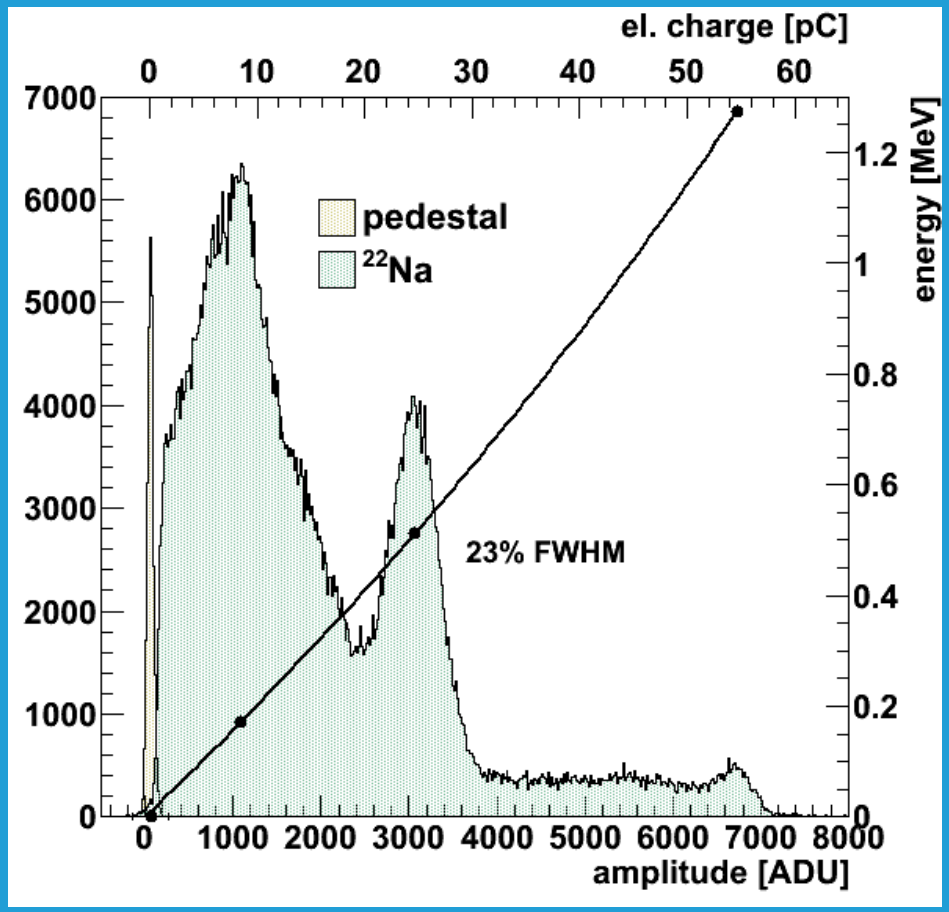


MPPC/LYSO with ASIC
Energy spectroscopy with Cd, Am, Co sources

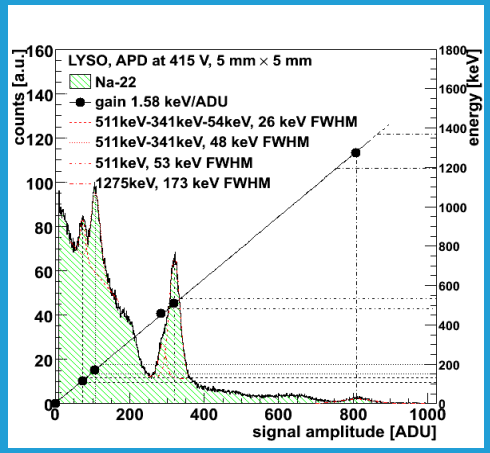
resolves photopeaks – FWHM not optimized

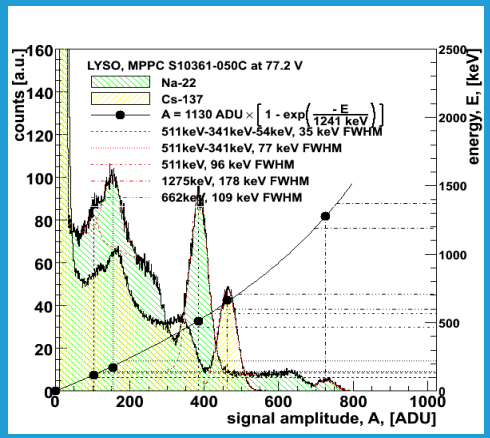
relatively low energy threshold

MPPC/LYSO/ASIC - Energy Spectra from Radiation



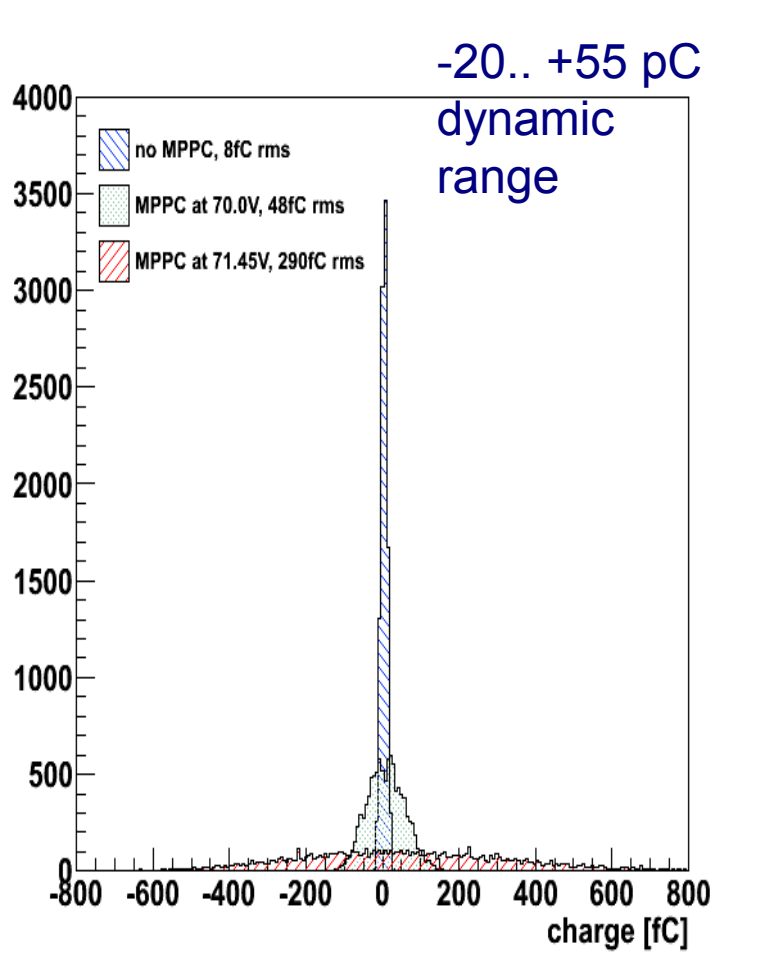
LYSO
6k to 7k ph.
at 511 keV

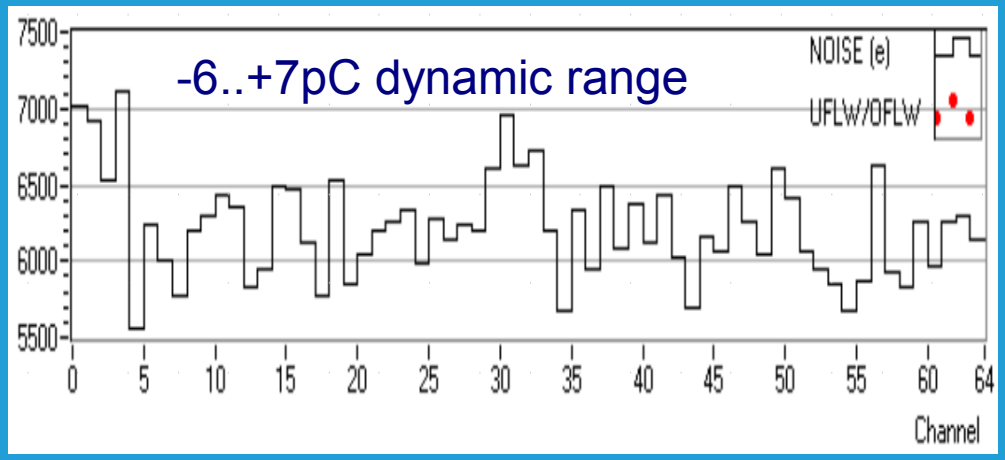




MPPC/LYSO resolves peaks from Na22, 23 % FWHM at 511 keV
observation is consistent with Szawlowski et al. Proc. NSS 2007.

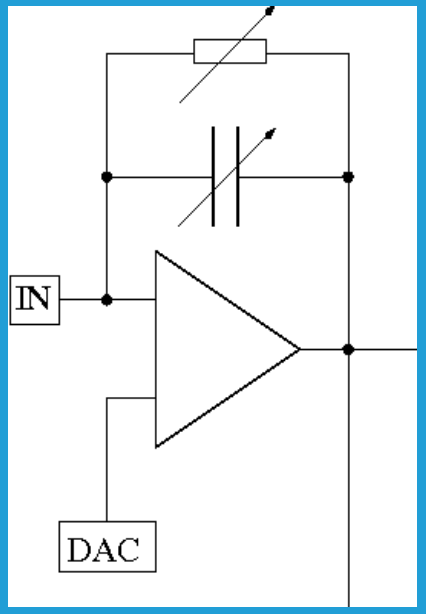
Equivalent Noise Charge

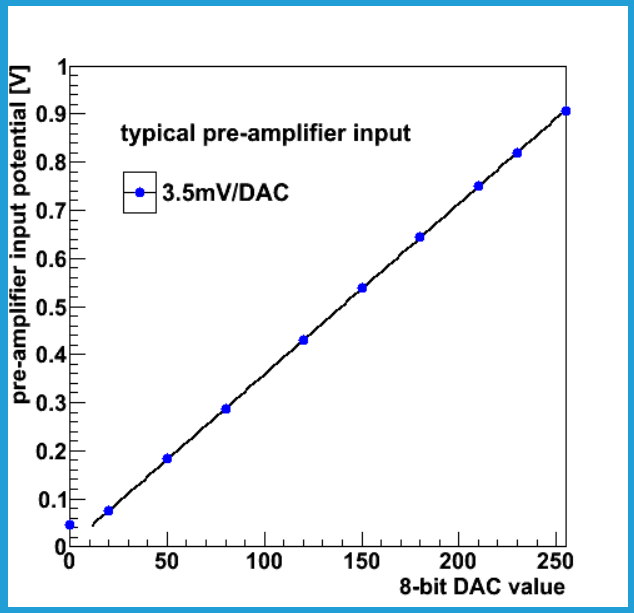


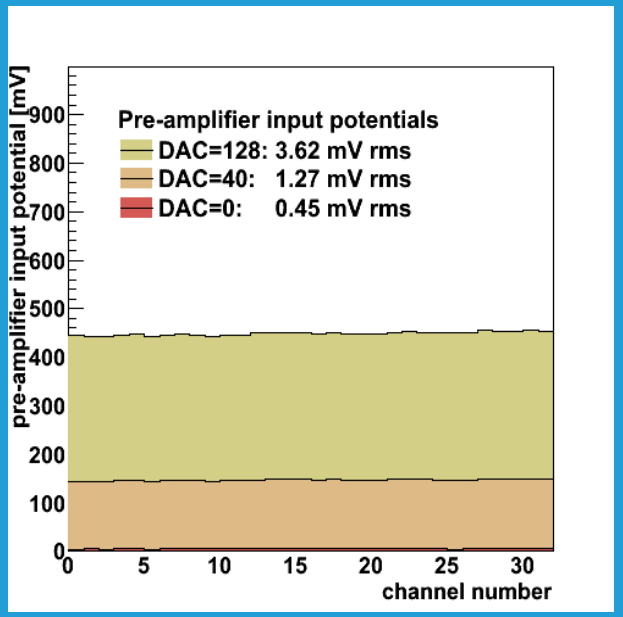


$$D_{dB} = 20\log_{10}(75000/8)$$
$$= 20\log_{10}(13000/1)$$
$$= 80\text{dB}$$

Measurement of the ASIC Input Potential



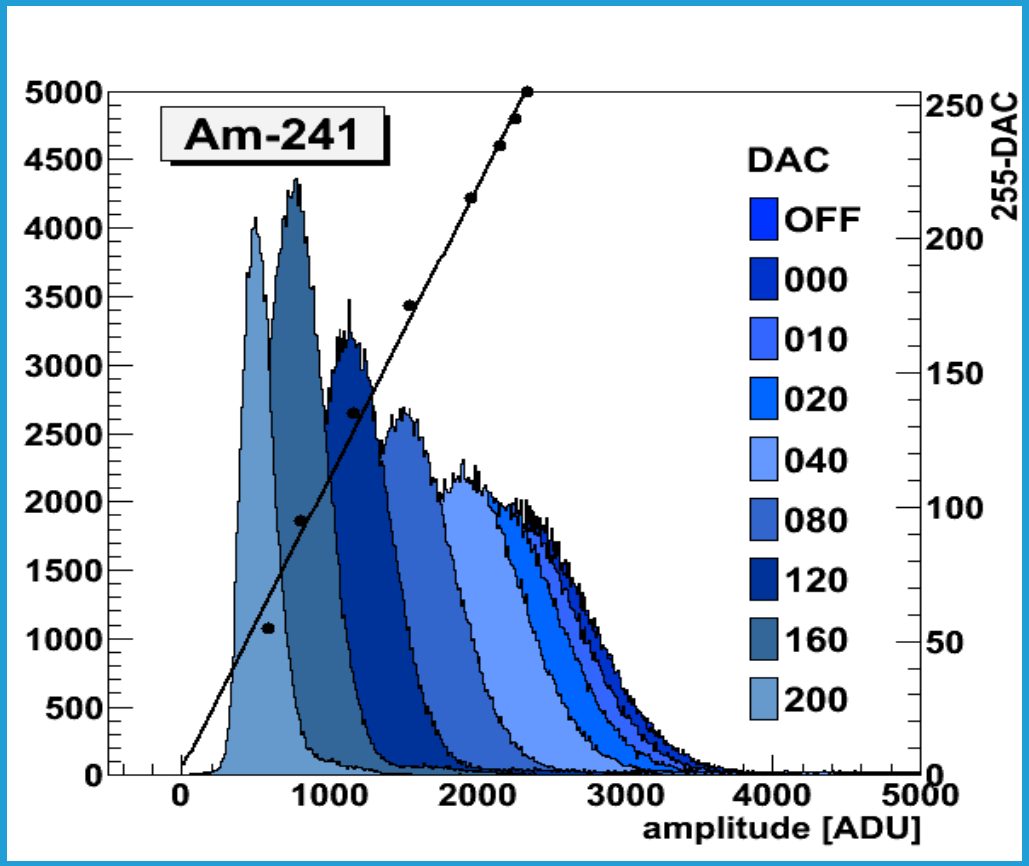




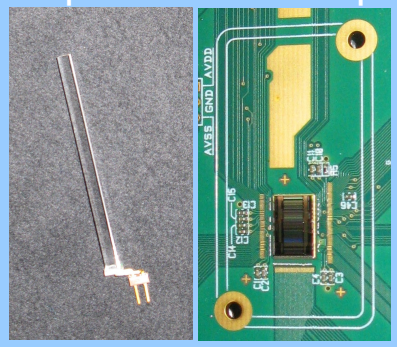
We measure the voltage at IN versus the DAC value.
We observe a linear relation between IN voltage and DAC value, 3.5mV/DAC.
Change by 3.5mV corresponds to gain change of 0.26% relative to G=750000.

The DAC value can be set for each input individually and can be used to fine tune the MPPC bias voltage above the breakdown.

Measurement of the Photopeak versus Input Potential



Experimental setup



$$G = \frac{(V_{\mathrm{op}} - V_{\mathrm{br}})C_{\mathrm{p}}}{e}$$

The DAC value can be used to fine tune the MPPC bias voltage above the breakdown – thereby adjust the combined gain of the assembly MPPC/ASIC.

Summary

We have developed an ASIC for the readout of up to 64 SiPMs/MPPCs.

The preliminary results agree with original specifications and satisfy the initial requirements.

Future improvements are possible, most desirable are:

- reduce power dissipation by factor 5 to 10
- reduce the ASIC size
- optimize ASIC for high input capacitance
- CFD – done in other ASICs
- ADC – e.g. Wilkinson ADC in every channel, done in other ASICs
- optimize for a specific application

Acknowledgments

Pier Simone Marrocchesi, Univ. of Siena and INFN - Pisa (Italy)

Alan Rudge and Peter Weilhammer, CERN

Thank you