

Review of ASIC developments for SiPM signal readout

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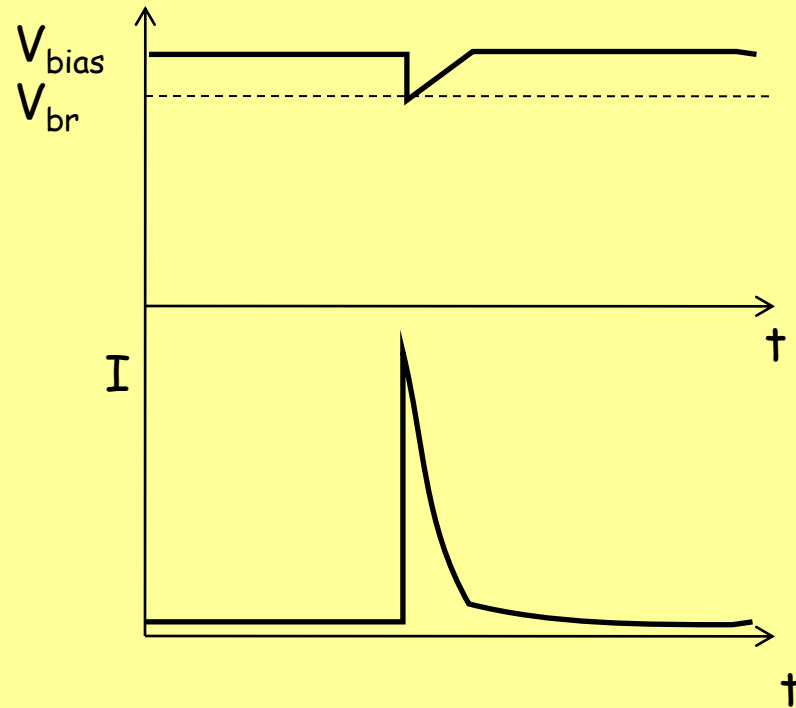
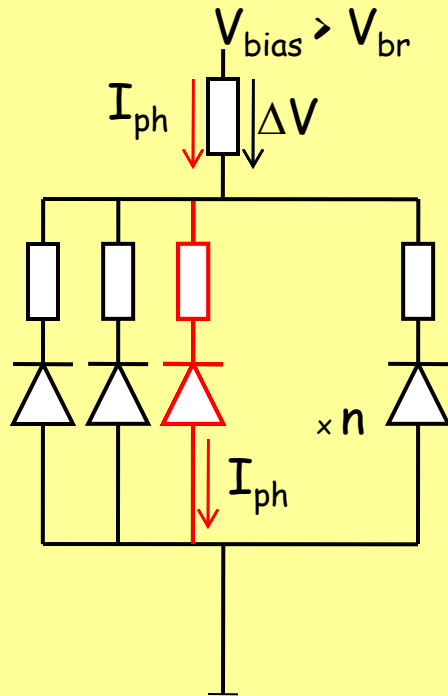


ASIC developments for SiPM

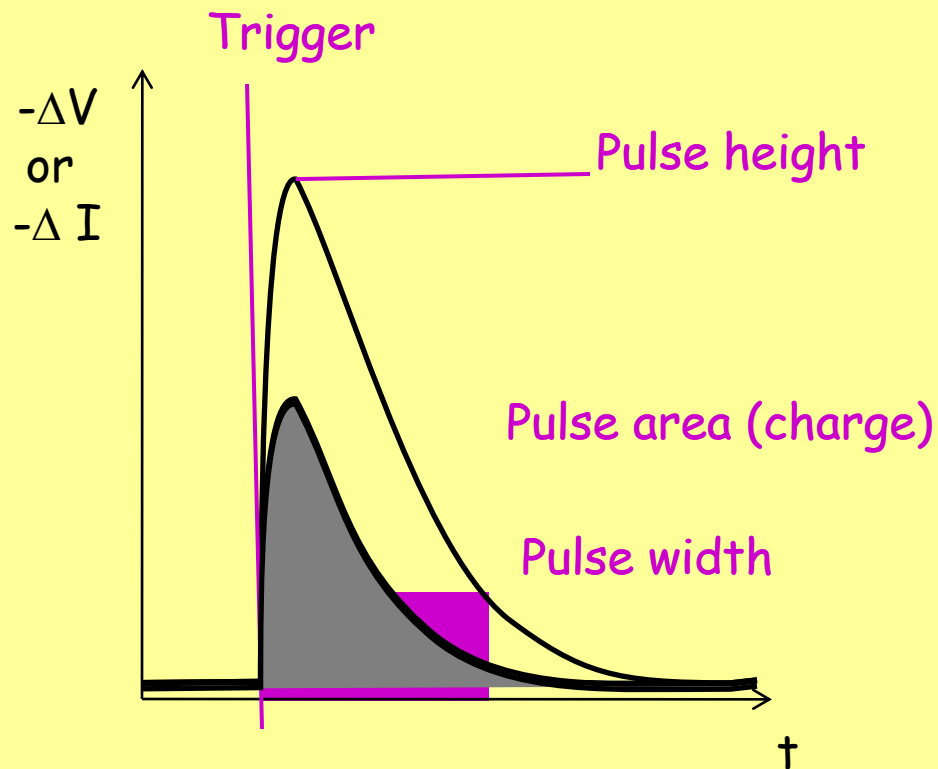
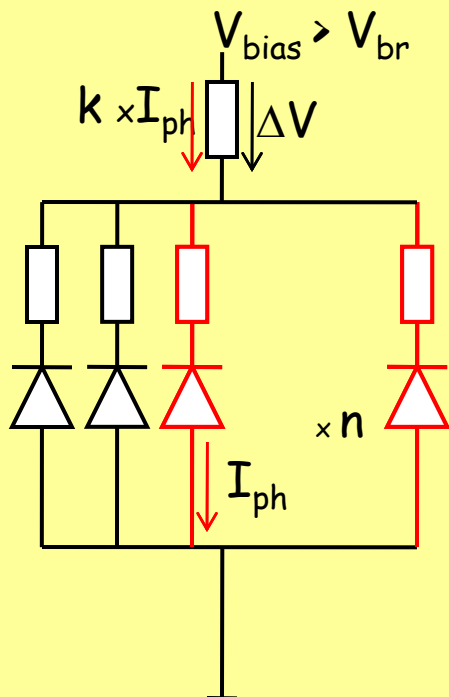
ASIC dedicated for SiPM:

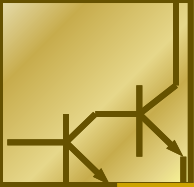
1. FLC_SiPM - Orsay
2. MAROC - Orsay
3. SPIROC - Orsay
4. NINO - CERN
5. PETA - Heidelberg
6. BASIC - Bari/Pisa
7. SPIDER - Siena/Pisa
8. RAPSODI - Krakow

ASICs for the SiPM



ASICs for the SiPM





ASIC developments for SiPM

FLC-SiPM

IN2P3/ LAL, Orsay

(C. de La Taille, G. Martin-Chassard, L. Raux)



FLC-SiPM

The FLC-SiPM was developed for the ILC Analog Hadronic Calorimeter

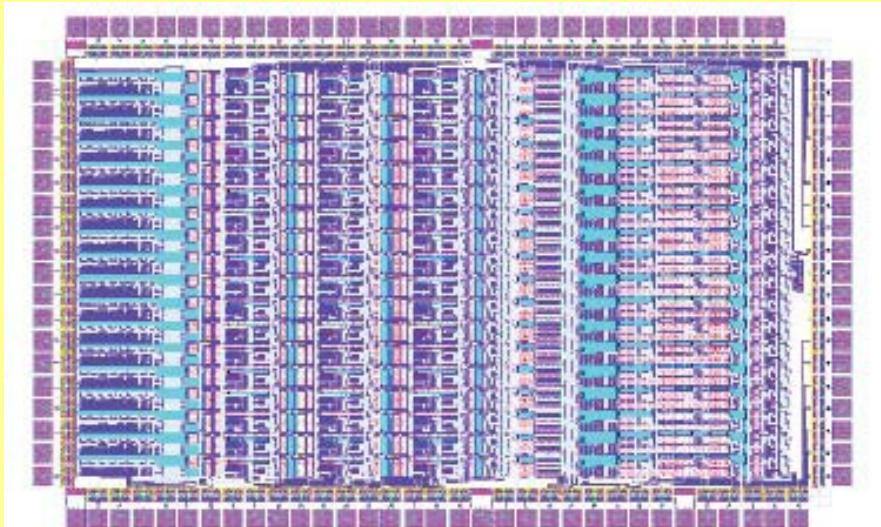
1. C. de La Taille, G. Martin-Chassard, L. Raux *FLC-SIPM: Front-End Chip for SIPM Readout for ILC Analog HCAL* - 2005 International Linear Collider Workshop - Stanford, U.S.A.

FLC-SiPM

The FLC-SiPM is an 18 channel charge input front-end circuit made in $0,8 \mu\text{m}$ CMOS technology (2004).

It provides a shaped signal proportional to the input charge. Each channel is made of a low noise variable-gain charge preamplifier followed by a CRRC^2 shaper with a variable shaping time. Each of the shaper output comes into a track and hold system giving a single multiplexed output.

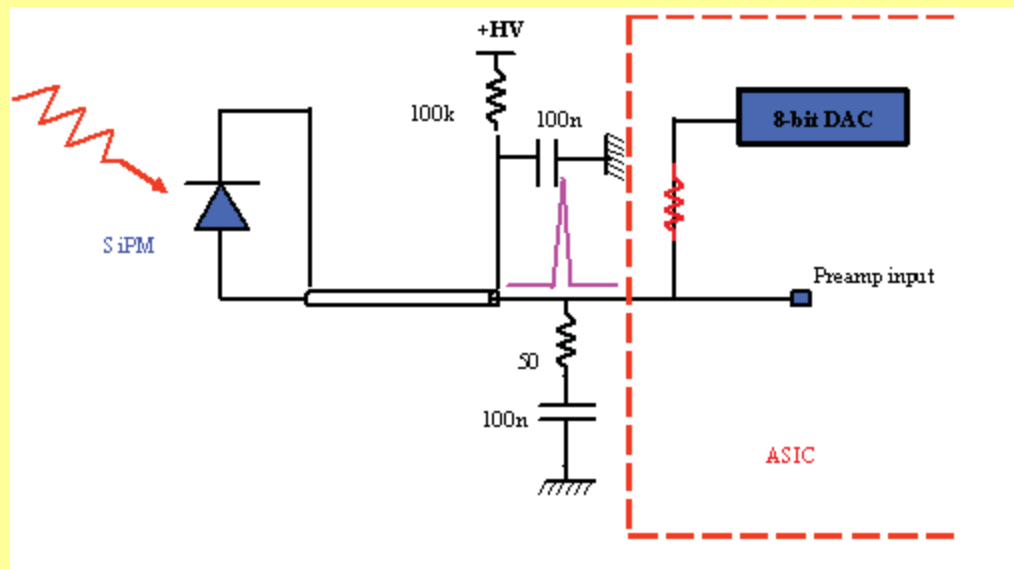
The total power consumption of the chip is around 200mW with 5V supply voltage.



FLC-SiPM

The SiPM gain strongly depended of the bias voltage, so it has to be adjusted for each diode.

An 8-bit DAC was added in parallel to each input of preamplifier.
The DAC provide up to 5 V bias voltage moderation.

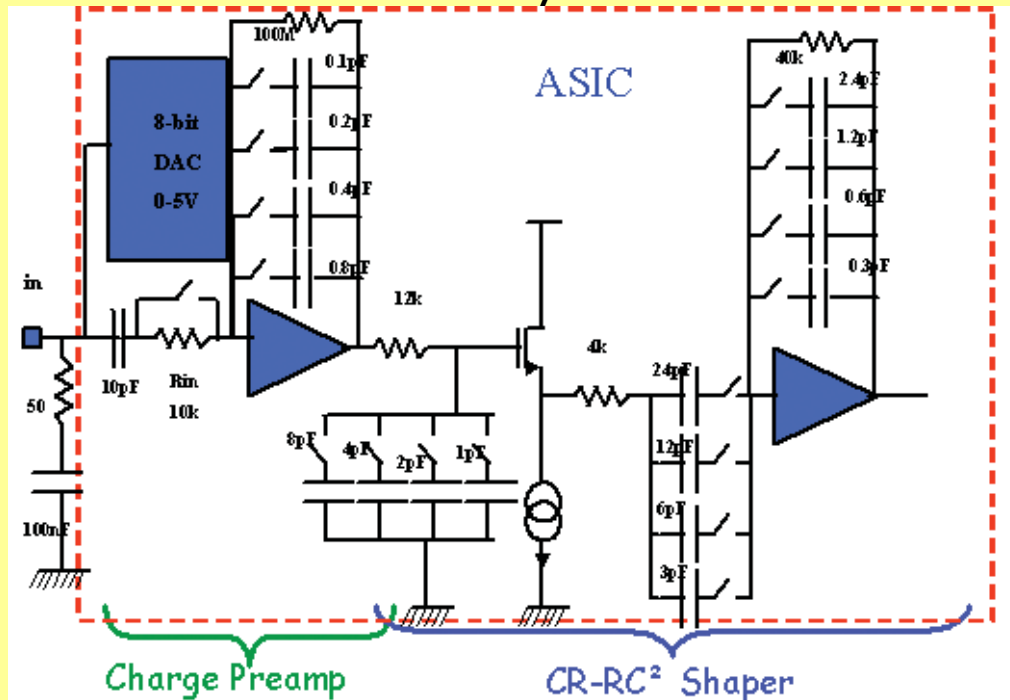


FLC-SiPM

The coupling capacitance at the input is decoupling of high voltage and makes first derivative.

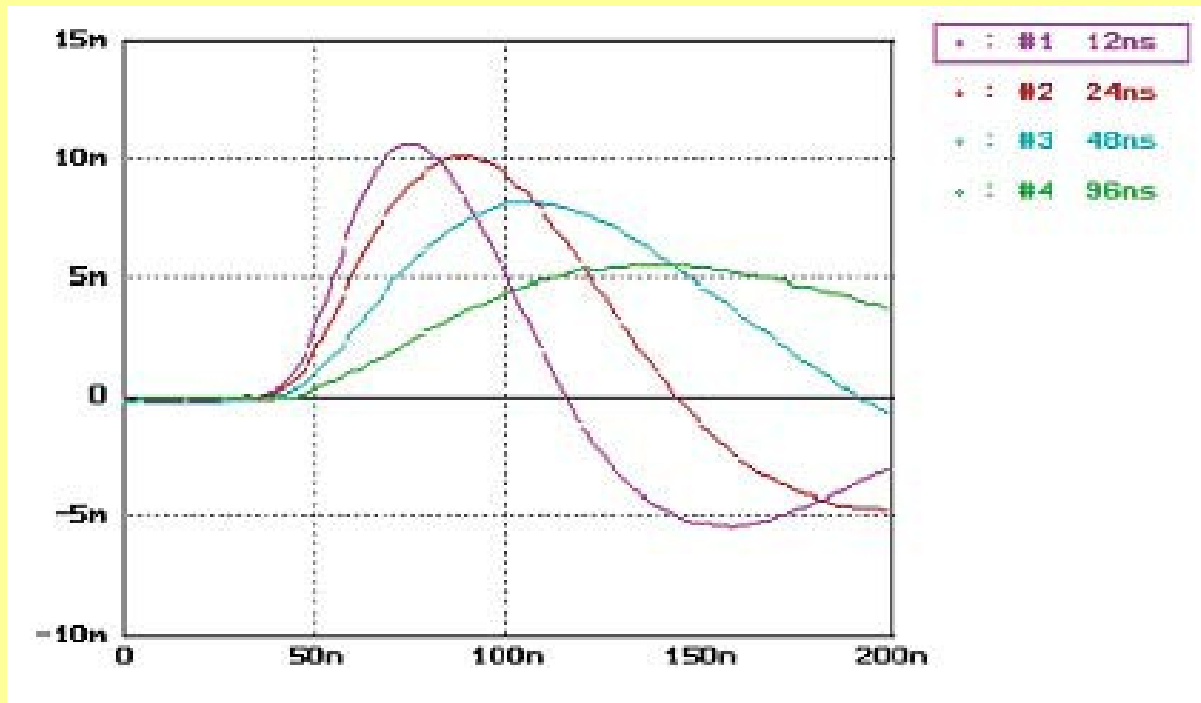
The gain of the preamplifier can be externally chosen by 4-bits switch adding the feedback capacitors (0,7 to 10 V/pC)

The CRRC² shaper allows to moderate time constant (12 to 180 ns) by similar way



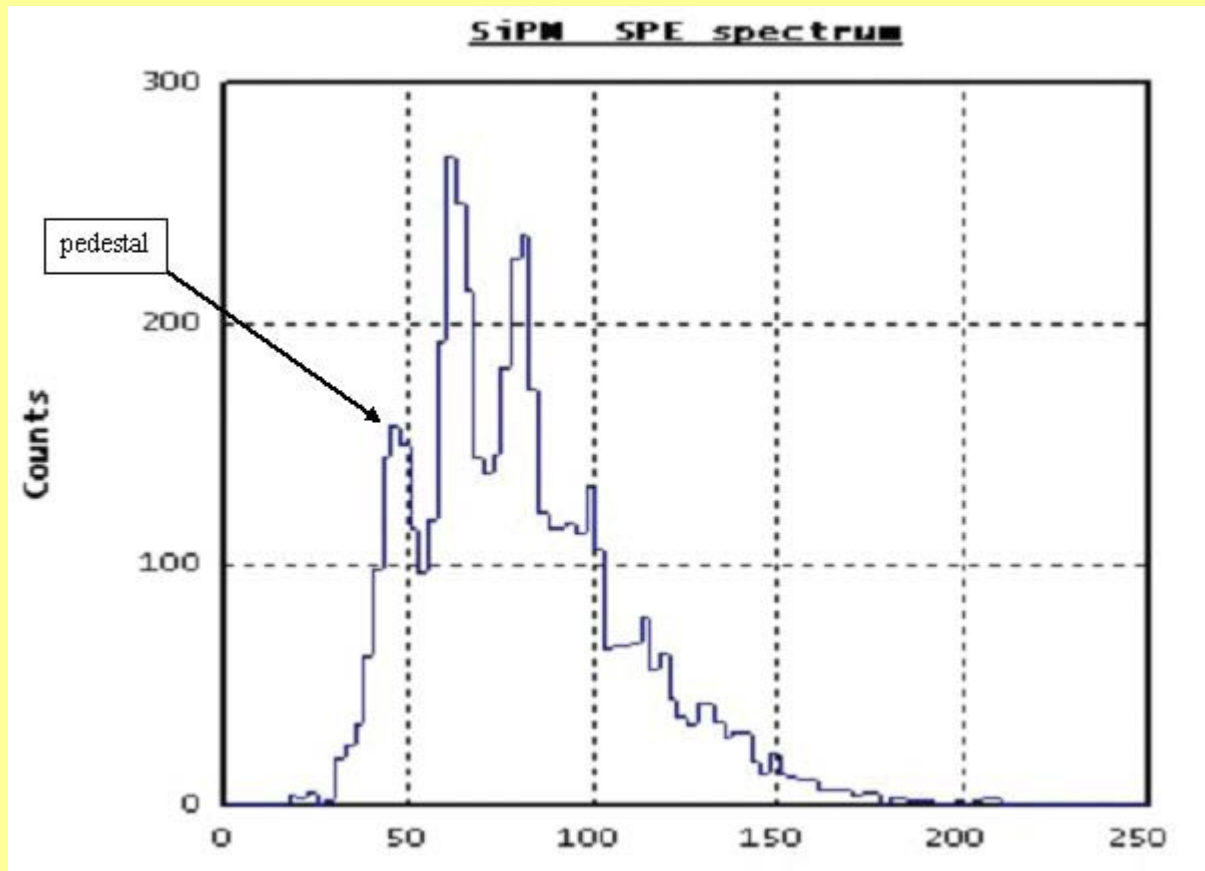
FLC-SiPM

Response of the circuit for single photoelectron with various shaping time.



FLC-SiPM

The spectrum of the output signals with SiPM connected to the input of the chip





ASIC developments for SiPM

MAROC

IN2P3/ LAL, Orsay

(P. Barrillon, S. Blin, M. Bouchel, T. Caceres, C. de La Taille,
G. Martin, P. Puzo, N. Seguin-Moreau)



MAROC

MAROC (**M**ulti-**A**node **R**ead**O**ut **C**hip) was developed for the ATLAS luminometer and it was an evolution of the OPERA_ROC ASIC designed and installed on the OPERA Experiment.

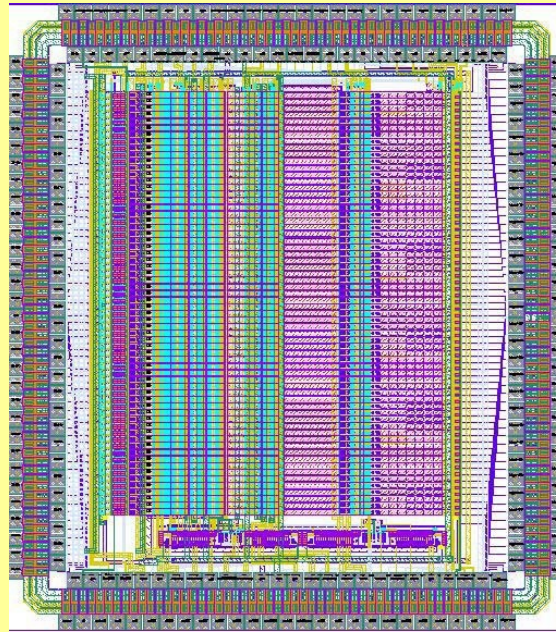
The MAROC 2 has been employed for the readout of the SiPM matrices

1. G. Llosa, N. Belcari, M.G. Bisogni, G. Collazuol, S. Marcatili, M. Boscardin, M. Melchiorri, A. Tarolli, C. Piemonte, N. Zorzi, P. Barrillon, S. Bondil-Blin, V. Chaumat, C. de La Taille, N. Dinu, V. Puill, J-F. Vagnucci, A. DelGuerra - First results in the application of silicon photomultiplier matrices to small animal PET - NIMA 610 (2009), p. 196
2. P. Barrillon, S. Blin, M. Bouchel, T. Caceres, C. de La Taille, member IEEE, G. Martin, P. Puzo, N. Seguin-Moreau - MAROC: Multi-Anode ReadOut Chip for MaPMTs - 2006 IEEE Nuclear Science Symposium Conference Record, p. 809
3. S. Blin, P. Barrillon and C. de La Taille - MAROC, a generic photomultiplier readout chip - TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,

MAROC

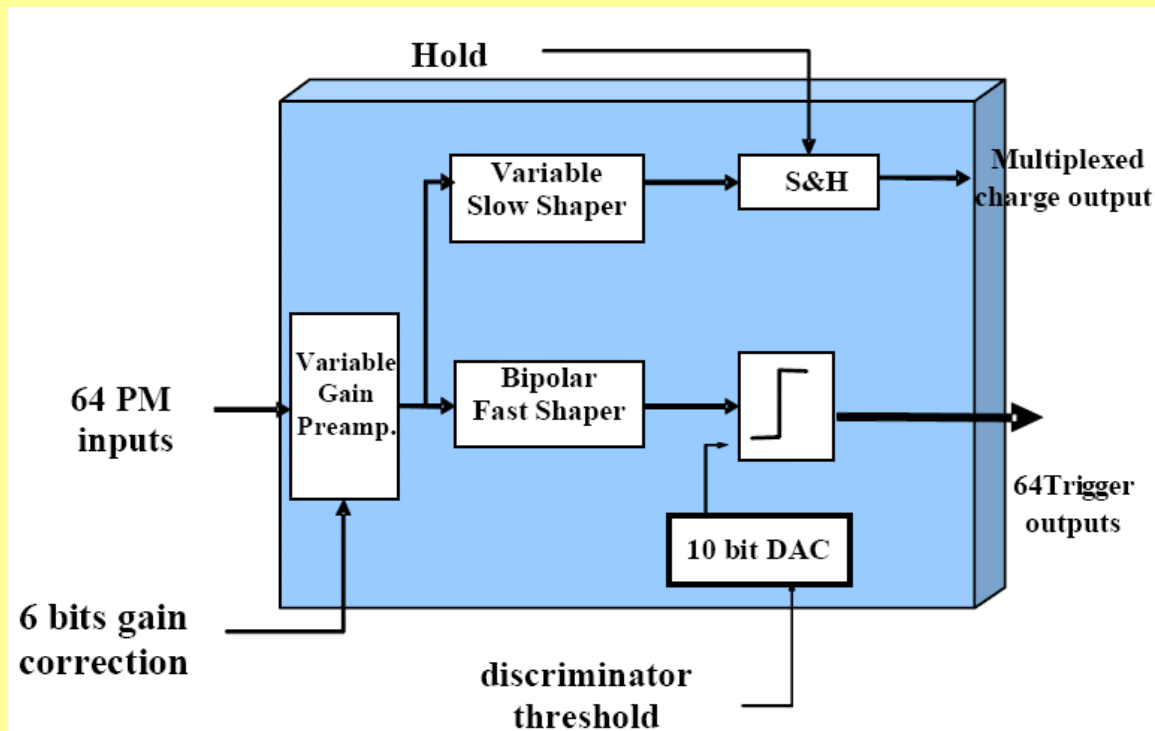
The MAROC is a 64 channel front-end circuit made in $0,35 \mu\text{m}$ Si-Ge AMS technology (2005).

Each channel is made of 6-bit variable-gain preamplifier which has low noise and low input impedance to minimize crosstalk. Then the amplified current feeds a slow shaper combined with two sample and hold capacitors. The digital charge output is provided by Wilkinson ADC. The chip operates with 5V supply voltage.



MAROC

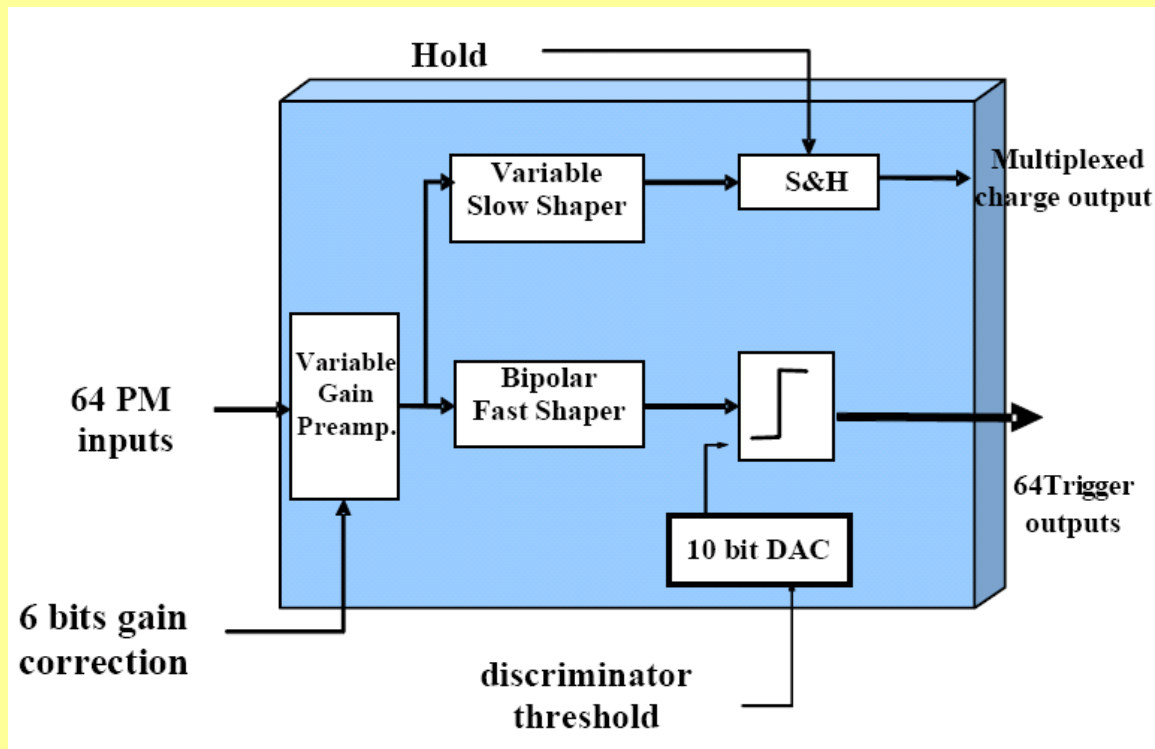
MAROC has 64 inputs, 64 trigger outputs and multiplexed charge output. Each channel is made of a variable gain preamplifier with low input tunable impedance (50-100 Ω). The variable gain allows to compensate the SiPM gain dispersion.



MAROC

The amplified current feeds two path:

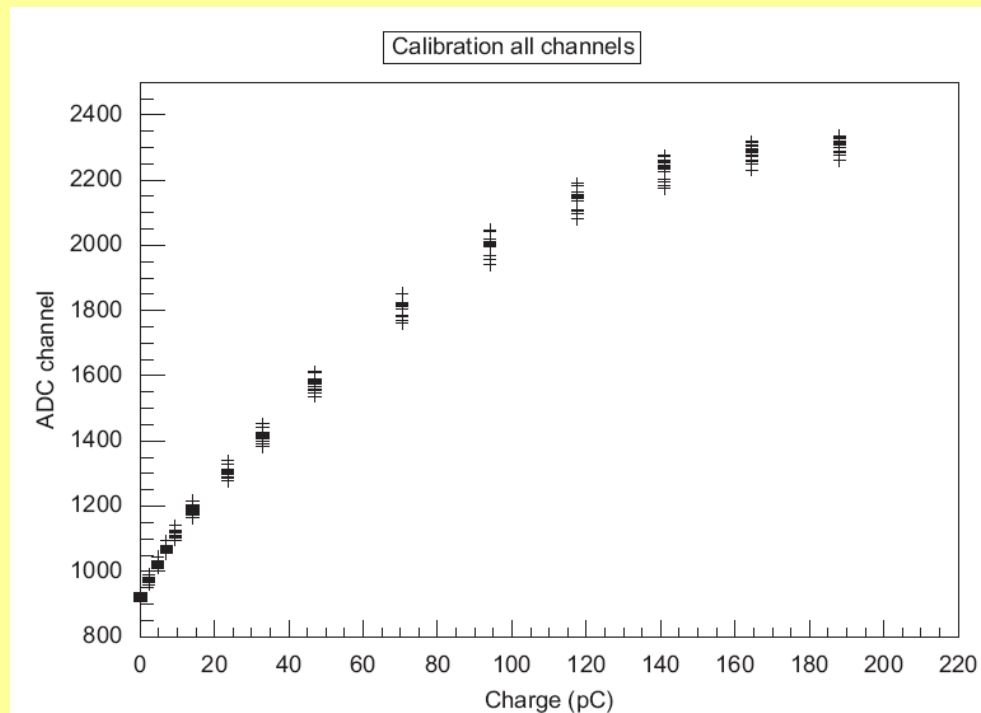
1. Slow shaper path with CRRC² Shaper and Sample and Hold block storing the charge for multiplexed readout
2. Fast shaper path with CRRC shaper followed by discriminator with 10-bit DAQ produced a trigger output.



MAROC

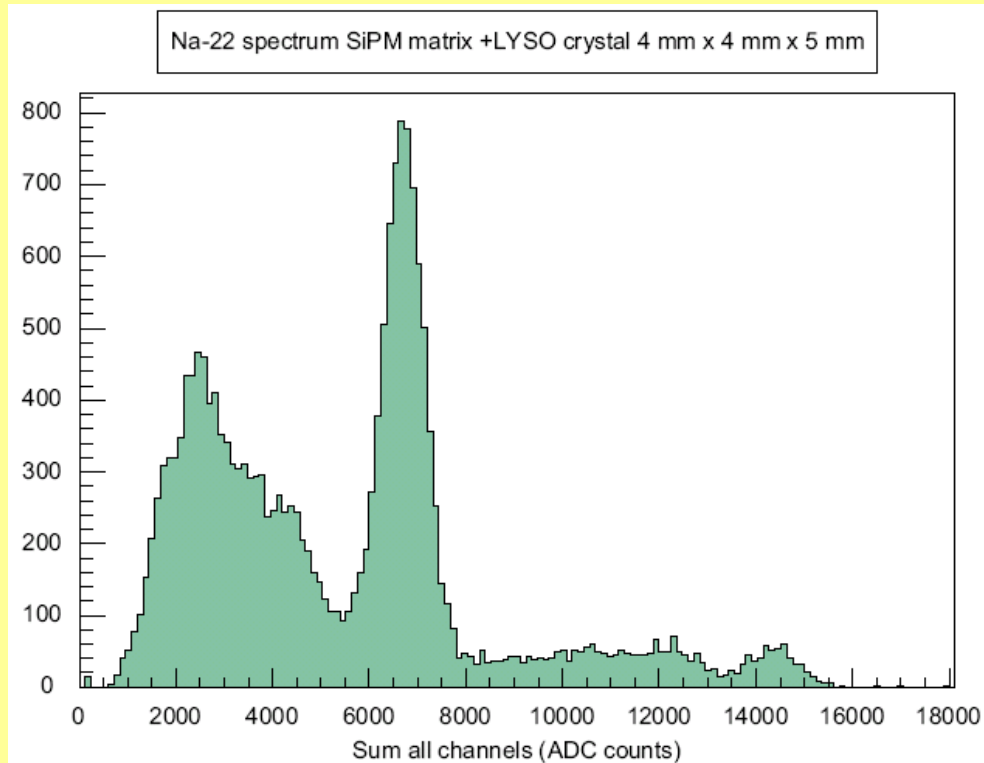
The MAROC2 version of the chip was used with SiPM as an input. It was attached to 16 pixel SiPM matrix (FBK). Such module would be used in small animal PET.

The ASIC calibration at minimum gain shows linear response up to 10 pC. Above 80 pC response clearly deviates from linearity.



MAROC

There was also performed test with LYSO crystal (4 x 4 x 5 mm) coupled to the SiPM matrix for measurement of ^{22}Na spectrum. The total energy of the event histogram shows photopeaks of 511 and 1275 keV.





ASIC developments for SiPM

SPIROC

IN2P3/LAL, Orsay

(M. Bouchel, F. Dulucq, J. Fleury, C. de La Taille, G. Martin-Chassard, L. Raux)



SPIROC

SPIROC (**SiPM Integrated ReadOut Chip**) was developed for the future ILC Hadronic Calorimeter

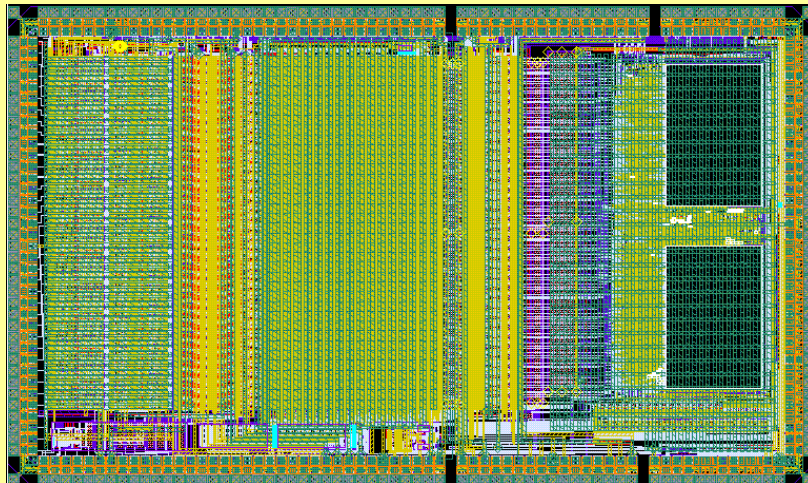
1. Callier S, Dulucq F, Fabbri R de La Taille C , Lutz B, Martin-Chassard G , Raux L, Shen W. - Silicon Photomultiplier integrated readout chip (SPIROC) for the ILC: measurements and possible further development - 2009 IEEE Nuclear Science Symposium Conference Record , p.42
2. Bouchel M, Dulucq F, Fleury J, de La Taille C, Martin-Chassard G, Raux L - SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out - 2007 IEEE NUCLEAR SCIENCE SYMPOSIUM - CONFERENCE RECORD, p. 1857
3. F.Duluca, M.Bouchel, C.De La Taille, J.Fleury, G.Martin-Chassard, L.Raux - Digital part of SiPM Integrated Read-Out Chip ASIC for ILC hadronic calorimeter - (2007)
4. M.Bouchel, F. Dulucq, J.Fleury, C. de La Taille, G. Martin-Chassard, L. Raux - SPIROC measurement: Silicon photomultiplier readout chip for the ILC - (2009)

SPIROC

The SPIROC is a 36 channel front-end circuit made in $0,35 \mu\text{m}$ Si-Ge AMS technology dedicated to SiPM readout (2007).

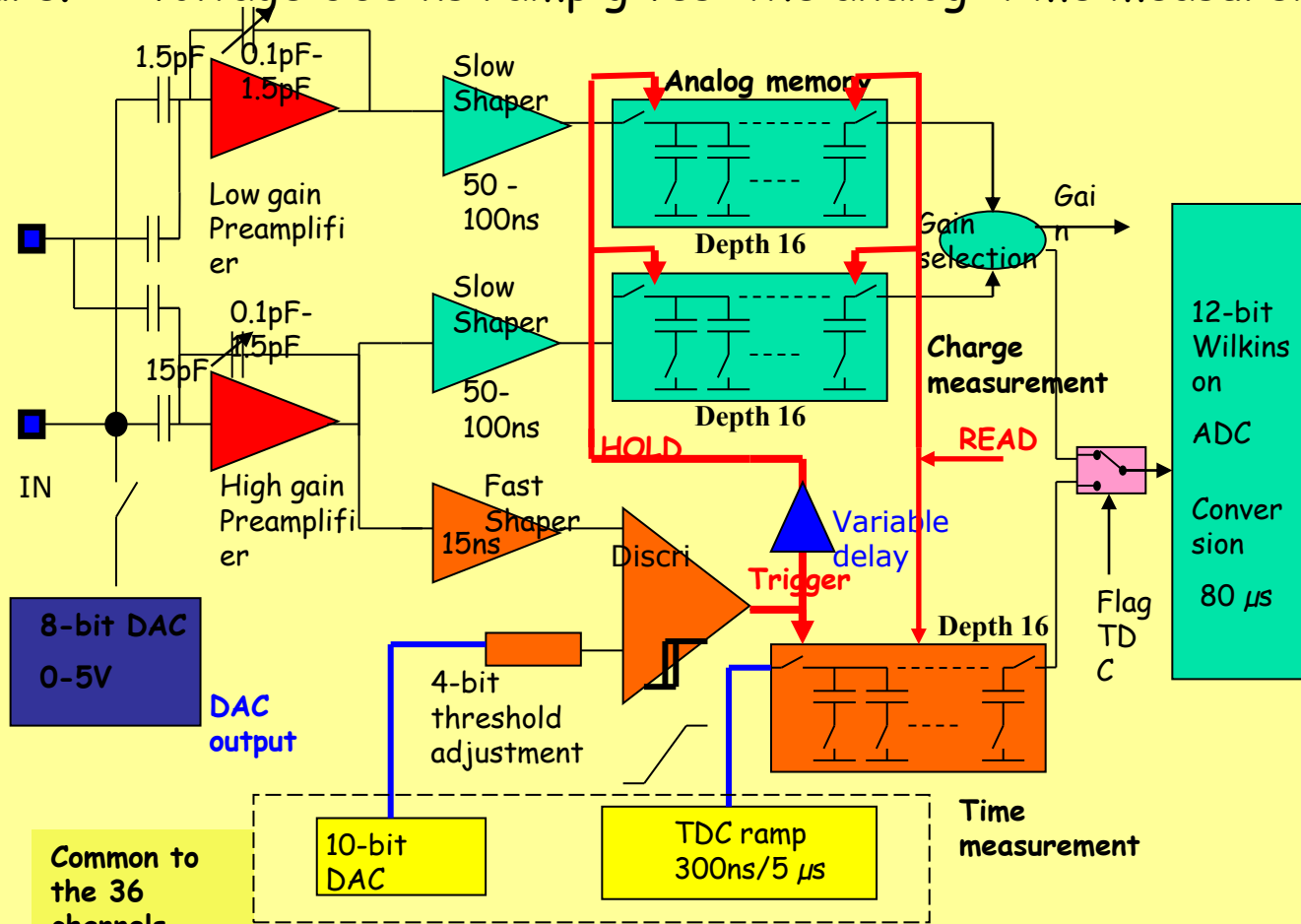
Each channel has 8-bit DAC for individual SiPM gain adjustment (0,5 - 4,5 V) attached to the input. Input signal is sent parallel to two preamplifiers (low and high gain). It allows to measure input signal with the range 1 to 2000 pe. Preamplifiers are followed by CRRC² shapers (25 to 175 ns) and two analog voltage memories.

In parallel, trigger outputs are obtained via fast shaper followed by a discriminator.



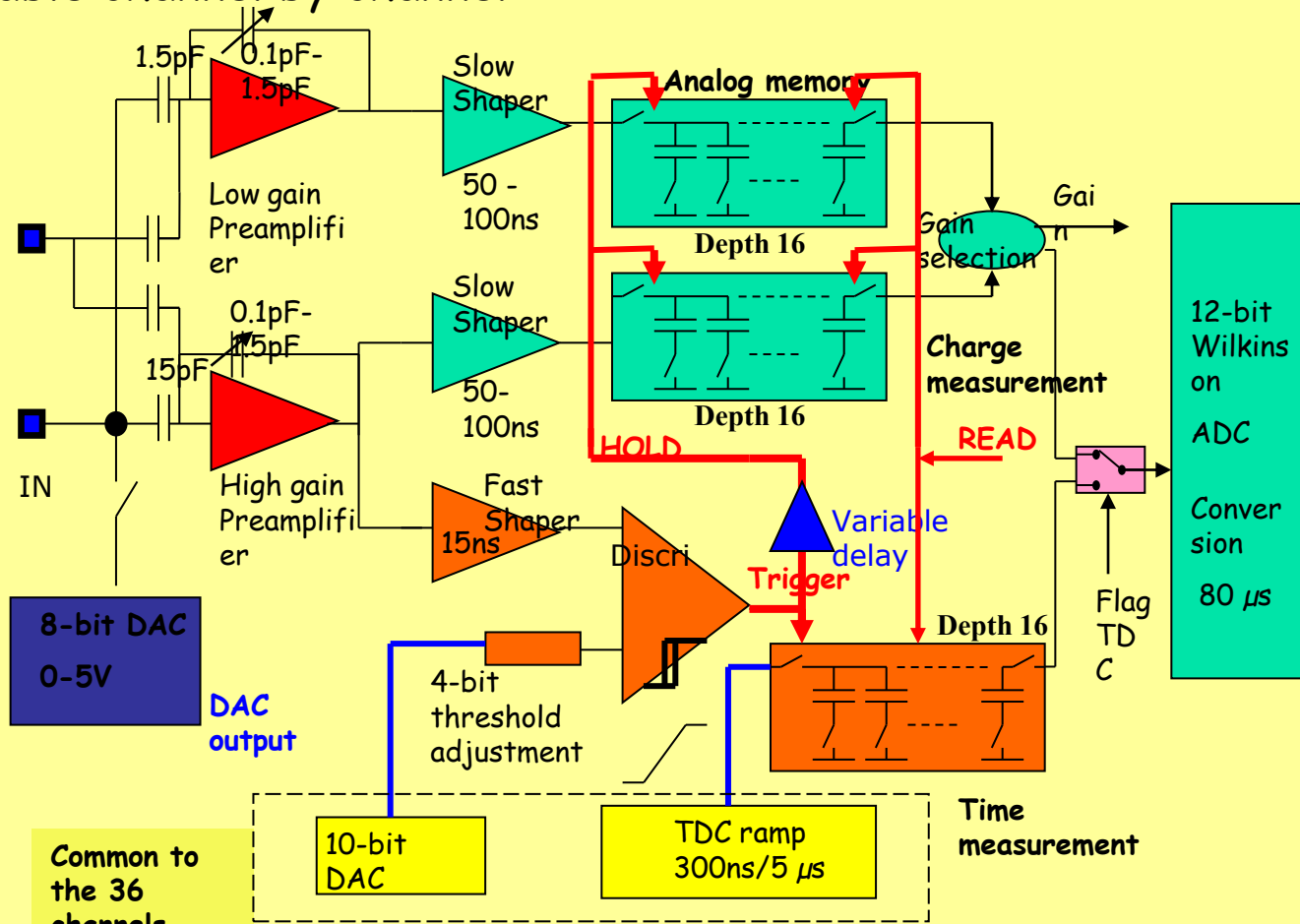
SPIROC

The SPIROC functionality has been designed to match the ILC beam structure. A voltage 300 ns ramp gives the analog time measurement.

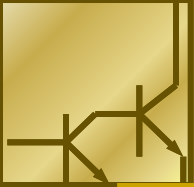


SPIROC

The trigger discriminator threshold is given by common 10-bit DAC with 4 bit tunable channel by channel



SPIROC

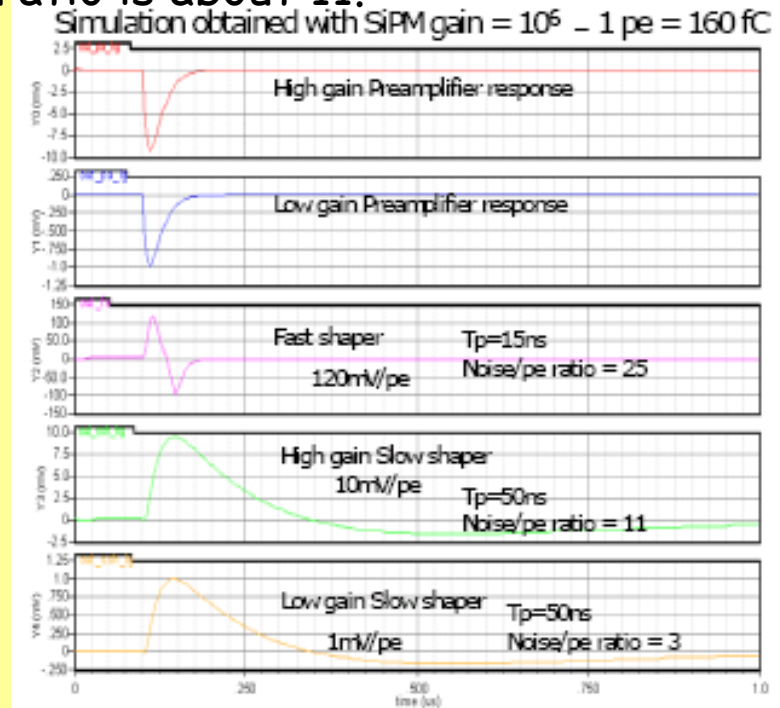


The simulation shows for time measurement a gain of 120 mV/pe with a peaking time of 15 ns. The photoelectron to noise ratio is about 24.

For the energy measurement, the simulation gives a gain of 10 mV/pe with a peaking time of about 100 ns on "high gain channel" (high gain preamplifier + slow shaper). The photoelectron to noise ratio is about 11.

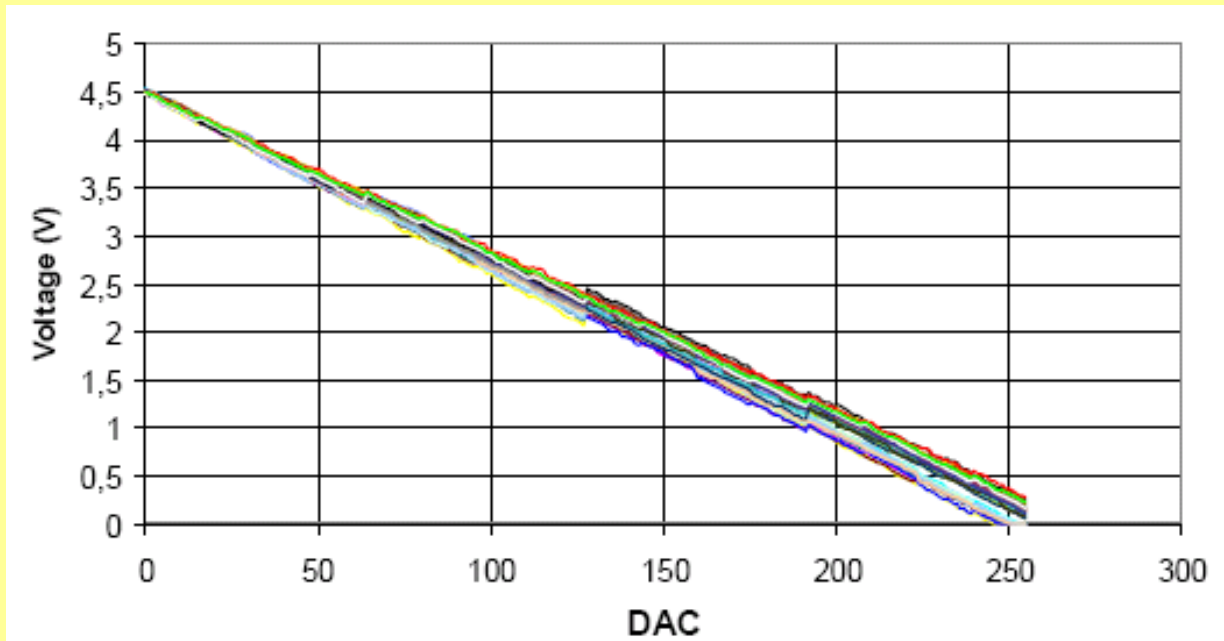
On the "low gain channel", the photoelectron to noise ratio is about 3.

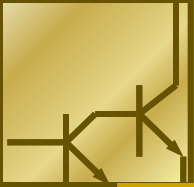
All results meet the ILC requirements.



SPIROC

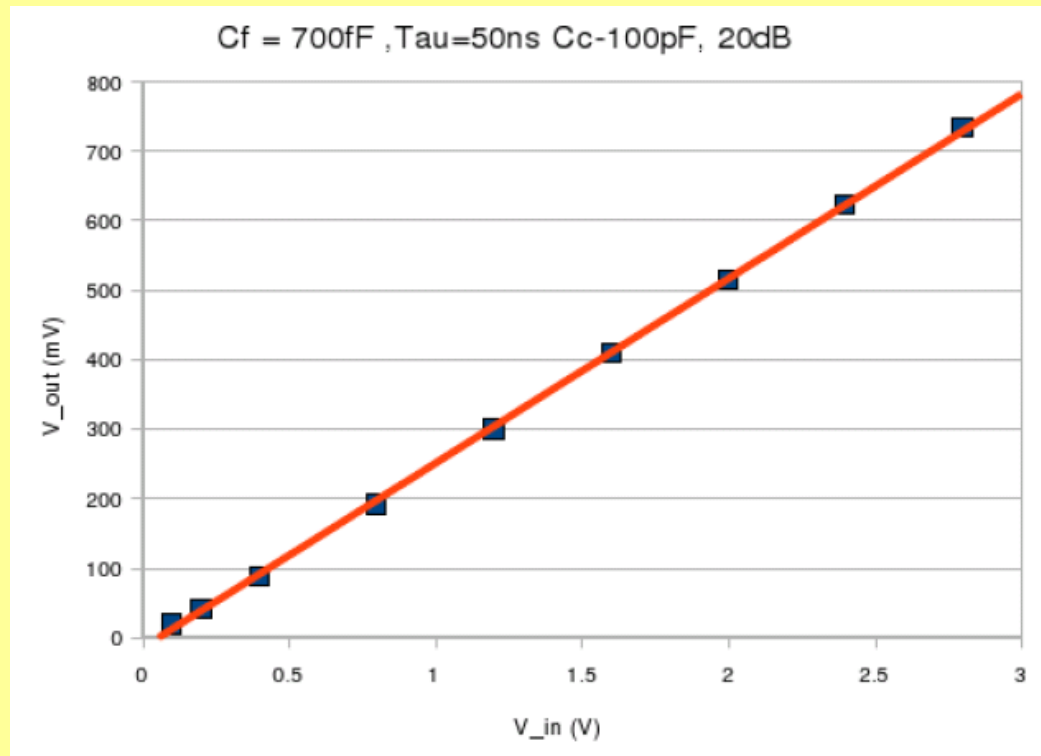
The input DAC span goes from 4.5V down to 0.5 V with a LSB of 20 mV. The default value is 4.5 V in order to operate the SiPM at minimum over-voltage, when the DAC is not loaded. The linearity is $\pm 2\%$ (5 LSB)





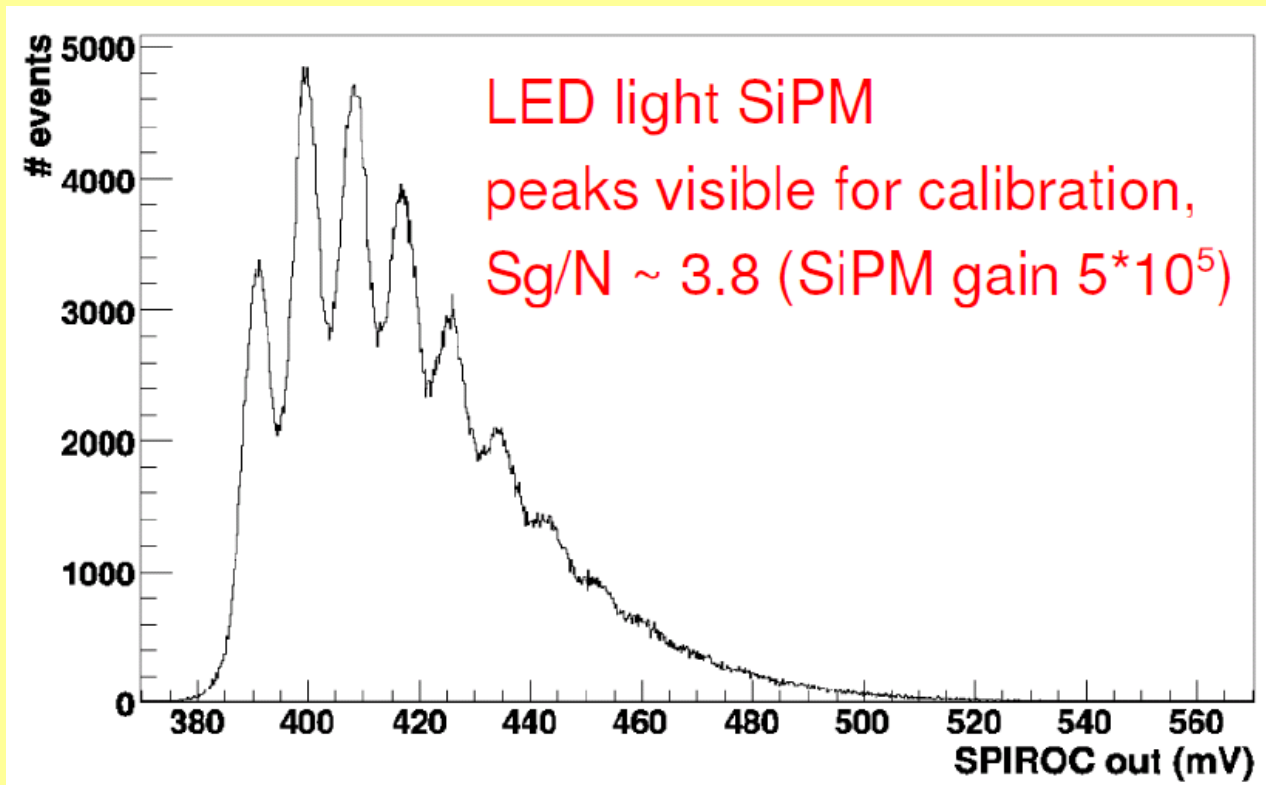
SPIROC

The high gain output signal amplitude as a function of the injected charge.
The fit of the linear part of the curve is better than 1 %



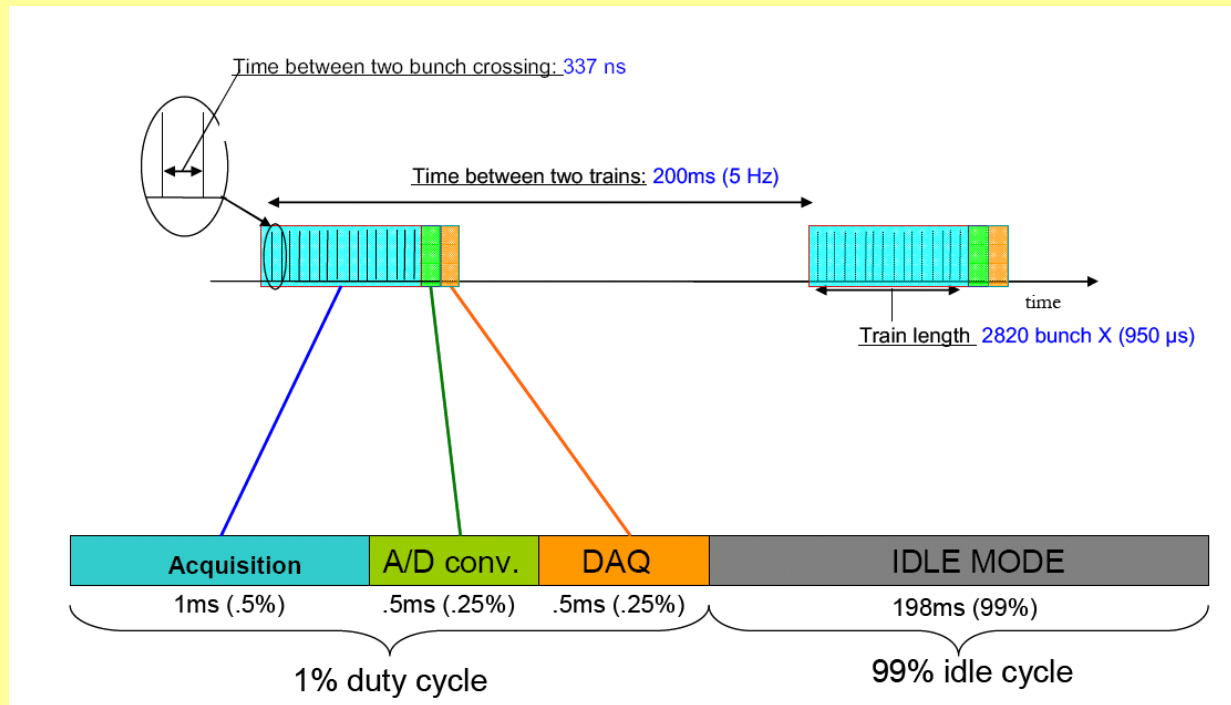
SPIROC

Test with LED light allows to nicely resolve the single photoelectrons peaks.



SPIROC

The SPIROC has been designed to match ILC beam structure.
The complete readout process is performed in 3 steps:
Acquisition phase (valid data are stored in analogue memories)
Conversion phase (data are converted into digital and stored in SRAM)
Readout phase (data are sent to DAQ during the inter-train)





ASIC developments for SiPM

NINO

CERN

(P. Jarron, E. Auffray, S.E. Brunner, H. Hillemanns, P. Lecoq,
T. Meyer, F. Powolny, W. Shen, H.C. Schultz-Coulon)

University of Bologna

(C. Williams)

EPFL/STI

(M. Despeisse)

DESY

(E. Garutti, M. Goettlich)

NINO chip was developed for the Time-Of-Flight detector (built using Multigap Resistive Plate Chambers) of ALICE Experiment
(not for SiPM application)

1. P. Jarron, E. Auffray, S.E. Brunner, M. Despeisse, E. Garutti, M. Goettlich, H. Hillemanns, P. Lecoq, T. Meyer, F. Powolny, W. Shen, H.C. Schultz-Coulon, C. Williams - *Time based readout of a silicon photomultiplier (SiPM) for Time Of Flight Positron Emission Tomography (TOF-PET)* - 2009 IEEE Nuclear Science Symposium Conference Record, p. 1212
2. F.Powolny, E.Auffray, S.Brunner, G.Condorelli, M.Despeisse, G.Fallica, H.Hillemanns, P.Jarron, A.Kluge, P.Lecoq, M.Mazzillo, T.C.Meyer, M.Morel, D.Sanfillipo, G.Valvo - *A time driven readout scheme for PET and CT using APDs and SiPMs* - NIM 617 (2010), p. 232
3. M. Despeisse, P.Jarron, F. Anghinolfi, S.Tiuraniemi, F.Osmic, P. Riedler, A.Kluge, and A. Ceccucci - *Low-Power Amplifier-Discriminators for High Time Resolution Detection* - (2009)
4. F. Powolny, E. Auffray, H. Hillemanns, P. Jarron, P. Lecoq, T. C. Meyer, and D. Moraes - *A Novel Time-Based Readout Scheme for a Combined PET-CT Detector Using APDs* - (2008)
5. F. Anghinolfi, P. Jarron, F. Krummenacher, E. Usenko and M.C.S. Williams - *NINO, an ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight detector in ALICE experiment* - (2004)
6. F. Anghinolfi, P. Jarron, A.N. Martemiyarov, E. Usenko, H. Wenninger, M.C.S. Williams, A. Zichichi - *NINO: an ultra-fast and low-power front-end amplifier/discriminator ASIC designed for the multigap resistive plate chamber* - (2004)



NINO

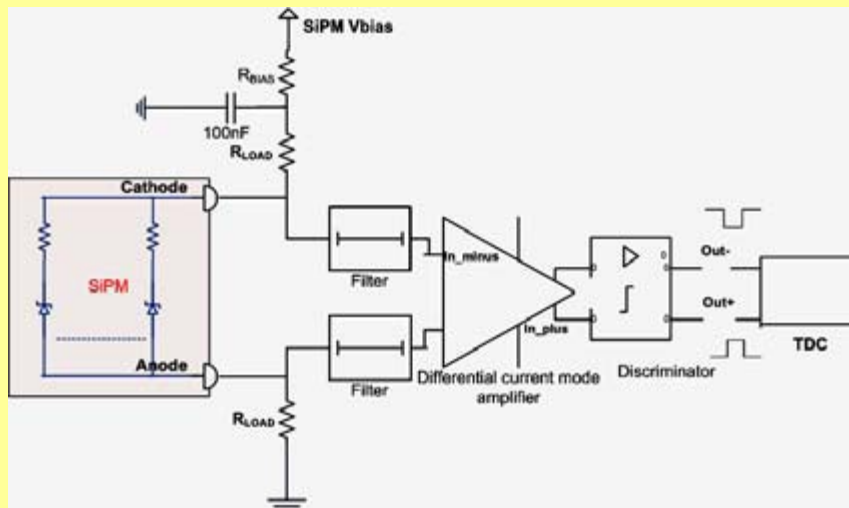
The NINO is an 8 channel front-end circuit for simultaneous time measurement, made in $0,25 \mu\text{m}$ IBM CMOS technology.

Input - fully differential current mode amplifier

Output pulse width dependent on the charge of input signal
Threshold discriminator adjustable in the range 10-100 fC.

SiPM Application: Time Of Flight Positron Emission Thomography (TOF-PET)

NINO

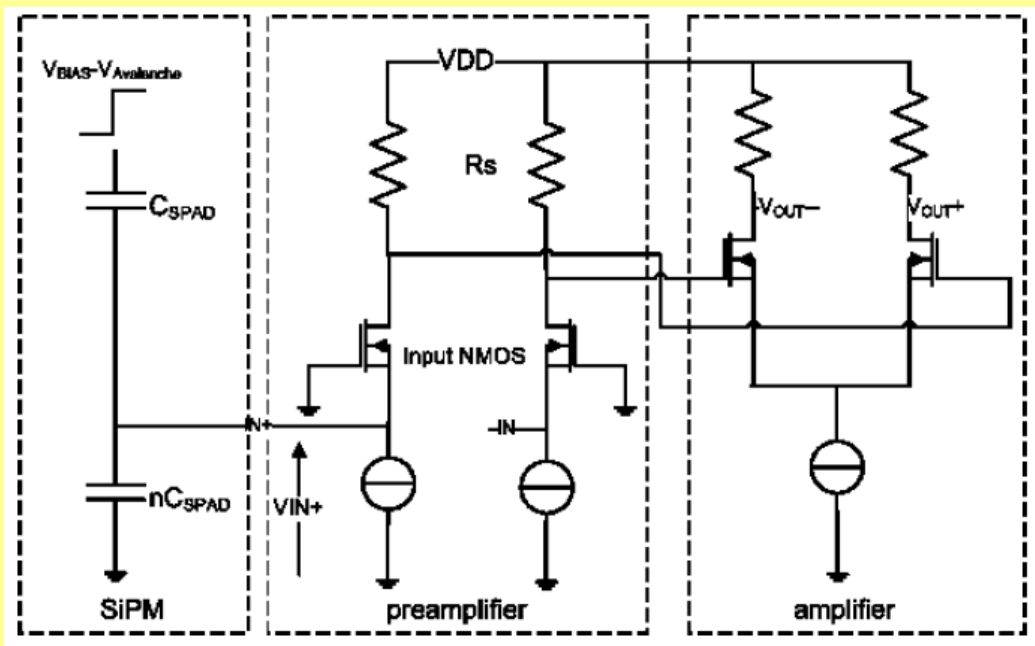


The circuit has a fully differential configuration from the SiPM terminals to the input of the TDC.

The differential connection between the SiPM and the amplifier inputs is obtained by adding a series load resistor to the cathode and anode terminals where the anode is referenced to ground.

The discriminator output are connected to TDC

NINO



The preamplifier stage base on a common gate input transistor pair with differential configuration to sense the unbalanced current produced by the input signal

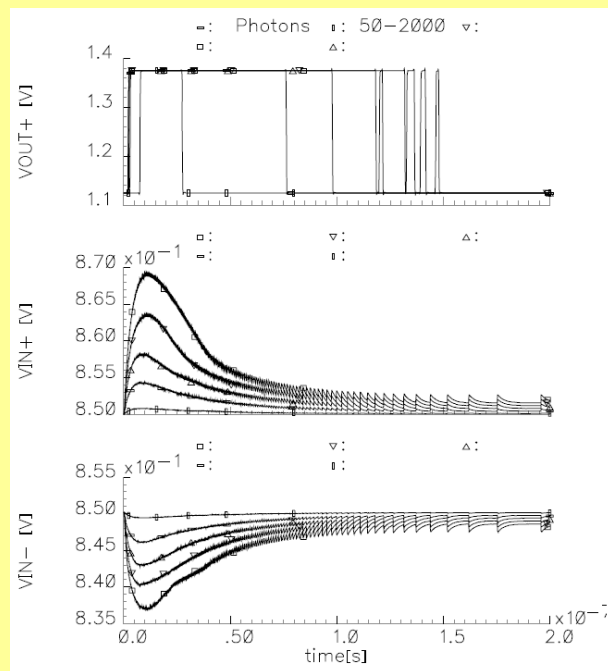
NINO

When 511 keV γ ray illuminated the LSO crystal typically ~ 2000 photons are impinging on the SiPM. Single photon signals are piling up to each other and form the signal.

The corresponding discriminator pulse width vary with the SiPM current signal from 20 ns/100 ph to 120 ns/2000 ph .

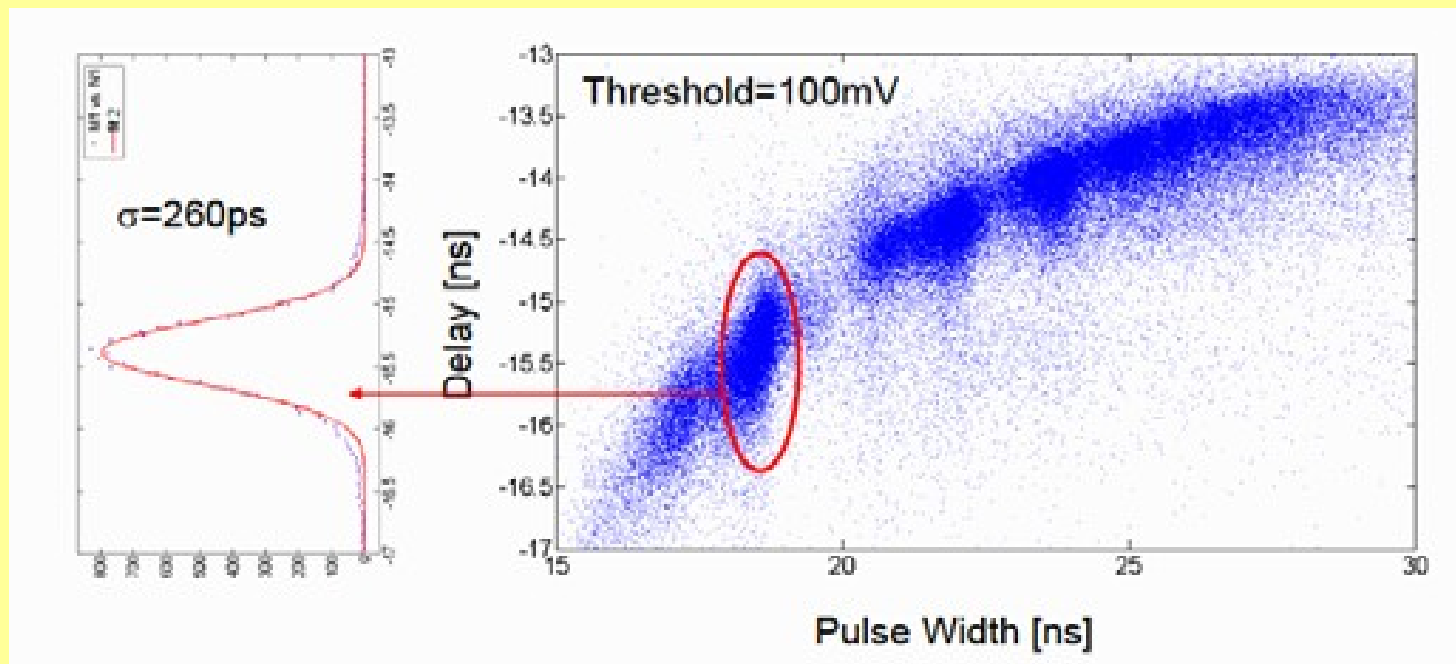
The discriminator response is nonlinear but it allows to encode signals with large dynamic range (from 1 to 2000 photons) Offering in addition the possibility of selecting windows around the photoelectric peak.

Amplifier response for a signal ranging from 100 to 2000 photons



NINO

Set up with illuminated SiPM by 405 nm laser pulse.
The cluster of single photon events are highlighted by red line.
Projection to the Y axis (delay between laser gate and discriminator output)
shows a jitter of 260 ps





ASIC developments for SiPM

PETA

University of Heidelberg

(P. Fischer, M. Ritzert, V. Mlotok, I. Peric)

Philips Research Europe, Aachen

(V. Schulz, T.Solf, and A. Thon)

Fondazione Bruno Kessler, Trento

(C.o Piemonte, N. Zorzi)



PETA

PETA (**P**osition-**E**nergy-**T**ime-**A**ASIC) chip was developed within FP7 EU Project HIPERIMAGE for γ detection in Time-Of-Flight PET/MR system

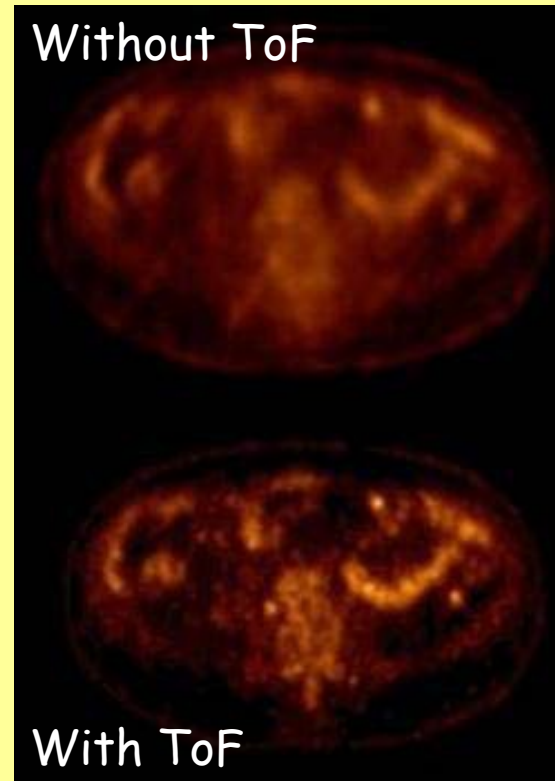
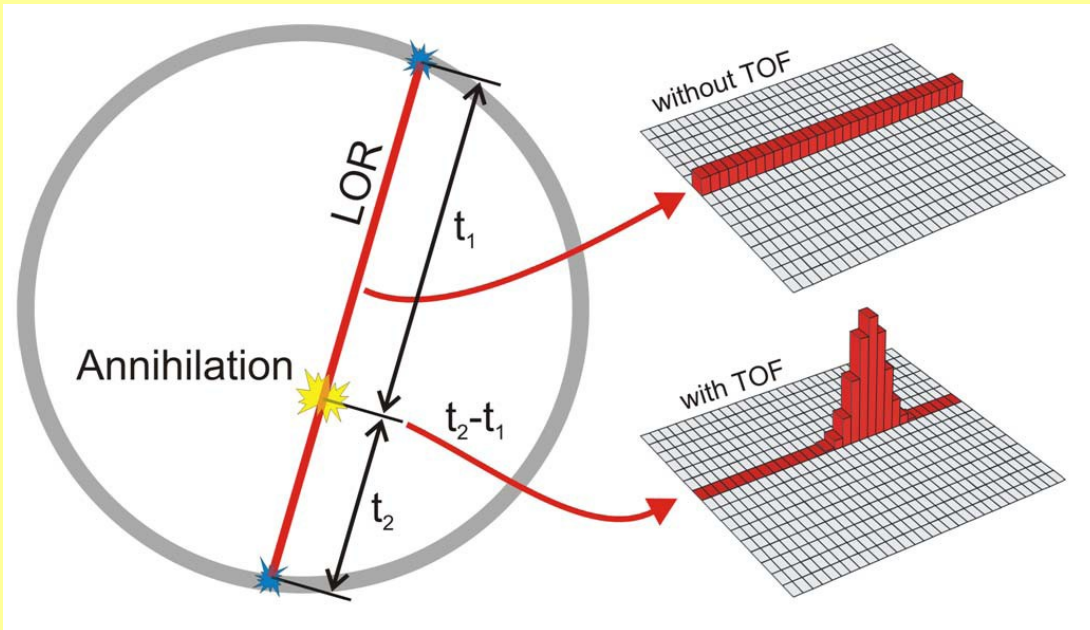
1. M. Ritzert, P. Fischer, V. Mlotok, I. Peric, C.o Piemonte, N. Zorzi, V. Schulz, T.Solf, and A. Thon - *Compact SiPM based Detector Module for Time-of-Flight PET/MR* - 2009 16th IEEE-NPSS Real Time Conference, p. 163
2. P. Fischer, I. Peric, M. Ritzert, and M. Koniczek - *Fast Self Triggered Multi Channel Readout ASIC for Time- and Energy Measurement* - IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 56, NO. 3, p.1153
3. P. Fischer, I. Peri, M. Ritzert and T. Solf- *Multi-Channel Readout ASIC for ToF-PET* - 2006 IEEE Nuclear Science Symposium Conference Record, p. 2523
4. V. Schulz - *Simultaneous Time-Of-Flight PET/MR* -, October 27th 2008

PETA

Benefits of TimeOfFlight - PET system

More information per coincidence event due to ToF measurement leads to better image quality

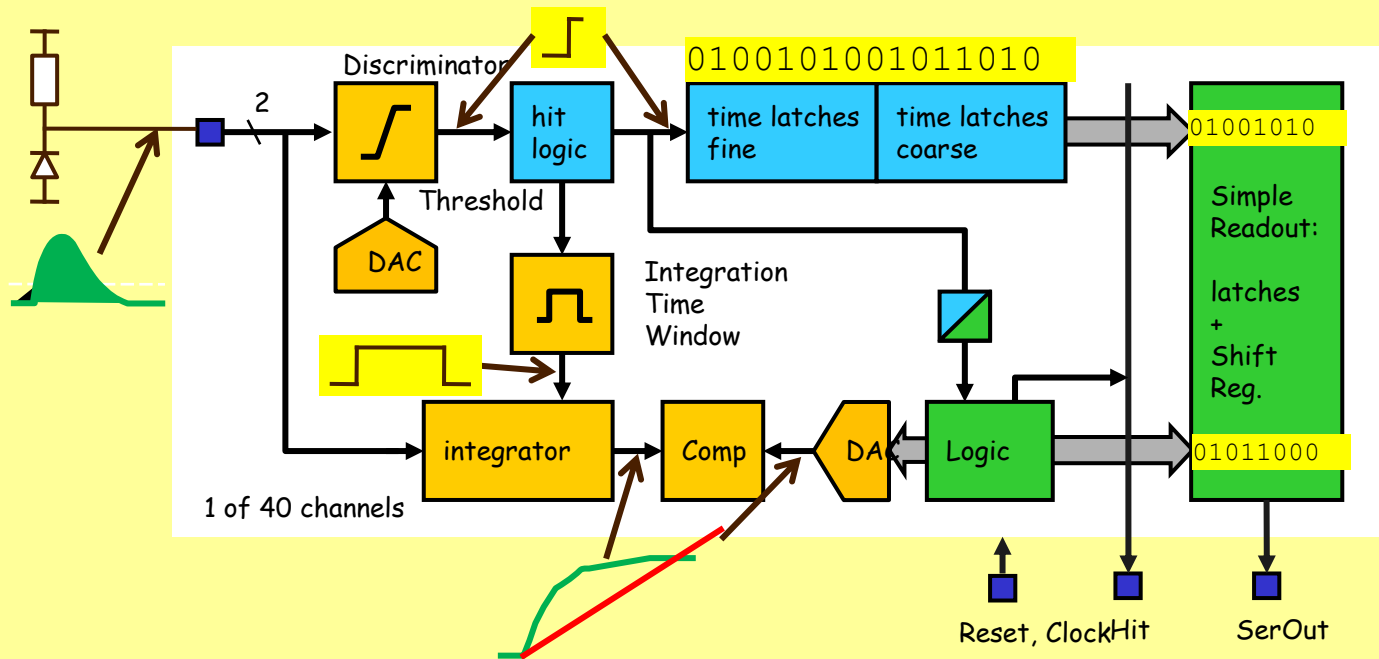
Increase contrast to background radiation (SNR)



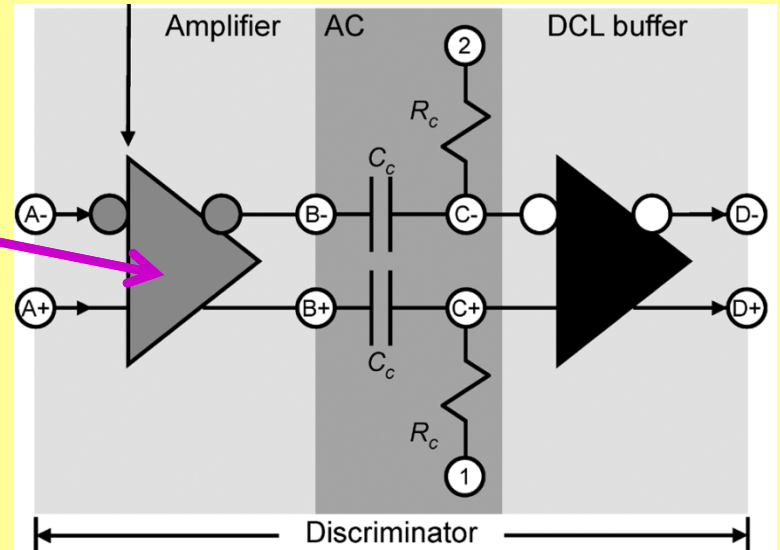
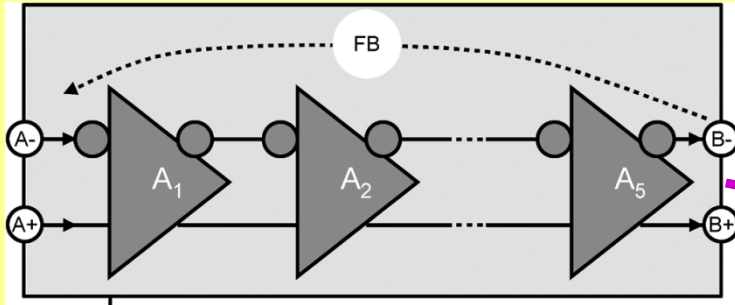
PETA

Fast discriminator generates a trigger signal, when it detects an input pulse over the threshold set by DAC. The trigger signal is used to freeze a set of latches, recording the current time stamp.

The integrator starts integration when input signal exceeds the trigger threshold and stops after defined period of time. Stored value is compared with signal generated by DAC and the final DAC value is readout.



PETA



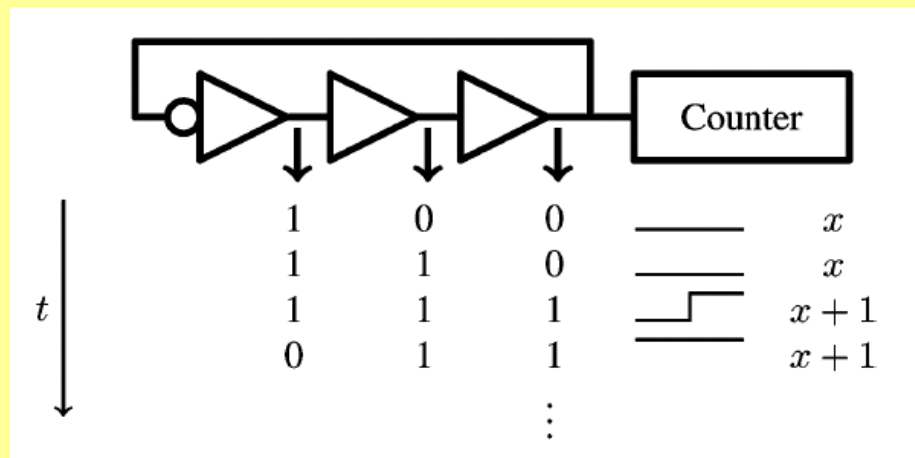
Discriminator:

The amplifier is implemented as cascade of 5 identical low-gain differential stages. The total voltage gain of the cascade is approximately 20.

The AC block allows to superpose the threshold ($T_h = V_2 - V_1$) to amplified signal.

The DCL buffer is optimized to receive differential logic signals, it has not been designed to amplify analog signals. Therefore the gain of the amplifier should be high enough to generate a signal amplitude of about 100 mV at the input of the buffer.

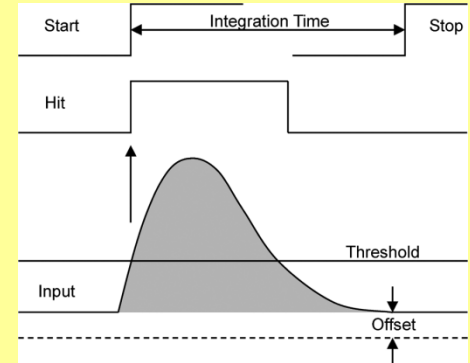
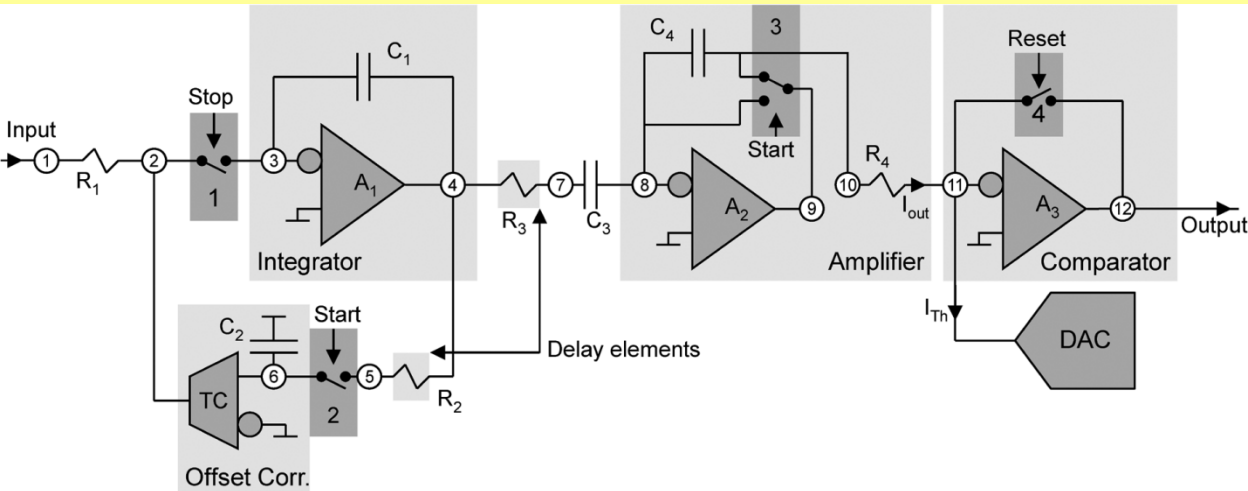
PETA



Timing Circuits:

The fine time bins are generated by voltage controlled oscillator (VCO) consists of 16 stages in differential logic. Signal from one point of VCO is locked to external coarse counter (15 bit) based on a linear-feedback shift register.

PETA



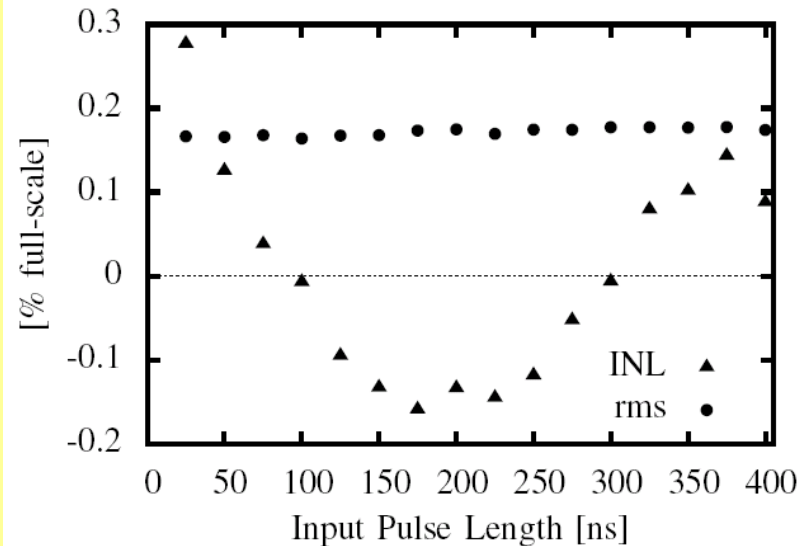
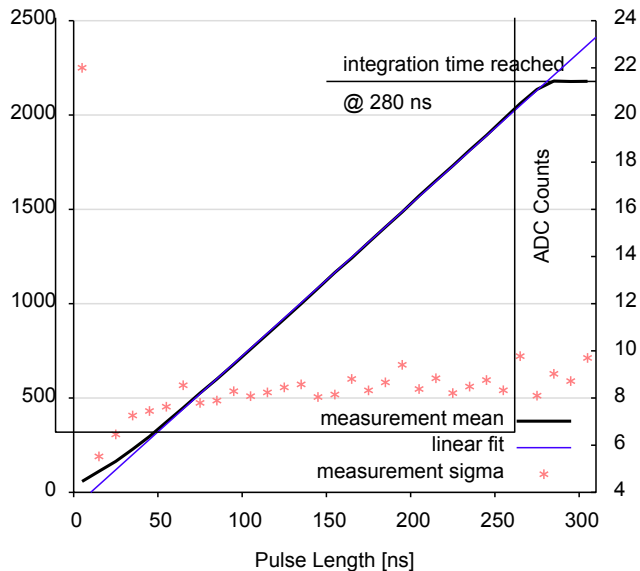
Integrator uses 3 differential amplifiers: first as integrator with offset correction circuit, second as difference amplifier and third as current comparator.

When the trigger signal occurs it starts signal integration for defined period of time.

DAC is increasing the threshold current up to the moment when comparator detects that it is larger than output current. The value of DAC is memorized at that moment.

Integrator/ADC Performance

Pulses with a fixed height and varying lengths have been injected. The integral non-linearity (INL), and standard deviation of the measured histograms

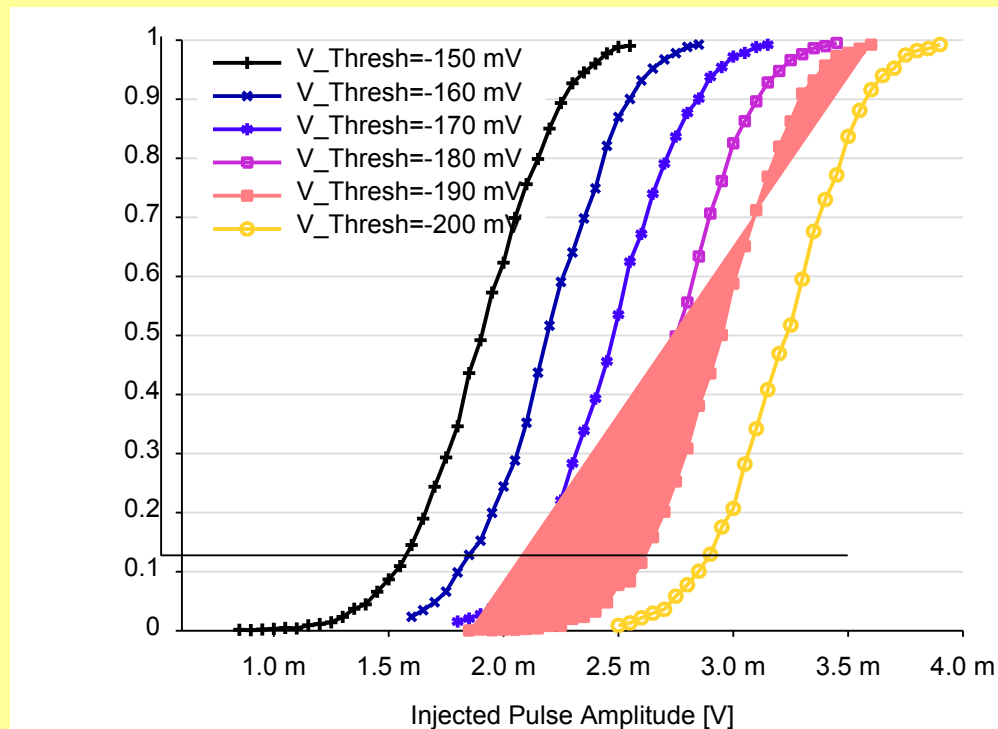


PETA

Discriminator Performance

Inject (small) pulses with increasing amplitude. Channel fires with 50% probability at threshold.

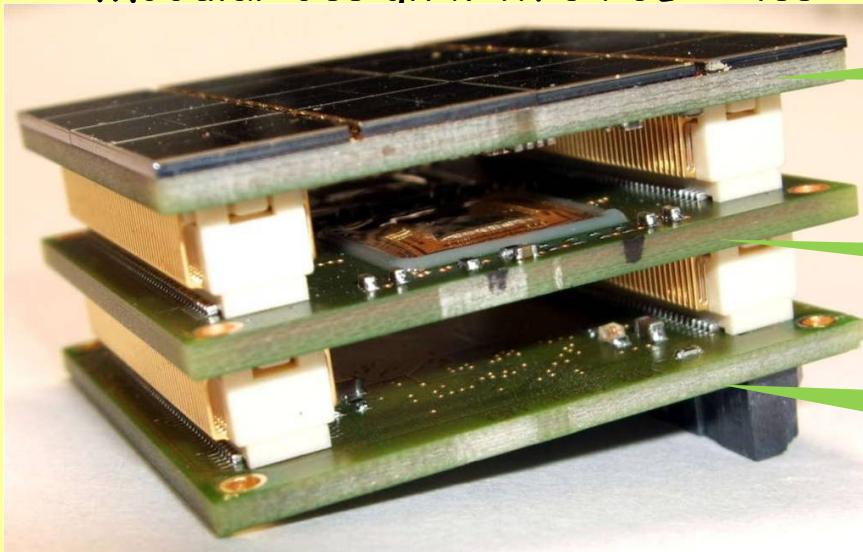
Thresholds as low as 2mV are possible, noise is $\sim 200\mu\text{V}$ (rms)



PETA

The hyperimage γ detection unit
Crystals + SiPM array + Electronics

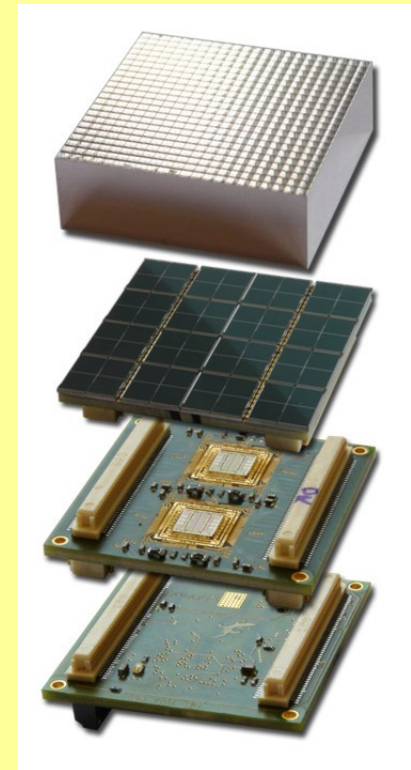
- Very compact Multi Channel Design
- $3 \times 3 \text{ cm}^2$ active area, very small edge
- 8×8 SiPMs + electronic channels
- Modular design with 3 PCB 'Tiles'



SiPM

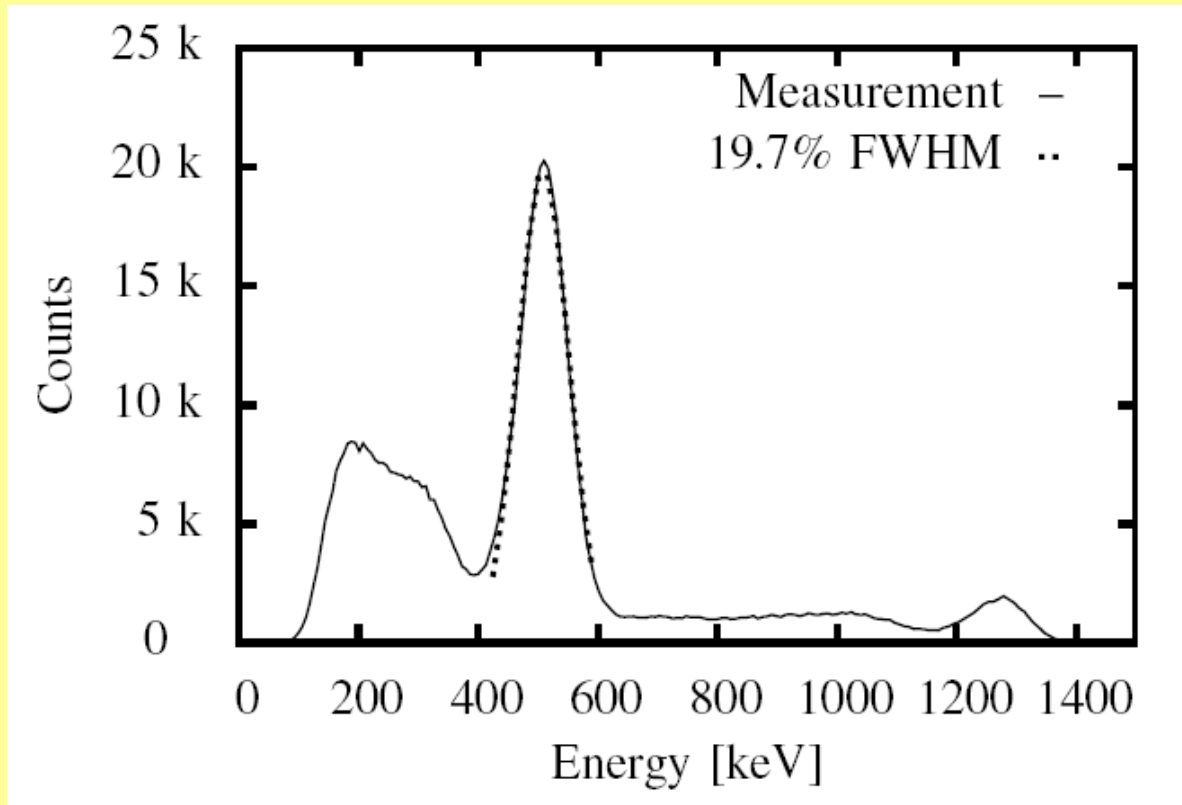
2 x PETA ASIC

FPGA Control
Power Regulator



PETA

Spectrum of ^{22}Na source measured with stack (first measurement with LYSO crystal without any optical coupling)





ASIC developments for SiPM

BASIC

Politecnico di Bari

(F. Corsi, M. Foresta, C. Marzocca, G. Matarrese)

Universita di Pisa

(N. Belcari, M. G. Bisogni, A. Del Guerra, S. Marcatili)



BASIC

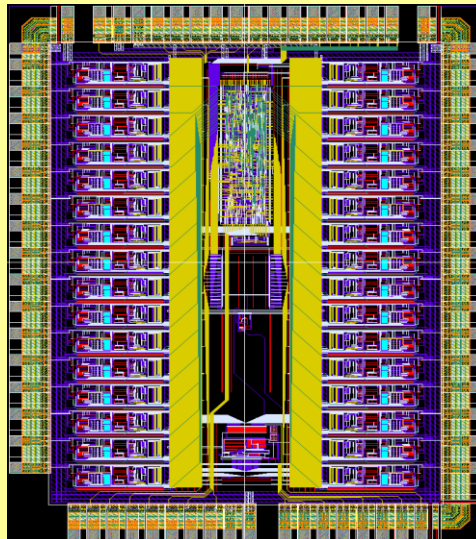
The BASIC chip was developed for γ detection in PET/MR system

1. F. Corsi, M. Foresta, C. Marzocca, G. Matarrese and A. Del Guerra - BASIC: an 8-channel Front-end ASIC for Silicon Photomultiplier Detectors - 2009 IEEE Nuclear Science Symposium Conference Record, p. 1082
2. F. Corsi, M. Foresta, C. Marzocca, G. Matarrese, A. Del Guerra - Current-Mode Front-End Electronics for Silicon Photo-Multiplier Detectors - (2007)
3. F. Corsi, A. Dragone, C. Marzocca, A. Del Guerra, P. Delizia, N. Dinu, C. Piemonte, M. Boscardin, G.F. Dalla Betta - Modelling a silicon photomultiplier (SiPM) as a signal source for optimum front-end design - NIMA 572 (2007) 416
4. F. Corsi, M. Foresta, C. Marzocca, G. Matarrese, A. Del Guerra - ASIC development for SiPM readout - (2008)
5. F. Corsi, M. Foresta, C. Marzocca, G. Matarrese, A. Del Guerra - CMOS analog front-end channels for silicon photo-multipliers - NIM
6. A. Del Guerra, N. Belcari, M. G. Bisogni, F. Corsi, M. Foresta, P. Guerra, S. Marcatili, A. Santos, G. Sportelli - Silicon Photomultipliers (SiPM) as novel photodetectors for PET - NIM

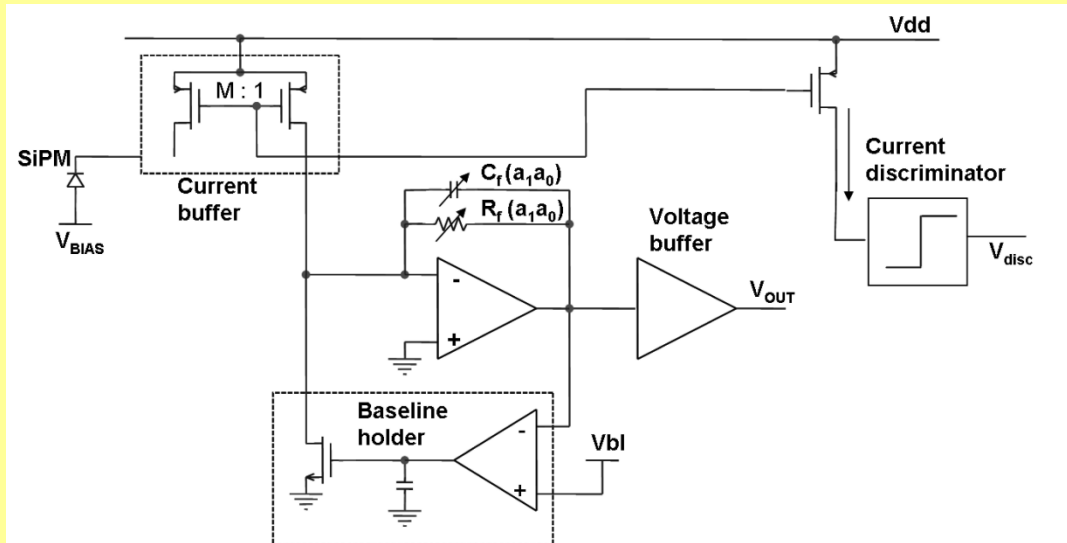
BASIC

BASIC is a 32 channel SiPM readout chip for simultaneous time and energy measurement, made in $0,35 \mu\text{m}$ CMOS AMS technology (2009).

Each front-end channel consists of a current buffer as input, reading on a very low impedance input node the current signal delivered by the detector. The current mirror at the input allows the splitting of the signal in two branches: one is used to send the output current to a current discriminator, which extracts the trigger signal associated to the timing of the event, while the other is sent to an integrator in order to obtain a voltage proportional to the charge

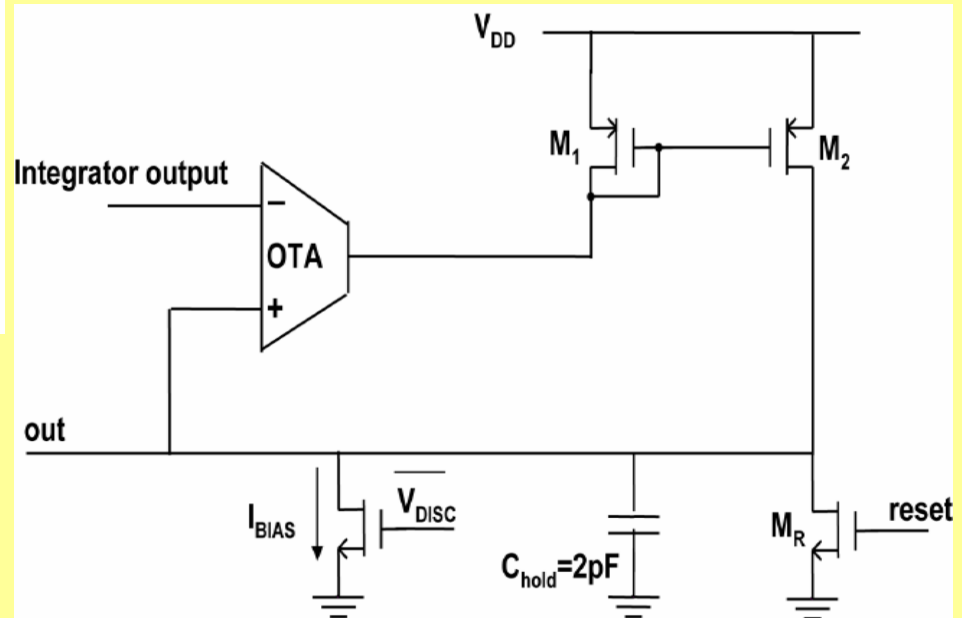
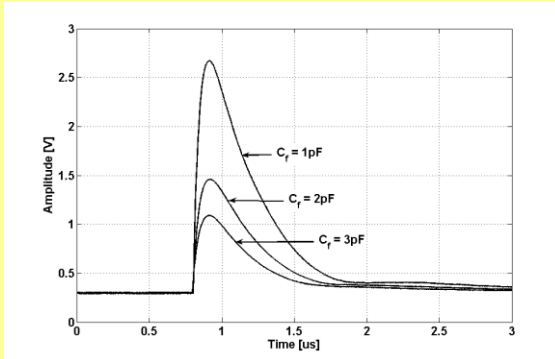


BASIC



Signal from current buffer is split in two branches: fast and slow. Fast one is used to send the output current to a current discriminator, which extracts the trigger signal associated to the timing of the event, while the slow one is sent to an integrator in order to obtain a voltage proportional to the charge delivered by the event. The integrator features a programmable gain to fit different detectors.

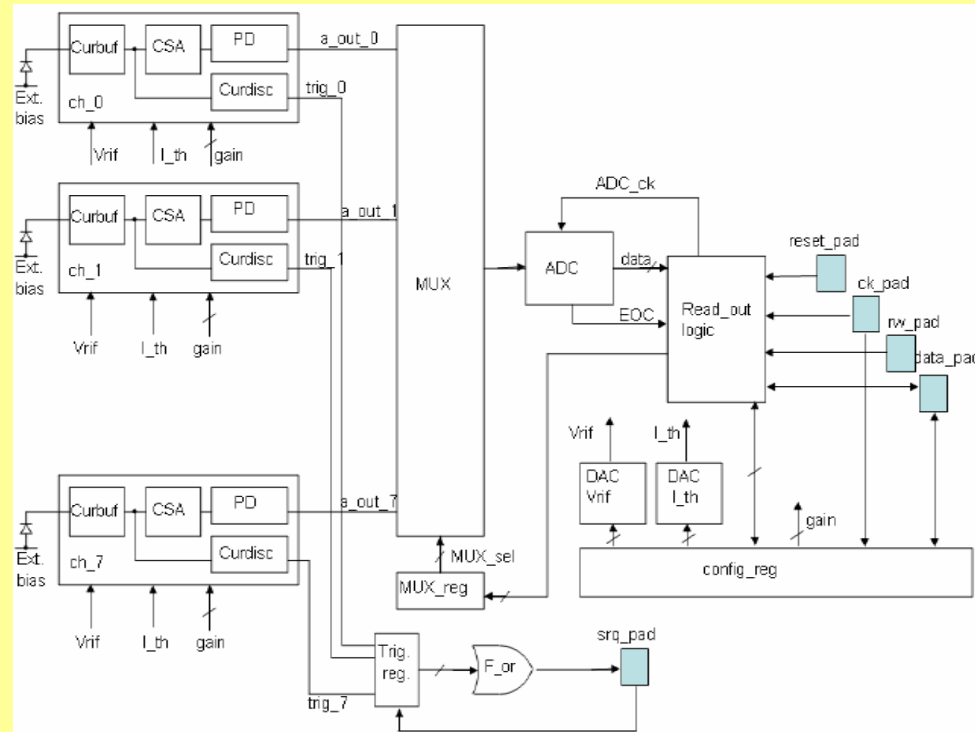
BASIC



Peak detector

The peak value of integrator output is stored on C_{hold} capacitor

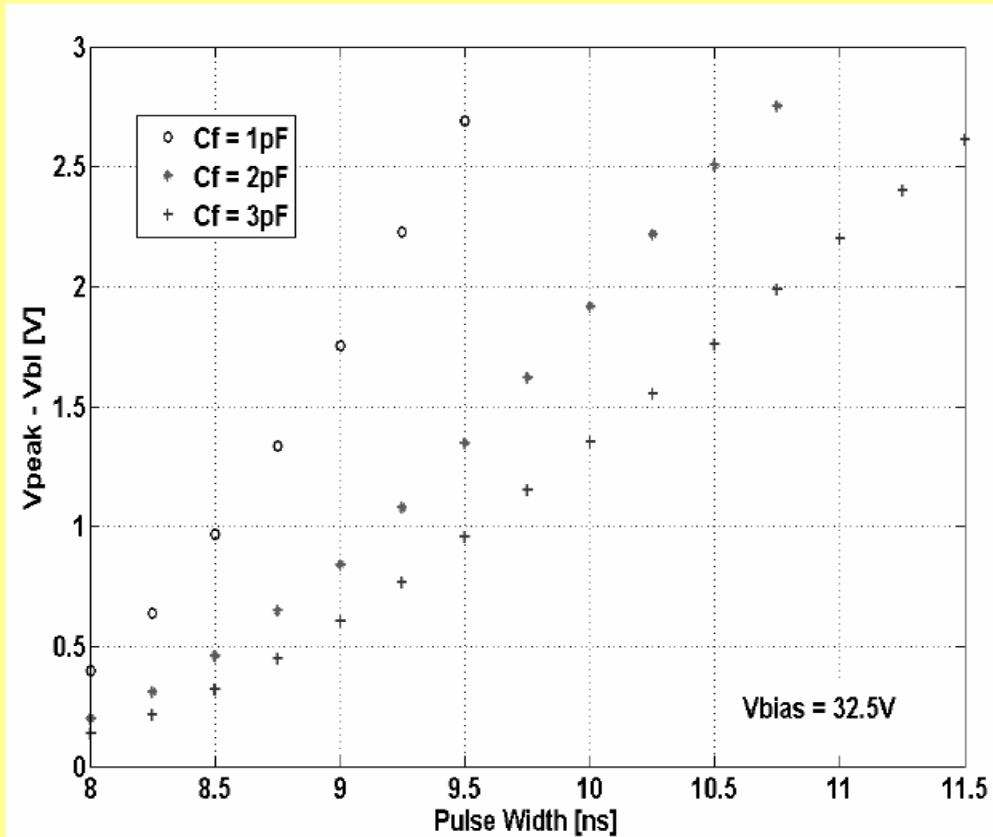
BASIC



Architecture of BASIC

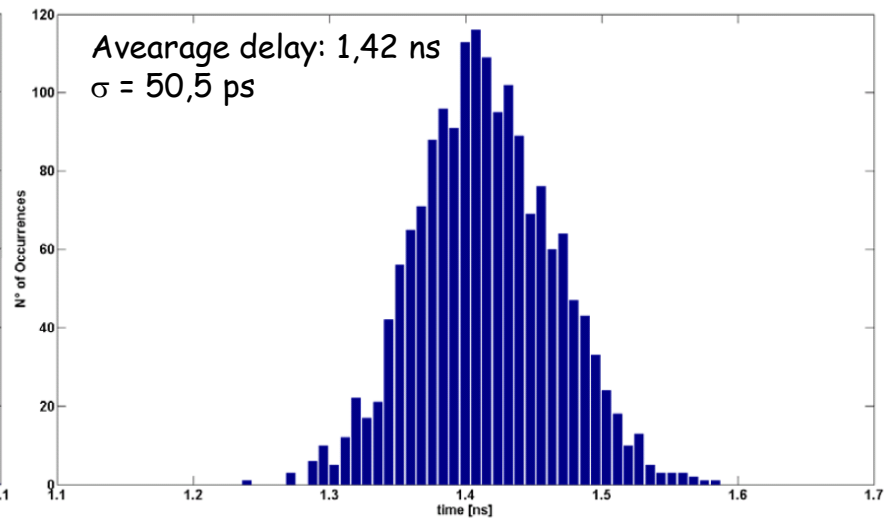
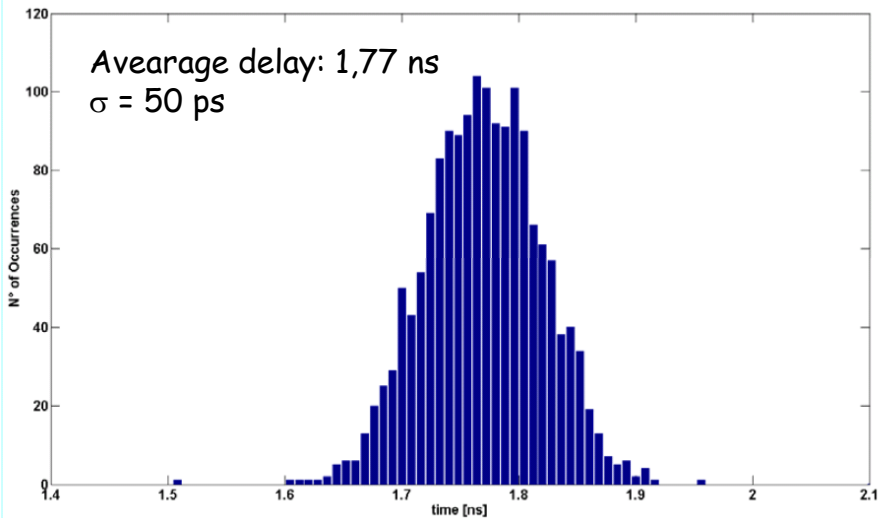
Analog signal is transfer to ADC channel by channel using multiplexer
The trigger signals are sent to an internal OR circuit in order to generate the trigger for readout of the whole chip

BASIC



Peak detector output vs. LED pulse width for different gain setting

BASIC

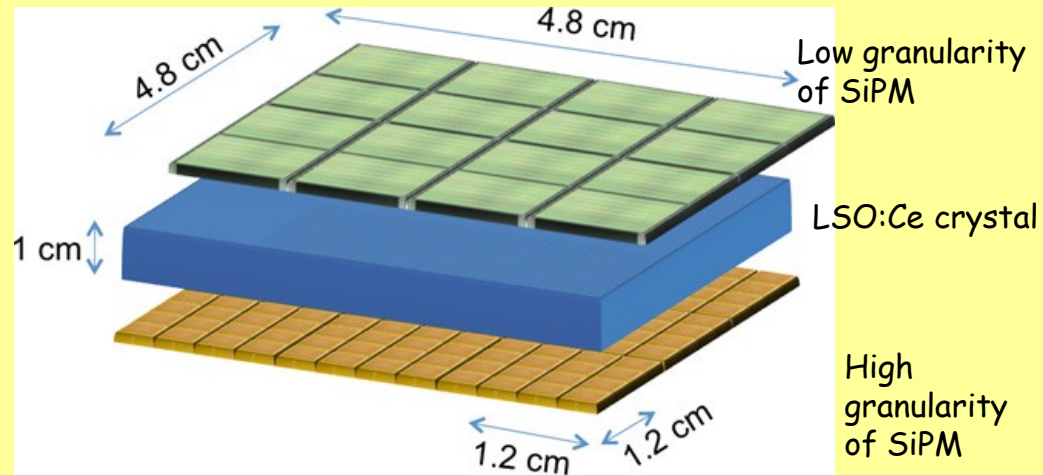


Slowest case: One excited channel above threshold

Fastest case: two excited channels above threshold

Jitter measurements worst case dispersion of 652 ps

BASIC



4D-PET module:

LSO:Ce scintillating crystal

Low granularity SiPM array (scintillating light provides the timing information and the trigger for acquisition)

High granularity SiPM array (scintillating light provides the hit position in the XY coordinates with resolution < 1 mm)



ASIC developments for SiPM

SPIDER (VATA64-HDR16)

University of Siena and INFN

(P. S. Marrochesi, M. G. Bagliesi, K. Batkov, G. Bigongiari, R. Cecchi, M. Y. Kim, P. Maestro, V. Millucci, R. Zei)

University of Pisa and INFN

(C. Avanzini, A. Basti, T. Lomtatz, F. Morsani)

IDEAS, Oslo



SPIDER

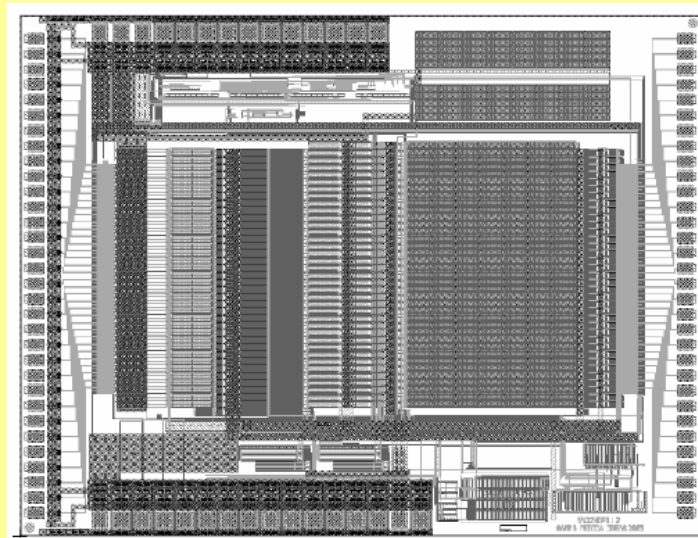
Chip VATA64-HDR16 was developed for SiPM applied in Ring Imaging Cherenkov Detector of SPIDER (Space Particle IDentifiER) Experiment

1. P.S.Marrocchesi - SPIDER -ESPERIMENTO DI RICERCA E SVILUPPO - (2007)
2. P. S. Marrocchesi, C. Avanzini, M. G. Bagliesi, A. Basti, K. Batkov, G. Bisignari, R. Cecchi, M. Y. Kim, T. Lomtatz, P. Maestro, V. Millucci, F. Morsani, R. Zet - Test of front-end electronics with large dynamic range coupled to SiPM for space-based calorimetry - 30TH INTERNATIONAL COSMIC RAY CONFERENCE (2007)

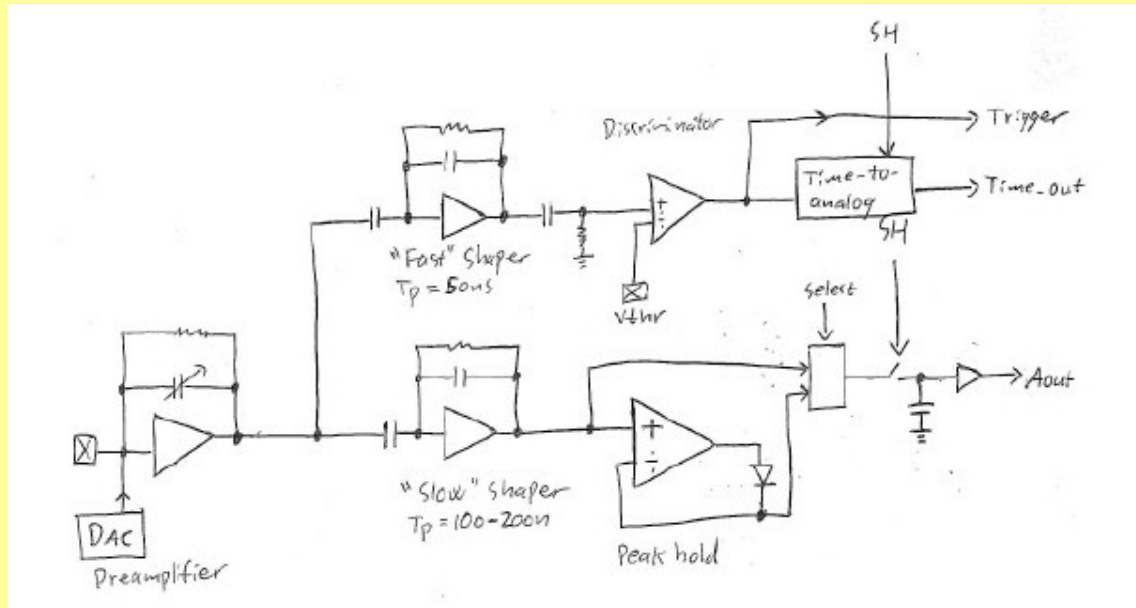
SPIDER

VATA64-HDR 16 is commercial chip developed with collaboration with IDEAS. It is 64 channel readout for SiPM. (2009).

Signal from preamplifier is split in two branches with fast and slow shaper. Branch with fast shaper measures time and other one measures charge.



SPIDER



The DAC on the input of preamplifier allows to moderate the bias voltage. Signal from preamplifier is shaped by fast (50ns) and slow (100-200ns) shapers.

Discriminator compared the signal from the output of fast shaper and generate the trigger pulse, which start time counter with 40ps resolution. Signal from slow shaper is sent to peak&hold detector which measure the pulse height.



ASIC developments for SiPM

RAPSODI chip

AGH - University of Science and Technology,
Krakow

(J. Barszcz, W. Kucewicz, J. Mlynarczyk, R. Mos, M. Sapor)

Forimtech, Geneve
(E. Grigoriev)



RAPSODI

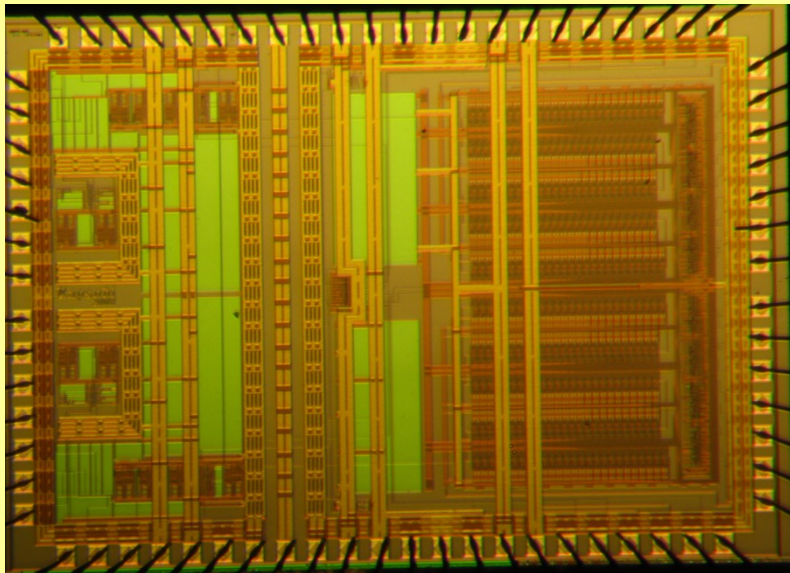
ASIC developed within the 6 FP RAPSODI for MICROSNOOPER (portable real time meter to detect and identify any type of radiation)

1. R. Mos, J. Barszcz, M.Jastrzab, W.Kucewicz, J. Mlynarczyk, E.Raus, M. Sapor - Front-End electronics for Silicon Photomultiplier detectors implemented in CMOS VLSI integrated circuit - Electrical Review NR 11a (2010), p.79
2. R. Mos, J. Barszcz, M.Jastrzab, W.Kucewicz, J. Mlynarczyk, E.Raus, M. Sapor - Front-end Electronics for Silicon Photomultipliers Implemented in CMOS VLSI - Preceedings of MIXDES 2009, 16th International Conference "Mixed Design of Integrated Circuits and Systems", June 25-27, 2009, p. 266
3. W. Kucewicz, J. Barszcz, J. Juraszek, R. Mos, M. Sapor - The two channel CMOS converter for silicon photomultiplier - Proceedings of ICSES 2008 - International conference on Signals and Electronic Systems : September 14-17, 2008, p. 165

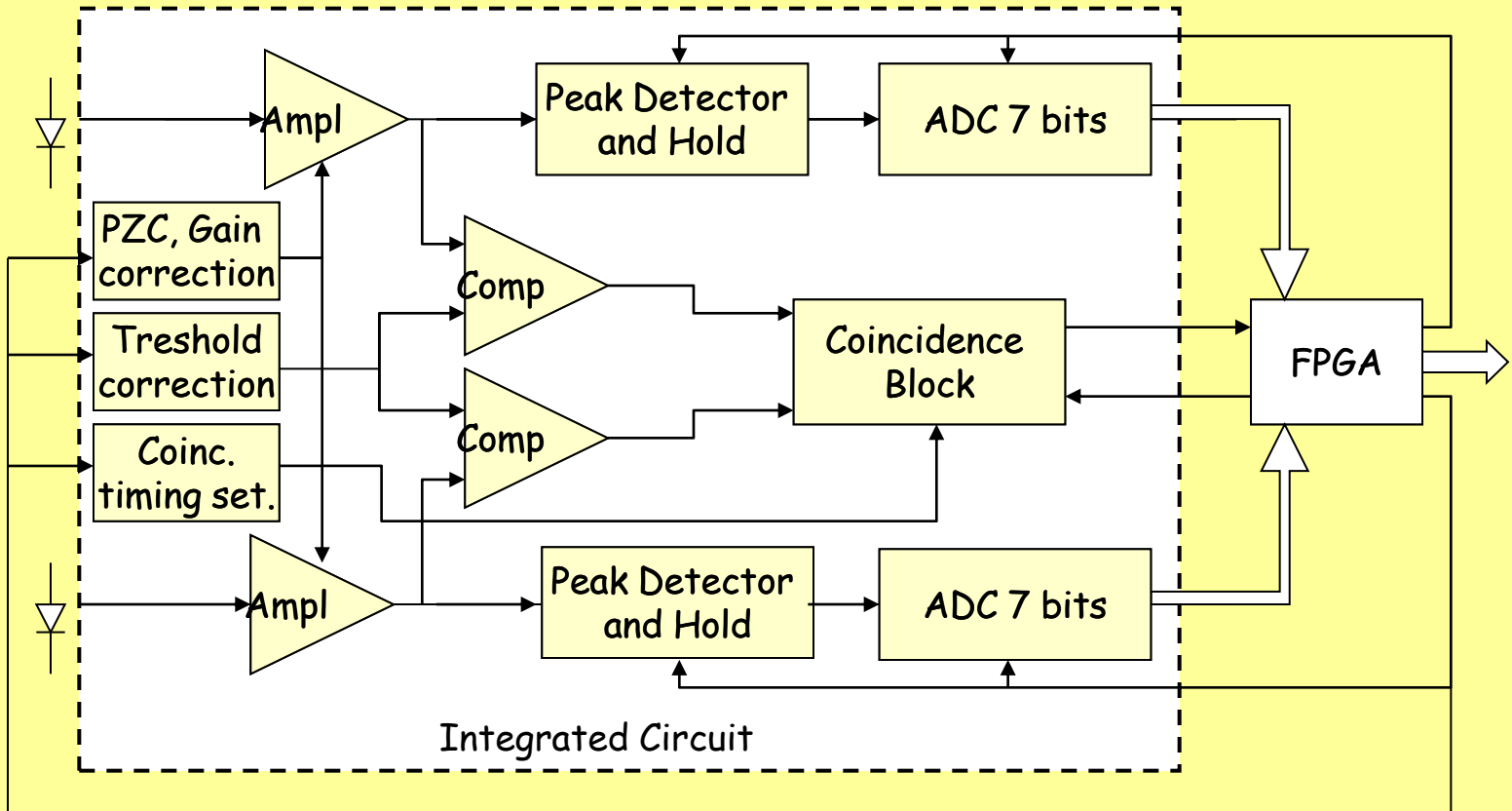
RAPSODI

ASIC is a 2 channel SiPM readout chip for energy measurement, made in $0,35\ \mu\text{m}$ CMOS AMS technology (2009).

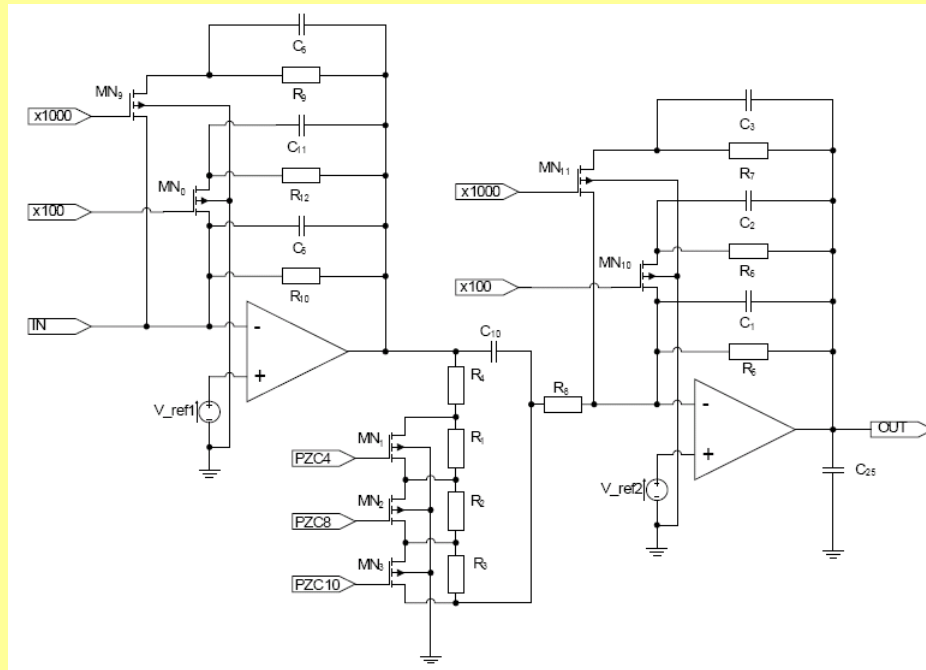
Each channel measures the amplitude of the signal from SiPM and converts it in 7-bit ADC. The channels can work separately or in coincidence mode.



RAPSODI

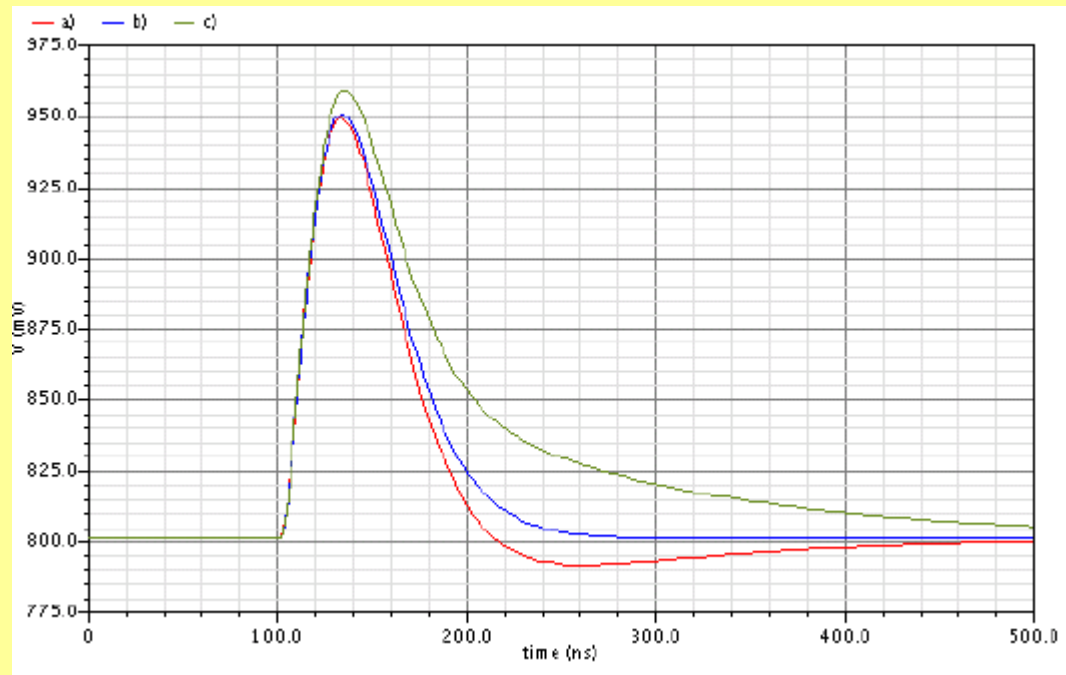


RAPSODI

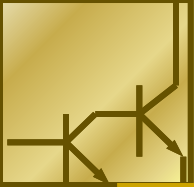


Two stage amplifier allows to switch ranges between 1, 10 and 100 pC.
The PZC block moderate the following edge of the signal.

RAPSODI



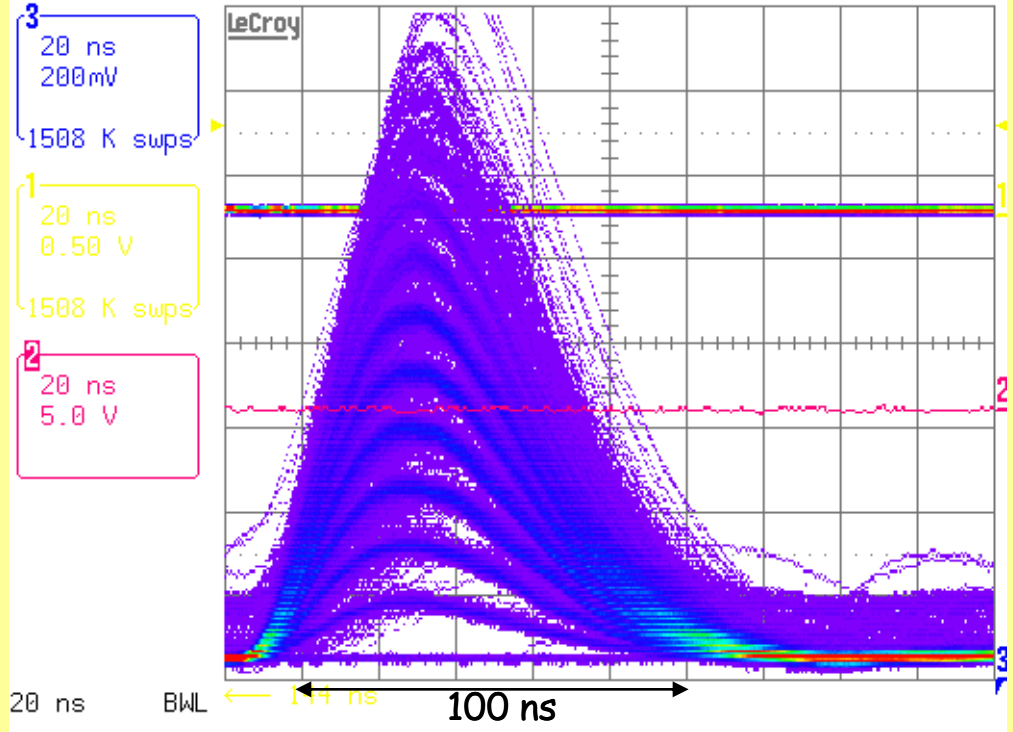
Two stage amplifier allows to switch ranges between 1, 10 and 100 pC.
The PZC block moderate the following edge of the signal.



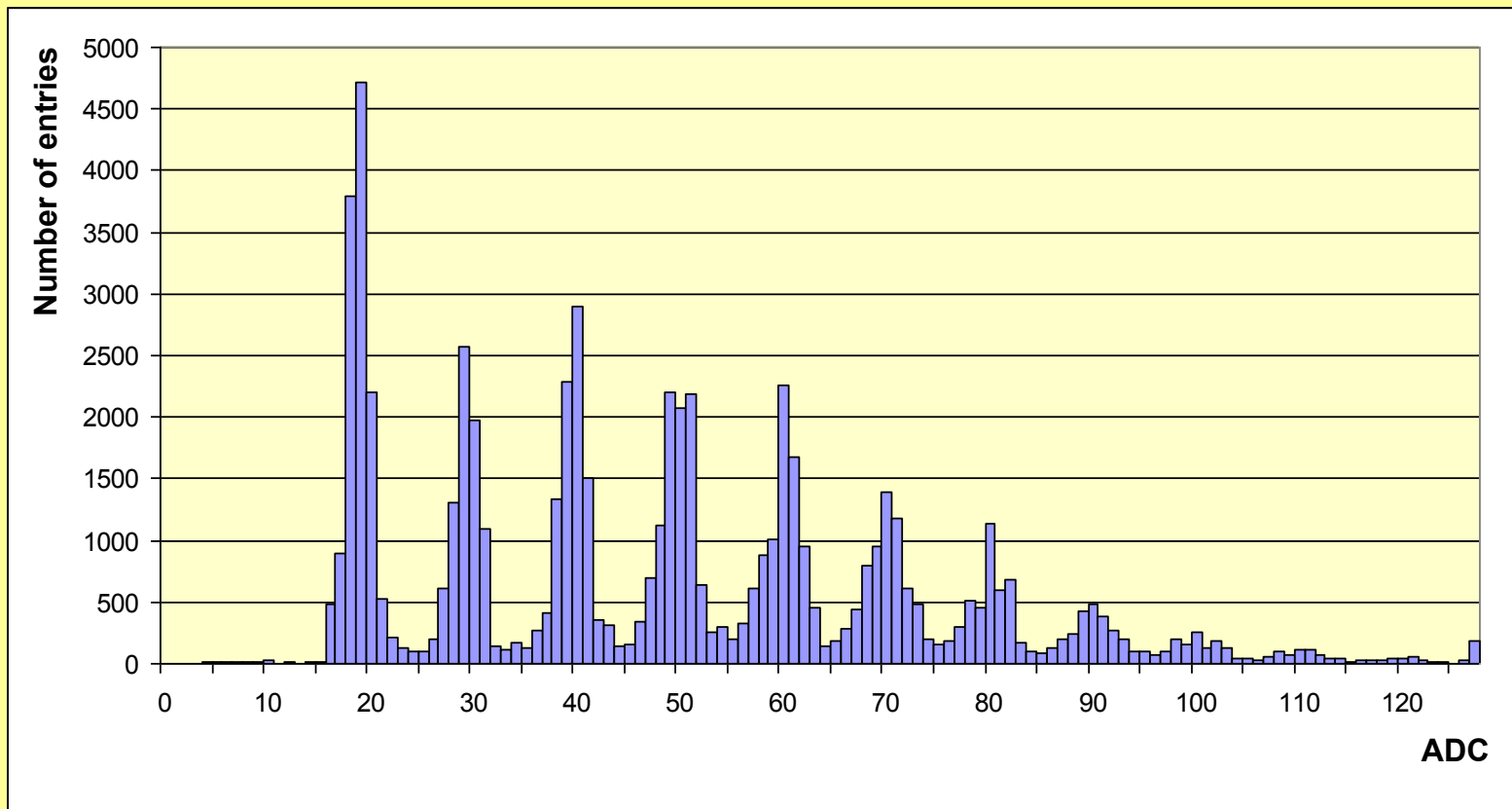
RAPSODI

27-Feb-09
14:56:41

Sensl SiPM diode
Bias 31V,
Laser 1060nm (12dB; f-100kHz, pulsewidth
4ns)
threshold 0.95V(just above 1 avalanche)



RAPSODI



Conclusions

Chip Name	Measured quantity	Application	Input configuration	Technology
FLC_SiPM	Pulse charge	ILC Analog HCAL	Current input	CMOS 0,8 μm
MAROC	Pulse charge, trigger	ATLAS luminometer	Current input	SiGe 0,35 μm
SPIROC	Pulse charge, trigger, time	ILC HCAL	Current input	SiGe 0,35 μm
NINO	Trigger, pulse width	ALICE TOF	Differential input	CMOS 0,25 μm
PETA	Pulse charge, trigger, time	PET	Differential input	CMOS 0,18 μm
BASIC	Pulse height, trigger	PET	Current input	CMOS 0,35 μm
SPIDER (VATA64-HDR16)	Pulse height, trigger, time	SPIDER RICH	Current input	
RAPSODI	Pulse height, trigger	SNOOPER	Current input	CMOS 0,35 μm

Conclusions

Chip Name	# of channels	Digital output	Power supply	Area [sq mm]	Dynamic range	Input resistance	Timing jitter	Year
FLC_SiPM	18	n	5V (0,2W)	10			-	2004
MAROC2	64	y	5 V	16	80 pC	50 Ω		2006
SPIROC	36	y	5 V	32				2007
NINO	8	n	(0,24W)	8	2000 pe	20 Ω	260 ps	2004
PETA	40	y	(1,2W)	25	8 bit		50 ps	2008
BASIC	32	y	3,3 V	7	70 pC	17 Ω	~120 ps	2009
SPIDER (VATA64-HDR16)	64	n		15	12 pC			2009
RAPSODI	2	y	3,3 V (0,2W)	9	100 pC	20 Ω	-	2008