CAS/DSP - Digital Signal Processing

Report of Contributions

https://indico.cern.ch/e/11749

Contribution ID: **2** Type: **not specified**

Types of Accelerators and Specific Needs I

Friday 1 June 2007 08:30 (1 hour)

Presenter: SHEA, Tom (SNS)

Contribution ID: **3** Type: **not specified**

Types of Accelerators and Specific Needs II

Friday 1 June 2007 09:30 (1 hour)

Presenter: SHEA, Tom (SNS)

Contribution ID: **4** Type: **not specified**

High Level Modeling Tools I

Friday 1 June 2007 12:00 (1 hour)

Presenter: EVANS, John (CERN)

Contribution ID: **5** Type: **not specified**

High Level Modeling Tools II

Friday 1 June 2007 11:00 (1 hour)

Presenter: EVANS, John (CERN)

Contribution ID: **6** Type: **not specified**

Math I

Saturday 2 June 2007 08:30 (1 hour)

Modern DSP makes use of a variaty of mathematical techniques. These are used to design and understand efficient filters for data processing and control.

Mathemathics for DSP in accelerator environment include statistics, one and multidimensional transformations and complex function theory. The basic concepts from the mathematical point of view are presented in 4 sessions including all you need to know about the harmonic oscillator which is investigated in the afternoon exercise sessions.

Presenter: Dr HOFFMANN, Markus (DESY)

Contribution ID: **7** Type: **not specified**

Control Theory I

Saturday 2 June 2007 09:30 (1 hour)

In engineering and mathematics, control theory deals with the behavior of dynamical systems. The desired output of a system is called the reference. When one or more output variables of a system need to follow a certain reference over time, a controller manipulates the inputs to a system to obtain the desired effect on the output of the system.

Rapid advances in digital system technology have radically altered the control design options. It has become routinely practicable to design very complicated digital controllers and to carry out the extensive calculations required for their design. These advances in implementation and design capability can be obtained at low cost because of the widespread availability of inexpensive and powerful digital processing platforms and high speed analog IO devices.

The emphasis of the course is on designing digital controls to achieve good dynamic response and small errors while using signals that are sampled in time and quantized in amplitude. Both transform (classical control) and state-space (modern control) methods are described and applied to illustrative examples. The transform methods emphasized are the root-locus method of Evans and frequency response. The state-space methods developed are the technique of pole assignment augmented by an estimator (observer) and optimal quadratic-loss control. The optimal control problems use the steady-state constant–gain solution. Other topics covered are system identification and non-linear control.

System Identification is a general term to describe mathematical tools and algorithms that build dynamical models from measured data. A dynamical model in this context is a mathematical description of the dynamic behavior of a system or process.

Non-linear control is a sub-division of control engineering which deals with the control of non-linear systems. The behaviour of a non-linear system cannot be described as a linear function of the state of that system or the input variables to that system. There are several well-developed techniques for analysis and design of nonlinear feedback systems.

Presenter: Dr SIMROCK, Stefan (DESY)

Contribution ID: **8** Type: **not specified**

Introduction to DSP I

Saturday 2 June 2007 11:00 (1 hour)

Digital Signal Processor (DSP) have been used in accelerator systems for more than 15 years and have largely contributed to the evolution towards digital technology of many accelerator systems, such as machine protection, diagnostics and control of beams, power supply and motors.

These three lectures aim at familiarising the student with DSP characteristics and processing development. Typical difficulties, problems and choices faced by DSP designers and developers are outlined and hints are given on the best solution.

The first lecture addresses DSP evolution over the years and looks into DSP hardware. In particular, distinctive DSP core components and peripherals are examined.

The second lecture focuses on real-time development flow and in particular on software development and debugging process.

The third lecture analyses code optimisation options and provides guidelines on ways to carry out code optimisation. The lecture then examines some of the choices DSP designers are faced with when devising a new digital system/ In particular, DSP and system architecture choice, together with code design are considered. The system integration phase is also addressed, and recommended practices and guidelines are summarised. Finally, an real-life digital system example is discussed to show how a one can profit from some of the features described during the course.

Presenter: ANGOLETTA, Maria Elena (CERN)

Contribution ID: **9** Type: **not specified**

Introduction to FPGA I

Saturday 2 June 2007 12:00 (1 hour)

Field Programmable Gate Arrays (FPGA) are, along with Digital Signal Processors, one of the platforms of choice for implementing complex digital signal processing systems. Thanks to Moore's law and the availability of high level modeling environments, more and more algorithms which previously required a software implementation can nowadays be carried out directly in hardware, with the concomitant performance increases. In these lectures, we start with the basics of digital design and go on to describe the design flow that allows us to target our design to an FPGA. A detailed description of the internal architecture of modern FPGA chips is also given, along with recipes to make the best possible use of all the available on-chip resources. Then we go on with hardware implementations of basic arithmetic blocks and more involved operations such as Distributed Arithmetic and CORDIC. Another important topic we treat concerns some potential pitfalls when doing DSP which apply specifically to FPGA implementations.

Presenter: SERRANO, Javier (CERN)

Contribution ID: **10** Type: **not specified**

From Analog to Digital I

Saturday 2 June 2007 14:30 (1 hour)

Analog to digital conversion and its reverse, digital to analog conversion, are ubiquitous in all modern electronics, from instrumentation and telecommunication equipment to computers and entertainment.

We shall explore the consequences of converting signals between the analogue and digital domains and give an overview of the internal architecture and operation of a number of converter types.

The importance of analogue input and clock signal integrity will be explained and methods to prevent or mitigate the effects of interference will be shown.

Examples will be drawn from several manufacturer's datasheets.

Presenter: BELLEMAN, Jeroen (CERN)

Contribution ID: **11** Type: **not specified**

Math II

Sunday 3 June 2007 08:30 (1 hour)

see description in “Math I”

Presenter: Dr HOFFMANN, Markus (DESY)

Contribution ID: **12** Type: **not specified**

Control Theory II

Sunday 3 June 2007 09:30 (1 hour)

see description in “Control Theory I”

Presenter: Dr SIMROCK, Stefan (DESY)

Contribution ID: **13** Type: **not specified**

Introduction to DSP II

Sunday 3 June 2007 11:00 (1 hour)

Presenter: ANGOLETTA, Maria Elena (CERN)

Contribution ID: **14** Type: **not specified**

Introduction to FPGA II

Sunday 3 June 2007 12:00 (1 hour)

see description in “Introduction to FPGA I”

Presenter: SERRANO, Javier (CERN)

Contribution ID: **15** Type: **not specified**

From Analog to Digital II

Sunday 3 June 2007 14:30 (1 hour)

see description in “From Analog to Digital I”

Presenter: BELLEMAN, Jeroen (CERN)

Contribution ID: **16** Type: **not specified**

Math III

Monday 4 June 2007 08:30 (1 hour)

see description in “Math I”

Presenter: Dr HOFFMANN, Markus (DESY)

Contribution ID: **17** Type: **not specified**

Control Theory III

Monday 4 June 2007 09:30 (1 hour)

see description in “Control Theory I”

Presenter: Dr SIMROCK, Stefan (DESY)

Contribution ID: **19** Type: **not specified**

Introduction to DSP III

Monday 4 June 2007 11:00 (1 hour)

Presenter: ANGOLETTA, Maria Elena (CERN)

Contribution ID: **20** Type: **not specified**

Introduction to FPGA III

Monday 4 June 2007 12:00 (1 hour)

see description in “Introduction to FPGA I”

Presenter: SERRANO, Javier (CERN)

Contribution ID: **21** Type: **not specified**

From Analog to Digital III

Monday 4 June 2007 14:30 (1 hour)

see description in “From Analog to Digital I”

Presenter: BELLEMAN, Jeroen (CERN)

Contribution ID: **22** Type: **not specified**

Math IV

Wednesday 6 June 2007 08:30 (1 hour)

see description in “Math I”

Presenter: Dr HOFFMANN, Markus (DESY)

Contribution ID: **23** Type: **not specified**

RF Application I

Wednesday 6 June 2007 09:30 (1 hour)

The rapid advances in digital technology on the one hand and the increasing demands in the field of Low Level Radio Frequency (LLRF) in terms of stability, accuracy, reproducibility and monitoring capabilities on the other hand has given a boost to the development of digital LLRF systems. In these lectures the fundamentals of amplitude and phase detection by means of I/Q detection, digital down converting (DDC), decimation and different versions of I/Q modulators will be illustrated.

Basic concepts of digital cavity field and phase control along with tuner servo loops will be introduced. Other applications of digital control like radial loops, klystron linearization, adaptive feed forward schemes and system identification approaches will be presented. Advantages and disadvantages of digital versus analogue RF applications have to be discussed. Examples of hard- and software implementations at various accelerator laboratories together with their performance will be shown.

Presenter: Dr SCHILCHER, Thomas (Paul Scherrer Institute)

Contribution ID: **24** Type: **not specified**

Multi Bunch Feedback Systems

Wednesday 6 June 2007 11:00 (1 hour)

Coupled-bunch instabilities excited by the interaction of the particle beam with the vacuum chamber or with RF cavities can seriously limit the performance of circular particle accelerators. These instabilities can be cured by the use of active feedback systems based on sensors capable of detecting the unwanted beam motion and actuators that apply the feedback correction to the beam. The advances in electronic technology allow nowadays to implement feedback loops using digital systems.

Besides important advantages in terms of flexibility and reproducibility, digital systems open the way to the implementation of novel diagnostic tools and additional features that enhance the system operability and the quality of the beam.

The lecture is divided into three parts. The first part concerns some basic concepts about coupled bunch instabilities in storage rings with a theoretical introduction to feedback techniques. The second part deals with technical issues regarding feedback components, with some references to real feedback implementations. The last part focuses on digital feedback systems and in particular on digital processing, diagnostics capabilities and offline data analysis.

Presenter: LONZA, Marco (Elettra - Trieste)

Contribution ID: **25** Type: **not specified**

Multi Bunch Feedback Systems (cont.)

Wednesday 6 June 2007 12:00 (1 hour)

Presenter: LONZA, Marco (Elettra - Trieste)

Contribution ID: **26** Type: **not specified**

Real Time Control of Beam Parameters I

Thursday 7 June 2007 08:30 (1 hour)

Real time feedback systems always are a trade off between bandwidth, latency and noise.
System bandwidth is often not only dictated by the time structure of the beam signal, but also by latency considerations. The thermal noise floor relating bandwidth and noise power is only one design criterion. High bandwidth, low latency systems often have to compromise on the resolution of the analog to digital and digital to analog conversion as well as digital data width giving rise to discretisation noise in amplitude and time. An efficient system design needs an explicit model specifying the different types and locations of the noise sources. The lecture demonstrates the approach for existing systems, an orbit feedback and a bunch by bunch stabilization system, discusses choices for hardware and software and takes a look at how future technology trends will affect system design and layout.

Presenter: DEHLER, Micha (PSI)

Contribution ID: **27** Type: **not specified**

RF Application II

Thursday 7 June 2007 09:30 (1 hour)

see description in “RF Application I”

Presenter: Dr SCHILCHER, Thomas (Paul Scherrer Institute)

Contribution ID: **28** Type: **not specified**

Controls Integration I

Thursday 7 June 2007 11:00 (1 hour)

Presenter: SHEA, Tom (SNS)

Contribution ID: **29** Type: **not specified**

BI Application I

Thursday 7 June 2007 12:00 (1 hour)

Applications of digital signal processing to beam instrumentation

Most beam measurements are based on the electro-magnetic interaction of the fields induced by the beam with their environment. Beam current transformers as well as beam position monitors are based on this principle. The signals induced in the sensors must be amplified and shaped before they are converted into numerical values. These values are further treated numerically in order to extract meaningful machine parameter measurements.

The lecture will first introduce the architecture of an instrument and show, where in the treatment chain digital signal analysis can be introduced. Then the usage of digital signal processing will be presented using multi-turn intensity measurements, tune measurements and orbit and trajectory measurements as well as longitudinal phase space tomography as examples.
The hardware as well as the treatment algorithms and their implementation on Digital Signal Processors (DSPs) or in Field Programmable Gate Arrays (FPGAs) will be presented.

Presenter: RAICH, Uli (CERN)

Contribution ID: **30** Type: **not specified**

Real Time Control of Beam Parameters II

Friday 8 June 2007 08:30 (1 hour)

Presenter: DEHLER, Micha (PSI)

Contribution ID: **31** Type: **not specified**

Dynamic Effects in superconducting Accelerators and related technical solutions

Friday 8 June 2007 12:00 (1 hour)

Due to the decay of persistant currents in superconducting magnets any cycling superconducting accelerator will suffer from dynamic effects with direct impact on machine parameters like closed orbit, tune, coupling, chromaticity or in a wider sense with direct impact on beam stability. The seminar will describe in a simple approach the phenomenon of persistent current decays and the resulting consequences for the LHC collider. Technical solutions to compensate the problem will be listed (cycle design, RT feedback on beam parameters, power converter control).

The main part of the lecture will be focused on the sophisticated design of the LHC power converter control using DSP techniques.

Presenter: SCHMICKLER, Hermann (AB-BDI)

Contribution ID: **32** Type: **not specified**

Controls Integration II

Friday 8 June 2007 09:30 (1 hour)

Presenter: SHEA, Tom (SNS)

Contribution ID: **33** Type: **not specified**

BI Application II

Friday 8 June 2007 11:00 (1 hour)

see description in “BI Application I”

Presenter: RAICH, Uli (CERN)

Contribution ID: **34** Type: **not specified**

Introduction to afternoon courses

Friday 1 June 2007 14:30 (1 hour)

Presenter: SCHMICKLER, Hermann (AB-BDI)