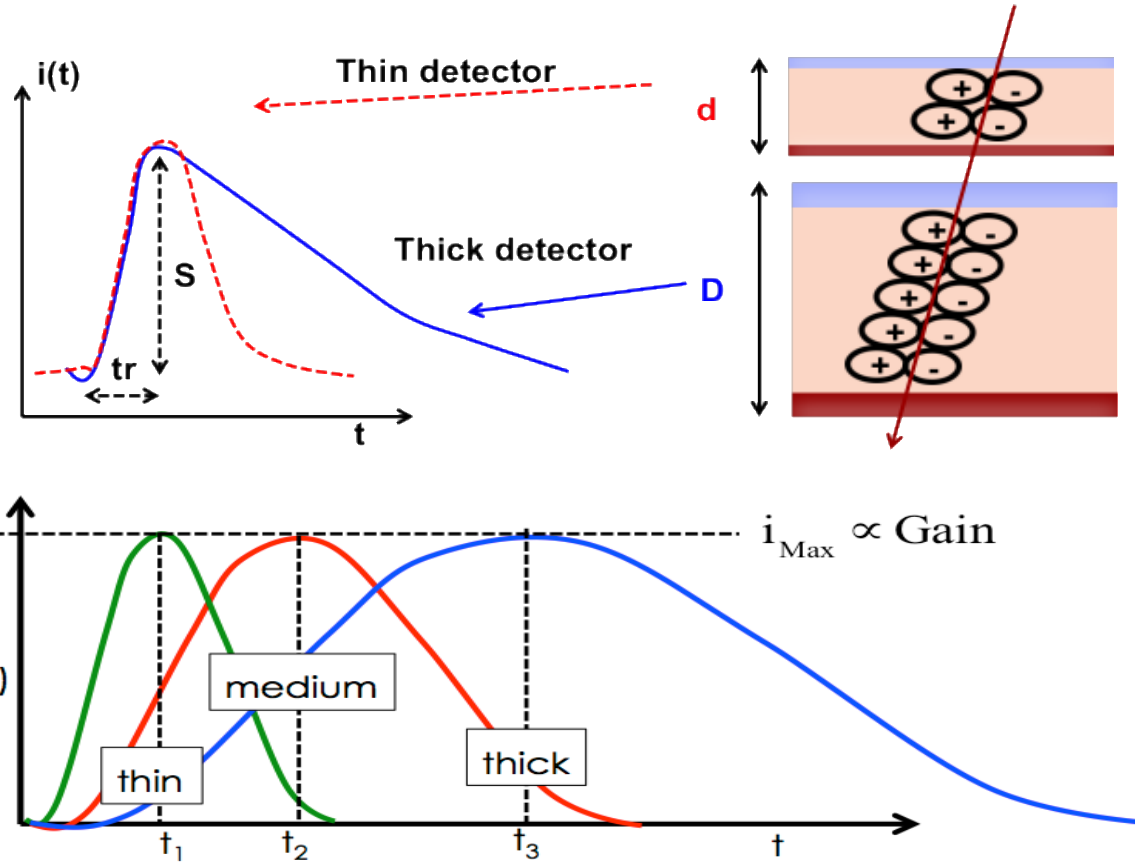
ATAR Electronics Topics

1) Sensor and signal characteristics: Proposed sensor is an 120 micron thick AC-LGAD. Would like thinnest sensor that is consistent with spatial constraints. 120 micron thickness determined by need to place many sensors with no gaps in coverage for Pioneer.

2) Work on readout for sensor. Will cover mostly SCIPP collaboration with other groups.

3) Some challenges for case of Pioneer and possible next steps.

Detector Thickness and Signal Shapes



Typical signal characteristics versus detector thickness for silicon detector with saturated drift velocity.

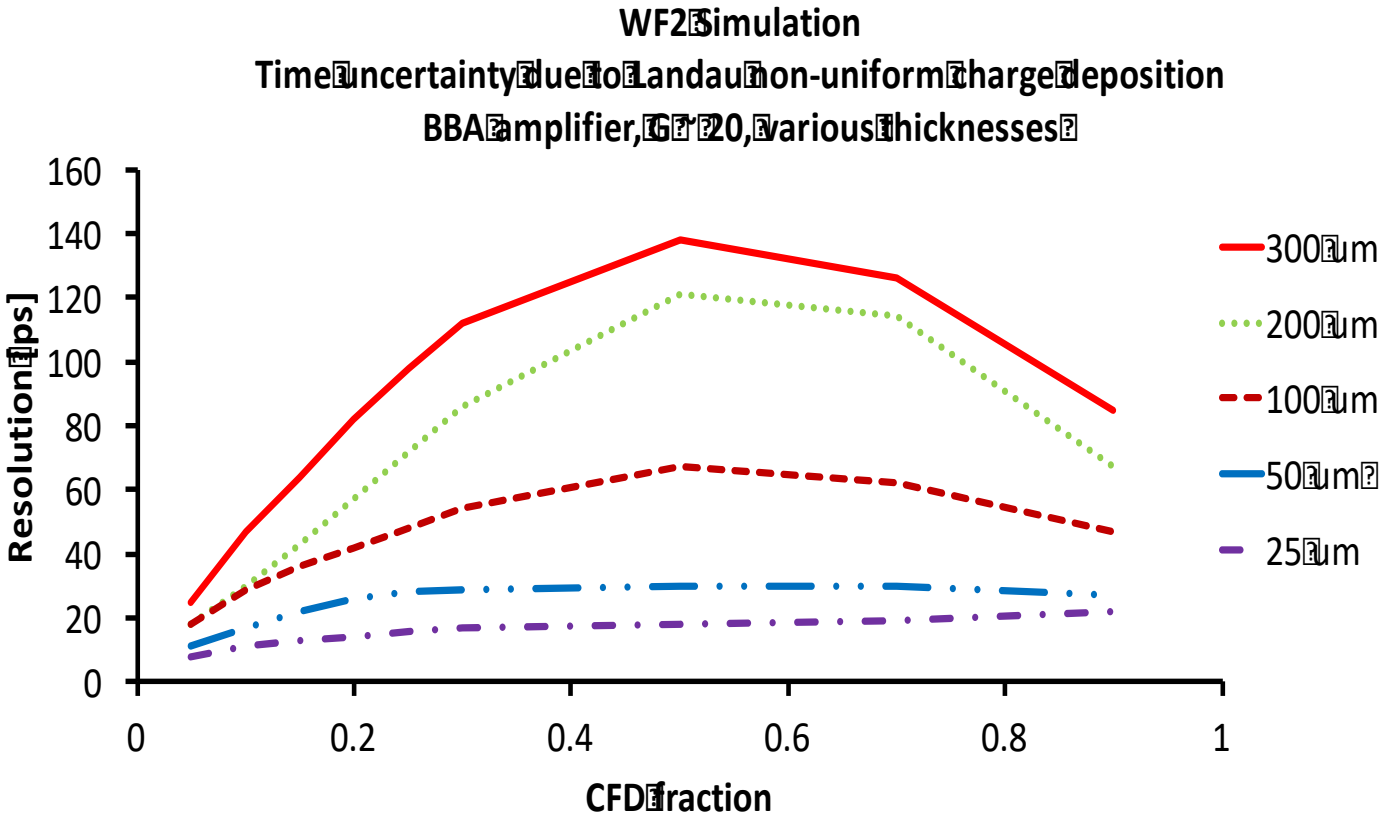
Conventional silicon detector: Rise time similar for thick and thin, same slew rate.

Detector with a gain of 20: Rise time (and slew-rate) are different for thick versus thin. Rise time ~ electron collection time, is proportional to the detector thickness. Makes thin detector better choice for timing. ATAR choice:120 microns. Results in ~ 1.5 nsec pulse rise-time.

Sensor Design Issues

The AC-LGAD strip detector behaves like a ladder network of distributed R's (from the n+ sheet) and C's (from the metal readout strip) driven by a current source of the detector. The signal sharing is determined by the impedances of these elements and to minimize the sharing we would like a large sheet resistance for the n+ and a large capacitance of the readout strip to the n+ requiring a thin oxide separating the n+ and the metal strip. Would however like to minimize the strip capacitance to the back plane. Also would like to minimize the resistance of the metal strip itself. These are design considerations for the sensor, which then impact its performance when combined with the electronics.

Landau Fluctuations: Large Contributor to the Time Resolution



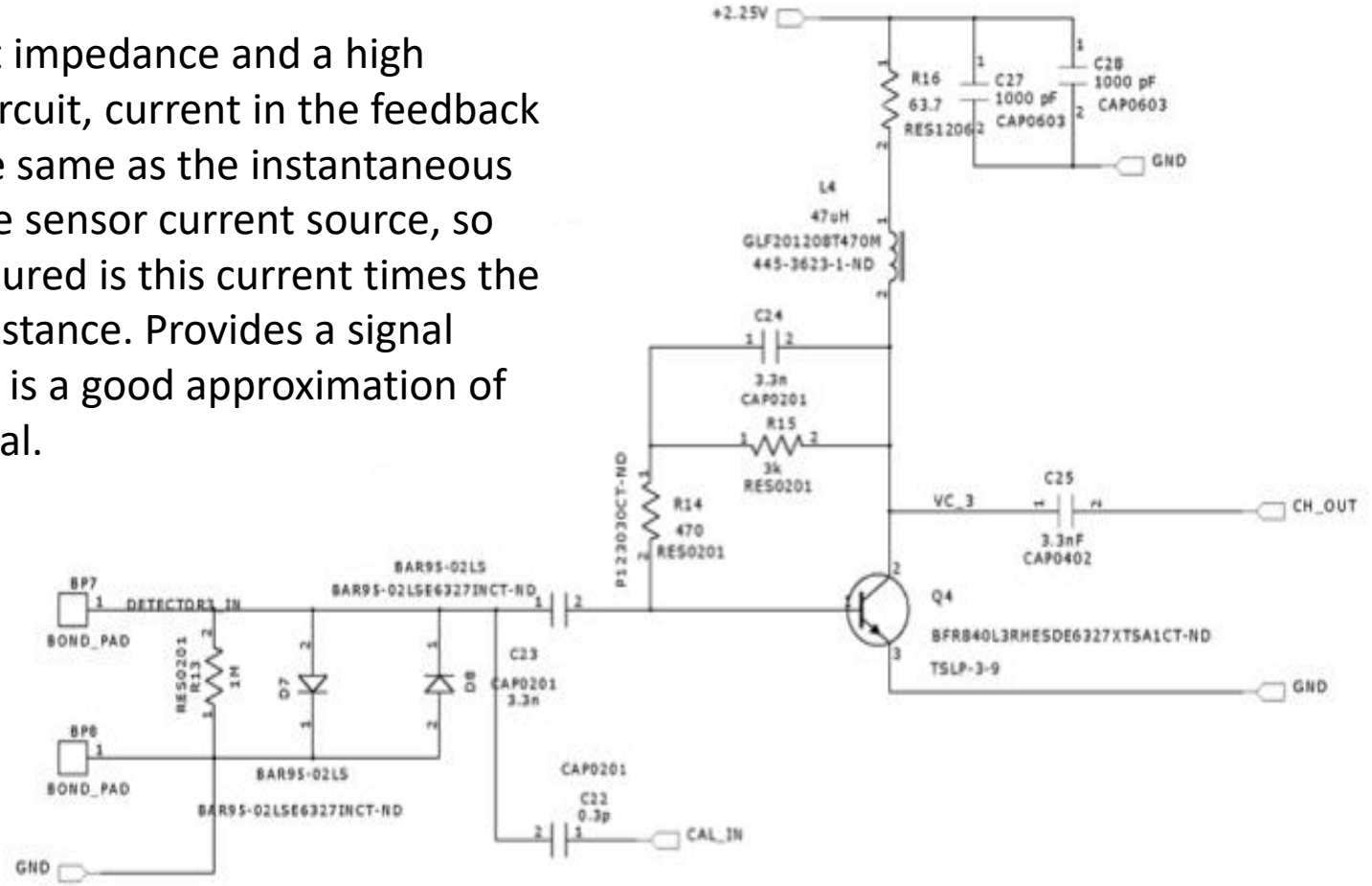
Contributions of Landau fluctuations to the time resolution as a function of a Constant Fraction Discriminator value for different detector thicknesses. Based on simulations and measurements for detectors of 20 – 50 micron thickness. For the ATAR can expect ~ **75** ps from Landau fluctuations.

Other Major Contributor to Timing Resolution: Electronics Jitter.

The second major contributor to the timing resolution is the jitter arising from the noise in the electronics. This is given by the signal rise-time/signal-to-noise ratio, where the signal is given by the peak height. For a rise-time of 1.5 nsec a signal-to-noise of at least 30 is required to get a jitter contribution of 50 psec, which adds in quadrature to the Landau term. A value of 50 ps would leave the Landau fluctuations as the major contribution to the timing resolution and removes the demand to go for the most demanding performance of the electronics.

UCSC Trans-Impedance Amplifier – uses 470 ohm Feedback Resistor. First circuit explicitly designed for LGADS.

For low input impedance and a high bandwidth circuit, current in the feedback resistor is the same as the instantaneous current of the sensor current source, so voltage measured is this current times the feedback resistance. Provides a signal whose shape is a good approximation of detector signal.



To get a large enough signal for this circuit typically use also a x10 post-amplifier. To avoid this recent circuits typically use a feedback resistor of a few thousand ohms. All recent developments use the trans-impedance configuration.

ASICs under Test at SCIPP

Three ASICs are being produced which will emphasize different performance goals. Here we leverage our partner's familiarity with the technology and our experience with sensors and readout systems. Also electronics in advanced development for the ATLAS and CMS experiments, performance in line with what we expect. None have been designed primarily with Pioneer in mind, they have typically aimed at thinner sensors. They can, however, illustrate some of the issues.

Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC*	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASROC**	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Simulations final Layout Board design

* HPSoC : High Pitch digitizer System on a Chip,
(L. Macchiarulo et al.: "Design of HPSoC - a 10GSa/s Waveform Digitizer for Readout of Dense Sensor Arrays", submitted to IEEE NSS-MIC 2022)

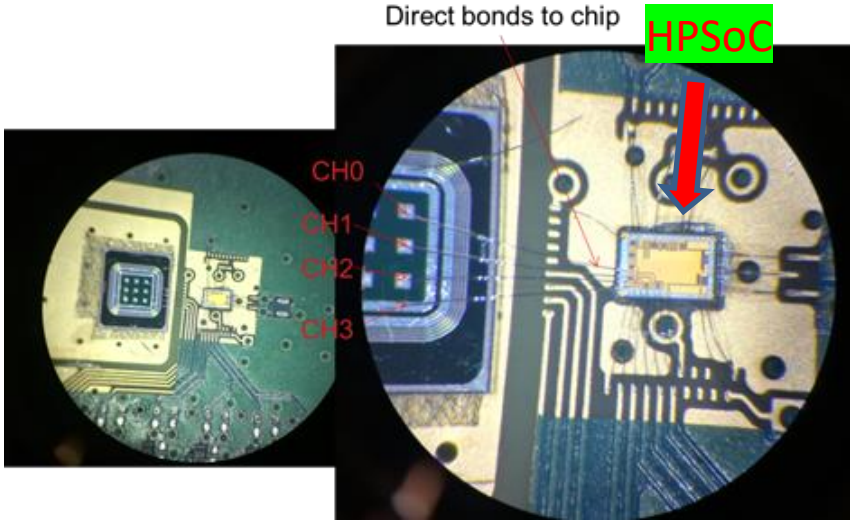
** ASROC: A custom amplifier/discriminator IC designed for AC-LGAD readout,
(G. Saffier-Ewing et al., "ASROC: A custom amplifier/discriminator IC designed for AC-LGAD readout " , TWEPP 2021)

For the CMOS amplifiers, to achieve a large transconductance needed for low input impedance, the front transistor requires a current ~ 1 mamp. Combined with a voltage of ~ 1 volt, gives a power ~ 1 mWatt per channel. Typical number for all the CMOS VLSI amplifiers to date.

Preliminary Test Results with HPSoC (NALU Chip)

The HPSoC was tested with fast calibration pulses to verify the performance of the first stage, the Trans-Impedance Amplifier (TIA).

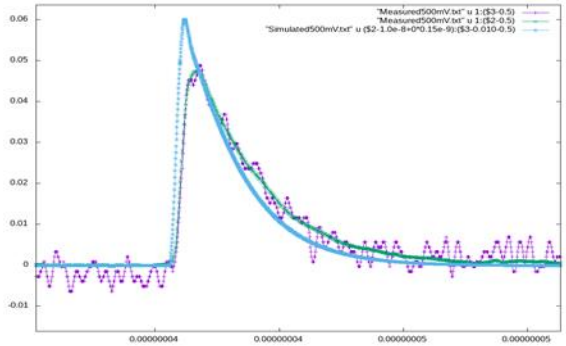
It was then mounted on a test board and wire bonded to a 60 um thick AC-LGAD pad sensor and tested with a β souce.



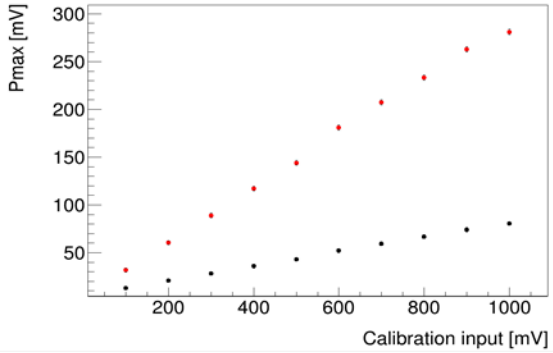
The expected analog performance of the ASIC can be derived from the analysis of the pulse shapes.
The contribution to the time resolution due to the electronics is the jitter

Jitter = rise time / (S/N)

Preliminary Test Results with HPSoC



Measured and simulated behavior with a fast Calibration Input Pulse.

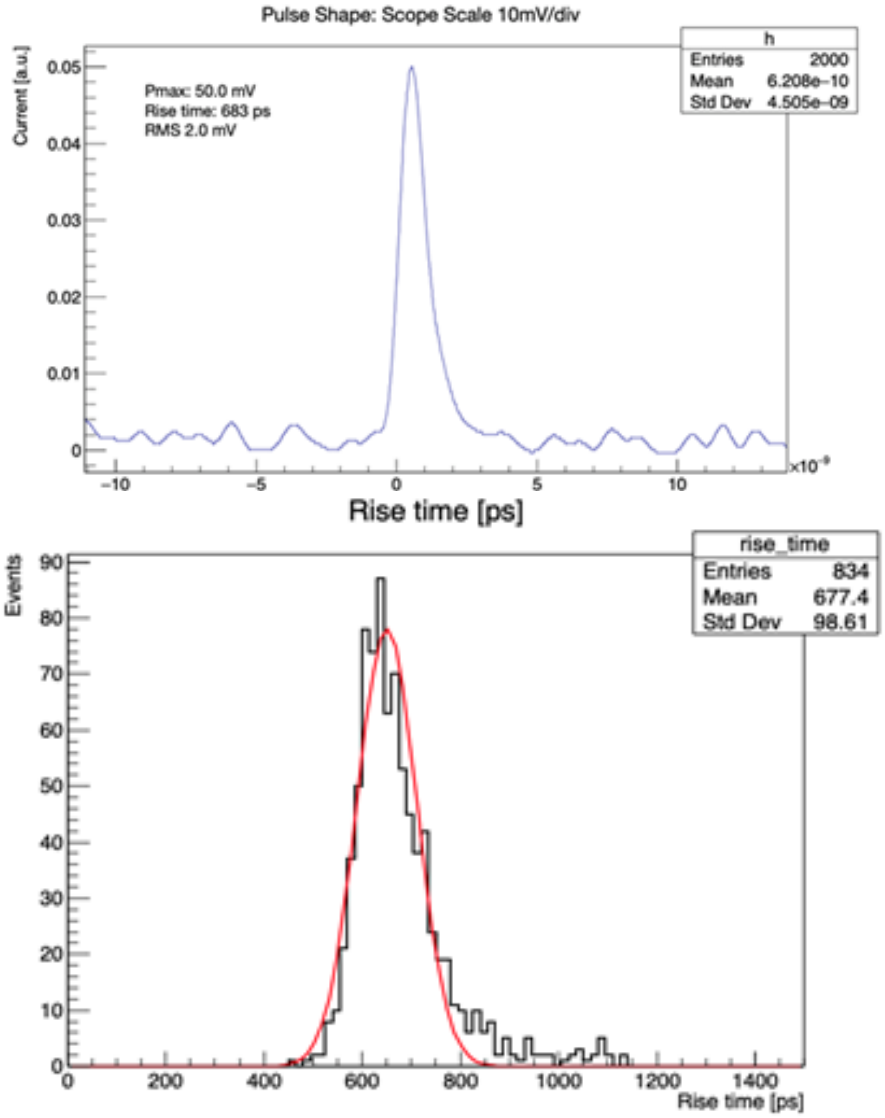


Calibration Curve with (red)
and without(black) 2nd gain Stage

Note there are two versions of the amplifier, a single stage (black) and two stage (red). The two stage amplifier provides a higher gain but not a lower jitter value.

Abstract & Summary submitted to TWEPP 2022

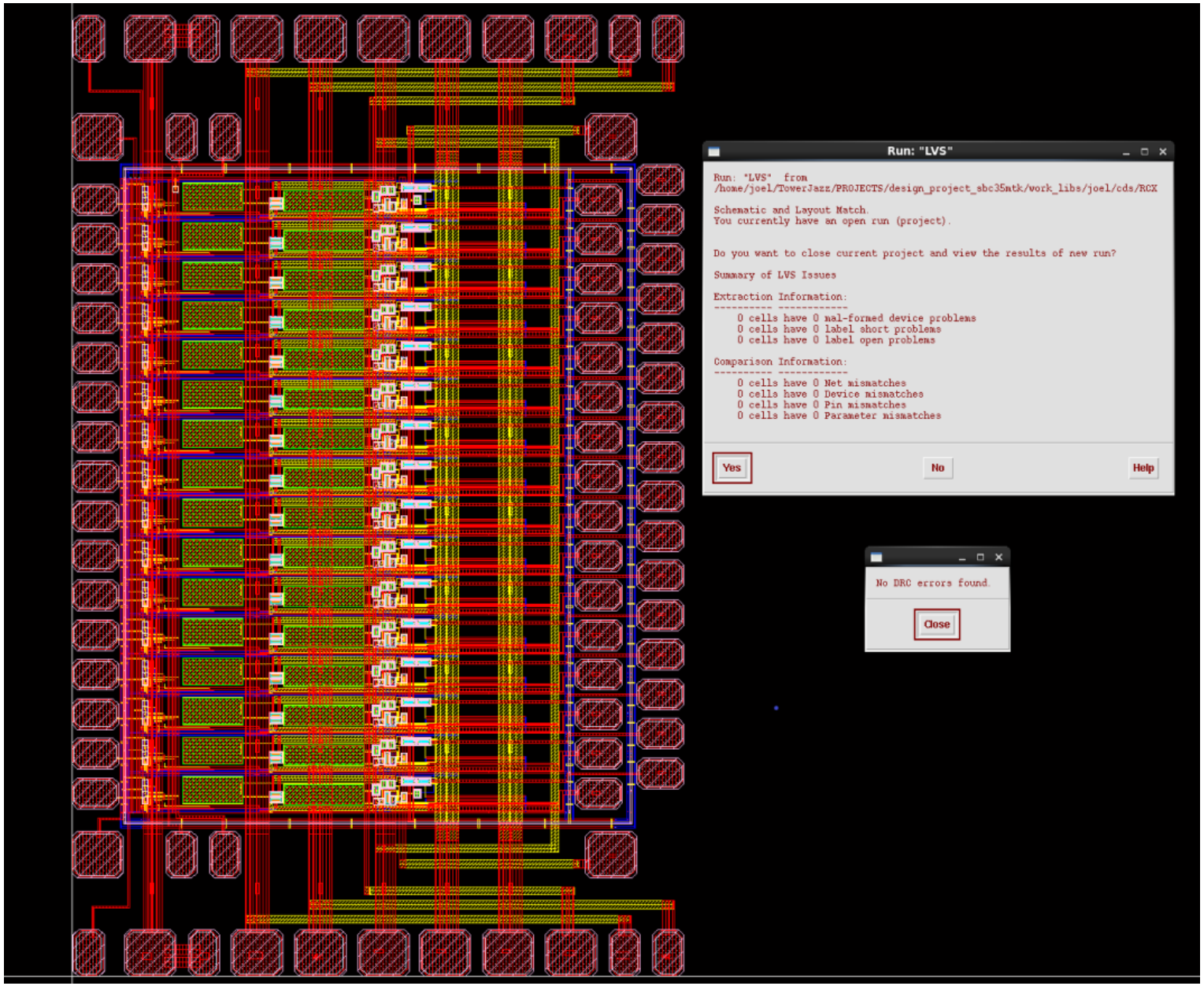
Very Preliminary β Test Results with HPSoC



Trise (60 um thick detector) = 677 ps.
Noise = Sqrt(RMS^2-$ScopeNoise^2$) =1.7 mV
(RMS = 2 mV, Scope Noise = 1mV)

Abstract & Summary submitted to TWEPP 2022

Layout of SiGe Amplifier (Anadyne)

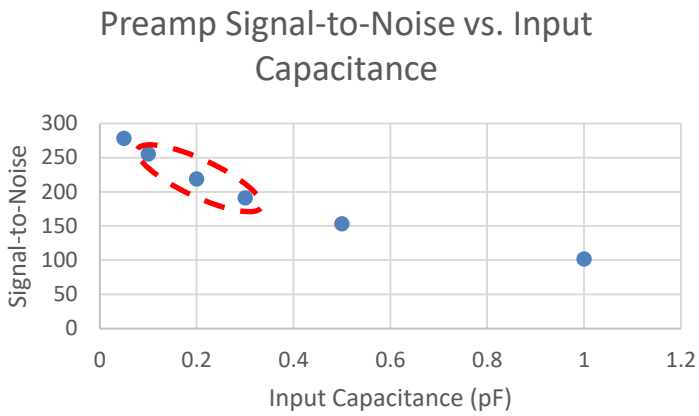


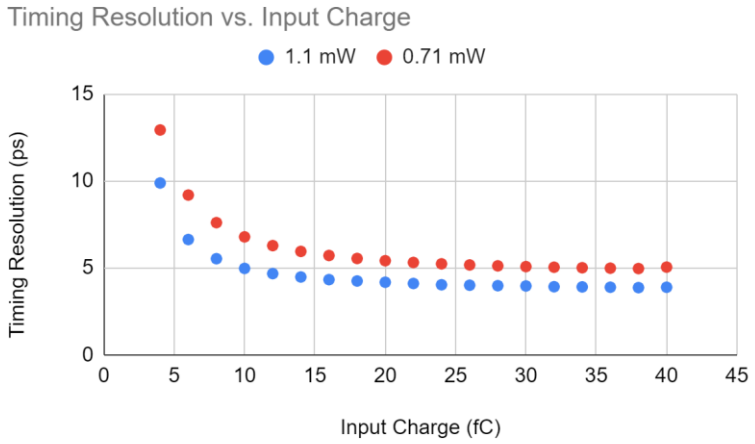
Anadyne ASROC Simulated Performance

Input capacitance increases noise and rise time. Signal-to-noise for 10 fC pulse and 710 uW/channel is very large for pad detectors with low input capacitance. Signal simulated is for 20 micron thick sensor. Not yet looked at how this circuit would perform for the Pioneer case.

Jitter vs input Q for two Power Settings (preamp + discriminator) (C_{in} = 200 fF)

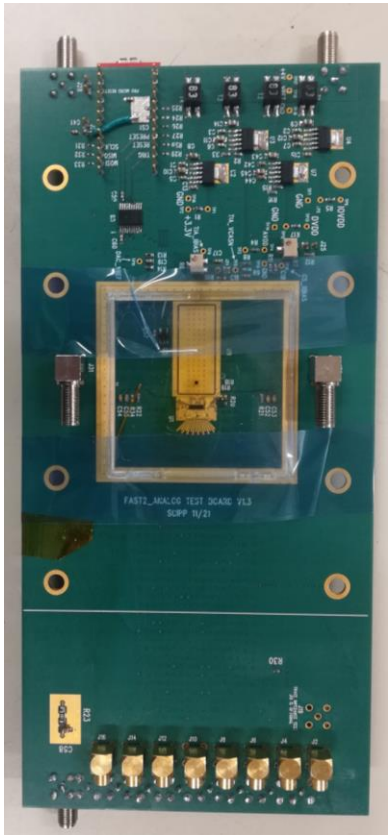
	Power [mW/channel]	
Input Q [fC]	0.71	1.1
4	13 ps	10 ps
5	11 ps	8 ps
10	7 ps	5 ps

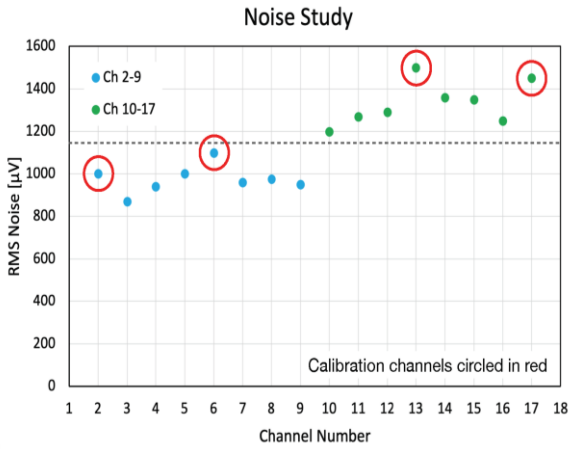


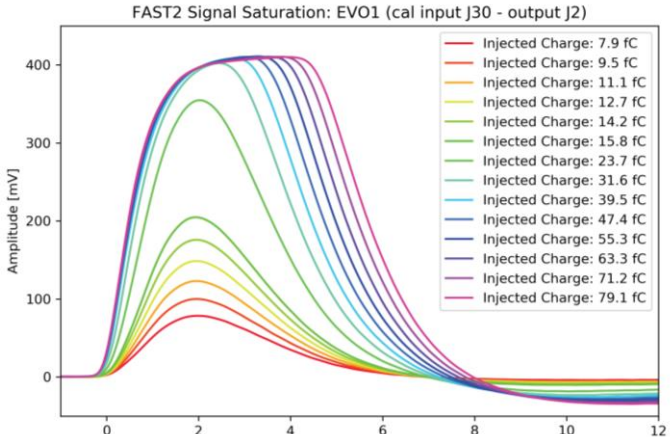


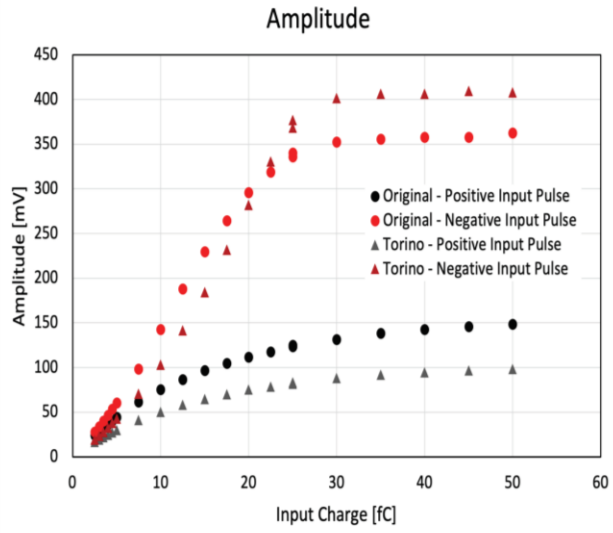
At low signals, trade-off of time resolution and power. Also illustrates the strong effect of the detector capacitance on the performance.

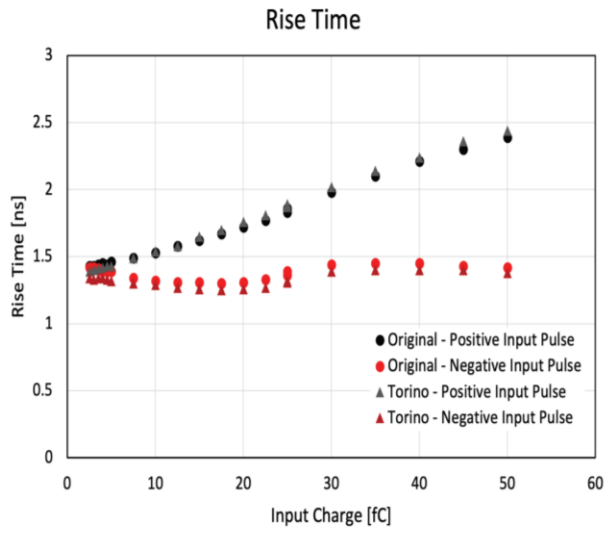
What about ASIC with larger Risetime: FAST2











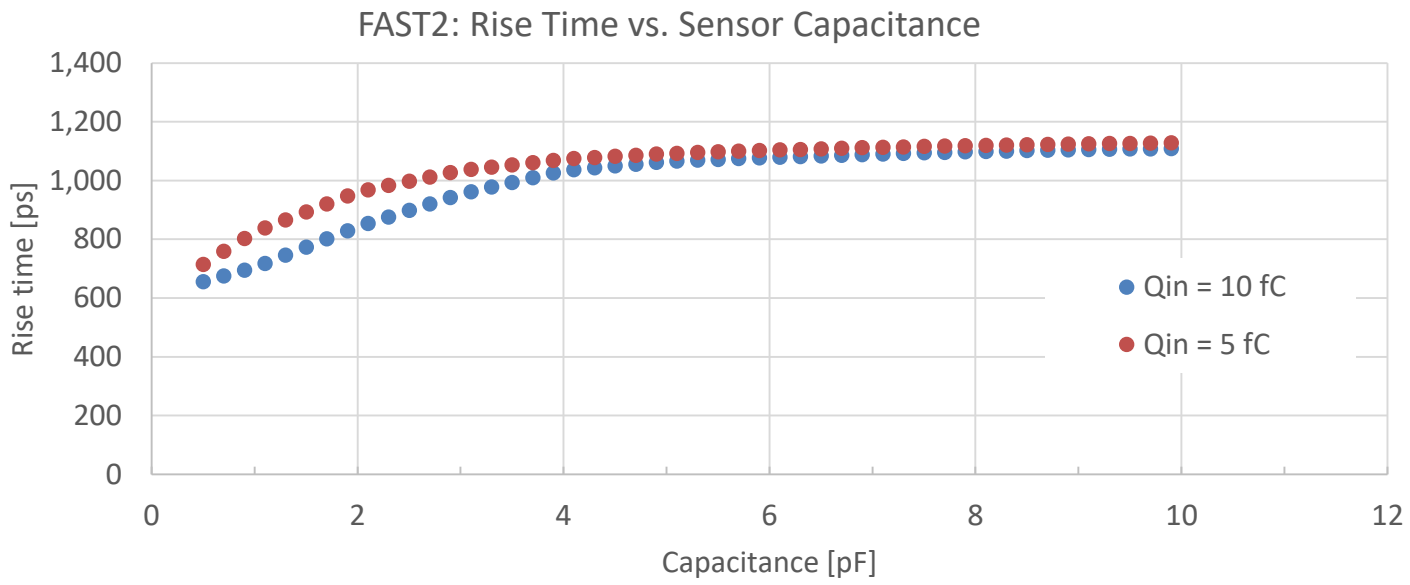
With C ~ 400 fF:

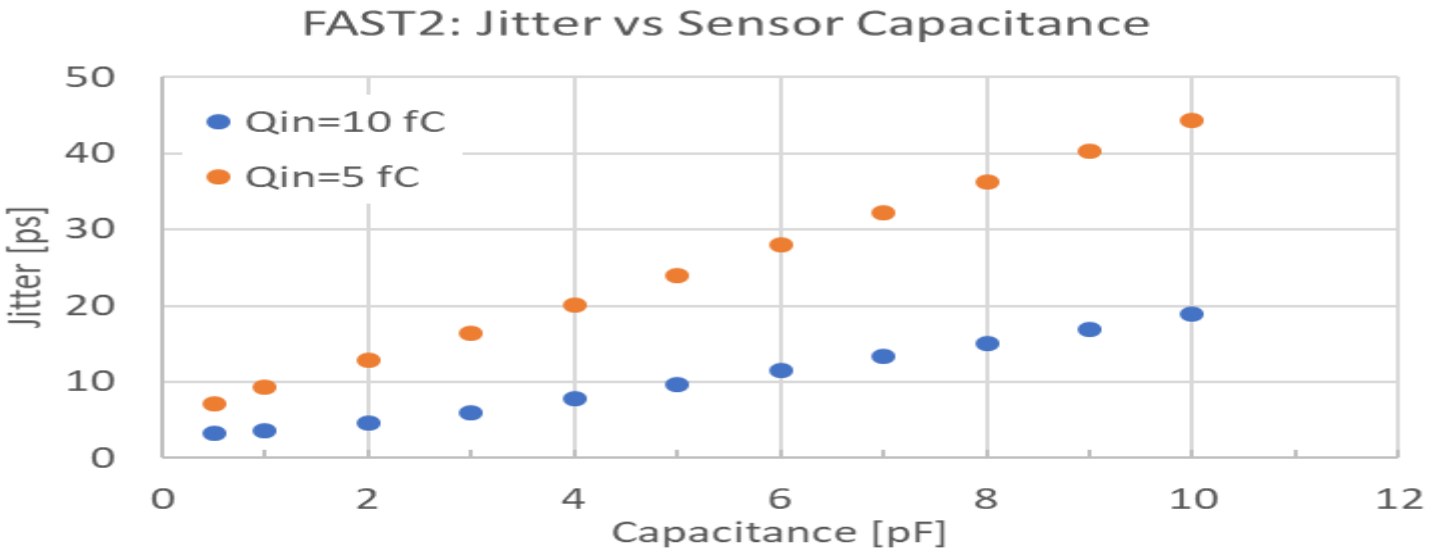
Jitter @ 20 fC: 1.26/(281/0.95) = 4 ps

Jitter @ 10 fC: 1.3/(150/0.95) = 8 ps

Chip has two amplifier designs (Called Evo1 and Evo2), both have two stages of amplification, give different noise values measured above. All data with 50 micron thick sensors. Note increased time duration of saturated signal with input charge.

FAST2 Simulation





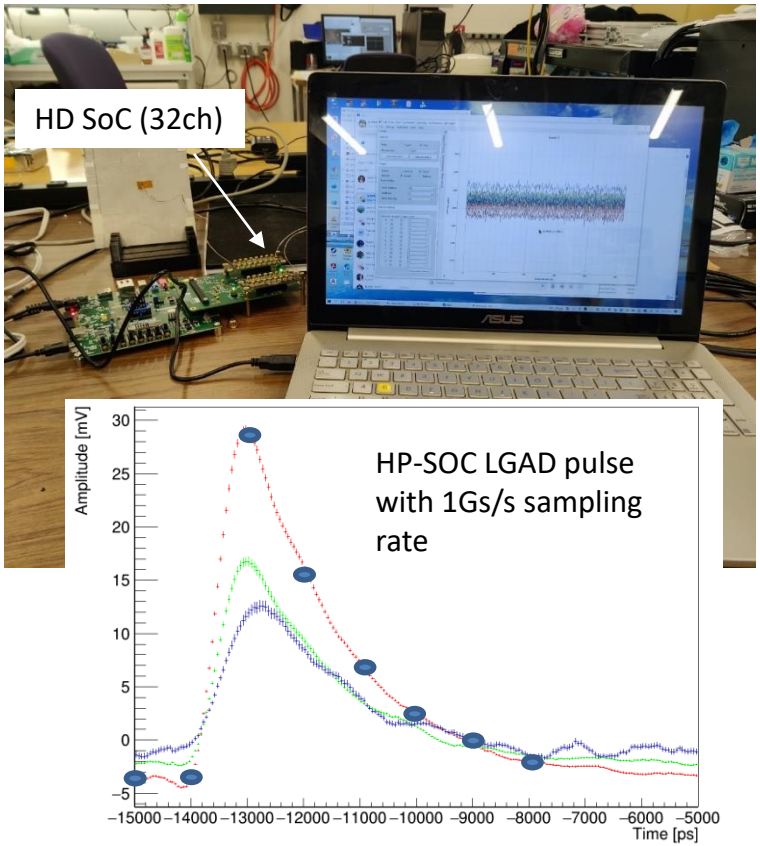
Chip Status:

Have in hand the NALU and FAST chips. We plan to map out performance with sensors and various capacitance values. For NALU chip we expect next year to have also the backend readout of the full waveform. This is very important since needed for Pioneer. Would also like to see if we can use the full signal information to improve the resolution limitation coming from the Landau fluctuations. FAST3, improved version of FAST, also due next year. FAST is the furthest along available chip, will be used for prototype Pioneer studies.

Almost ready for submission of the Anadyne chips (will be two, a low power and high power version). Next year map out performance with sensors and various capacitance values. Want to verify the simulated performance advantages in power and signal-to-noise for the Si-Ge technology.

Note: We expect the Pioneer strip sensor to have a capacitance ~ 1.5 pF, with flex perhaps doubling this. These numbers need to be determined and depend on strip pitch and metal width.

Digitizer chip (back end)



- Back-end is a digitizer chip
- ~5000 channels to be digitized
  - Commercial solution readily available (e.g. DRS4 chip), however it would be too expensive
  - Not all channels can be digitized for each event (data rate too high)
  - Same dynamic range as the front end (solved if front end chip has gain/no-gain or log settings)
- → need ad-hoc chip specific for PIONEER
  - Production can be adapted to our needs

- HD-SoC from Nalu Sci. in evaluation at UCSC
  - 32 channel, 1Gs/s digitizer chip (up to 2Gs/s possible)
  - Asymmetric single channel trigger: if one channel is over threshold is triggered or can trigger the group of 8 channels
  - Digitization rate (to add)
- To be studied: is 1Gs/s enough for pulse separation and good performance?

Future Needs

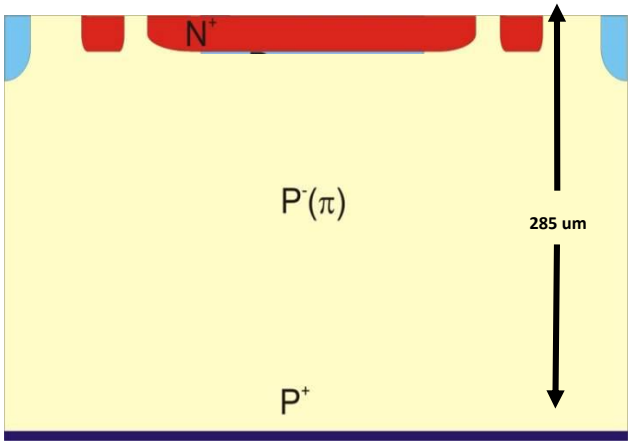
- Need to establish a Pioneer specific electronics effort. Most likely technology is TSMC 65 or 130 nm CMOS. Front-ends pretty well understood and HPSoC may offer a good choice for backend pulse digitization. Bandwidth of front-end can probably be reduced somewhat with thicker sensor to lower noise compared to requirements stemming from 50 micron thick sensors, which determined previous designs.
- However a significant issue is the dynamic range of 100 between stopping particles and mips from positrons. No other application has had this problem. One approach would be an amplifier with a non-linear response (for example logarithmic amplifier) but this is probably a major development project. A simpler approach would be to send out an unamplified and amplified signal for each strip. Doubles the backend channel count. Have to avoid a large dead-time from the large signal saturating the amplifier. Important for recognizing decays in Pioneer.
- Have to be sure that the chip developed can drive a reasonably long flex and develop the DAQ system to receive the signals.
- Would be good to have a system engineer to lead this work. Should work closely also with group developing the sensor.

Backup Slides:

Low-Gain Avalanche Detectors (LGAD)

"Simple" extension of silicon detector results in perfect sensor for timing

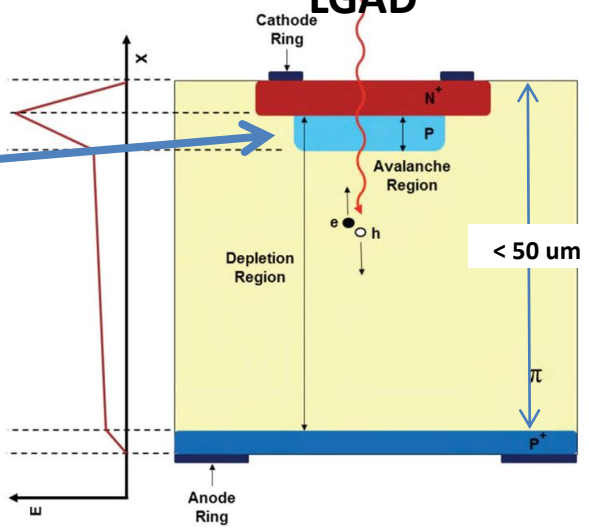
N-in-p PIN



Create **high field**
by introducing
gain layer
to increase signal

Reduce t**hickness**
to decrease
rise time

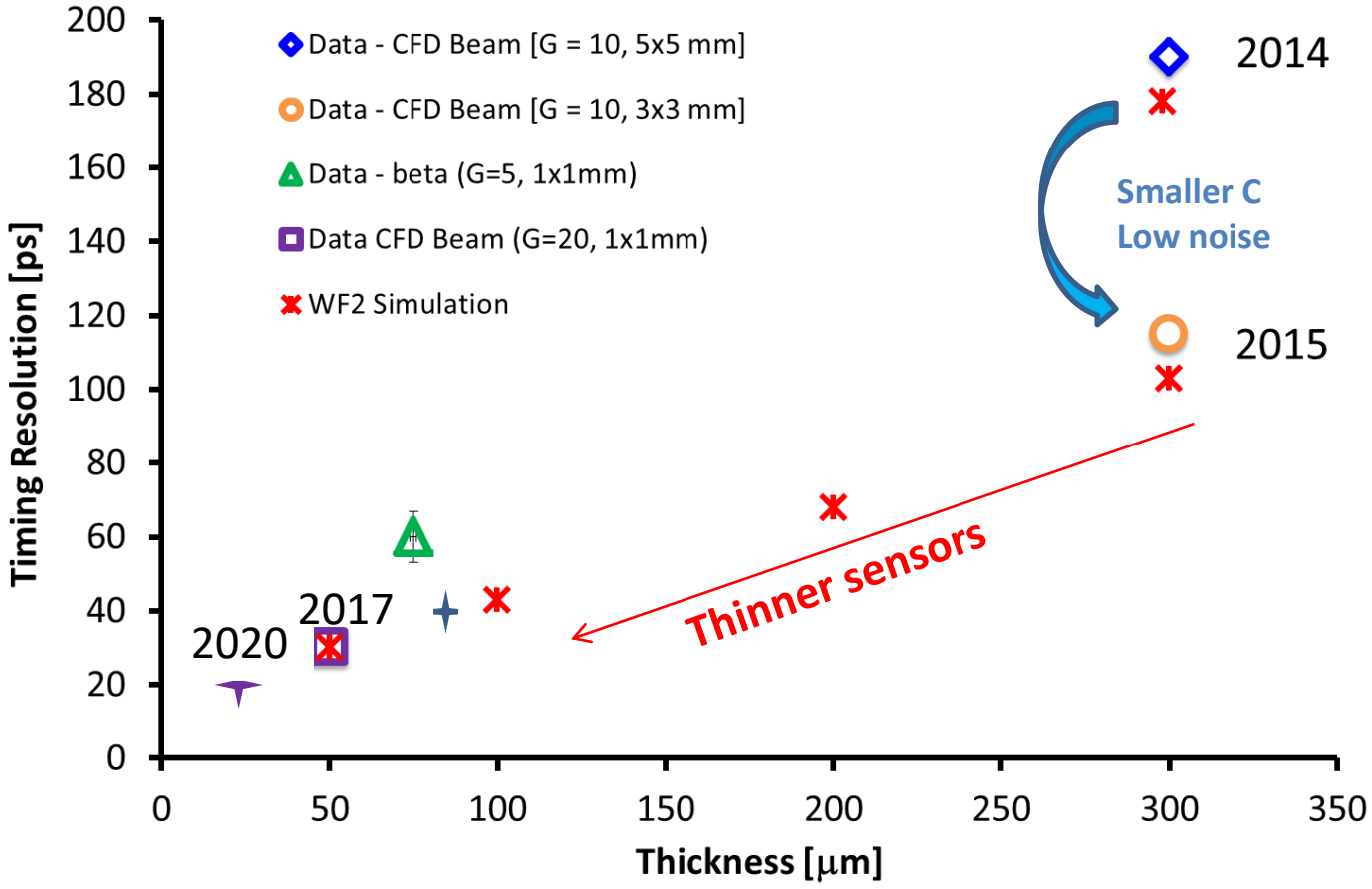
LGAD



LGAD have large and fast signals

G. Pellegrini *et al.*, Technology developments and first measurements of LGAD for high energy physics applications, Nucl. Instrum. Meth. A765 (2014) 12 – 16.
H.F.-W. Sadrozinski, A. Seiden and N. Cartiglia, 4D tracking with ultra-fast silicon detectors, 2018 Rep. Prog. Phys. 81 026101.

Trend of Time Resolution



The temporal resolution as a function of LGAD thickness is well simulated by WF2.

F. Cenna, et al., "Weightfield2:", NIM A796 (2015) 149