Overview of BNL silicon sensor capability

Gabriele Giacomini

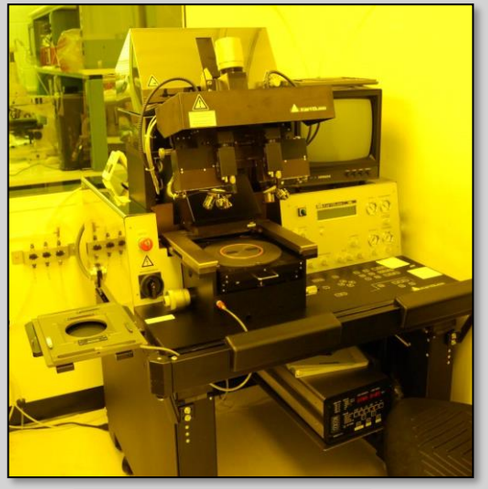
giacomini@bnl.gov

October 7th, 2022

Class-100 silicon clean room

- Dedicated to silicon – while other BNL clean rooms are used for germanium, diamond, selenium, high-Z
- Process flow and design highly customizable
- Fast turn around

Furnaces for dry oxidations and annealings



Double-sided mask aligner

Wet bench (HF, RCA I & II, piranha, polyetch, …)

Sputtering (Al, Al1%Si, Ti)

Laser dicing

+ dry etching and thin films deposition at CFN (user facility at BNL).
Capabilities to outsource:

- Ion implantation
- Polysilicon deposition
- Wafer fabrication and photomask production

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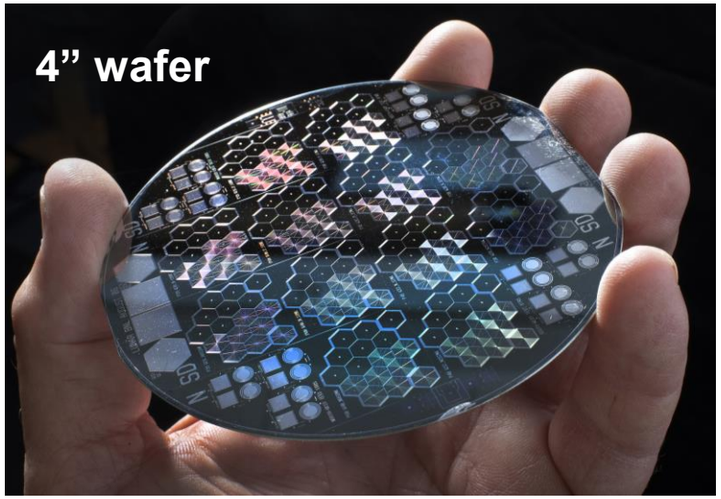
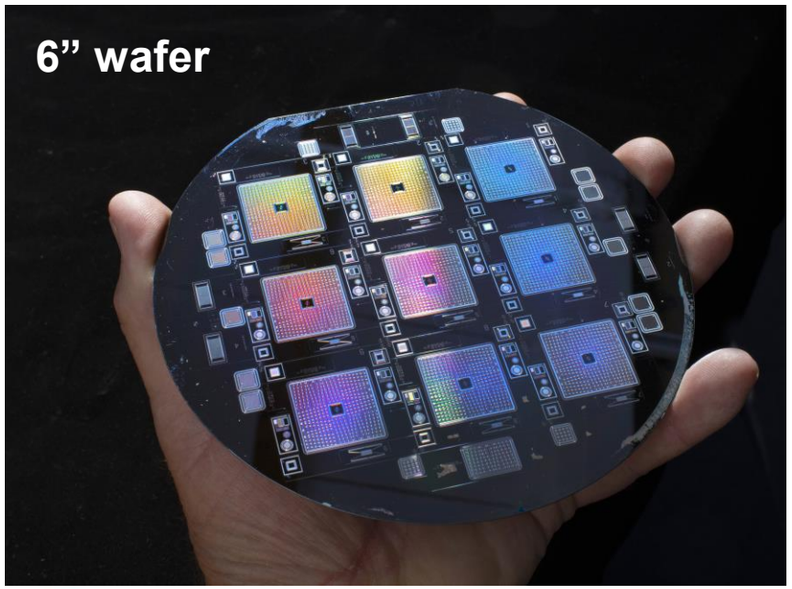
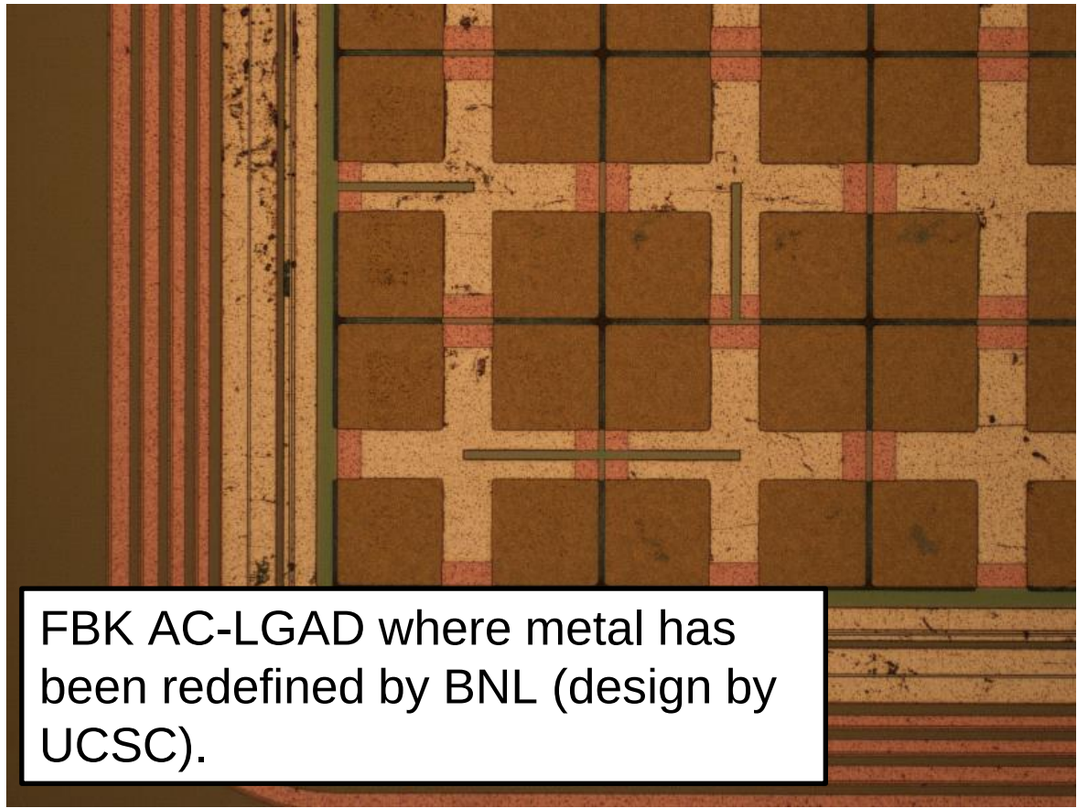
Silicon wafers from 1” to 6”

The process in clean room allows great flexibility in terms of substrate dimensions.
Usually 4” wafers are processed but we can even process small pieces (lithos included).







FBK AC-LGAD where metal has been redefined by BNL (design by UCSC).

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Fabrication on 120um thick 3” wafers

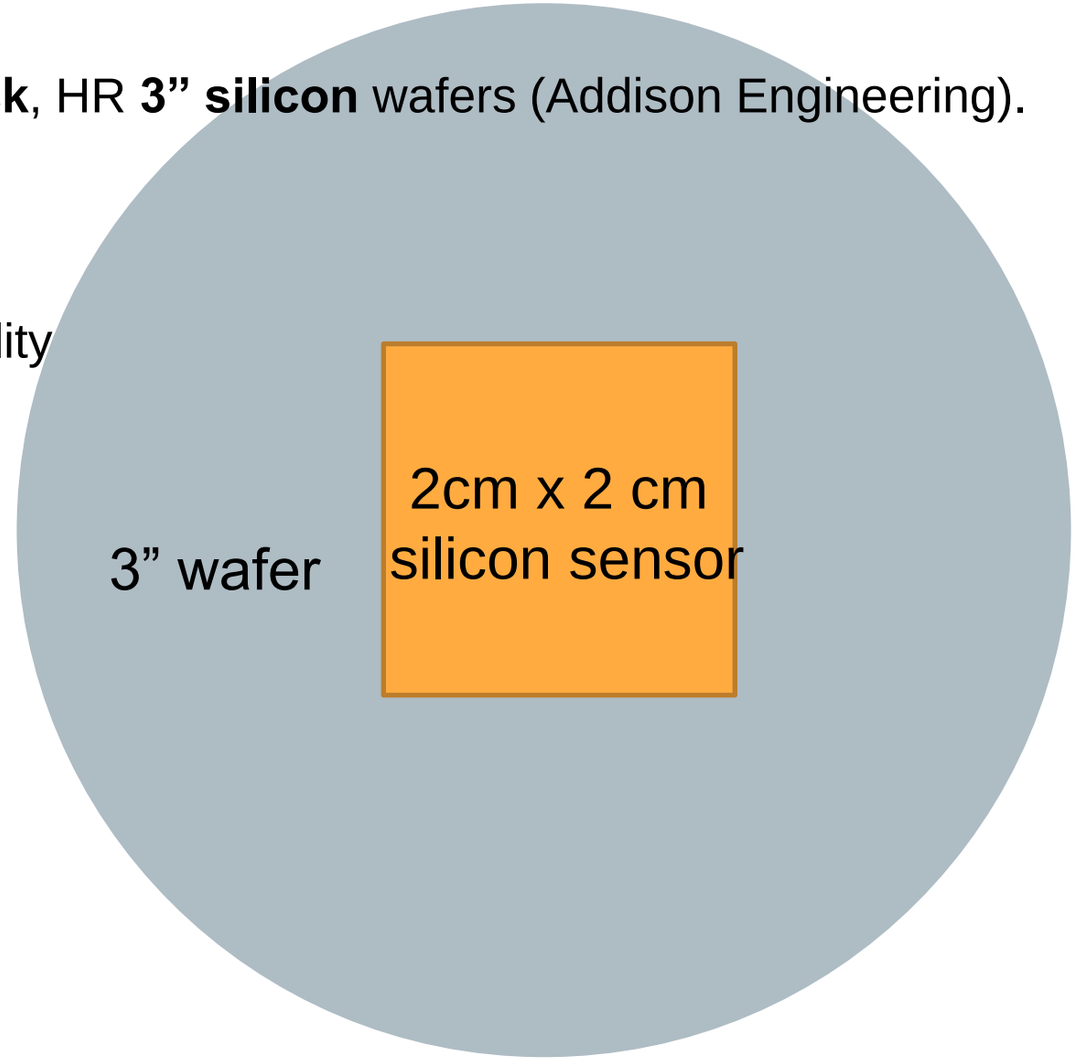
BNL has past experience in handling 3” 120um thick wafers.
Fragility of wafers is the issue here.

→ LDRD just started:

Recently placed an order for **120um thick**, HR **3” silicon** wafers (Addison Engineering).

plan to fabricate double-sided strip //
double-sided AC-LGAD
to put under test current handling capability

<u>If successful, 50 layers for ATAR look feasible</u>



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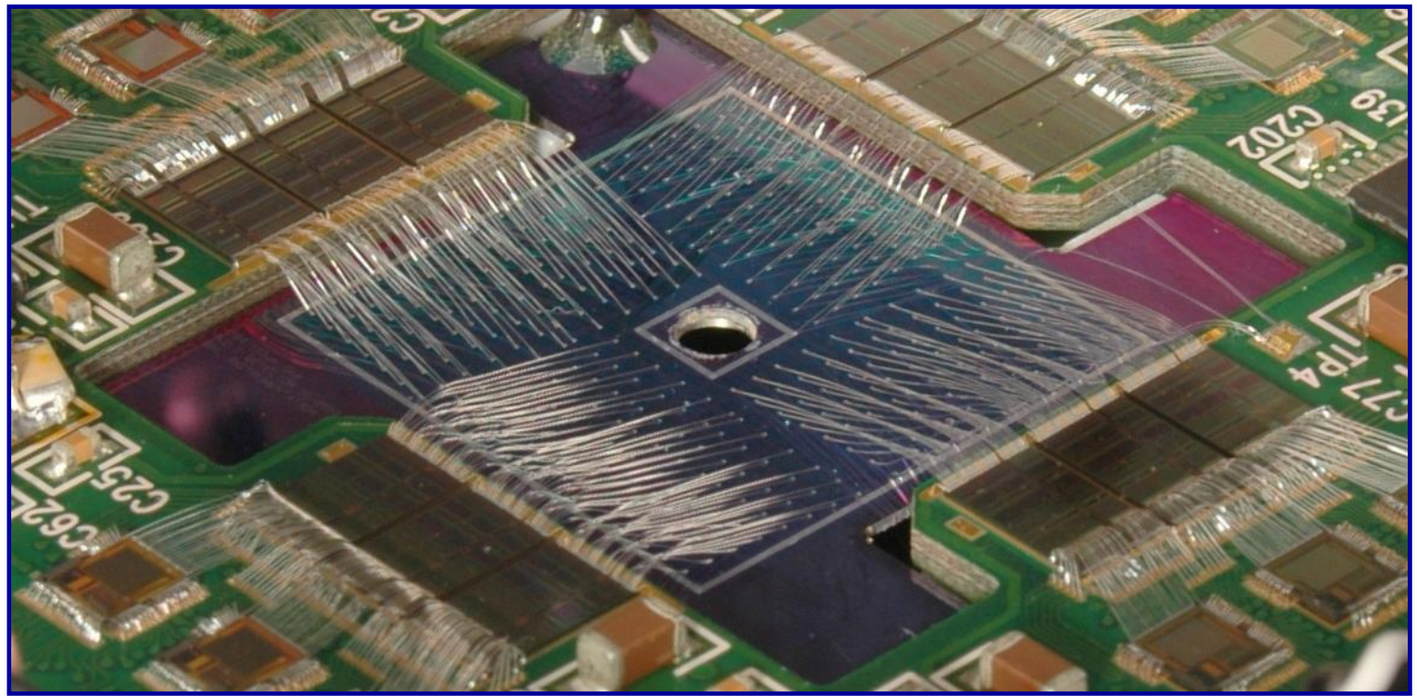
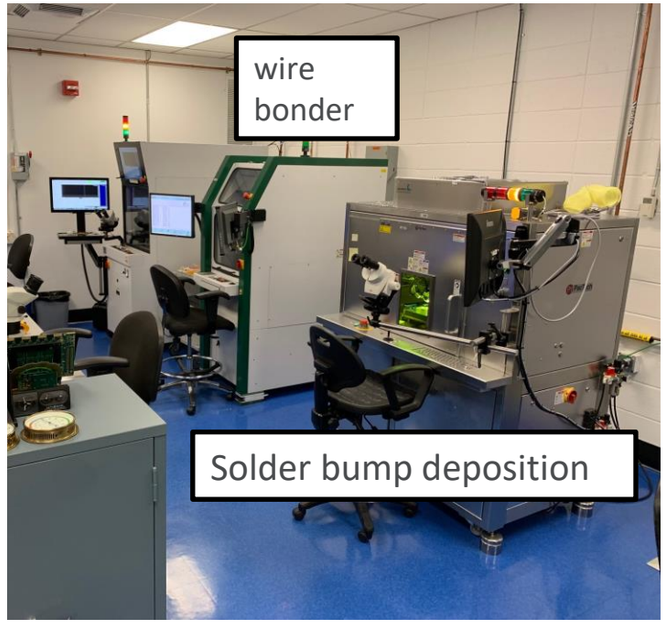
Interconnection lab

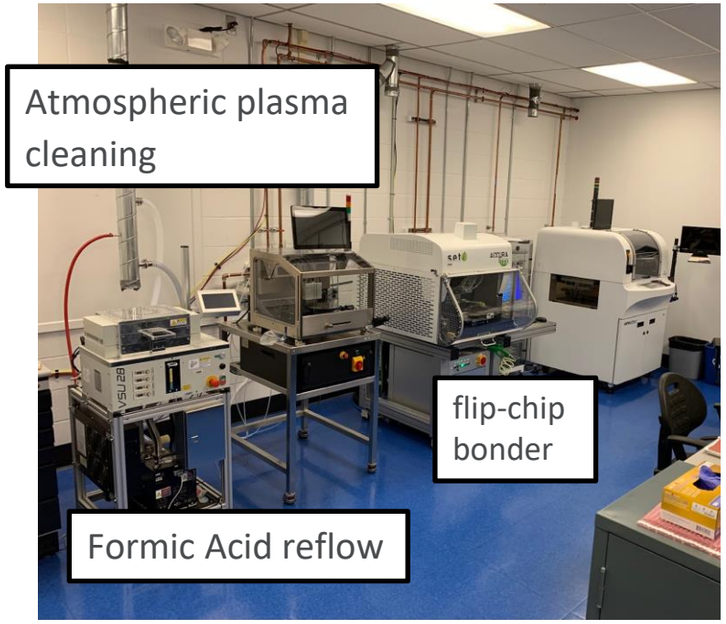
Wire-bonding of intricate detectors

Maia microprobe array: low-noise high-rate detector for fluorescence imaging at synchrotrons



Bump-bonding





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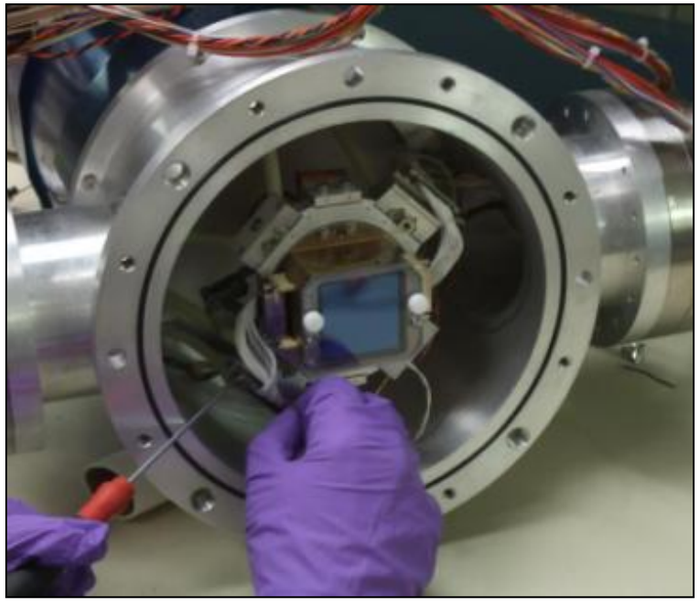
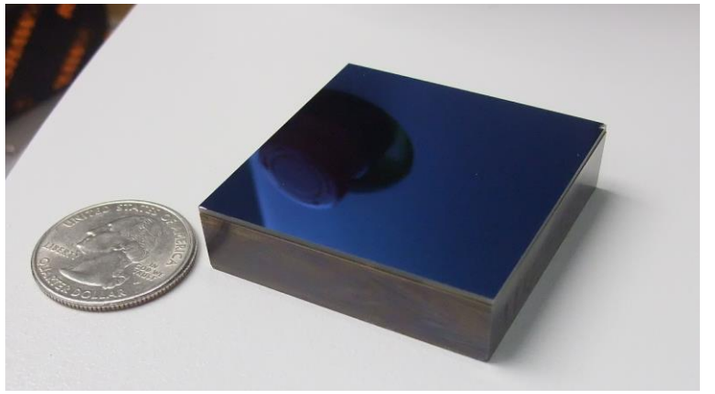


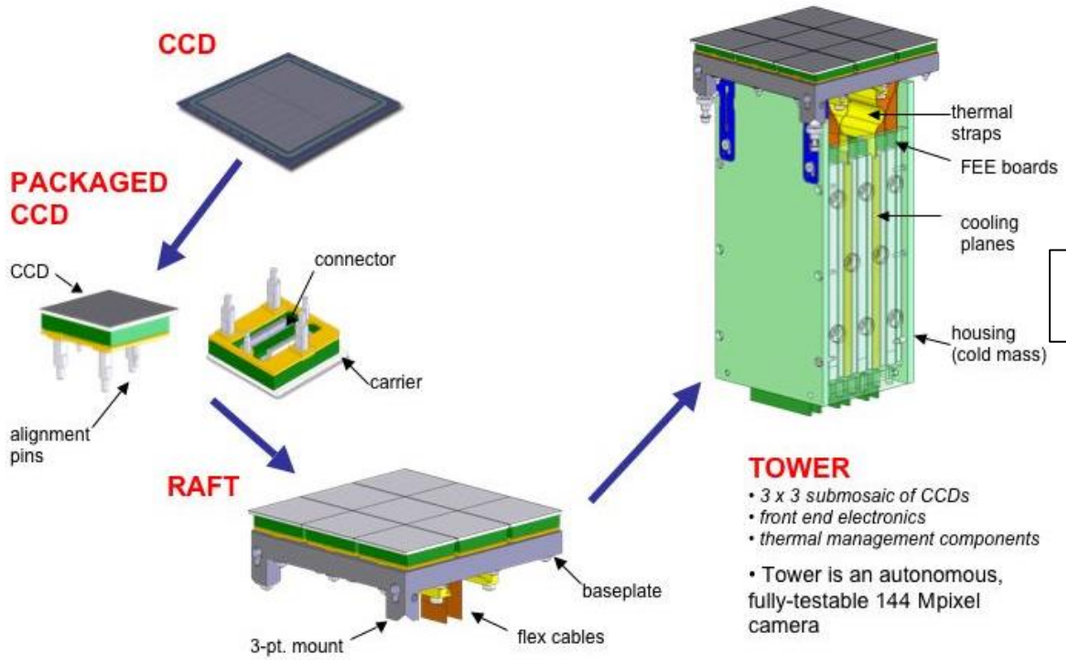
LSST Science Rafts



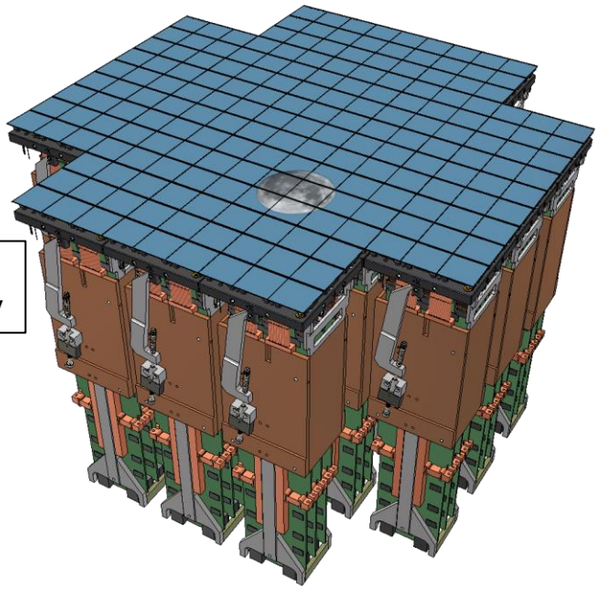
CCD for Vera C. Rubin observatory

Assembly & Test Facility at BNL

- Electro-Mechanical Assembly
- Metrological Tests
- Electro-Optical Tests



21 Towers form focal plane array

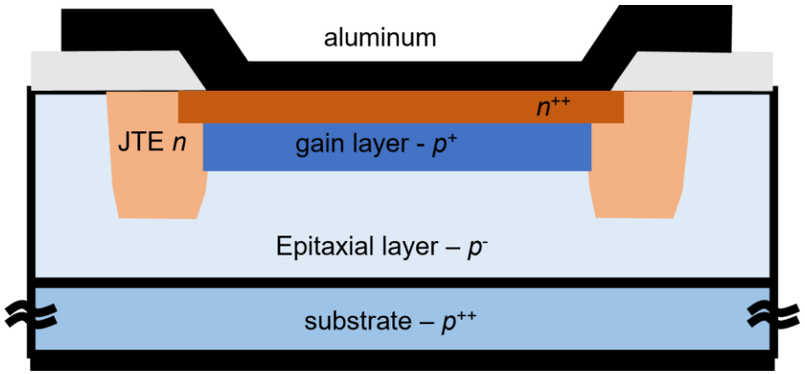


First LSST science raft delivered to SLAC in November 2017:

LGAD

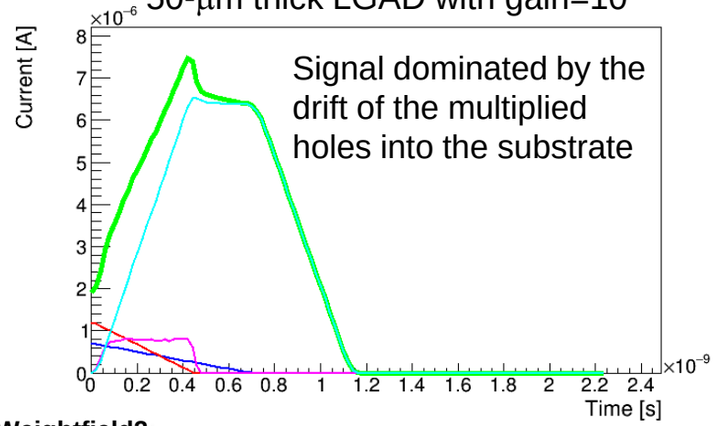
Low Gain Avalanche Diode (LGAD) will be used at HL-LHC

- Process similar to standard n-in-p sensors + built-in multiplication
- 300 kV/cm over ~ 1 μm near junction by a Gain Layer
- Bulk electric field ~ 20 kV/cm for high hole drift velocity (~ 10^7cm/s)
- High S/N thanks to gain
- Moderate gain (10-100) through electron impact ionization
- Time resolution: ~25 ps with 50 μm active thickness
- Radiation tolerance ~2.5x10^{15} neutrons/cm2

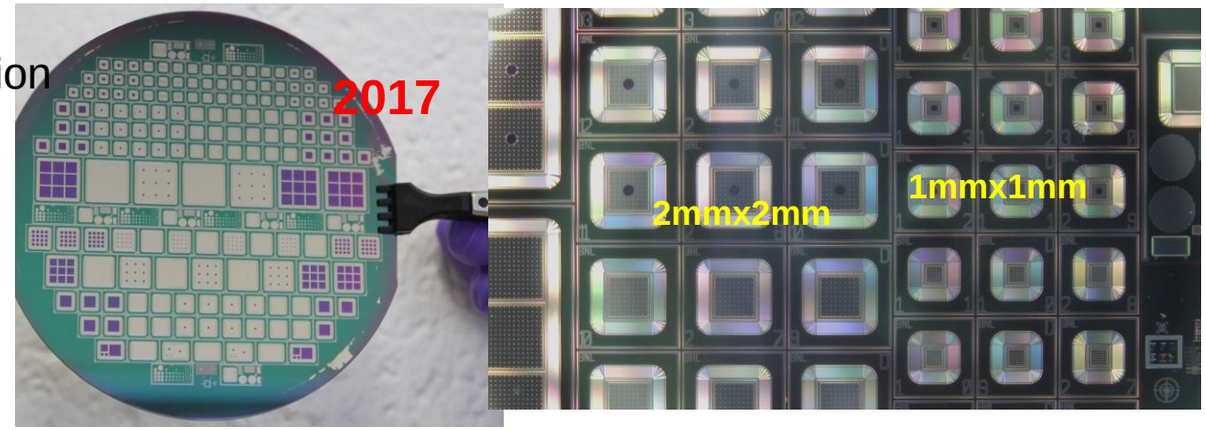


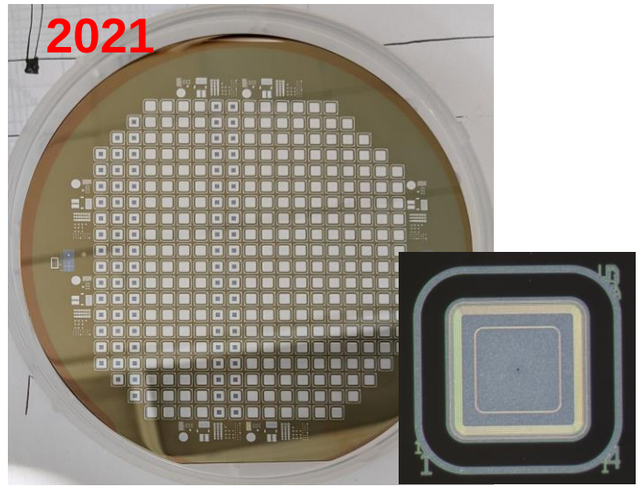
Weightfield2 Simulation

Current pulse generated by a mip in 50-μm thick LGAD with gain=10



Weightfield2:
http://personalpages.to.infn.it/~cartigli/Weightfield2/Main.html





2021 DC-LGAD

- new LGADs fabricated on HR silicon
- 20 and 50um thick wafers
- Soon on 30 um

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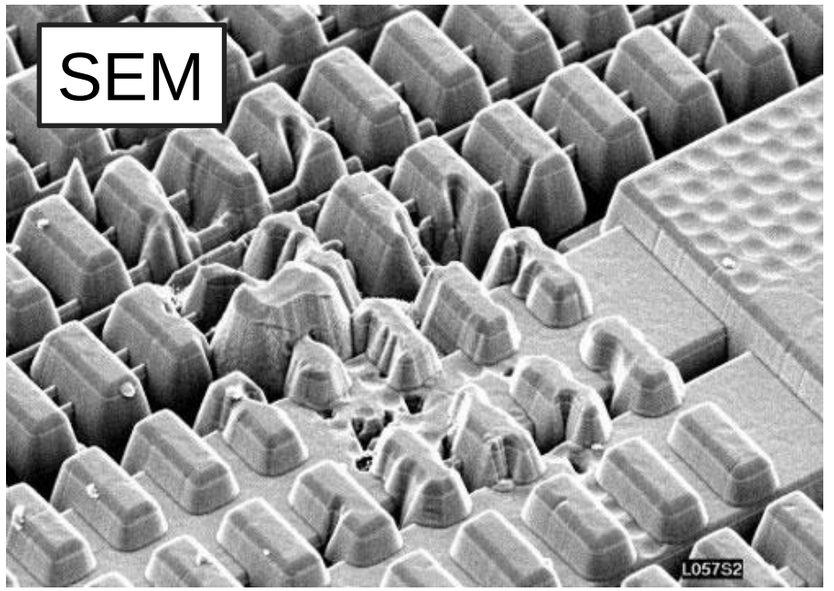
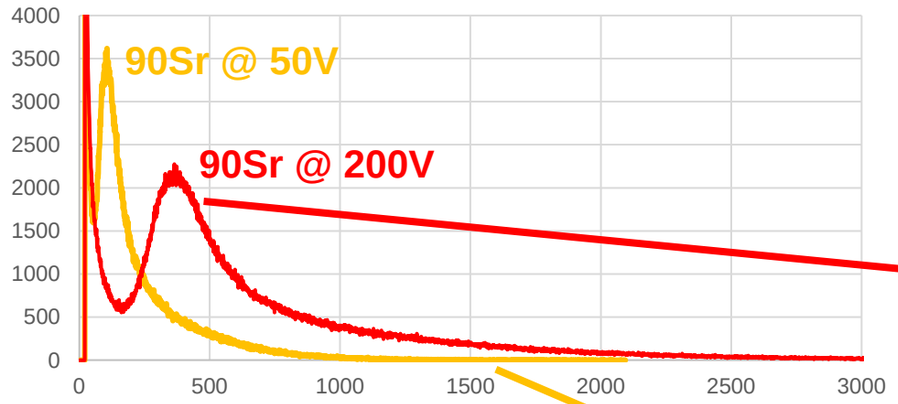
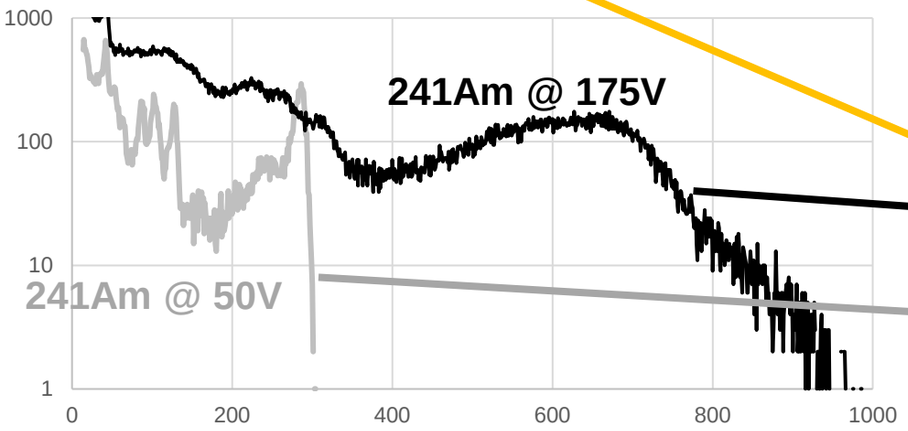
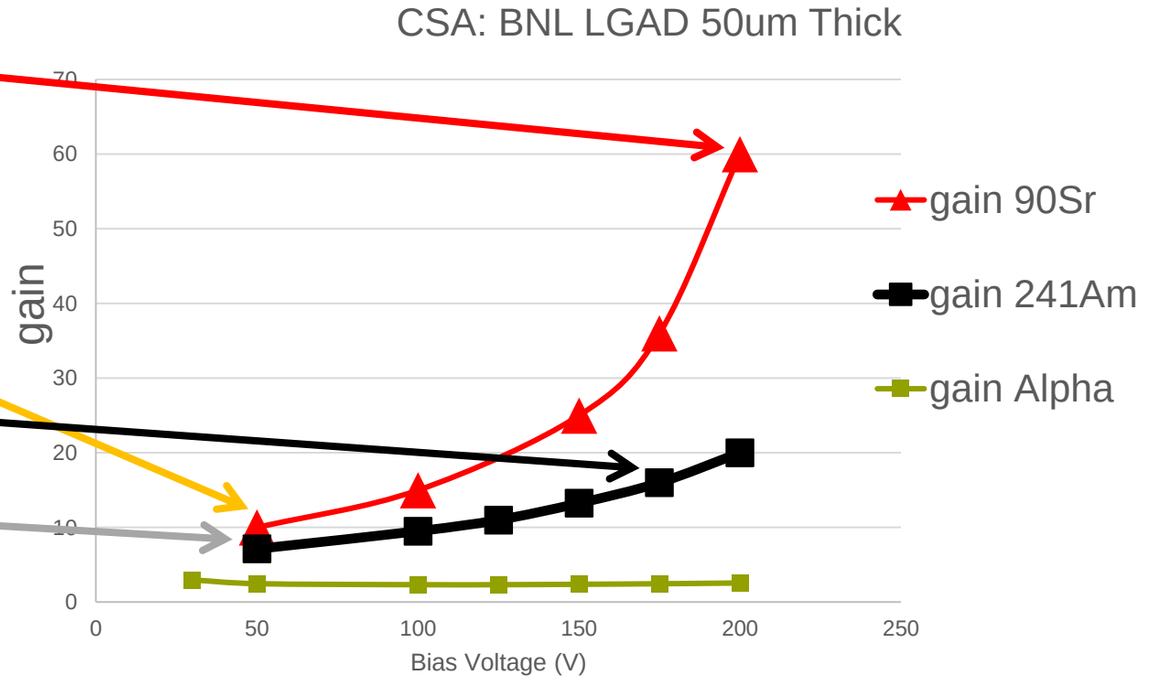
Characterization labs

- Probe stations for Current/capacitance – High Voltage scan, to be upgraded to Cold Probe Station
- Transient Current Technique with laser scan
- Gain measurement with low-noise CSA









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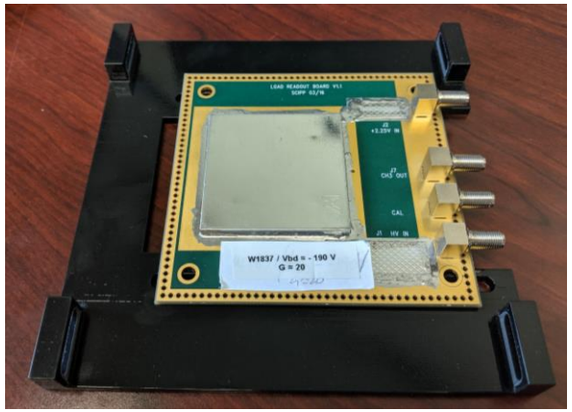
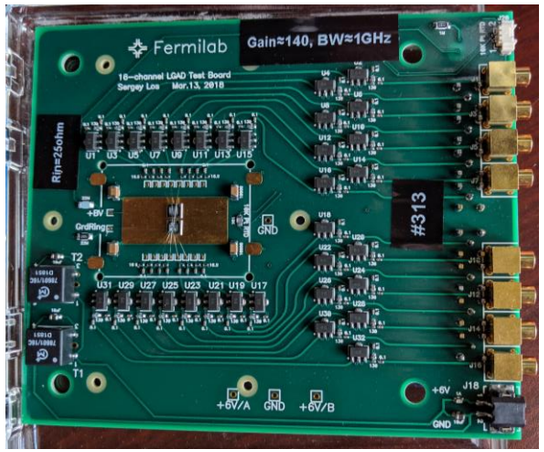
Timing in LGAD

- LGADs are optimized to be fast sensors for mips
- Landau noise dominates: thin sensors can have timing resolution down to 20 ps
- Price to pay: poor spatial resolution (mm pitch in ATLAS CMS)

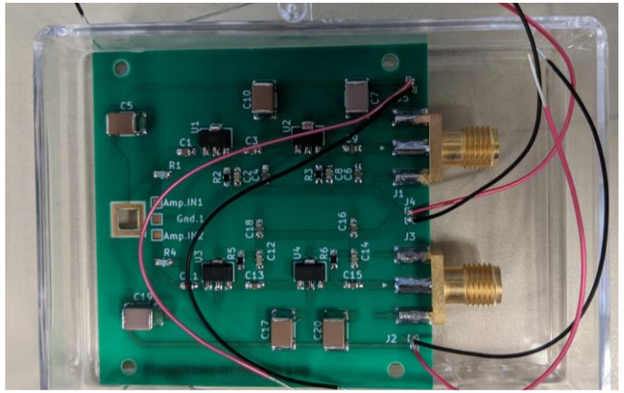
Single channel UCSC TA board



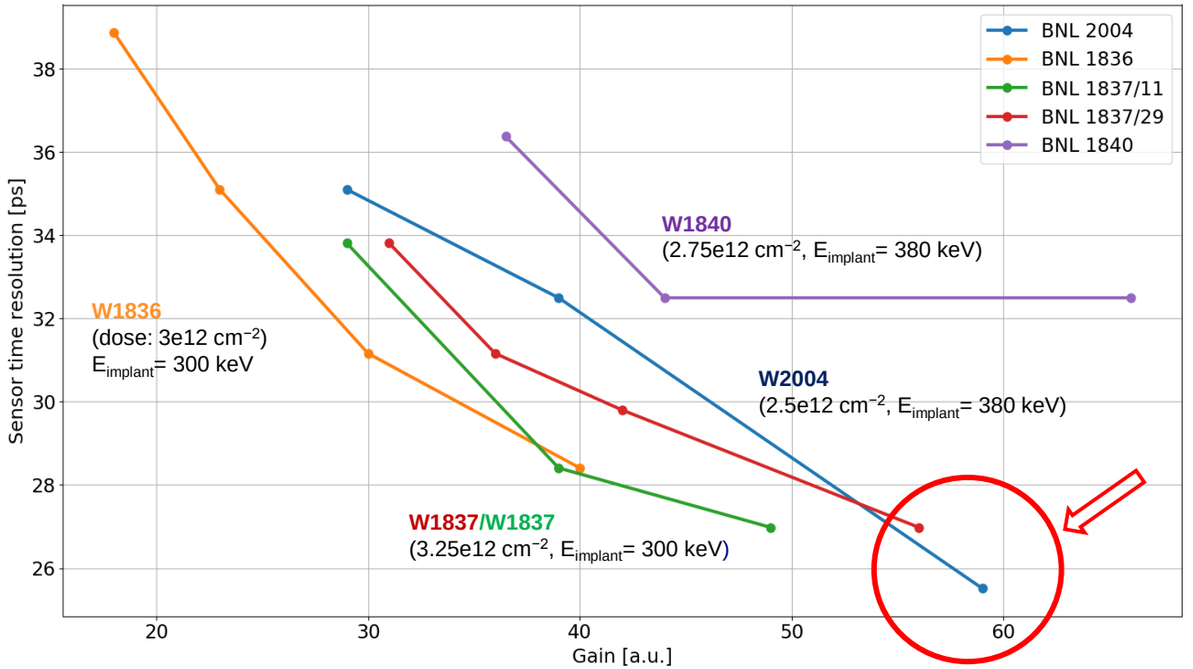
16-channel FNAL RF board



2-channel BNL RF board (under test)



➔BNL's LGAD Time resolution 26 ps
(50 μm sensor thickness)

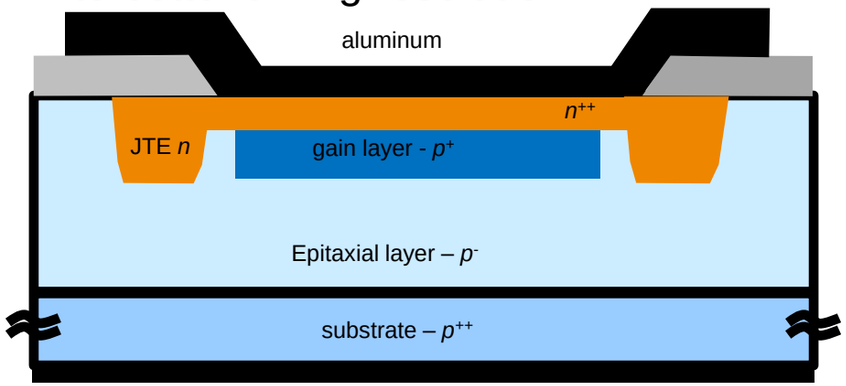


LGAD families

As spatial resolution is poor, an R&D towards a 4D detector (excellent timing and spatial resolution) is needed
→ modification of the original LGAD concept

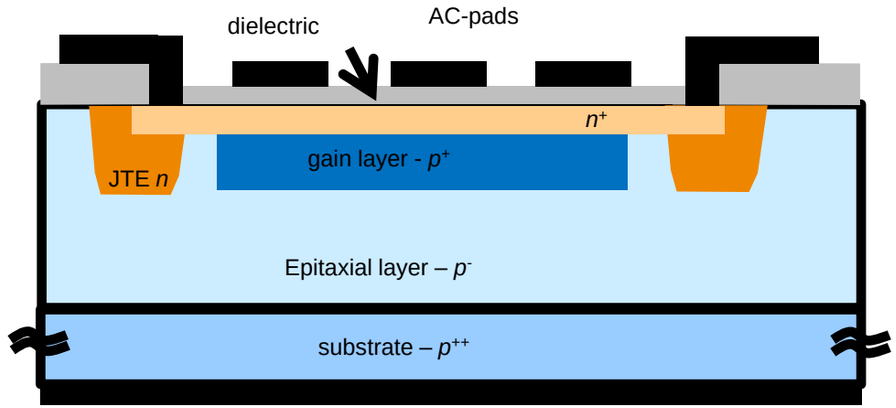
DC-LGAD on thin substrates

Thin substrates (~20-30um) lead to better timing resolution.



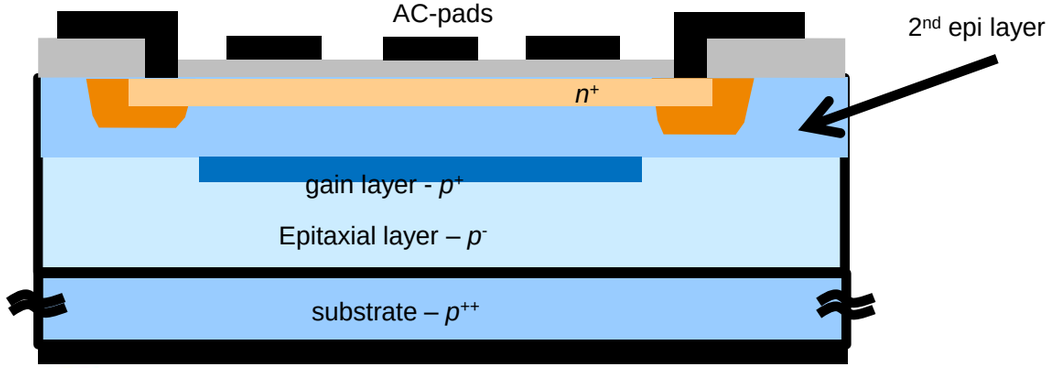
AC-LGAD

Excellent spatial resolution with smart position reconstruction algorithms, possibly for low interaction rates



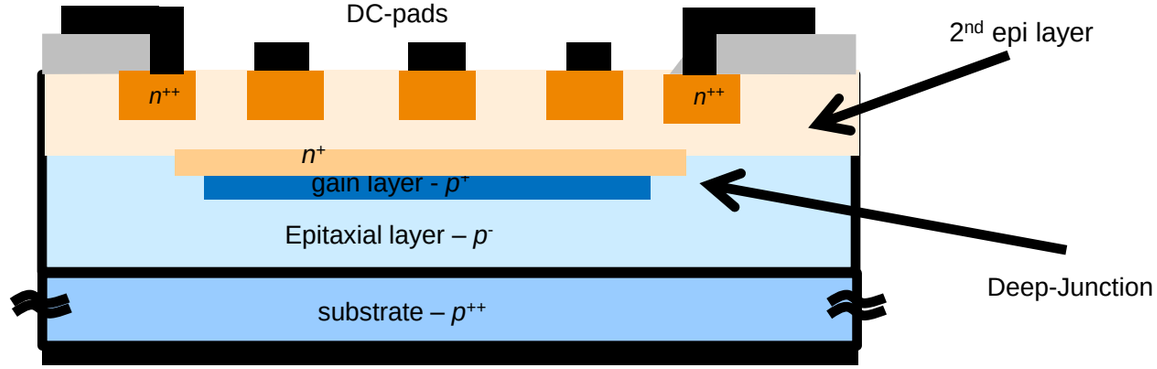
Deep-Layer AC-LGAD

(FNAL, Cactus, UCSC):
an AC-LGAD with a higher rad-hardness



Deep-Junction LGAD

(UCSC, Cactus) Position resolution given by pitch, as in std pixel/strip detector



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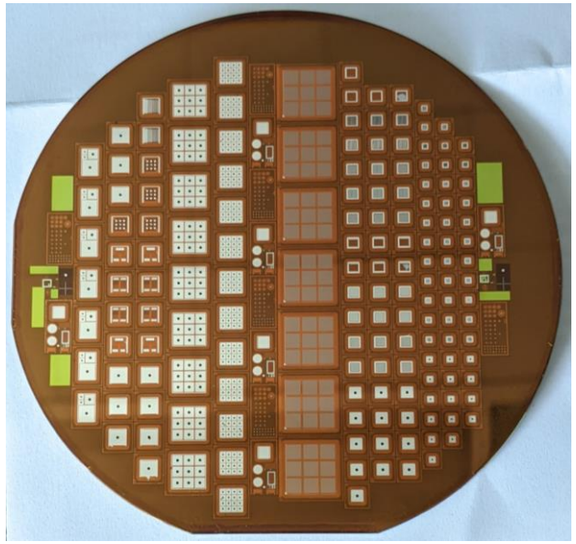
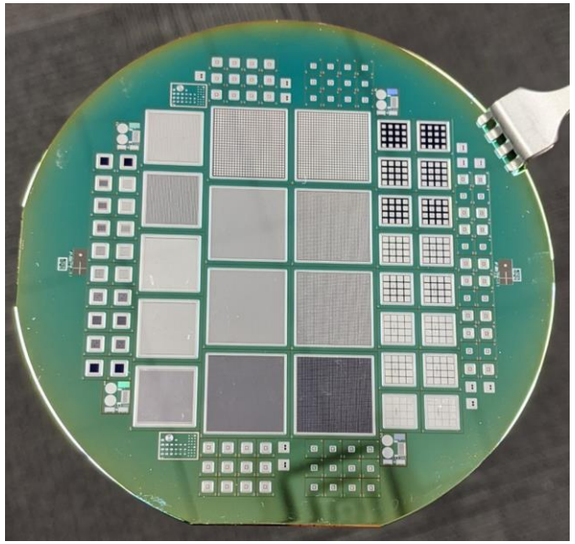
AC-LGAD

- First sensor based on LGADs having both fast timing and good spatial resolution
- Several geometries and batches fabricated
- Current sharing among AC-coupled metal electrodes placed over an insulator on top of the n+ allows great accuracy in hit position reconstruction
- → σ_x < pitch/10
- Fill factor = 100%
- Intense activity on test beams at FNAL, CERN with many collaborators (FNAL, UCSC, Rice, UIL, INFN, Uni Geneva, LANL)
- Towards EIC

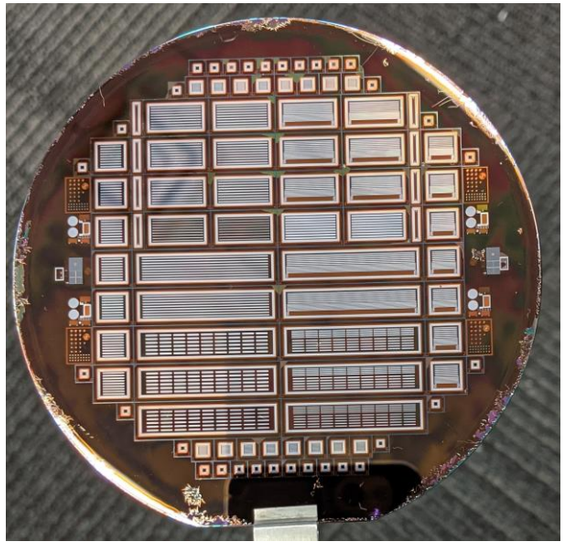
Layout # 1:
- Based on first LGAD masks



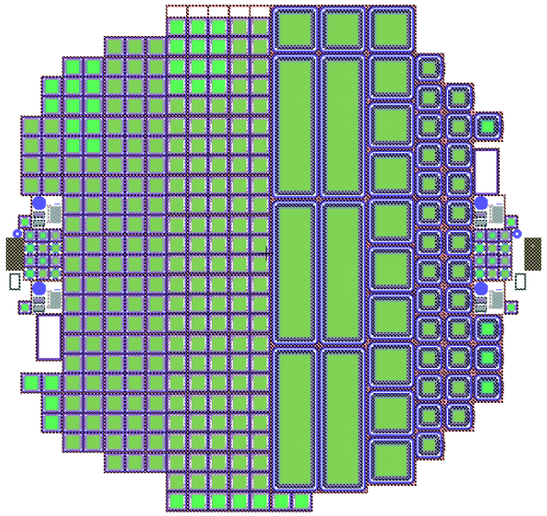
Layout # 2:
- Larger devices



Layout # 3:
- ACLGAD strips



Layout # 4:
- ACLGAD for EIC ROC test



Conclusions

BNL has wide experience in:

- Highly customizable silicon process and designs
- Collaborative environment with Universities, Nat Labs and industry
- Testing capabilities
- Wire-bonding / bump-bonding from basic test boards to complex full-size detectors
- Silicon sensors for ATAR : LDRD on-going to test capability