



PIONEER Electronics

From sub detector to DAQ

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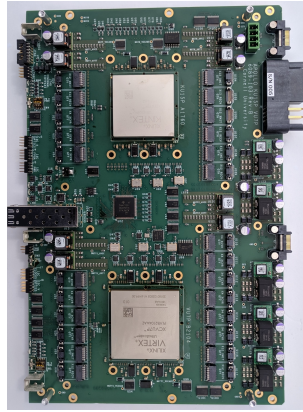
Guiding principles

- Minimize complexity / engineering effort
 - What can we leverage from elsewhere (eg., LHC)?
 - g-2 realized significant time/cost/effort savings by adapting CMS DAQ electronics
 - Maximize uniformity: avoid 2 types of boards where 1 can serve both purposes
- Concept for PIONEER:
 - utilize LHC APOLLO platform as backbone

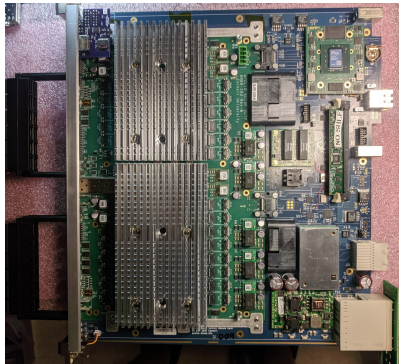
APOLLO system



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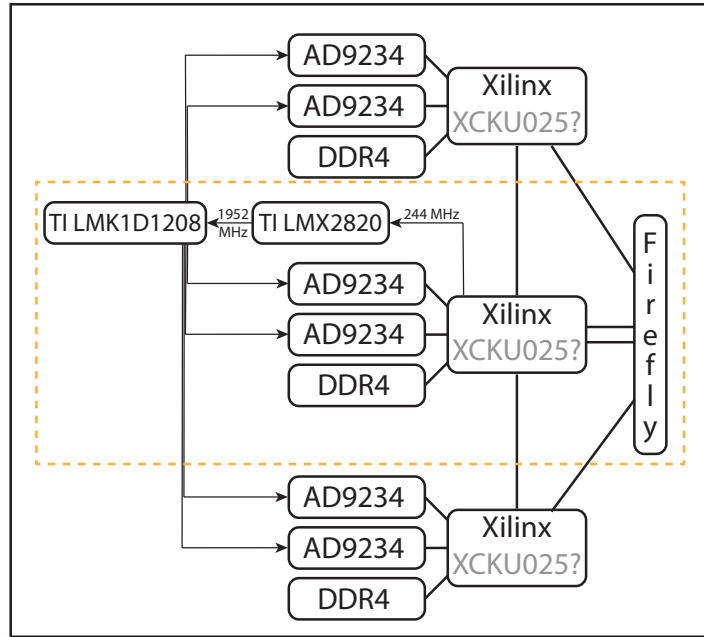


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- Universal “service module”
 - ATCA protocol, ethernet, ...
- Application-specific insert
 - For PIONEER, CU-developed Command Module (CM)
 - data movement independent of ATCA backplane
 - CM-only solution?

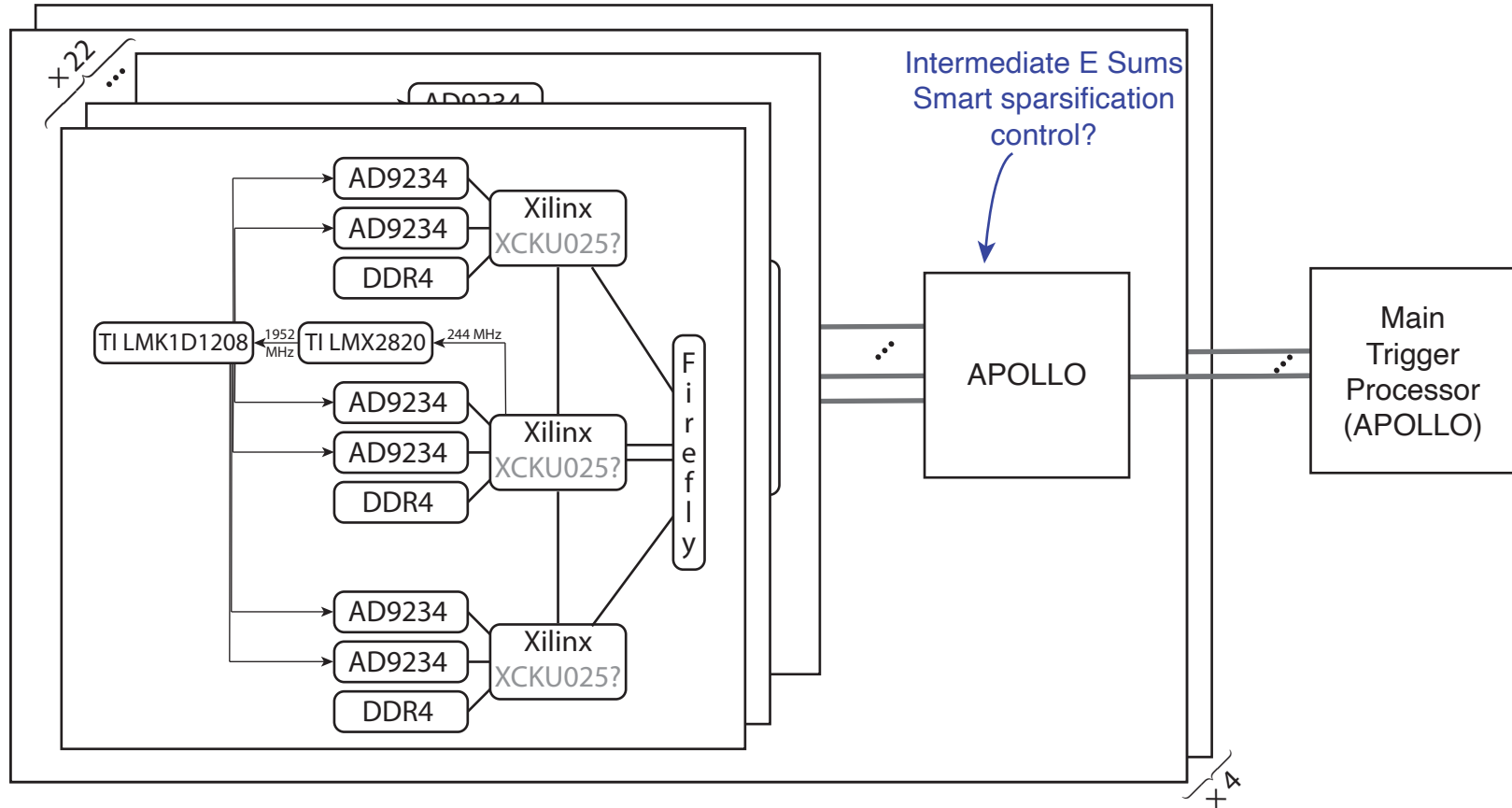
Calorimeter ADCs



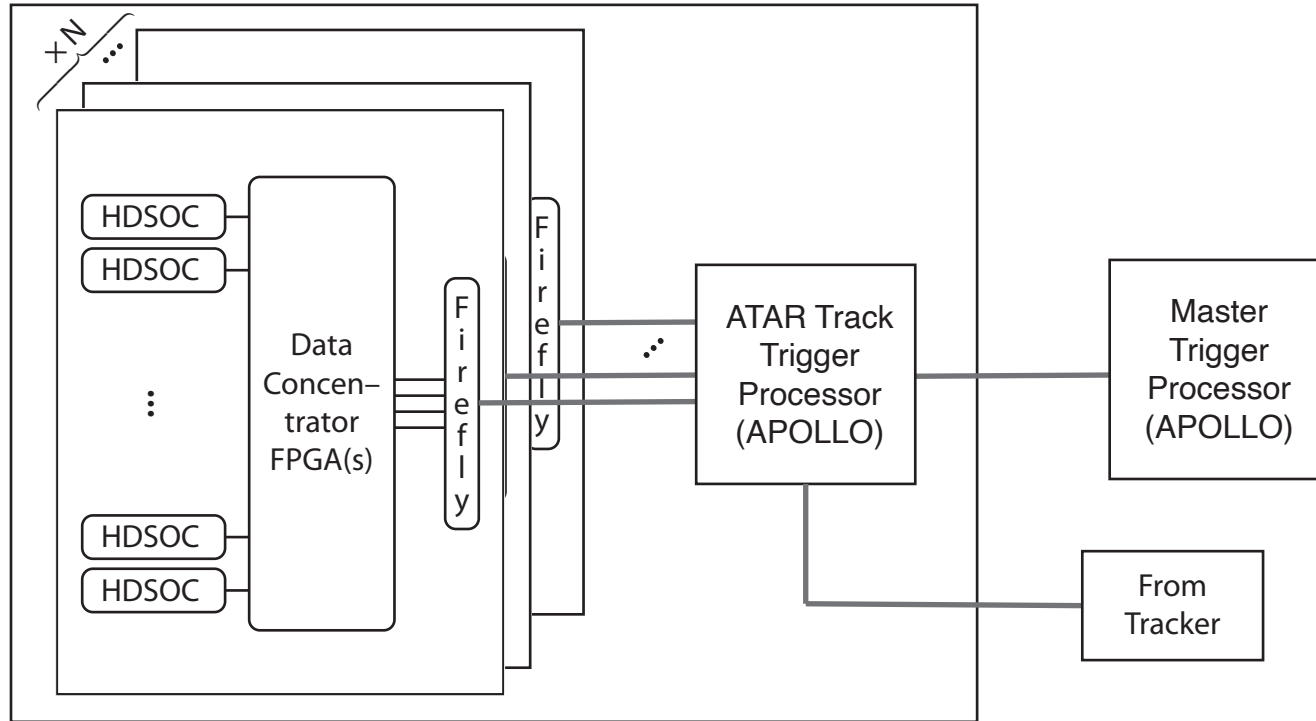
Triggering info: 16 bits 4 × ADC: 12 bits each

- 4 firefly channels / ADC board
 - 3 → quad channel data / triggering
 - 1 → PCIe config/control (IPBus)
- Master ADC clock: recover/clean from recovered firefly serial links
- sample continuously to ring buffer
 - master trigger: move to DDR4 event buffer for DAQ readout
 - essentially deadtime-less
- TX link: continuous triggering info + 4 channel event readout
- RX link: synchronous triggering + control

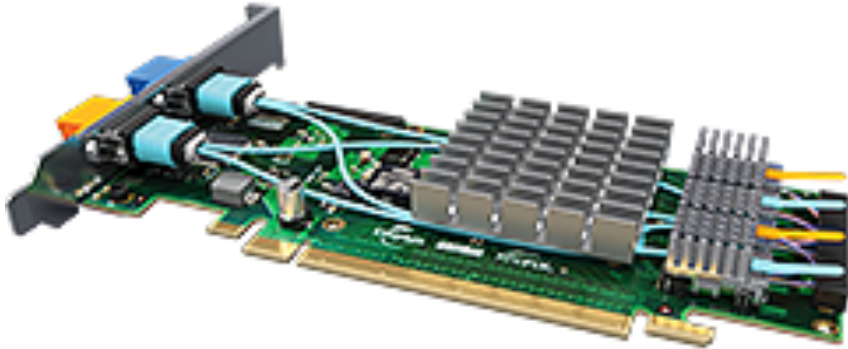
Instrumenting a ~1000 channel calorimeter



Similar topology for Active TARget (ATAR)



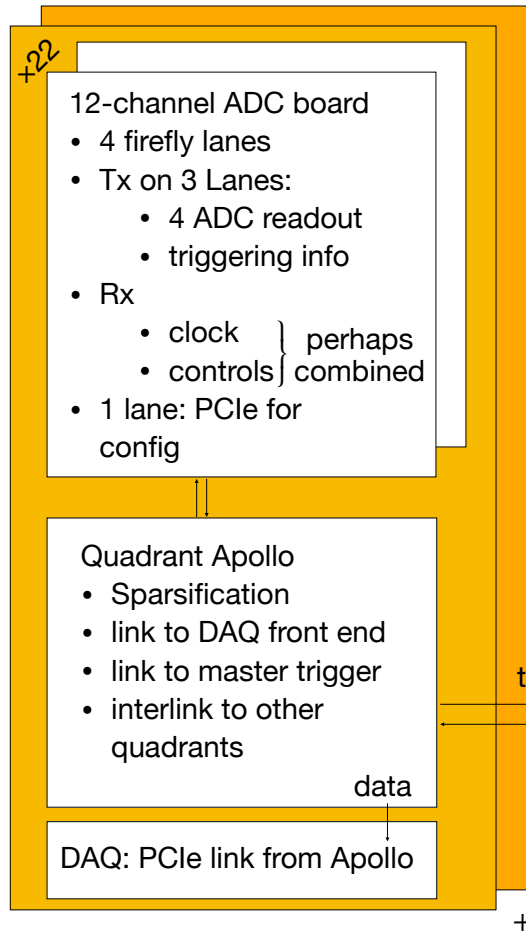
DAQ links



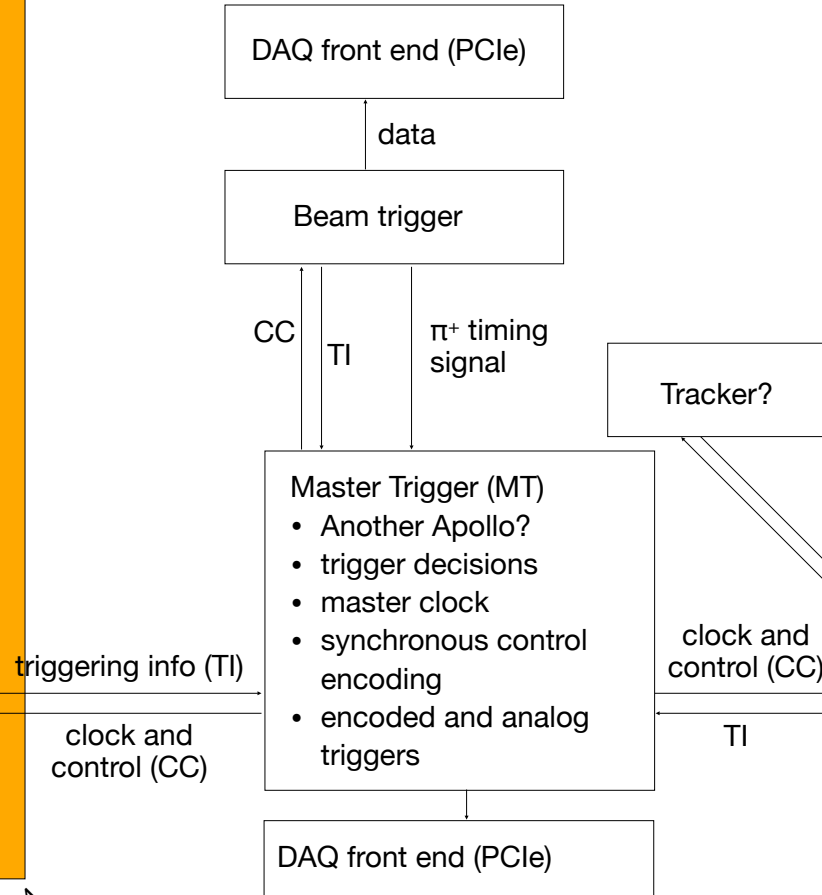
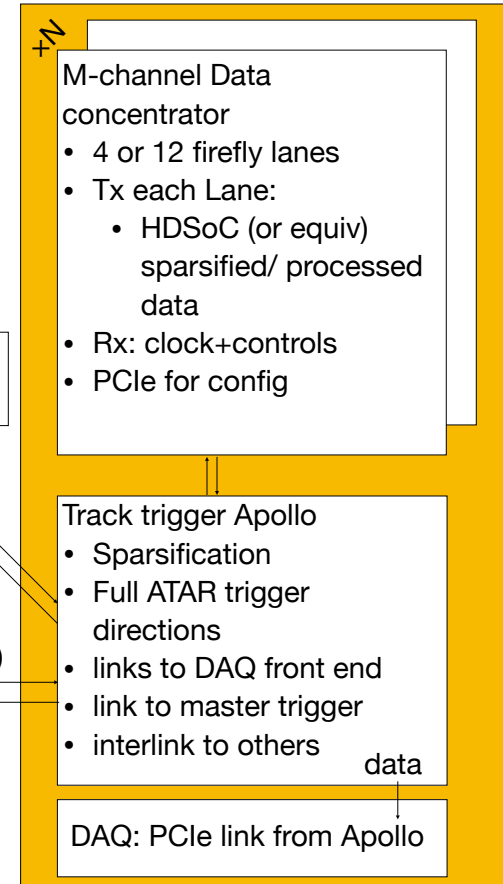
- PCIe gen 3 and gen 4 cards already in the works for firefly
 - 4-lane gen 3 already sufficient for calo readout
- PCIe attractive for dedicated point-to-point topologies as in DAQ systems
- Samtec's availability prognostication:
 - Oct. release for scheduling
 - O(44 weeks) for delivery ARO

Apollo based conceptual model

Calorimeter electronics



ATAR electronics

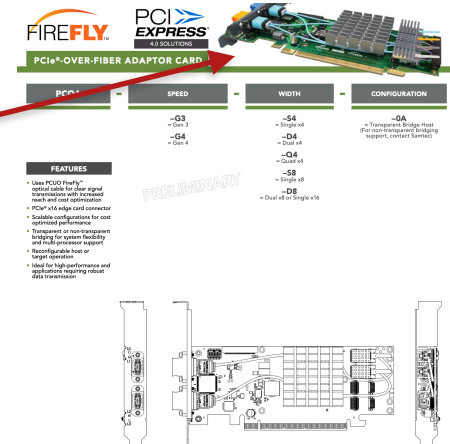


Latencies

- #'s based on Xilinx GTY transceivers
 - many options in the TX/RX (de)serialization
 - CERN studies suggest we can get away with the more minimal approaches
 - 16.1 gbps latencies:
 - TX: 16 ns – 40 ns
 - RX: 16 ns – 49 ns
- AD9234 latency: data input through JESD serialization → 59 ns
- JESD deserialization: typically “10’s of ns” — assume 30 ns
- Total energy sum in calo, just as a simple exercise
 - Two Apollo hops: 64 ns – 178 ns
 - ADC → FPGA: O(90 ns)
 - Cascading sum of pairs (plus pedestal subtraction): ~12 clock cycles → ~30 ns
 - Trigger decision latency: 184 ns – 300 ns
 - Trigger communication back to detector: 64 - 178 ns
 - 500 ns trigger decision + communication feasible
 - (analog trigger communication paths also available)

Getting a start

- CU CMS group finished with initial Apollo CM prototype
 - We can begin using to:
 - test clock recovery
 - measure speed of triggering algorithms
 - begin exploring protocol issues
 - explore what existing CMS firmware may be useful
 - https://github.com/apollo-lhc/CM_FPGA_FW
- Ordered an eval board for the calo ADC
- PCIe over firefly: PC card on order from samtec (in beta)
 - IPBus explorations
 - event building / data transfer to MIDAS



Some Institution-level tasks

1. Calo ADC boards (CU)
 - Calo quadrant Apollo firmware (or equiv) (CU)
2. ATAR HDSoc (or equiv) host board (UCSC)
 - Full track trigger firmware for Apollo / equiv
3. Clock and Control Infrastructure firmware (eg., CERN TCDS)
4. Master trigger firmware for Apollo / equiv (D. Ries)
5. others, depending on tracker, beam instrumentation needs, etc.

