UNIVERSITY OF BIRMINGHAM

Status of MAPS tracking

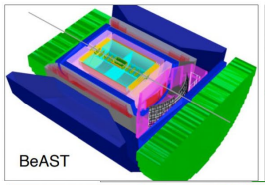
Laura Gonella on behalf of the EIC R&D WP1 MAPS group

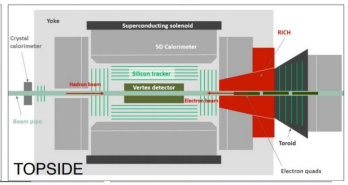
EIC UK Discussion Meeting

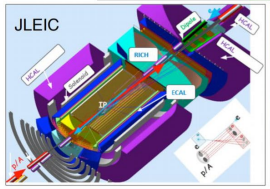
30 June 2022

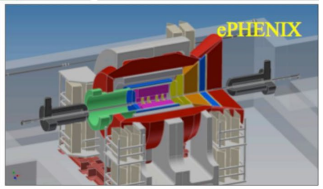
EIC Detector Concepts

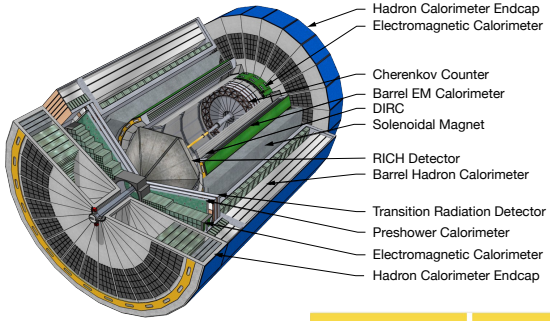
White paper (2012, 2014), initial concepts











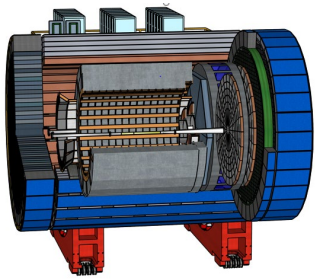
Yellow Report reference detector (2020), global effort of the EIC Users Group

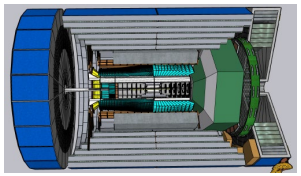
Call for Detector proposals (2021)

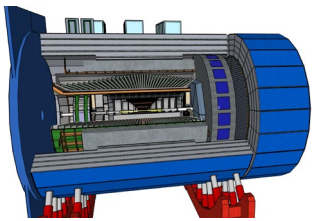
ATHENA: A Totally Hermetic Electron-Nucleus Apparatus
- General purpose detector inspired by YR studies, new central magnet of up to 3T

CORE: COmpact detectoR for the Eic
- Nearly hermetic, general purpose compact detector, 2T baseline

ECCE: EIC Comprehensive Chromodynamics Experiment
- General purpose detector, 1.5T BaBar magnet







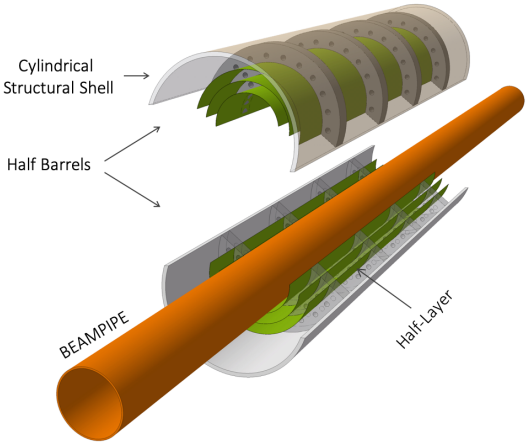
2022: Merging of ECCE and ATHENA proposal strengths forming a new collaboration and a new concept for DETECTOR 1.

Starting point: reference detector (i.e. design).

Detector 1 Silicon Vertex and Tracker

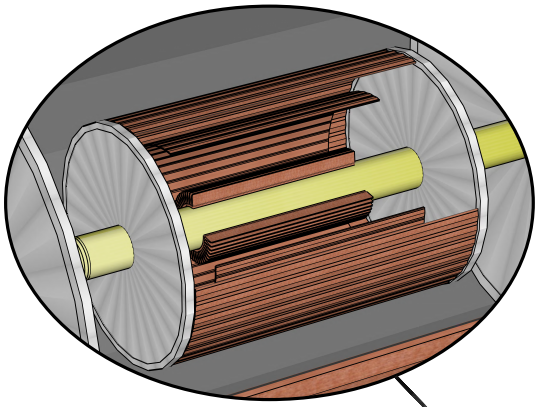
- The EIC Detector 1 SVT concept is derived from the ALICE ITS3 technology.

- Vertex layers ITS3 like
  - ITS3 wafer-scale stitched sensor, thinned and bent around beam pipe.
  - No services in active area, air cooling, minimal support structure.
  - 0.05% X/X0.

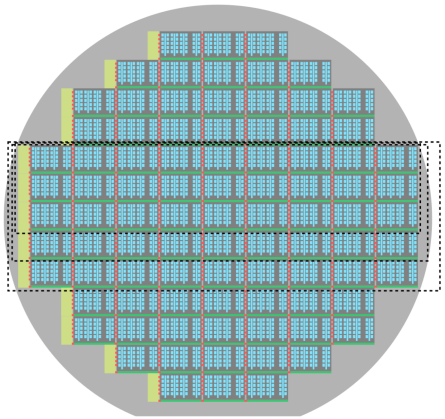


ITS3 detector layout

EIC Vertex Layers layout
(as in ATHENA Proposal, same for ECCE)



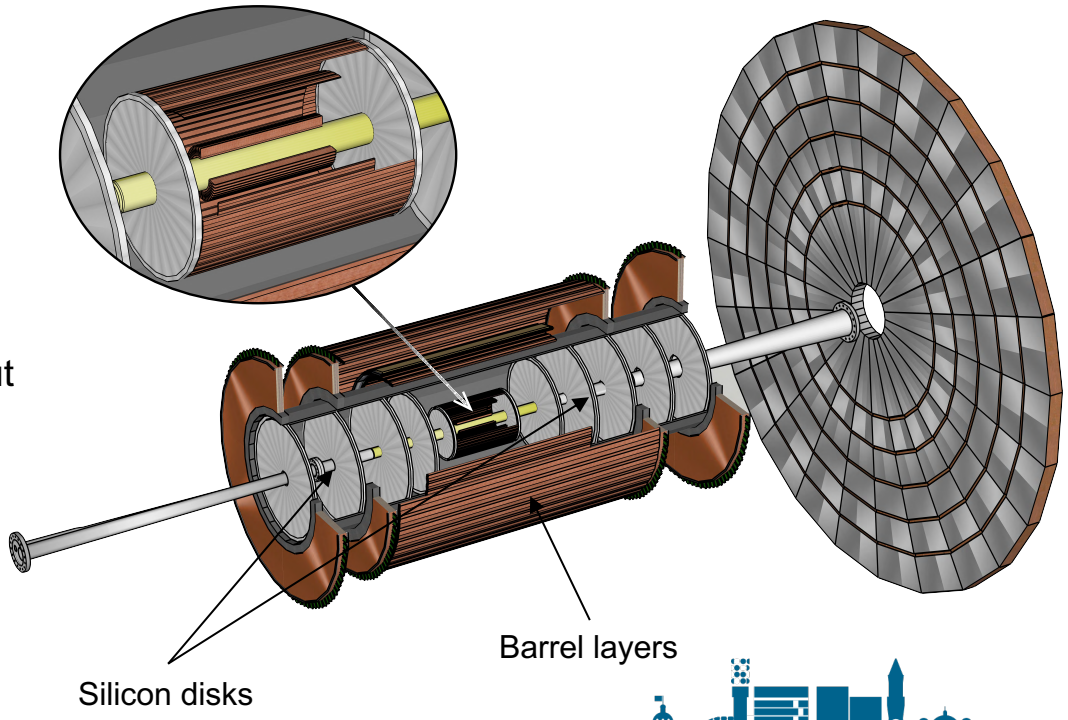
Stitched sensor wafer
layout example



Detector 1 Silicon Vertex and Tracker

- Barrel layers and disks
  - EIC Large Area Sensor (LAS), i.e. ITS3 sensor size optimised for high yield, low cost, large area coverage.
  - Convectional carbon fibre support structures with integrated cooling.
  - Conservative material budget estimates: 0.24% X/X0 per disk, 0.55% X/X0 per barrel layer

Example of EIC SVT layout (ATHENA design)



EIC R&D WP1 MAPS

- Institutes involved:
  - Universities: Birmingham, Brunel, Lancaster, Liverpool.
  - STFC Labs: RAL, DL.

- Work is carried out within the EIC Silicon Consortium and EIC project and in collaboration with ITS3 and the CERN EP R&D programme.

- Work packages
  - WP1.1 – Sensor design
  - WP1.2 – Sensor characterisation and DAQ
  - WP1.3 – Modules and system tests
  - WP1.4 – Detector layout simulations

WP1.1 – Sensor Design

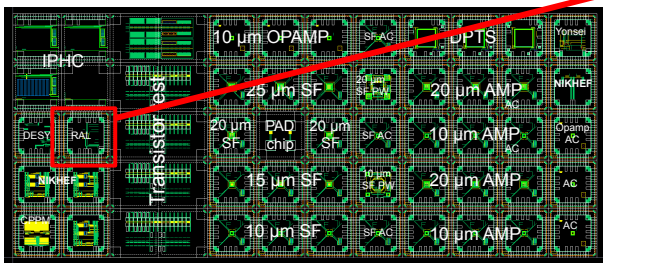
- RAL TD is actively involved in the development of 65 nm MAPS sensor and IP blocks in collaboration with CERN EP R&D WP1.2 and ITS WP2.

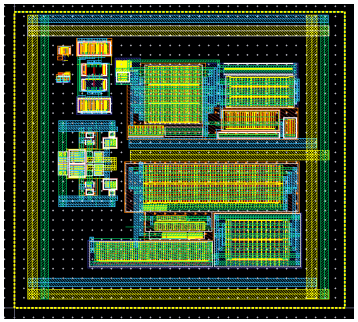
- Main contribution: development of high-speed data transmission IP blocks that will be used in the final version of the large area ITS3 sensor.

- MLR1 submission Q1-2021: LVDS receiver and CML transmitter.

MLR1: RAL LVDS-CML

MLR1 submission

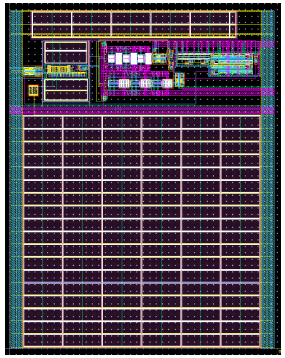




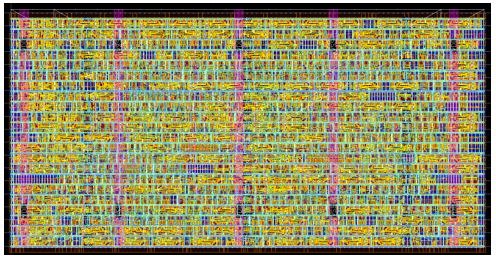
WP1.1 – Sensor Design

- ER1 submission Q2-2022:
  - PLL and CML receiver; the PLL will be integrated with the MLR1 IP blocks.
  - I2C block; of interest to the ITS3 large area sensor development for on-chip signal transmission.
  - DFM cells improvements required by the collaboration also carried out by RAL TD.

ER1: RAL PLL



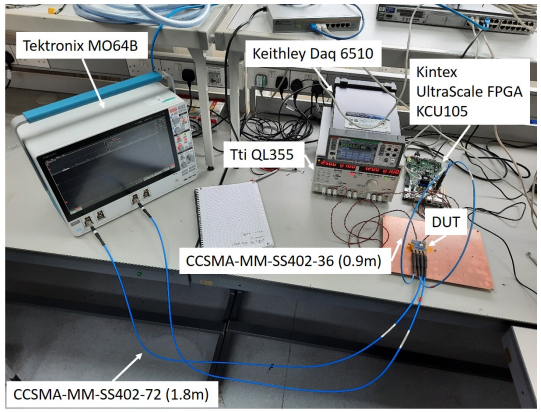
ER1: I2C



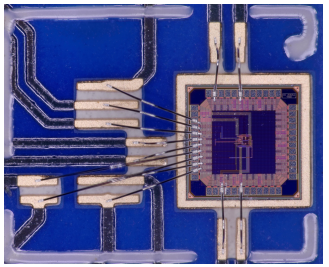
- Contributions being defined for the ITS3 ER2/EIC 1st ER in 2023.
  - RAL TD/PPD starting work on shunt regulator design for serial powering.

WP 1.2 – Sensor Characterisation

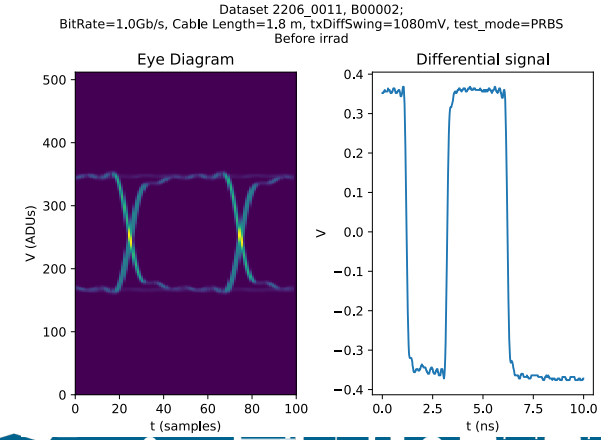
- Structures available for characterisation are those submitted in the MLR1.
  - ITS3 Analogue and Digital Pixel test Structures (APTS, DPTS).
  - IP blocks from various institutes.



- APTS/DPTS
  - Organised within the ITS3 WP3.
  - BHM/LIV contributing to wire bonding of APTS sensors for testing by the ITS3 and EIC communities.
  - Waiting for ITS3 test system distribution.



- RAL IP block
  - DL/RAL TD developed testing setup.
  - Chips bonded at BHM/LIV.
  - Preliminary results from RAL/DL.
  - X-rays irradiations at CERN planned for summer.

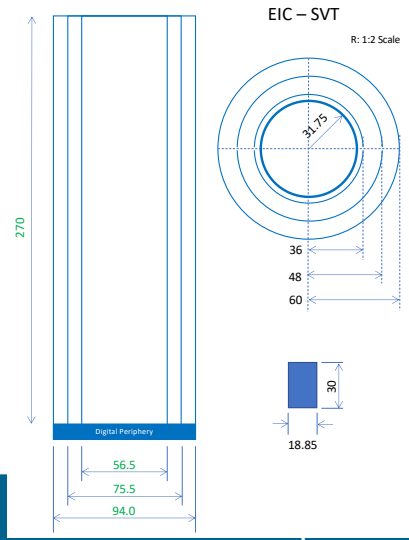


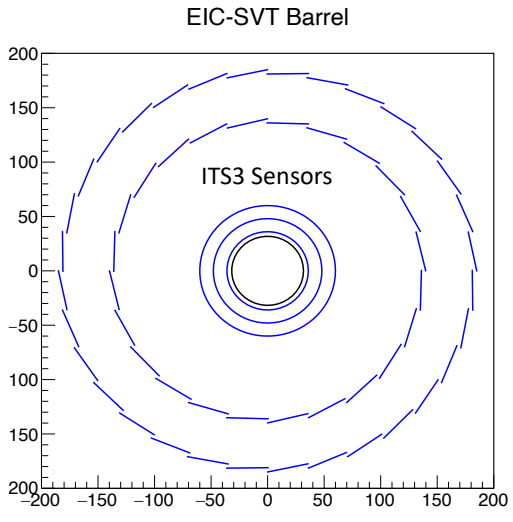
WP1.3 – Modules and system tests

- Activities in WP1.3 are connected to the tasks in the EIC funded eRD111 and eRD104 projects.
  - The UK participates in: eRD111 Task 1 Modules, eRD111 Task 2 Staves, eRD104 Task 1 Powering.
  - Ongoing conceptual design and layout studies at BHM/DL.

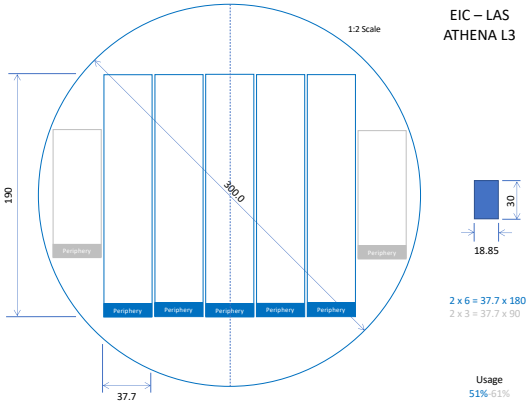
- Vertex layers with ITS3 sensor, EIC LAS in barrel layers
  - For barrel layers consider options for sensor size to maximise use of wafer and tile staves with at most 2 sensors to keep services outside active volume.

ITS3 sensor size and achievable EIC vertex layers radii



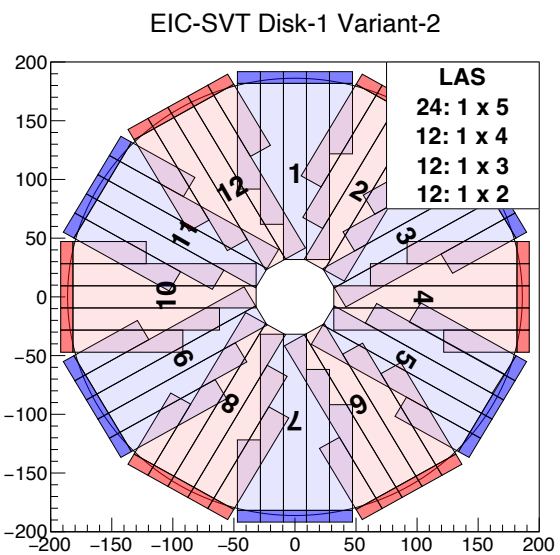


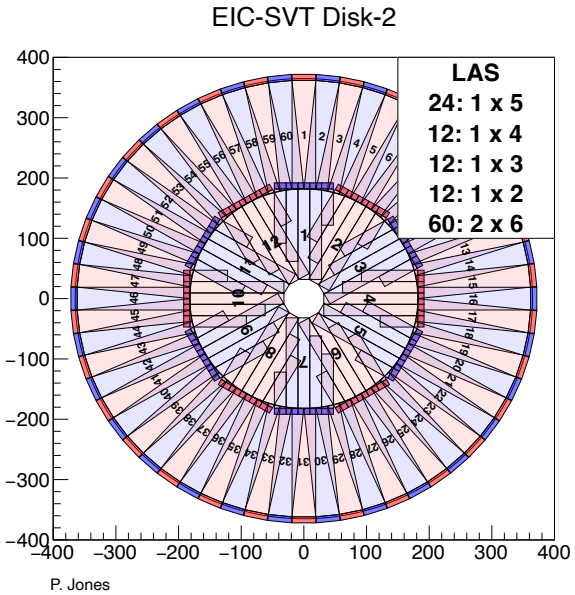
Example study of LAS sizes to maximise wafer usage using ECCE/ATHENA radii.



WP1.3 – Modules and system tests

- Sensor layout on disks challenging.
  - Maximise acceptance around beam pipe with low material
  - Current approach aims at a combination of elements common to most/all disks and an element specific to the beam-pipe opening at a particular location.



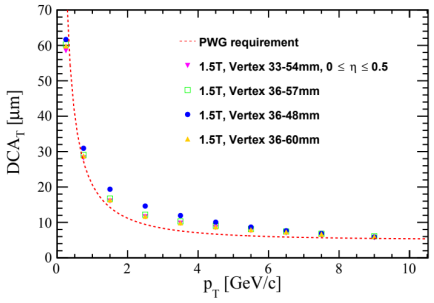


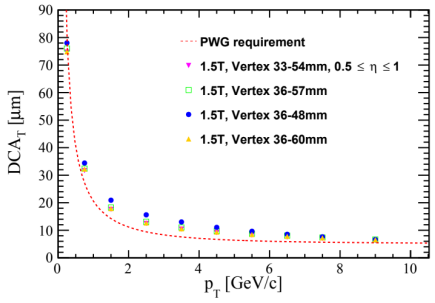
- Accompanying work on mechanics and CAD about to start.

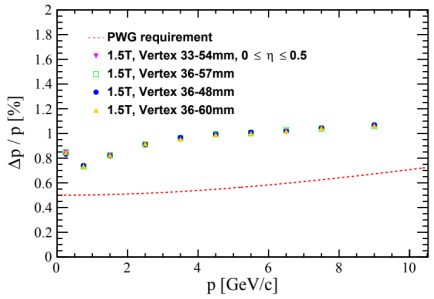
WP1.4 – Detector layout simulations

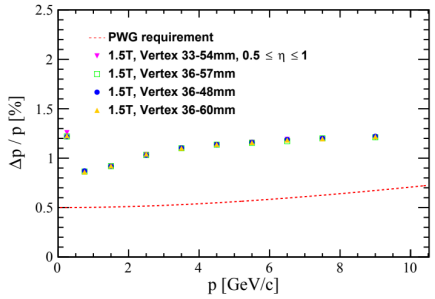
- Work carried out in support of the reference detector optimisation within the EIC Detector 1 Tracking Working group.

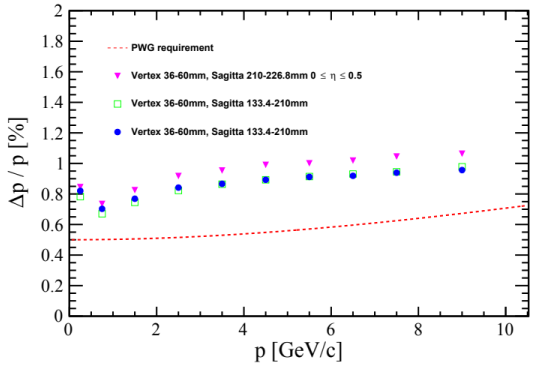
- Study of DCA_T and dp/p for updated reference detector design with inputs from WP1.3.
  - Updated material budget estimates and vertex layers radii.
  - Study of barrel layers position to avoid services in active area.

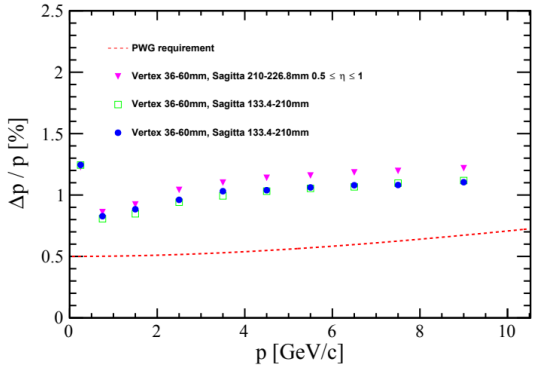












Conclusion

- Through the EIC R&D funding, seven UK groups are leading the development of the Silicon Vertex and Tracking system for the EIC Detector 1.
  - Work carried out within the EIC SC, EIC project R&D,ITS3 project, CERN EP R&D programme, EIC Detector 1 tracking WG.

- We are contributing to the design of the next generation 65 nm MAPS and their characterisation.
  - IP blocks contributed to both MLR1 and ER1; characterisation of MLR1 RAL IP block ongoing; preparations for MLR1 APTS/DPTS testing underway.

- Work on the overall detector design optimisation and layout proceeds with conceptual studies supported by simulations and by engineering work to start soon.