4D tracking at FCC

An overview of the present activities aimed at developing trackers with excellent spatial and temporal resolutions for FCC

- **Extensive collaborations within the RD50 CERN collaboration**

- **4D tracking is a key strategic development of the ECFA roadmap**
  - **RD50, RD42, MAPS, … ==> DRD3 R&D community**

UFSD

PRIN 4DInSiDe

AIDA Innova

4D tracking:
Where, when, how the R&D will take place?

ECFD Roadmap: DRDT 3.2 - Sensors for 4D-tracking.

- Understand the ultimate limit of precision timing in sensors with and without internal multiplication;
- Develop sensors with internal multiplication with 100% fill factors and pixel-like pitch;
- Investigate the production of sensors with internal multiplication in a monolithic design;
- Increase radiation resistance, push the limit of 3D sensors and explore LGAD and MAPS capabilities;
- Investigate the use of BiCMOS MAPS, exploiting the properties of SiGe.

DRD3 task force: implementation of the ECFA roadmap

Town meeting: March 22-23rd.

Join DRD3 and participate!

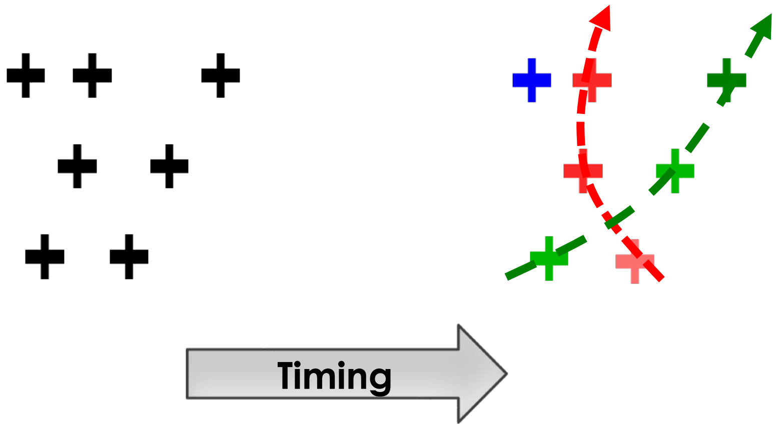
https://indico.cern.ch/event/1214410/

Future R&D in 4D tracking

In the following slides, I present a few R&D paths that will be explored in DRD3

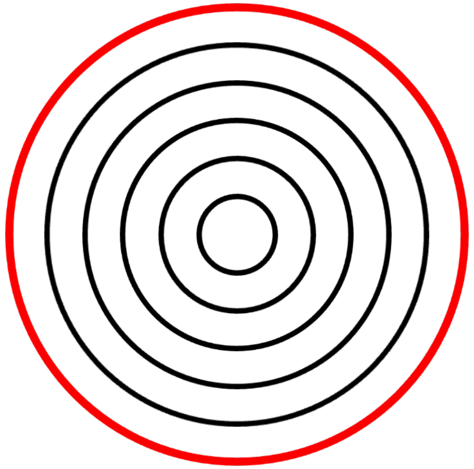
Timing layers and 4D tracking

By “**4D tracking**” we mean the process of assigning a spatial and a temporal coordinate to a hit.



Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)



Timing layers and 4D tracking

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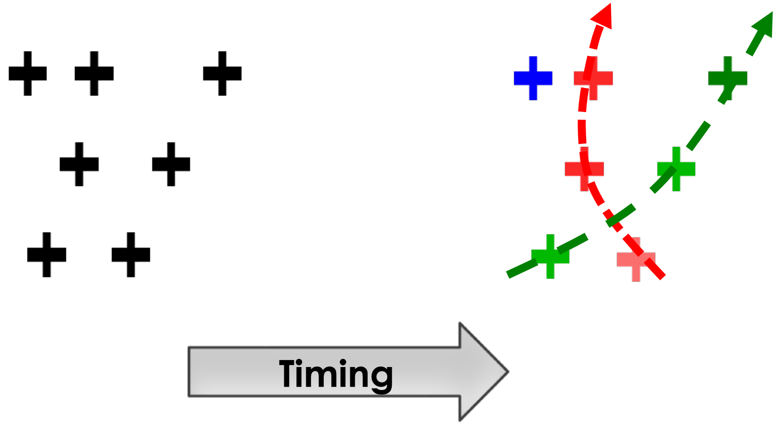
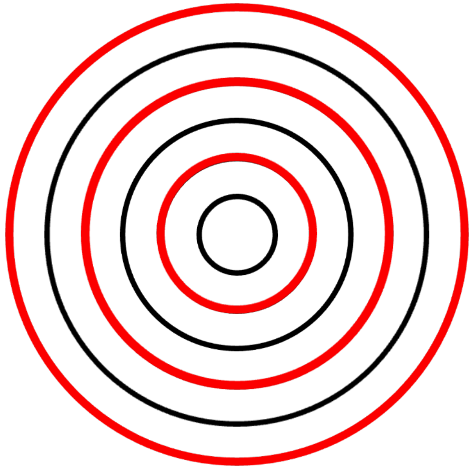


Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)
2) Timing at some points along the track



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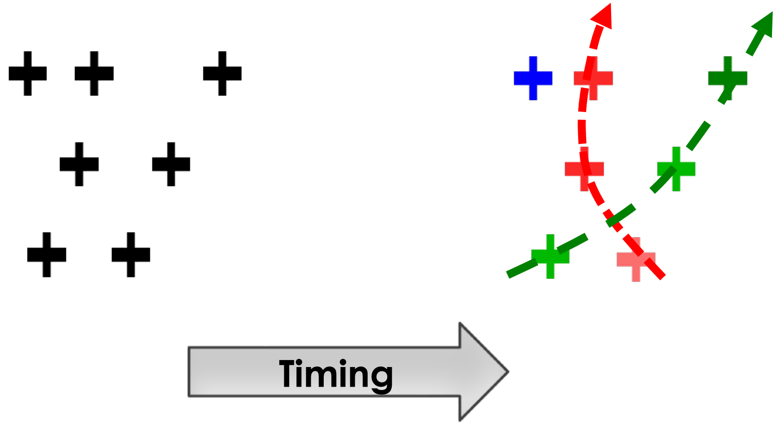
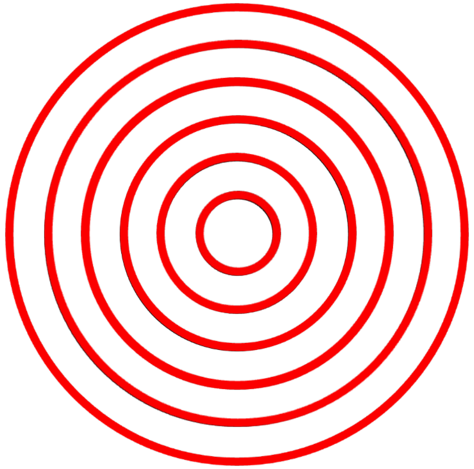


Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)
2) Timing at some points along the track
3) Timing at each point along the track



Timing layers and 4D tracking

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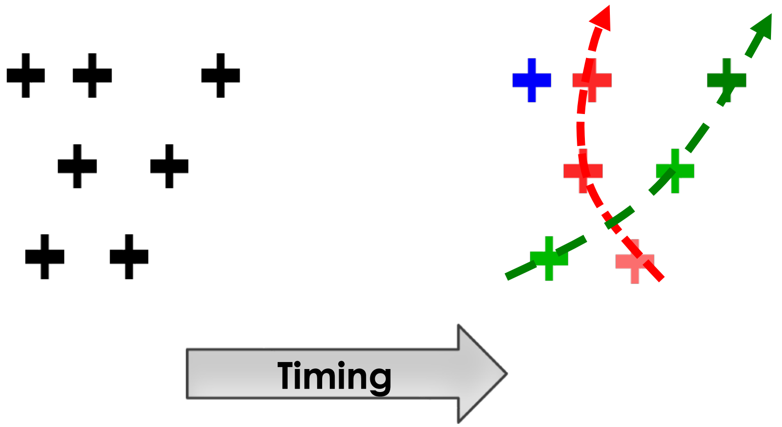


Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)
2) Timing at some points along the track
3) Timing at each point along the track

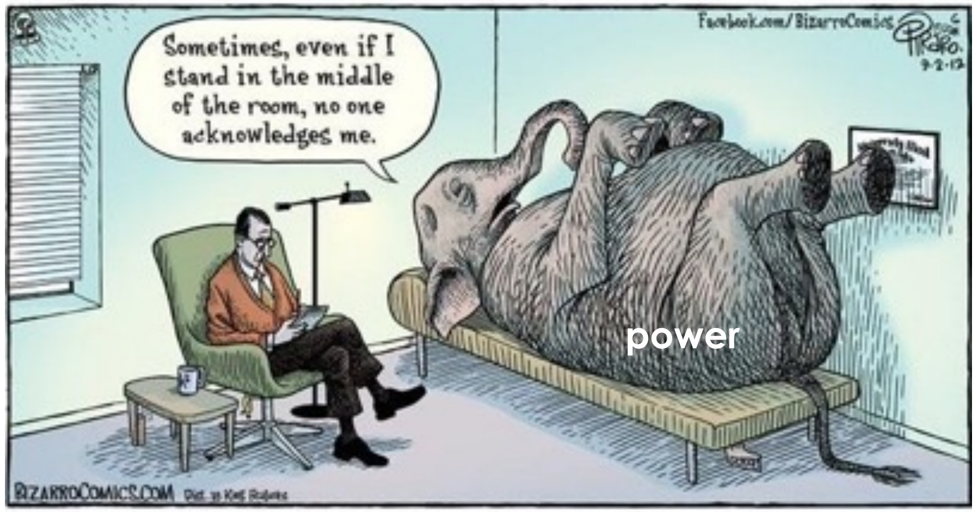
Many timing coordinates per track yield to better performing detectors, but require much more complex read-out systems.

Some projects will be perfectly fine with having a limited set of timing points

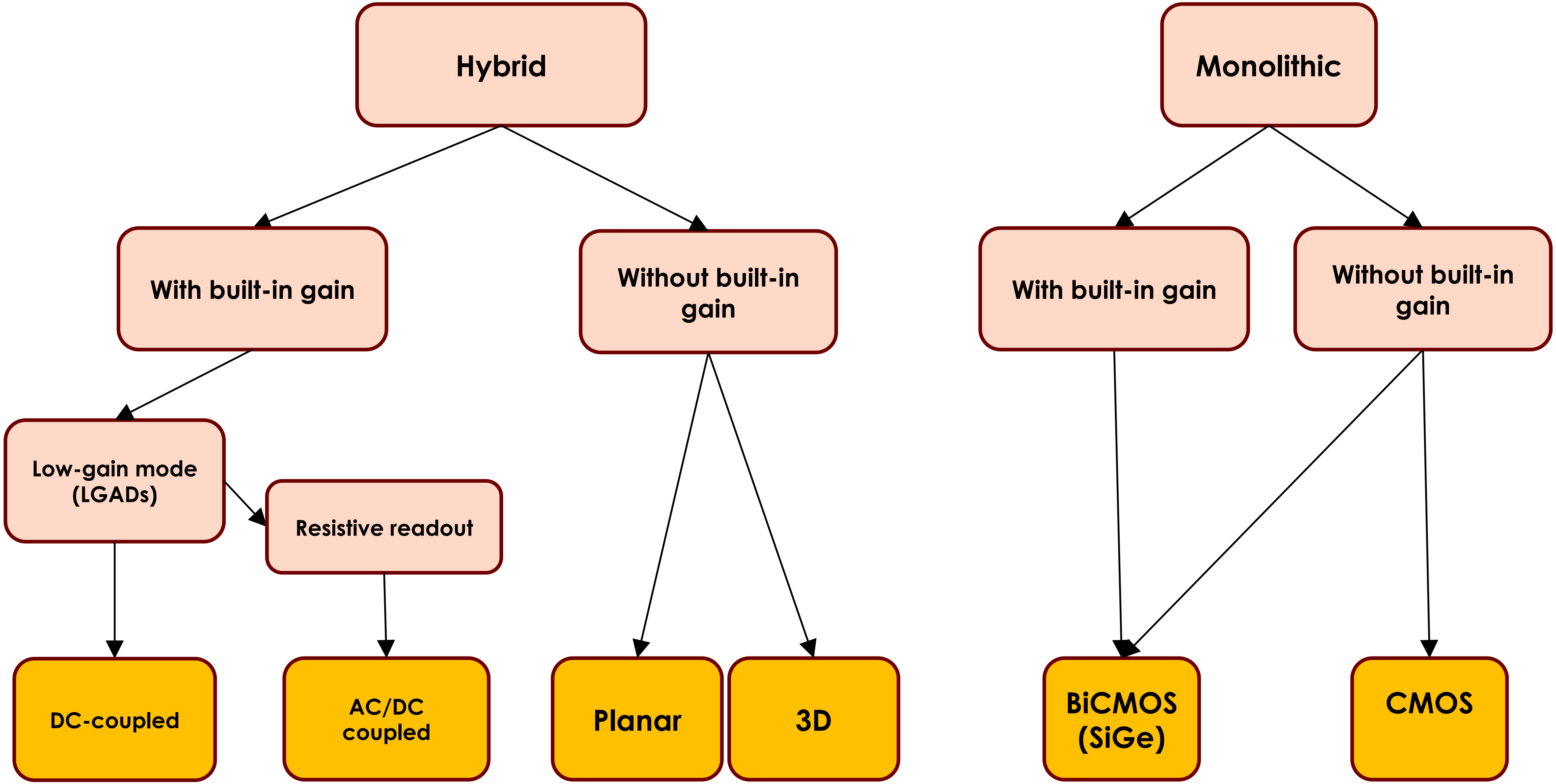
Interplay of power, pixel size, and electronics

Personal view:

- The electronics design is much harder than the design of the sensors.
  - As the community gain experience from present projects, in the next few years, we will witness strong evolution of the electronics.
- Power/cooling will determine:
  - The architecture of 4D tracking detectors (how many layers will be 4D and how many will be 3D)
  - The pixel size and the temporal precisions.



Present sensors for 4D trackers



Hybrid

With built-in gain

Without built-in gain

Low-gain mode (LGADs)

Resistive readout

DC-coupled

AC/DC coupled

Planar

3D

Monolithic

With built-in gain

Without built-in gain

BiCMOS (SiGe)

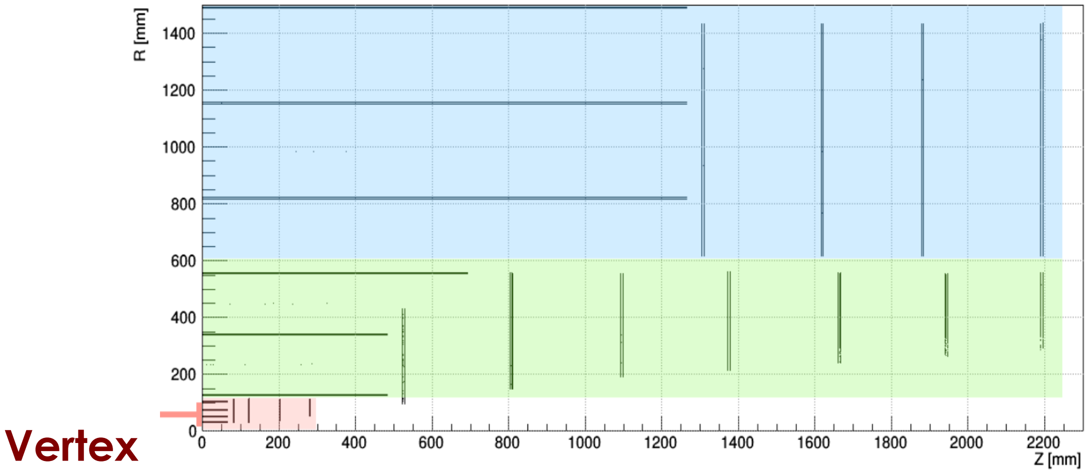
CMOS

Two different environments: vertex and tracking

From a technological point of view, in a generic tracking system, the vertex detector has different needs than the rest of the tracking:

In particular:

- Very high occupancy
  - ==> Small pixels
- Highest radiation
  - ==> fluence >5E15 n/cm^2



These two requirements are well-matched by the capabilities of 3D detectors:

- Very radiation hard, no built-in amplification, (so they should be rather thick)
- Require small pixels (25 x 25 um^2 or 50 x 50 um^2) to have fast signal and small capacitance.

Sensors without internal gain

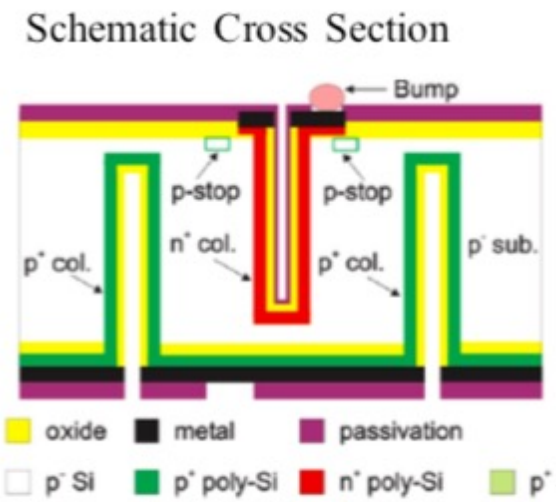
Hybrid

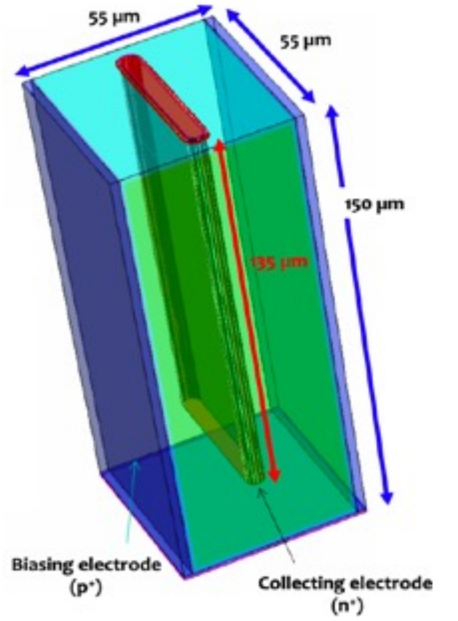
No gain

3D

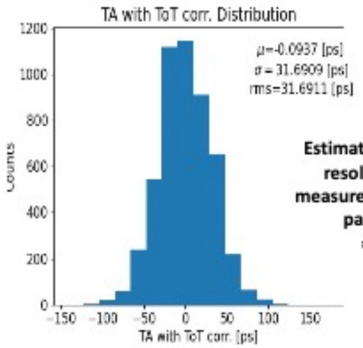
Two possible options:
- Column
- Trenches
- The amount of charge is controlled by the sensor thickness (~1-2 fC)

Both requires small pixels to achieve good temporal precision
==> very good position resolution





Timespot1: 28 nm ASIC



Estimate of full chain resolution using measurement-extacted parameters ≈ 30 ps

Pixels size = 55 μm

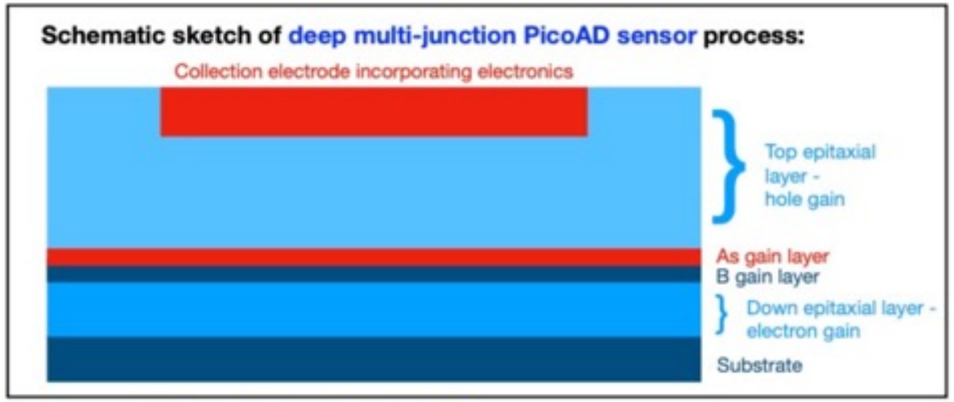
Resolution ASIC+Sensor ~ 30 ps for single channel (about 20 ps per contribution)

Monolithic sensors with internal gain

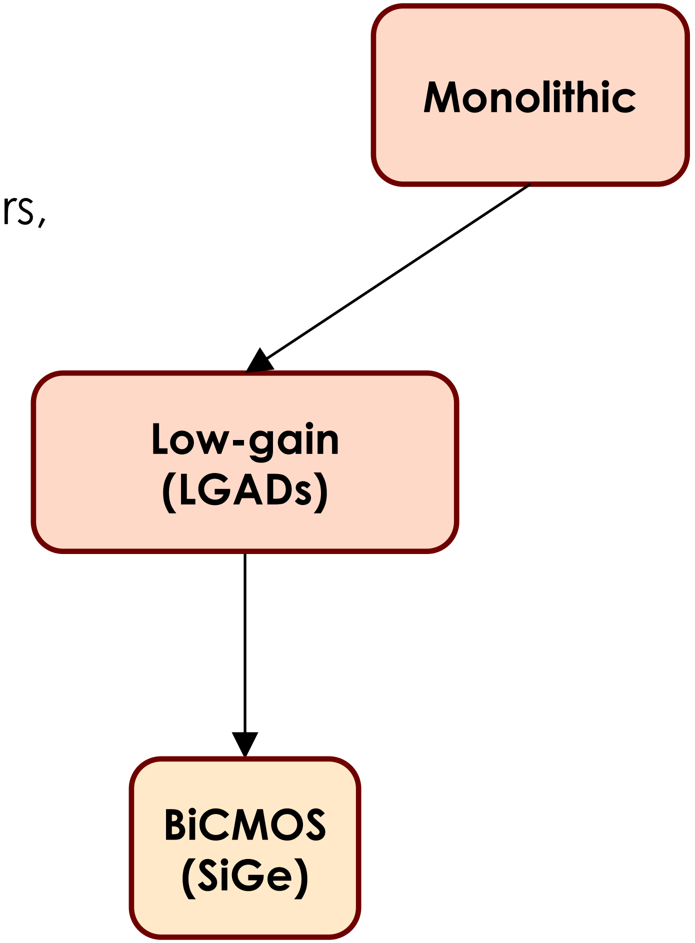
This is a very powerful research path pursued by the **“Monolith” project.**

Monolith merges low noise from SiGe with high dVdt from multiplications.
It aims at reducing the Landau term by using very thin sensors, and high pixelation by buring the high-field avay form the surface junction

Schematic sketch of deep multi-junction PicoAD sensor process:



Placement of gain layer deep inside sensor:
De-correlation from pixel implant size/geometry —> high pixel granularity possible (*spatial precision*)
Only small fraction of charge gets amplified —> reduced Landau charge fluctuations (*timing precision*)



Monolithic

Low-gain (LGADs)

BiCMOS (SiGe)

See R. Cardella ”Monolith”, VCI2022 Thursday afternoon

Setting the stage for FCC-ee

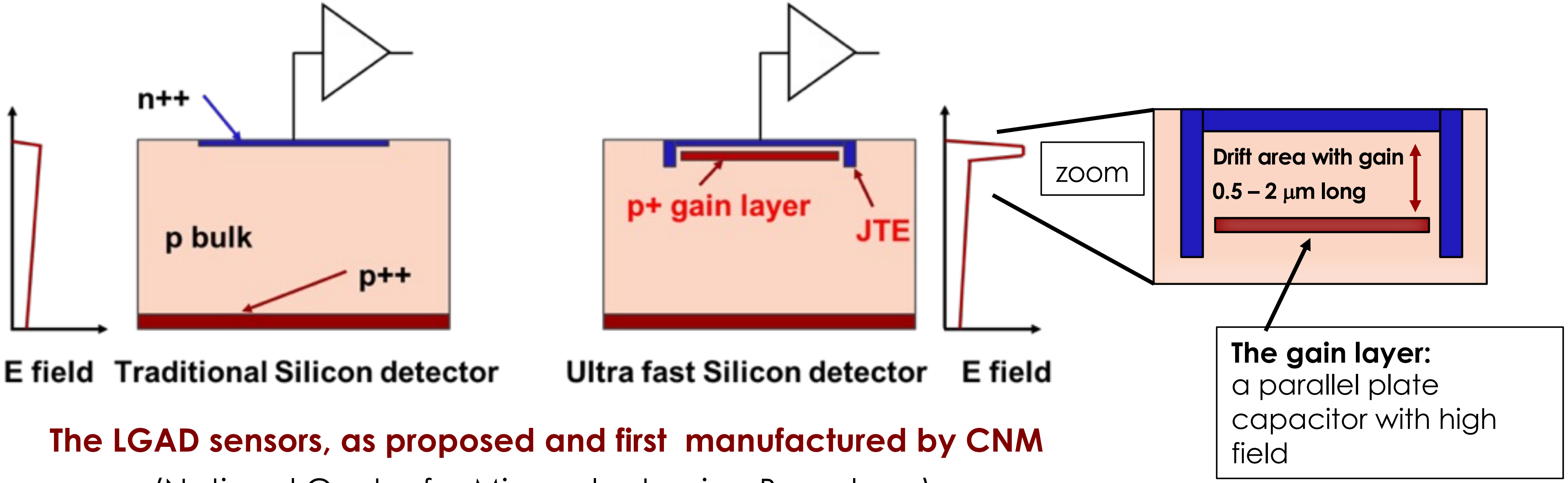
The first step is to define the phase space of the required performances (table from the ECFA Roadmap document)

	Vertex	**Tracker**
Position precision (um)	< 3	~ 6
material X/Xo	0.05	1
Power (mW/cm^2)	20	<100
Rates (GHz/cm^2)	0.05	
Timing precision (ns)	25	< 0.1

Summary:

- **very good spatial and temporal resolutions**
- **very low material budget**
- **very low power consumption**

First design innovation: low gain avalanche diode (LGAD)



The gain layer:
a parallel plate
capacitor with high
field

The LGAD sensors, as proposed and first manufactured by CNM

(National Center for Micro-electronics, Barcelona):

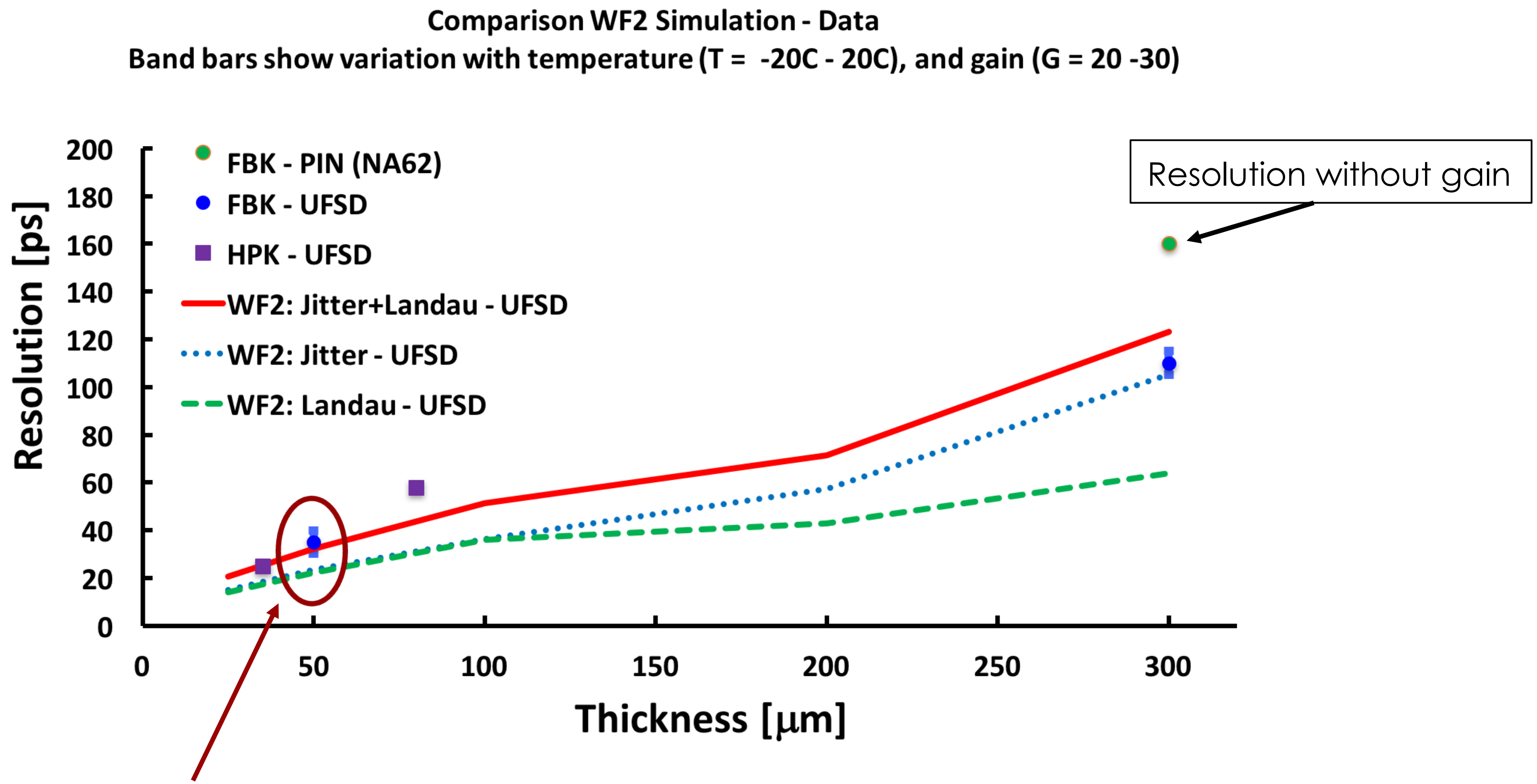
High field obtained by adding an extra doping layer

E ~ 300 kV/cm, closed to breakdown voltage

- The low-gain mechanism, obtained with a moderately doped p-implant, is the defining feature of the design.
- The low gain allows segmenting and keeping the shot noise below the electronic noise, since the leakage current is low.

Low gain is the key ingredient to good temporal resolution

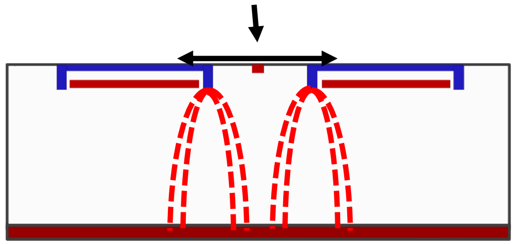
Summary of LGAD temporal resolution



There are now hundreds of measurements on 45-55 μm-thick LGADs

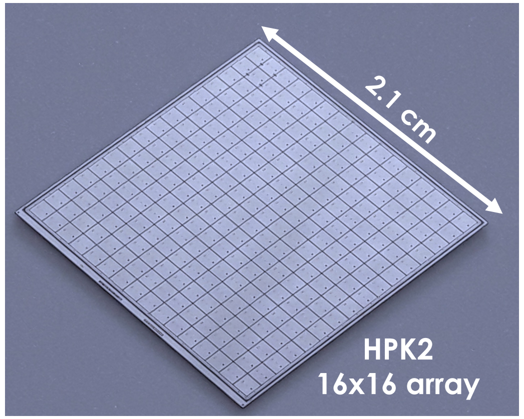
➔ **Current sensor choice for the ATLAS and CMS timing layers**

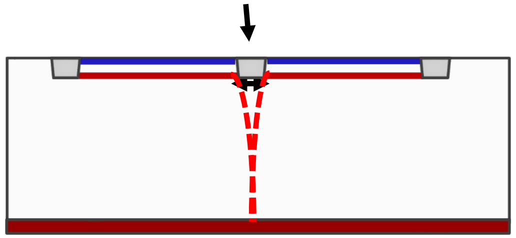
LGAD: State-of-the art


No gain area ~ 50 um

JTE + p-stop design

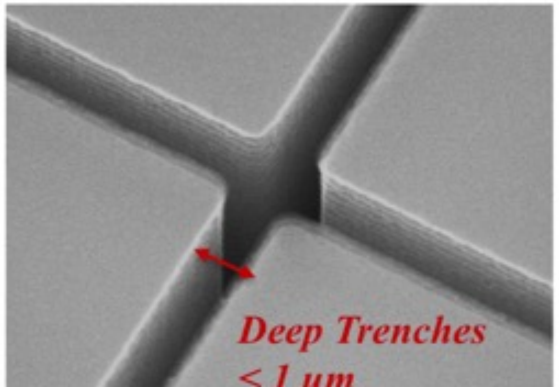
- CMS && ATLAS choice
- Not 100% fill factor
- Very well tested
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness ~ 2-3E15 n/cm2




No gain area ~ 5 um

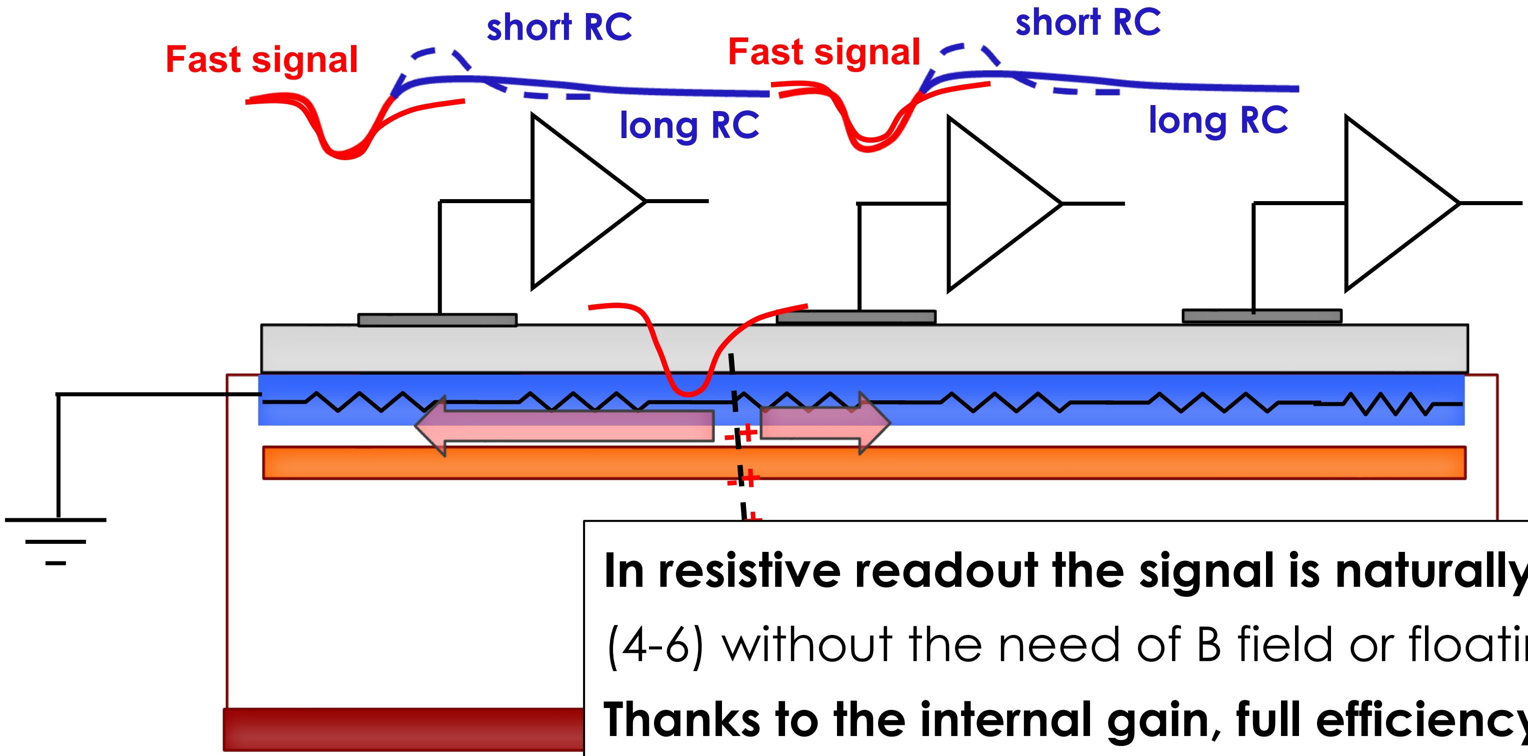
Trench-isolated design

- Almost 100% fill factor
- Temporal resolution (50 μm) : 35-40 ps
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness: to be studied



Second design innovation: resistive read-out (Tredi conf. 2015)

- **The signal is formed on the n+ electrode ==> no signal on the AC pads**
- **The AC pads offer the smallest impedance to ground for the fast signal**
- **The signal discharges to ground**

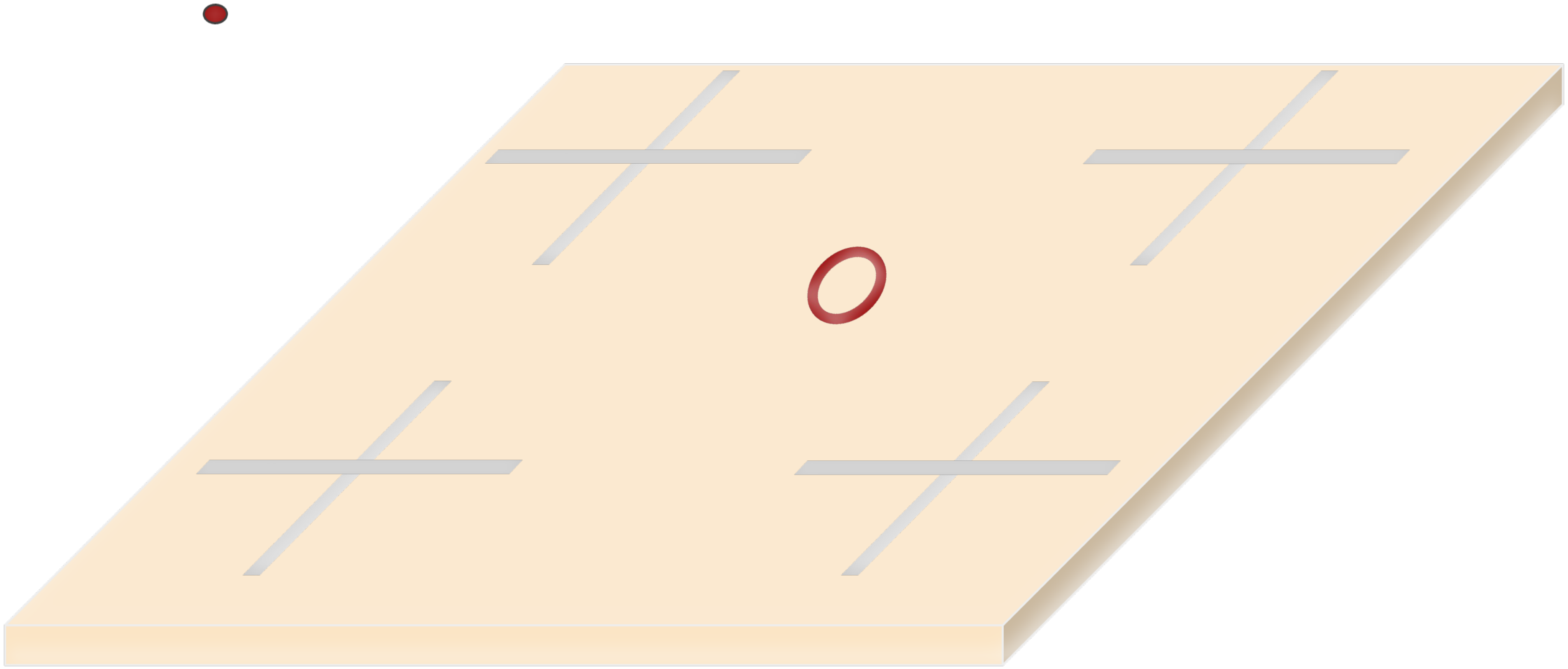


In resistive readout the signal is naturally shared among pads (4-6) without the need of B field or floating pads

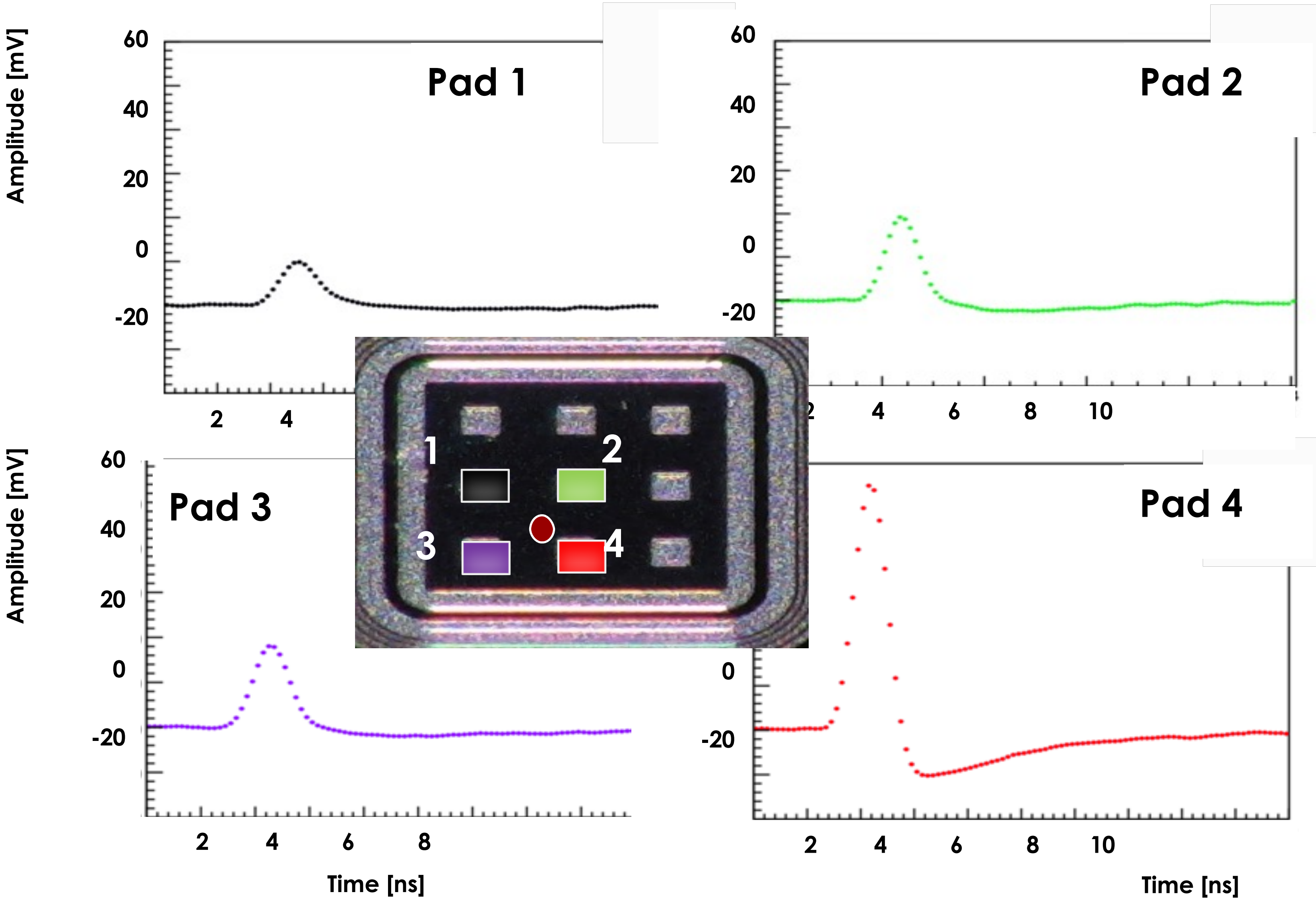
Thanks to the internal gain, full efficiency even with sharing

Results presented here are from the FBK RSD2 production

RSD principle of operation in motion



Example of signal sharing

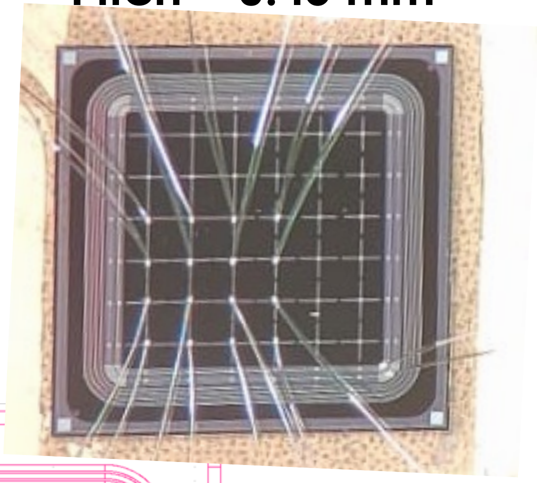


50-mm thick RSD, Gain ~ 20

The laser is shot at the position of the red dot: the signal is seen in 4 pads

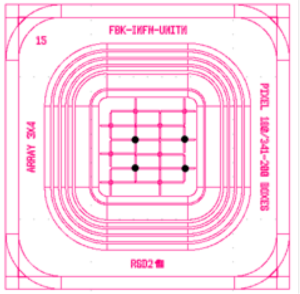
Example: FBK production of resistive silicon sensors

Pitch = 0.45 mm



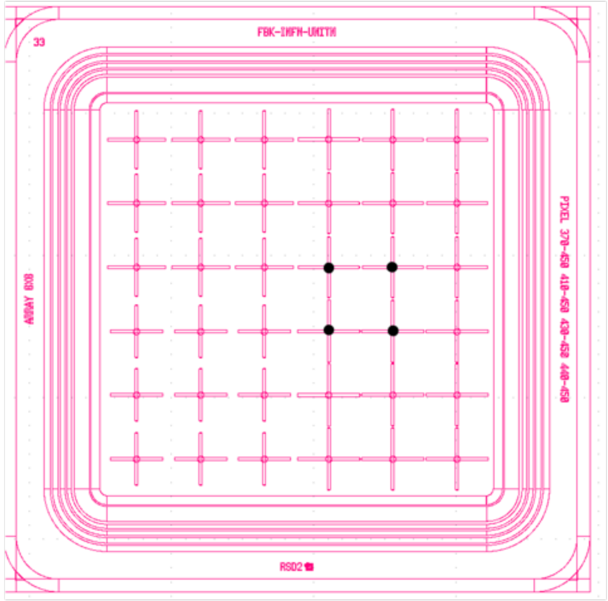
To optimize the signal spread, the electrodes are cross-shaped

4 different dimensions: 200, 340, 450, and 1300 μm



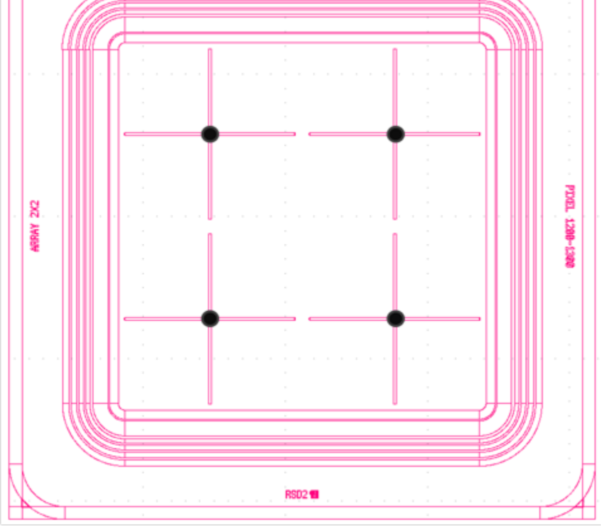
(A)

200 x 340 μm²



(B)

Pitch = 450 μm



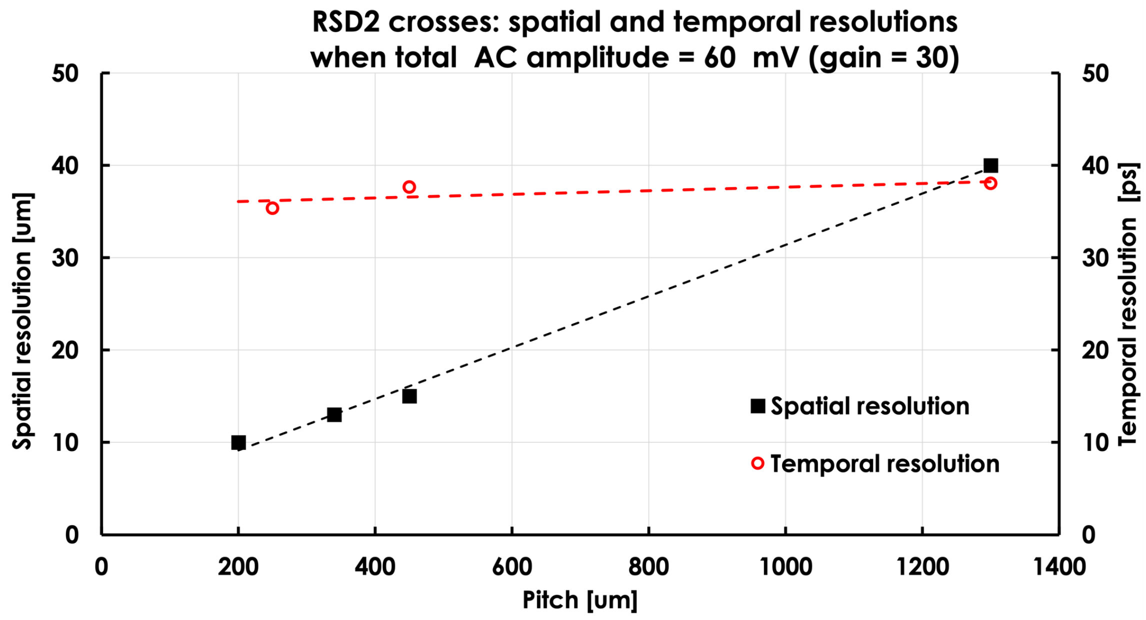
(C)

Pitch = 1300 μm

RSD2 performance summary

Spatial resolution ~ 3% of the pixel pitch

Temporal resolution ~35-40 ps (50 um thick)

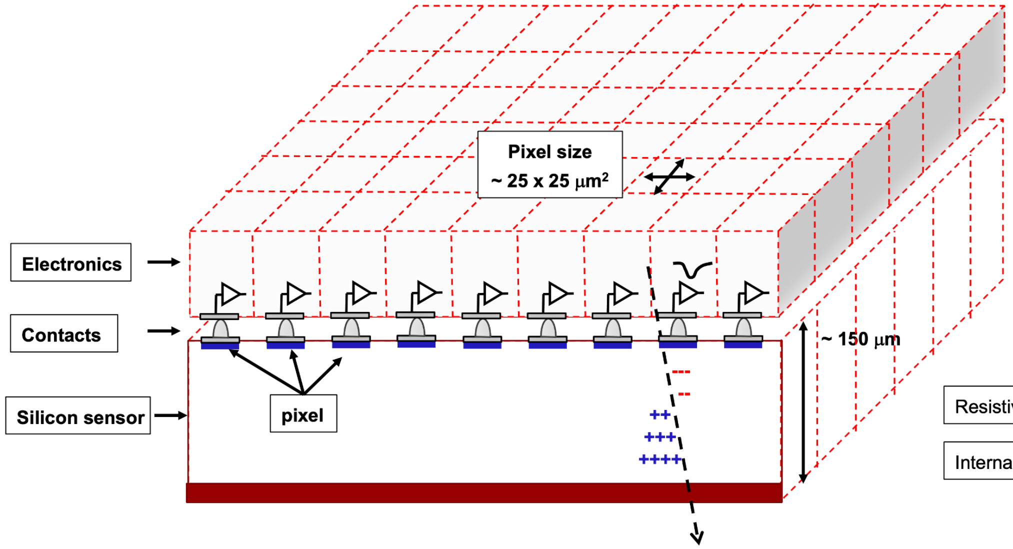


Key message:

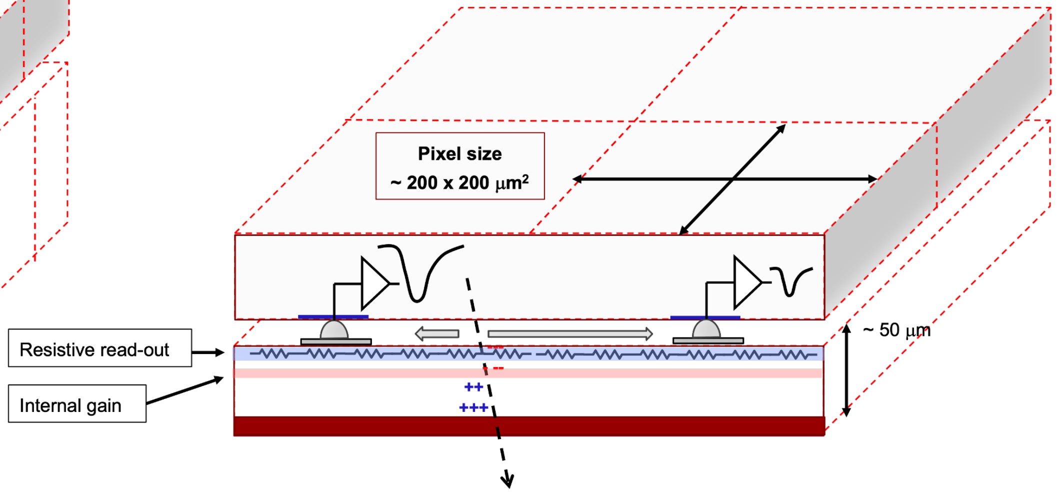
even very large pixels achieve excellent position and spatial resolutions

==> no need to use smal pixels, it saves a lot of power

RSD based tracker: low power, low material budget



Standard tracker



RSD-based tracker

The design of a tracker based on RSD is truly innovative:

- It delivers ~ 20 - 30 ps temporal resolution
- For the same spatial resolution, the number of pixels is reduced by 50-100
- The electronic circuitry can be easily accommodated
- The power consumption is much lower; it might even be air-cooled (~ 0.1-0.2 W/cm^2)
- The sensors can be really thin, very low material budget

Conclusions

Very strong R&D in the field of 4D tracking

- In a 4D tracker, not all layers need to be 4D-capable
- Power will be the driving constraint,
  - it is "very difficult" to do excellent timing without a lot of power
- Vertex detectors (high occupancy, high radiation levels) require unique solutions.
- New developments (monolithic, SiGe, built-in gain, resistive read-out) might match the requirements of FCC 4D tracking needs

Where the R&D will happen: DRD3 (implementation of the ECFA roadmap)

Town meeting: March 22-23rd.

Join DRD3 and participate!

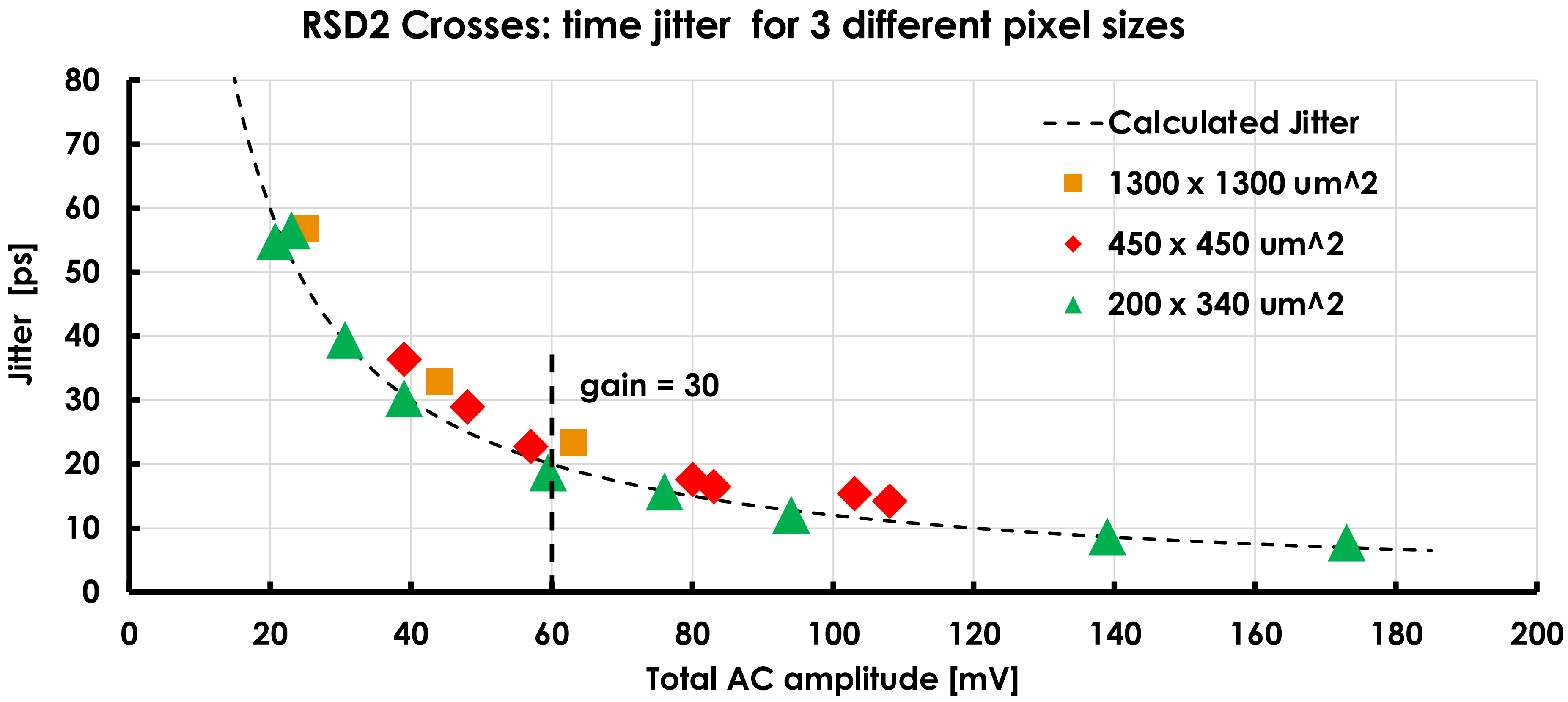
https://indico.cern.ch/event/1214410/

Extra

RSD temporal resolution (FBK RSD2 production)

The resolution depends mostly upon the signal size and **weakly on the pixel size**

RSDs at gain = 30 achieve a temporal jitter of about 20 ps



RSD position resolution (FBK RSD2 production)

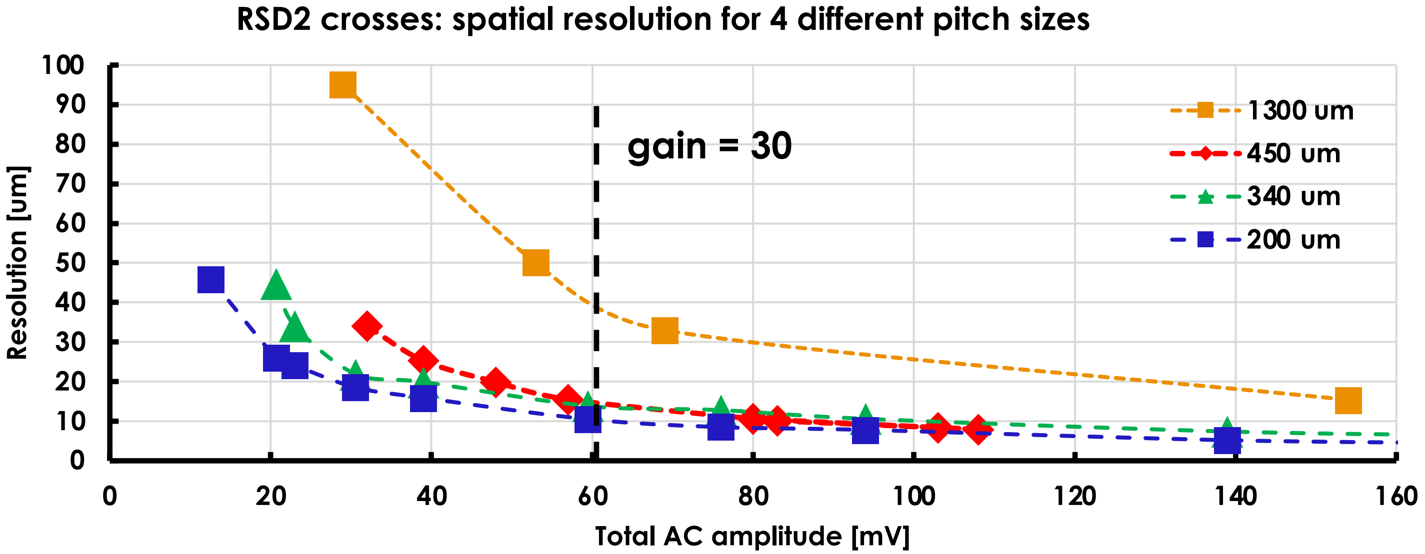
RSDs at gain = 30 achieve a spatial resolution of about 2-3% of the pitch size:

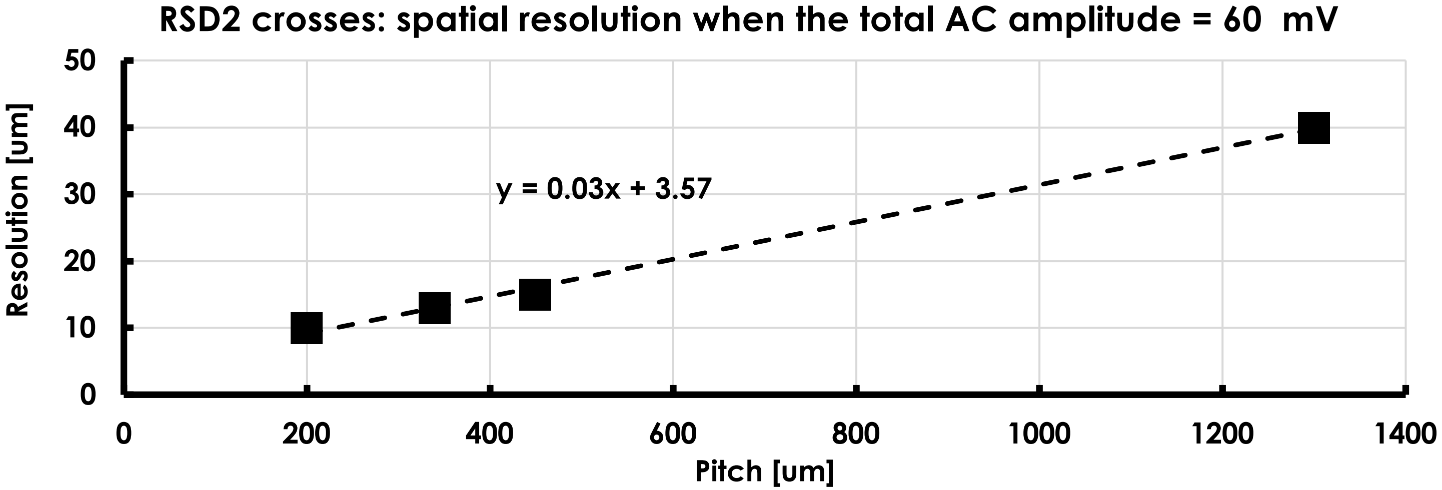
RSD:

- **1300 x 1300 mm^2: $\sigma_x \sim 40\ \mu m$**
- **450 x 450 mm^2: $\sigma_x \sim 5\ \mu m$**

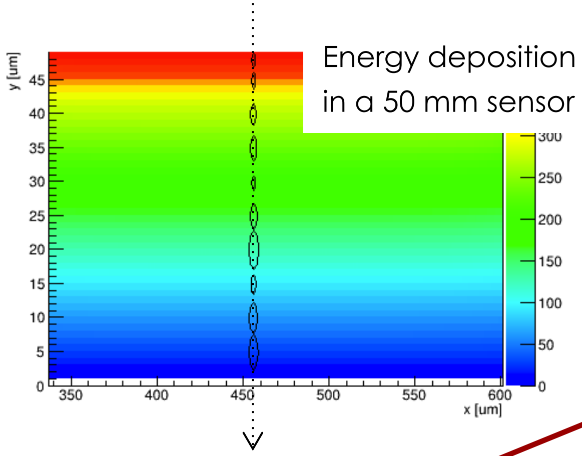
Compared to a standard pixel

- **1300 x 1300 mm^2: $\sigma_x \sim 920\ \mu m$**
- **450 x 450 mm^2: $\sigma_x \sim 320\ \mu m$**

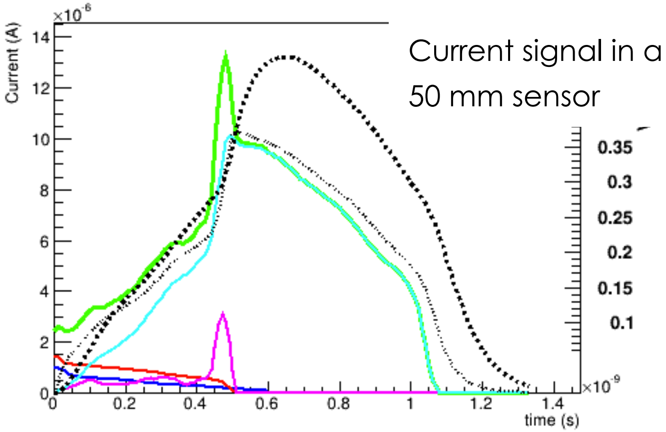

RSD2 crosses: spatial resolution for 4 different pitch sizes


RSD2 crosses: spatial resolution when the total AC amplitude = 60 mV

Brief considerations about electronics: pre-amp design



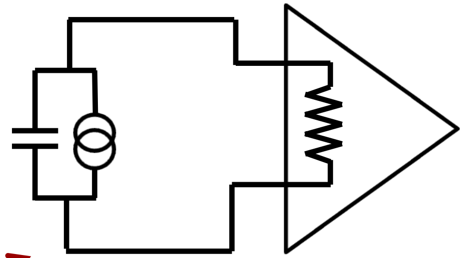
Energy deposition in a 50 mm sensor



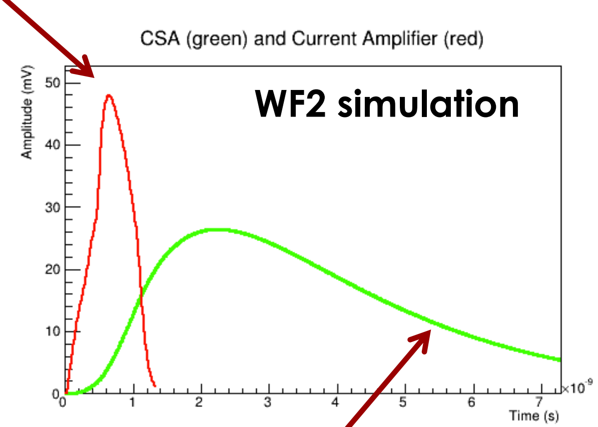
Current signal in a 50 mm sensor

WF2 simulation

Current Amplifier

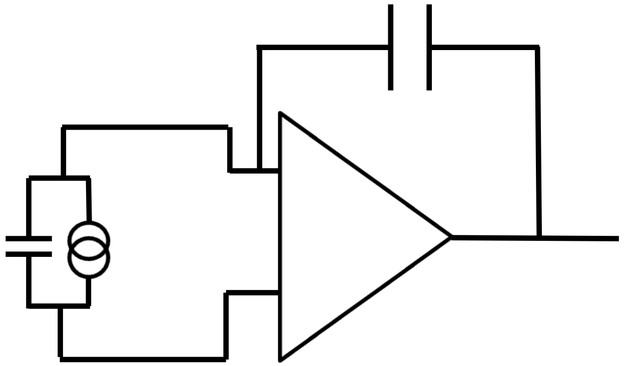


- Fast slew rate
- Higher noise
- Sensitive to Landau bumps



WF2 simulation

Charge Sensitive Amplifier



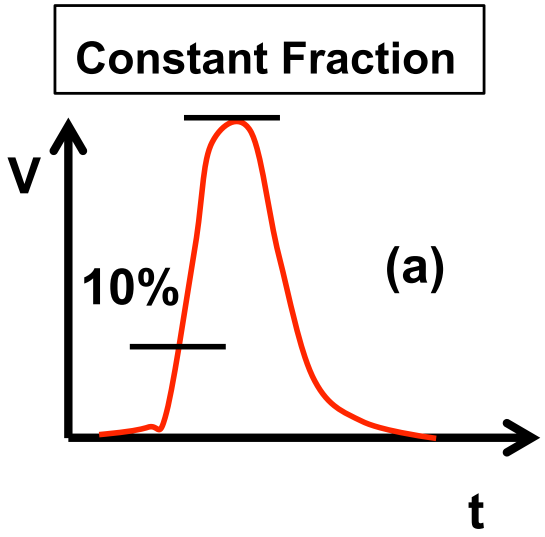
- Slower slew rate
- Quieter
- Integration helps the signal smoothing

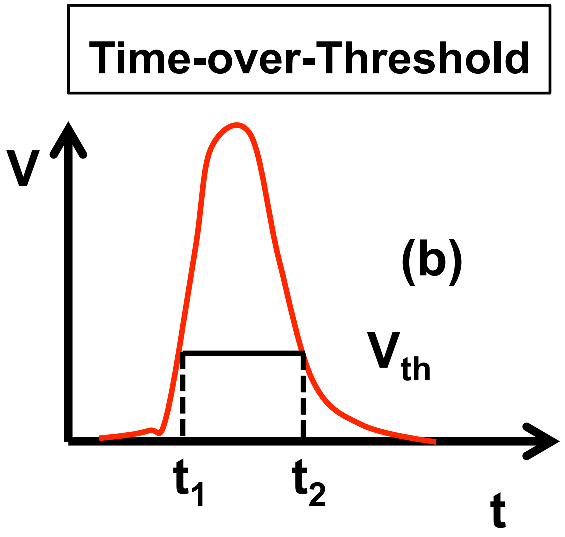
NOT MY TALK!!

Experts in the room…

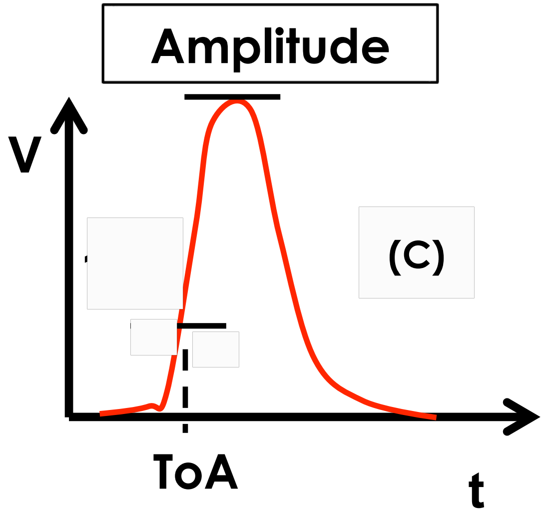
Brief considerations about electronics: Time walk corrections

On paper both seem feasible,
in practice
ToT is much easier to implement





My favorite: **ToA and Amplitude**
➔ The tail of the signal is prone to changes due to charge trapping

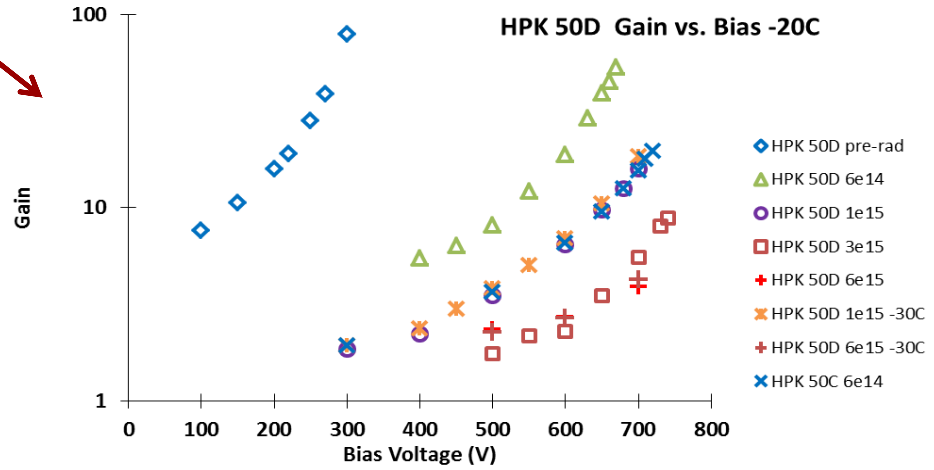


Radiation hardness of the gain implant

Irradiation decreases the active doping in the gain layer

Acceptor removal,
Gain layer deactivation

$$N(\emptyset) = N(0) * e^{-c\emptyset}$$



Concluded R&D

Defect Engineering of the gain implant

- Carbon co-implantation mitigates the gain loss after irradiation

Modification of the gain implant profile

- Narrower Boron doping profiles with high concentration peak are less prone to be inactivated

Future R&D

Compensation: gain implant obtain as difference of p- and n- doping

- Concurrent acceptor and donor removal might limit the disappearance of effective doping

Carbon shield:

- A deep implant of carbon might prevent defects to reach the gain implant

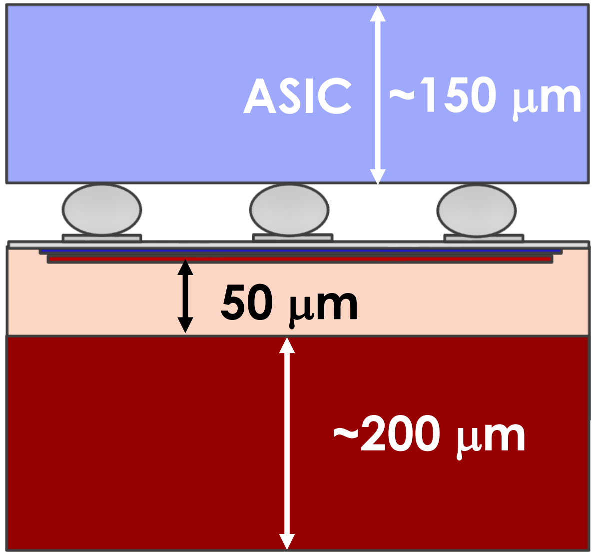
See V. Sola "Silicon sensors for extreme fluences", VCI2022 Thursday afternoon

Reduced material budget

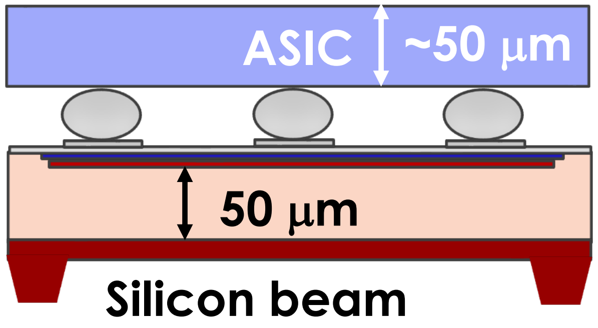
The active thickness of UFSD sensor is rather small ~ 50 um.

In the present prototypes, the active part is attached to a thick "handle wafer"

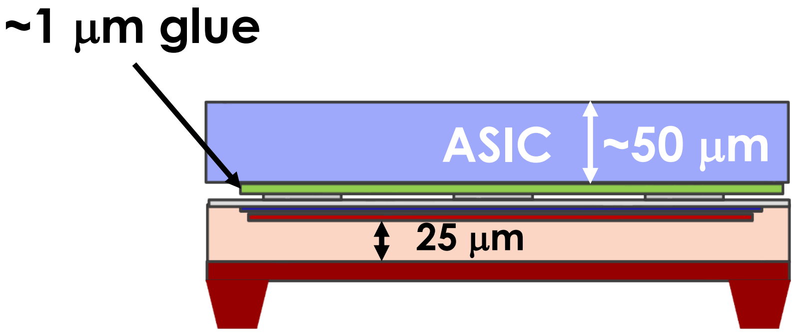
There is a clear path leading to < 100 μm material:



Present design: no material budget optimization



- Thinned handle wafer:
  500 um ➔ 10-20 um



- Thinned handle wafer:
  500 um ➔ 10-20 um
- Thinned active area:
  50 um ➔ 25 um
  50 ps ➔ 25 ps