AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Readout electronics for Magnet Station

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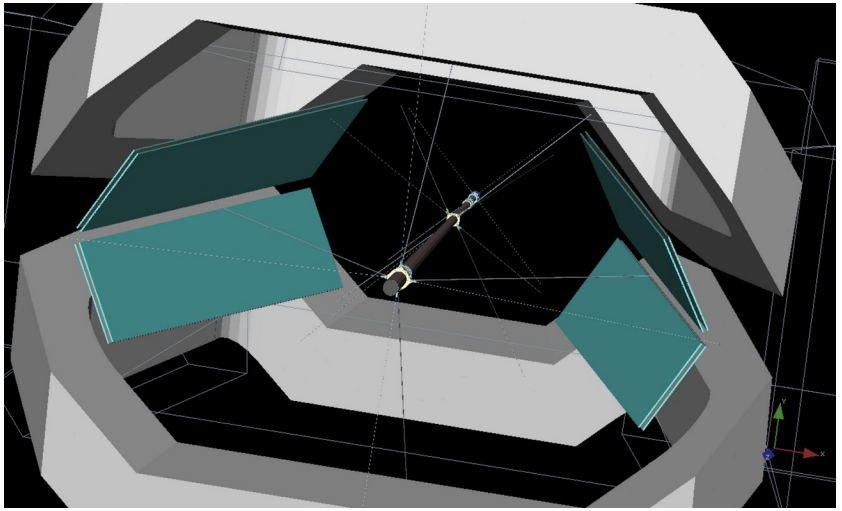
Outline

- Intoduction
- Magnet Station Readout for Upgrade 1b
  - SiPM board, PACIFIC, Cluster board, Tracking board
- Magnet Station Readout for Upgrade 2
- Summary and Plans

Magnet Station Readout in Upgrades

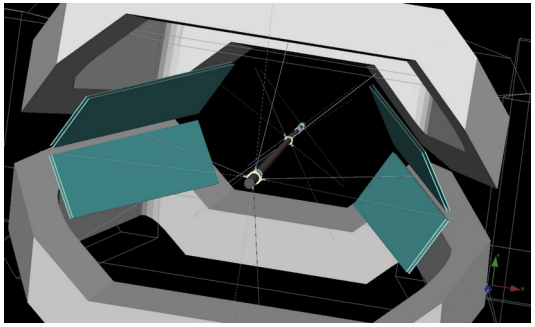
- Magnet Station detector, based on scintillating fibers and SiPMs, is planned to be added for Upgrade 1b and Upgrade 2
- MS readout will include high performance FPGA-based back-end to obtain particle trace information online
  - In Upgrade 1b the front-end will be based on existing PACIFIC chips from SciFi detector
  - For Upgrade 2 new front-end ASICs, delivering the amplitude and timing information, are foreseen



Magnet Station architecture & No. of channels

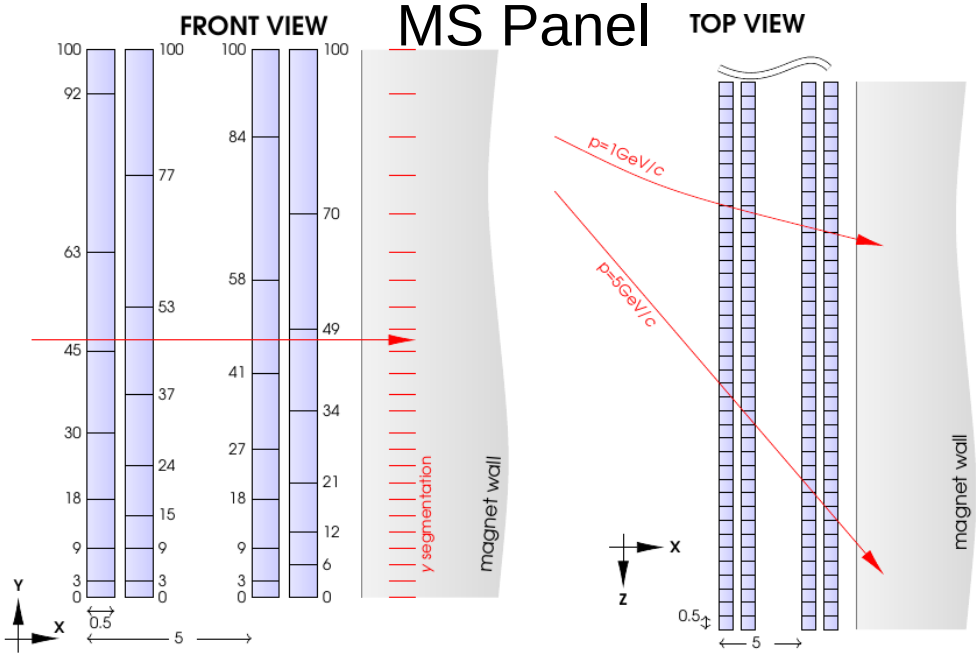
- **MS** detector has 4 **panels**
  - Each **panel** is built with 4 **layers**
    - Each **layer** has ~5600 **channels**:
      - 7-8 **channels** in "y" for each „z" segment
      - ~5600/8 = ~700 **channels** in "z"
- Channels in total:
  - 4 layers * 5600 channels = 22400 channels/panel
  - 4 panels * 22400 = 89600 channels in MS

- To obtain a resolution of ~0.6 mm in "z" a detector segmentation of 5mm was selected. A coarser and non-uniform segmentation in "y" was adopted



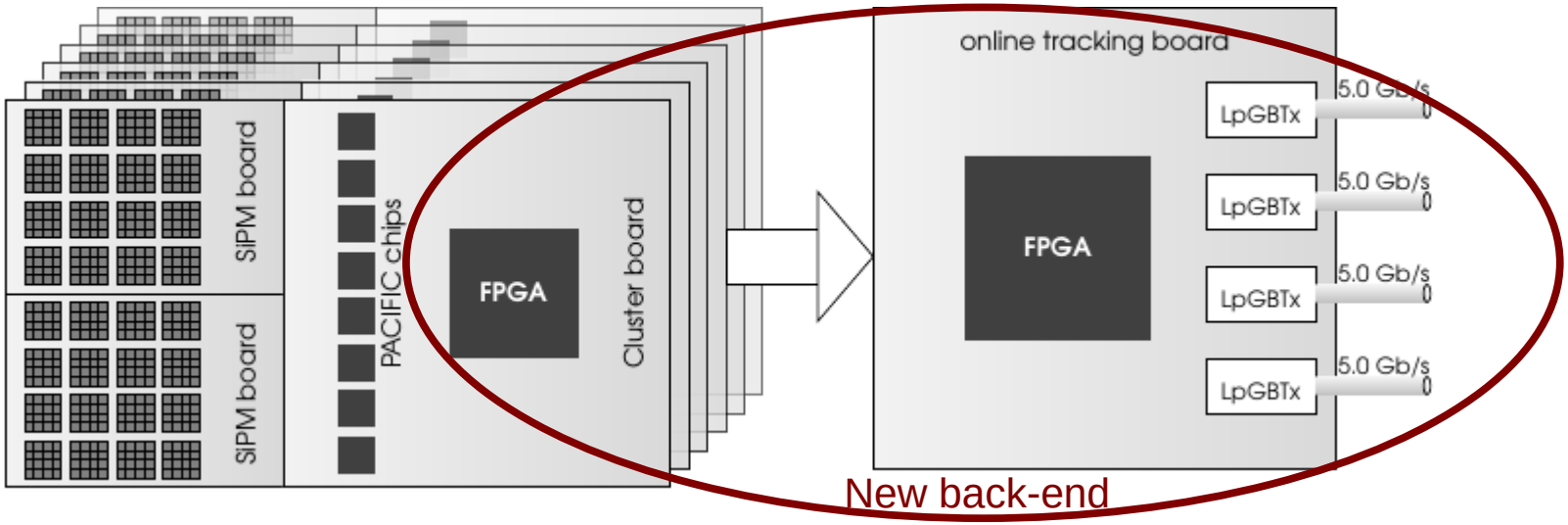
MS Detector

MS Panel



Not in scale, numbers are panel coordinates and sizes in cm

Upgrade 1b MS Readout Architecture
SiPM boards, PACIFICs, and new Back-end

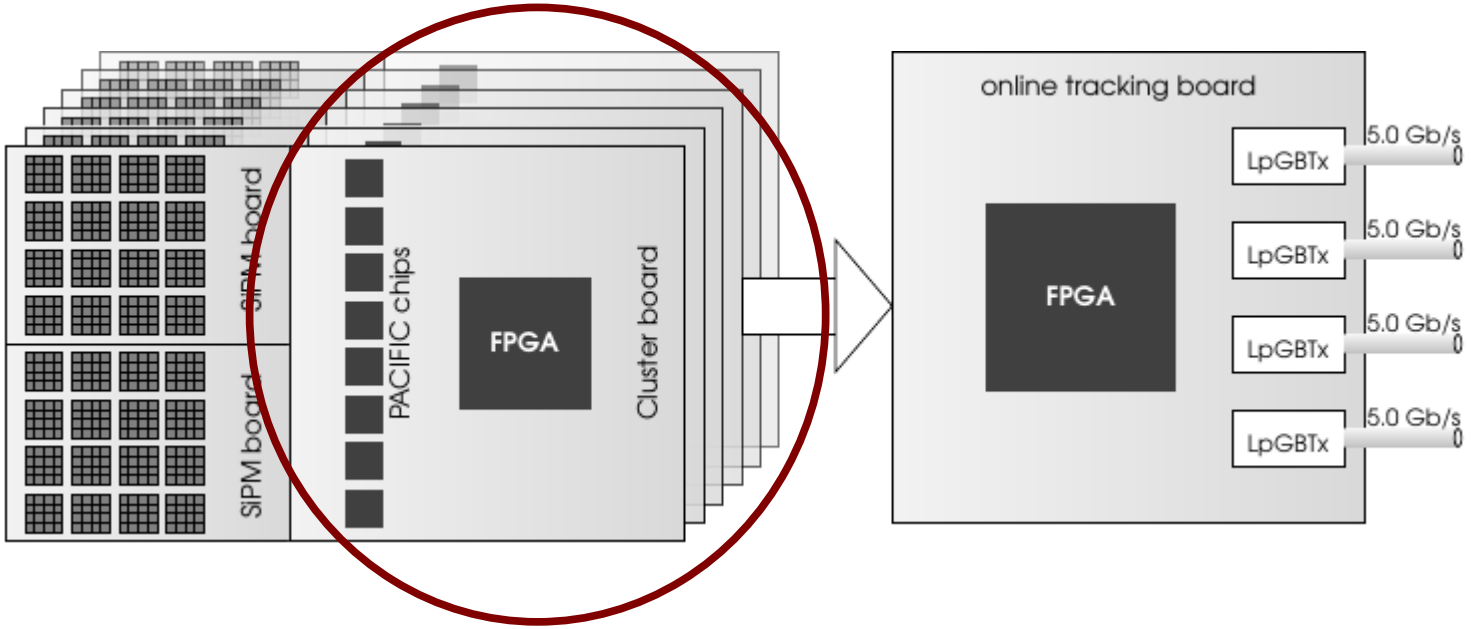


SiPM boards (2x256chan) with New Back-end:

⇨ Cluster boards (8 PACIFICs=512chan + FPGA)

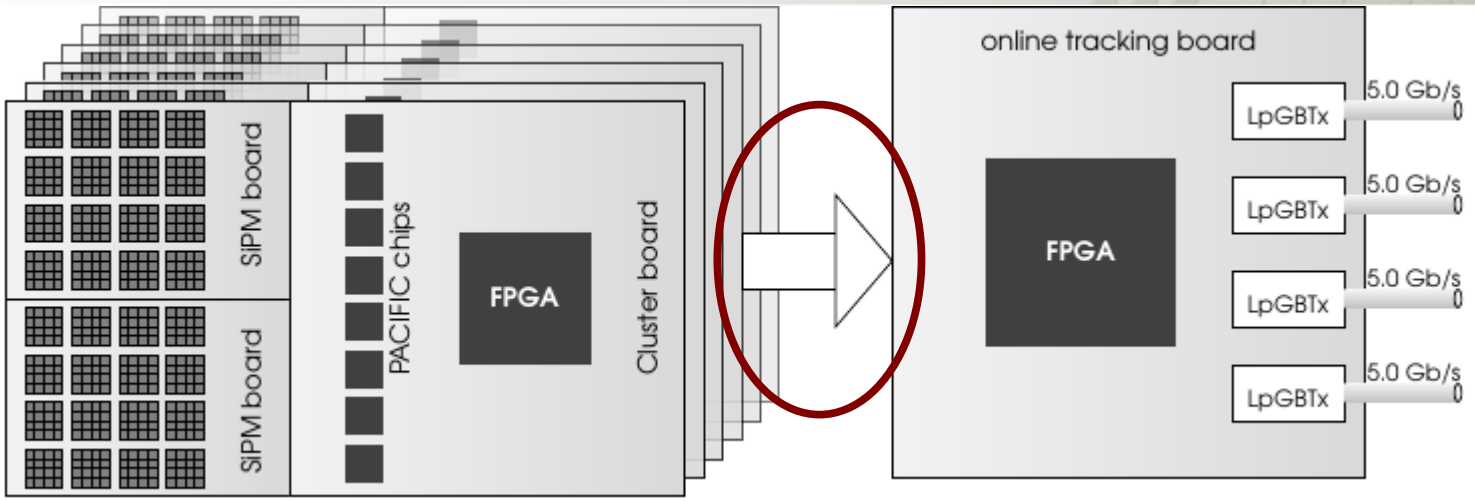
⇨ Tracking boards

Upgrade 1b MS Readout Architecture
Cluster board considerations



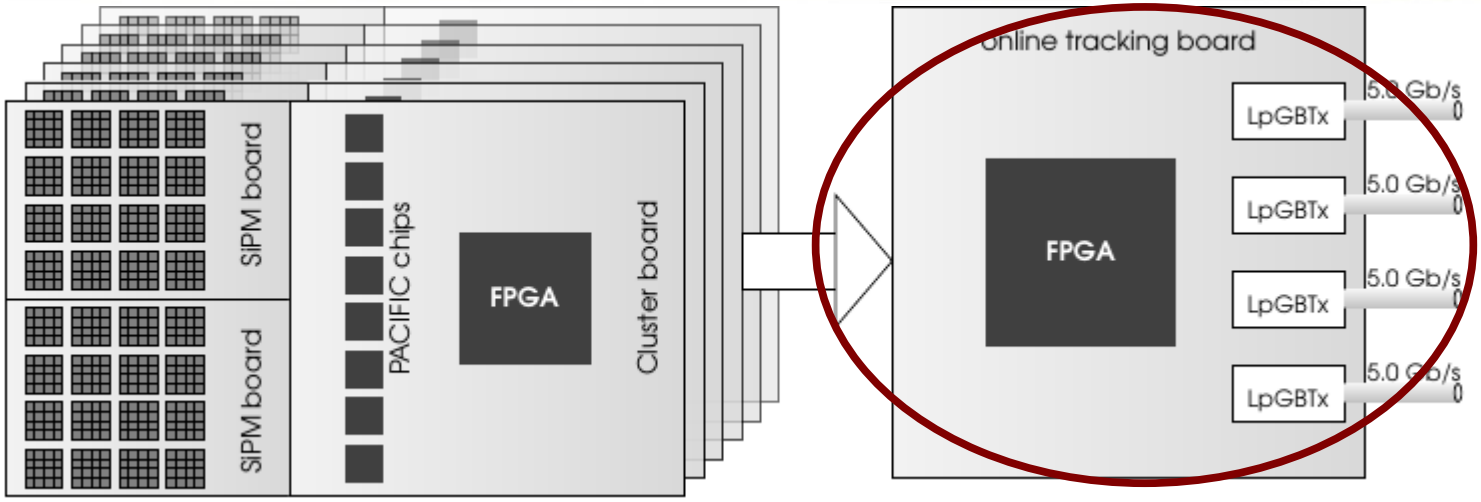
- Per panel there are 22400/512 =~ 44 Cluster boards, followed by Tracking board(s)
- Cluster board – FPGA considerations:
  - To serve 8 PACIFICs the FPGA should have about 136 differential inputs and 128 single-ended inputs
  - To handle the above number of inputs possible FPGAs are: Xilinx Kintex7 XC7K70T (65K Logic Cells) or higher XC7K160T (162K Logic Cells), up to XC7K410T(410K Logic Cells)

Upgrade 1b MS Readout Architecture
Data rate from Cluster board to Tracking board



- For 512-channel ClusterBoard (64 chan. in „z” * 8 chan. in „y”) the data size per cluster:
  - 6 bits (64 channels in "z") + 3 bits (fine inter-segment resolution in "z") +
  - 4 bits (cluster size in "z") +
  - 3 bits (7-8 channels "y") + 1 bit (resolution in "y") =
  - 6+3+4+3+1 = 17 bits/cluster Remark! 11Bits/cluster - Cesar slides…, clarify
- From simulations ~6.3 clusters per Cluster board (512 channels) per event are expected
- Cluster board output rate = 40MHz (clock) * 6.3 (clusters/event) * 17 bits/cluster = 4.3 Gbps
- Remark! 7 Gbps - Cesar slides…, clarify
- One high speed serial output link per Cluster board should be enough

Upgrade 1b MS Readout Architecture
Tracking board considerations



- Assuming 44 Cluster boards per panel, each with single high speed output link, Tracking board(s) serving 44 high speed input links are needed
- Assuming data reduction in Tracking board by factor 4-5, about 10 high speed output links are needed
- Would it be possible to limit the number of Tracking boards to only ONE per panel ? Assuming sufficient computing power (to be verified!) there are few FPGAs able to handle the needed number of high speed data links:
  - XilinxVirtex-7 XC7VX550T (80 GTH 13.1Gbps, 555K Logic Cells)
  - XilinxVirtex-7 XC7VX1140T (96 GTH 13.1Gbps, 1140K Logic Cells)

Enough for LUT in the Panel ?

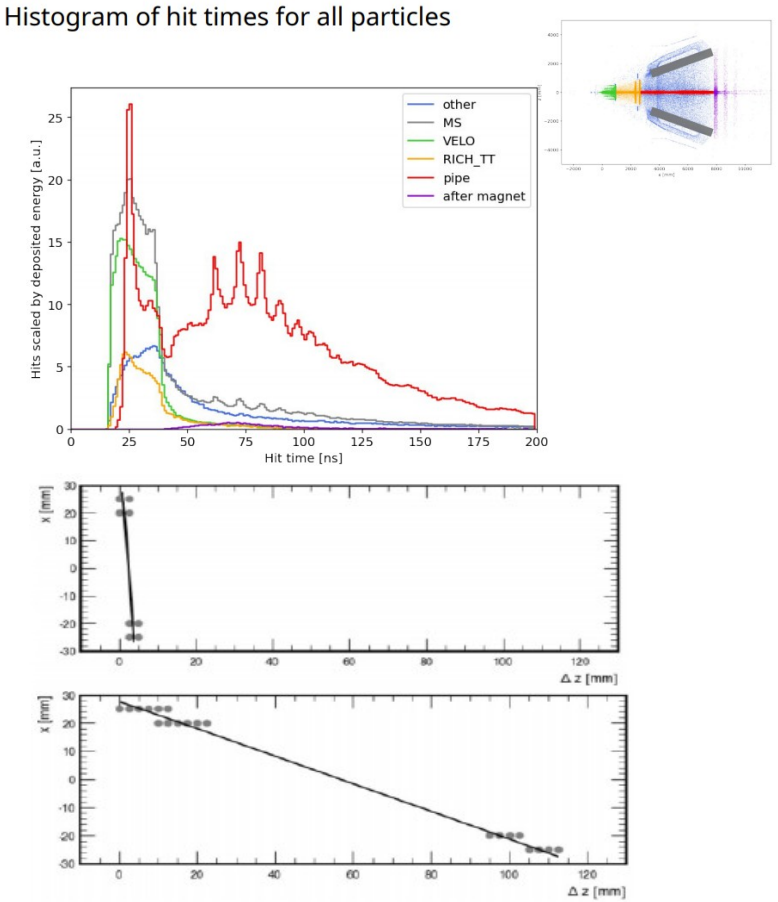
Upgrade 1b MS Readout Architecture
Near future – to do...

- Short term: We would like to „put hands” on existing SciFi readout and get acquainted practically with this system
- Next step: Start the design of the Cluster board
- Tracking board issues – we would like to get procedures or code or LUT in order to estimate/simulate computing resources needed...

Upgrade 2 MS Readout
New Readout ASIC with TDC and more ADC bits

- Majority of tracks come from slow particles produced inside the magnet and detector material
- TDC is needed to make large rejection of tracks coming from very slow particles
- Requested TDC resolution – simulations and discussions in progress...

- For online tracking clustering is an important step, in particular for large slope tracks
- More ADC bits would help in clustering and reduction of ghost tracks
- Requested ADC resolution – simulations and discussions in progress...



At the moment, the design has not yet started, only general discussions, since the readout for Upgrade 1b is a priority.

Could such new ASIC serve as common scintillator readout in the Tracker?

Summary and Plans

- Works on the Readout of Magnet Stations for LHCb upgrades, particularly on its general architecture, have been started
- Because of the time-scale, presently we focus mainly on the Upgrade 1b MS Readout, which uses PACIFIC chips and needs new Cluster and Tracking boards. In next step we would like to:
  - assemble the setup with existing SciFi SiPM&PACIFIC boards plus an FPGA development board
  - start design of the Cluster board
  - study computing resources needed in the Tracking board
- In parallel some thoughts are also given to new Readout ASIC for Upgrade 2. Definitely more simulations and discussions are needed to understand better the required specs.