Welcome to the University of Geneva and to the

MONOLITH

workshop

UNIVERSITÉ DE GENÈVE

Swiss National Science Foundation

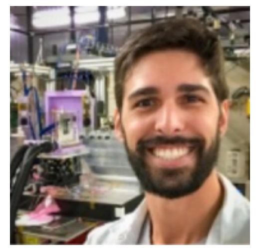
European Research Council
Established by the European Commission

The UNIGE silicon Team

Giuseppe Iacobucci
- project P.I.
- System design

Thanushan Kugathasan
- Lead chip design
- Digital electronics

Roberto Cardella
- Sensor design
- Laboratory test

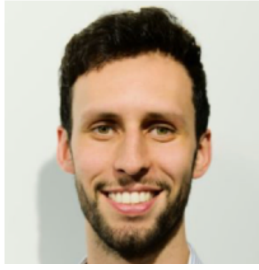


Mateus Vicente
- System integration
- Laboratory test

Matteo Milanesio
- Laboratory test
- Data analysis

Antonio Picardi
- Chip design
- Firmware

Jihad Saidi
- Laboratory test
- Data analysis



Carlo Alberto Fenoglio
- Chip design
- Firmware

Lorenzo Paolozzi
- Sensor design
- Analog electronics

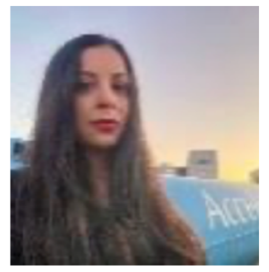
Magdalena Munker
- Sensor design
- Laboratory test

Stefano Zambito
- Laboratory test
- Data analysis

Fulvio Martinelli
- Chip design
- Firmware

Théo Moretti
- Laboratory test
- Data analysis

Chiara Magliocca
- Laboratory test
- Data analysis



Rafaella Kotitsa
- Sensor simulation

Luca Iodice
- Chip design
- Firmware

Didier Ferrere
- System integration
- Laboratory test

Sergio Gonzalez-Sevilla
- System integration
- Laboratory test

Yannick Favre
- Board design
- RO system

Stéphane Débieux
- Board design
- RO system

Main research partners:

Roberto Cardarelli
INFN Rome2 & UNIGE

Holger Rücker
IHP Mikroelektronik

Marzio Nessi
CERN & UNIGE

Funded by:

Swiss National Science Foundation

European Research Council — Established by the European Commission

Sinergia

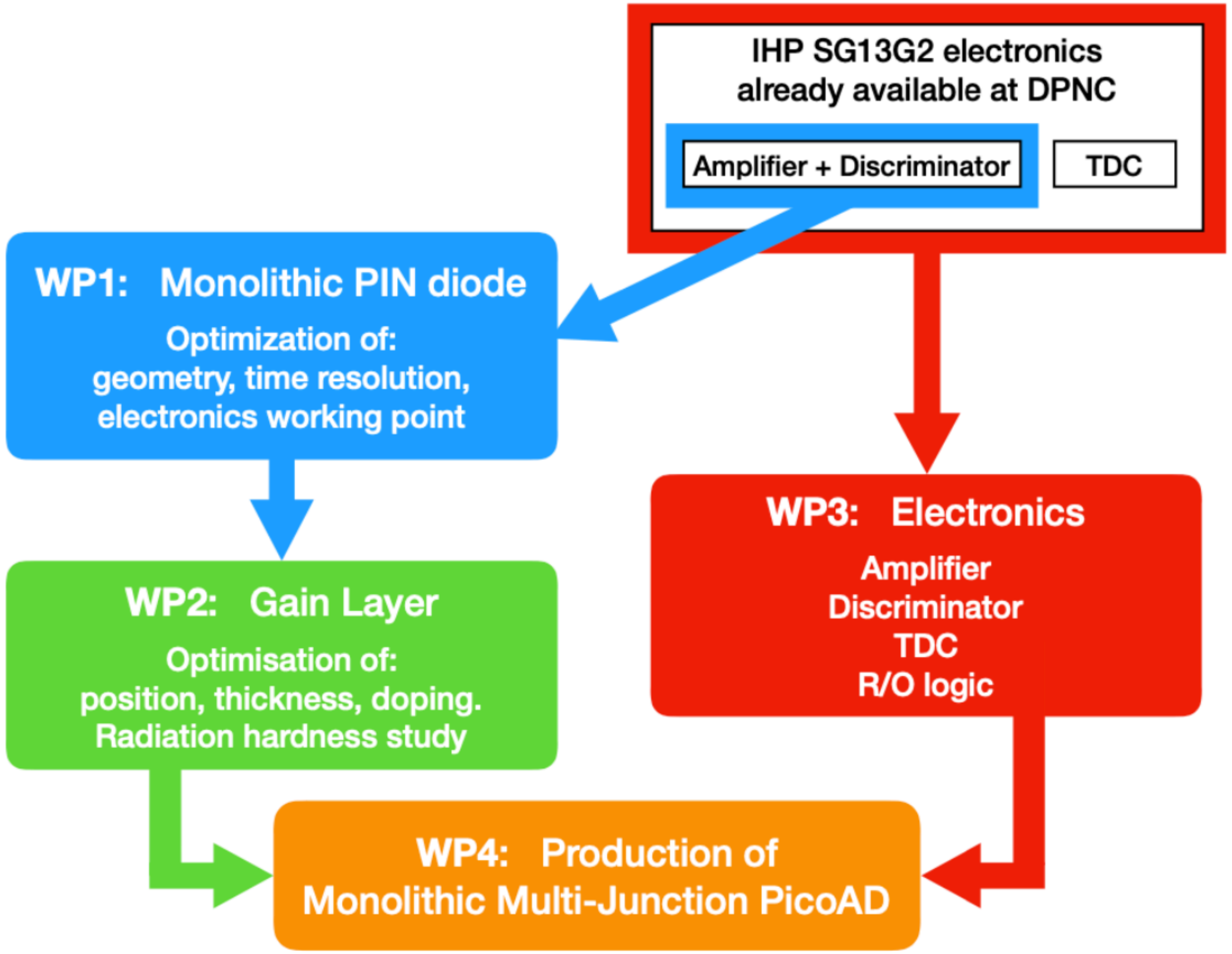
ATTRACT

UNIVERSITÉ DE GENÈVE | UNITEC

What is MONOLITH ?

Funded by the H2020 ERC Advanced grant 884447[1]
2020 - June 2025, to produce:

- **Monolithic silicon sensor** able to:
  - precisely measure 3D spatial position of charged particles and at the same time
  - provide picosecond time resolution
- **NEEDS**:
  1. Fast and low-noise **SiGe BiCMOS** electronics
  2. Novel sensor concept: the **Picosecond Avalanche Detector (PicoAD)**



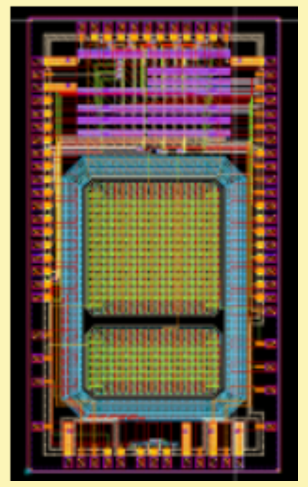
- **Summer 2025:** delivery of full-reticle chip with 50µm pitch

[1] MONOLITH H2020 ERC Advanced Project Web Page - https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/monolith-erc-advanced-project/

MONOLITH: First PicoAD Prototype

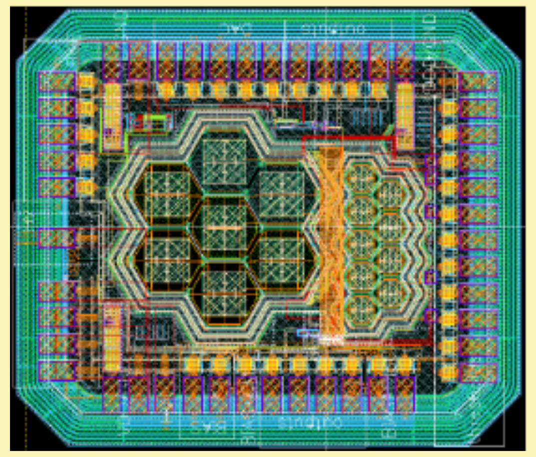
Prototypes without internal gain layer

2016

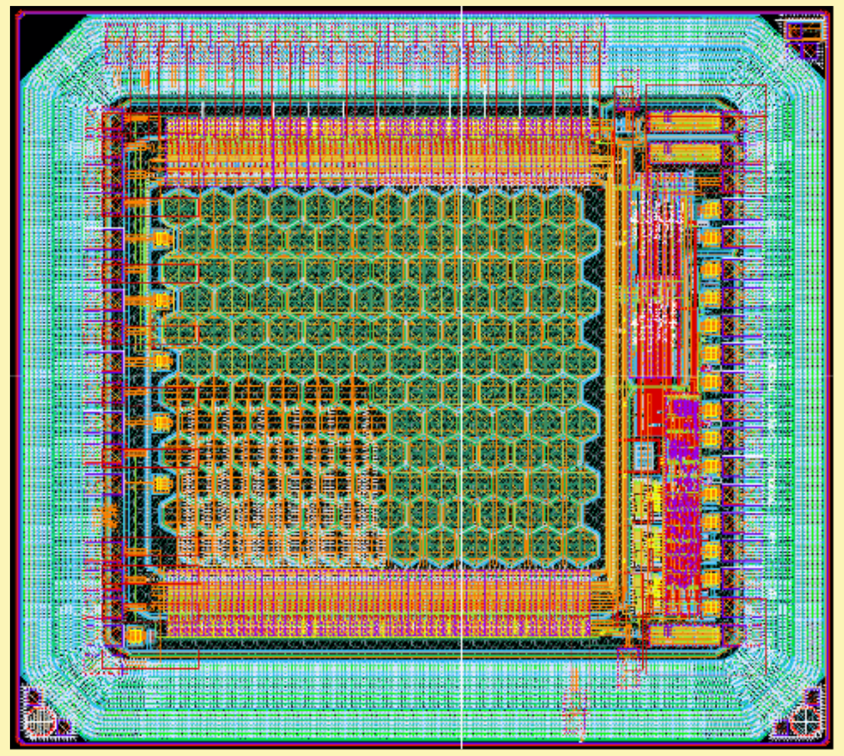


2017

2018



2019



200ps
- 1 and 0.5 mm^2 pixels
- Discriminator output

110ps
- 30 pixels 500x500µm^2
- 100ps TDC +I/O logic

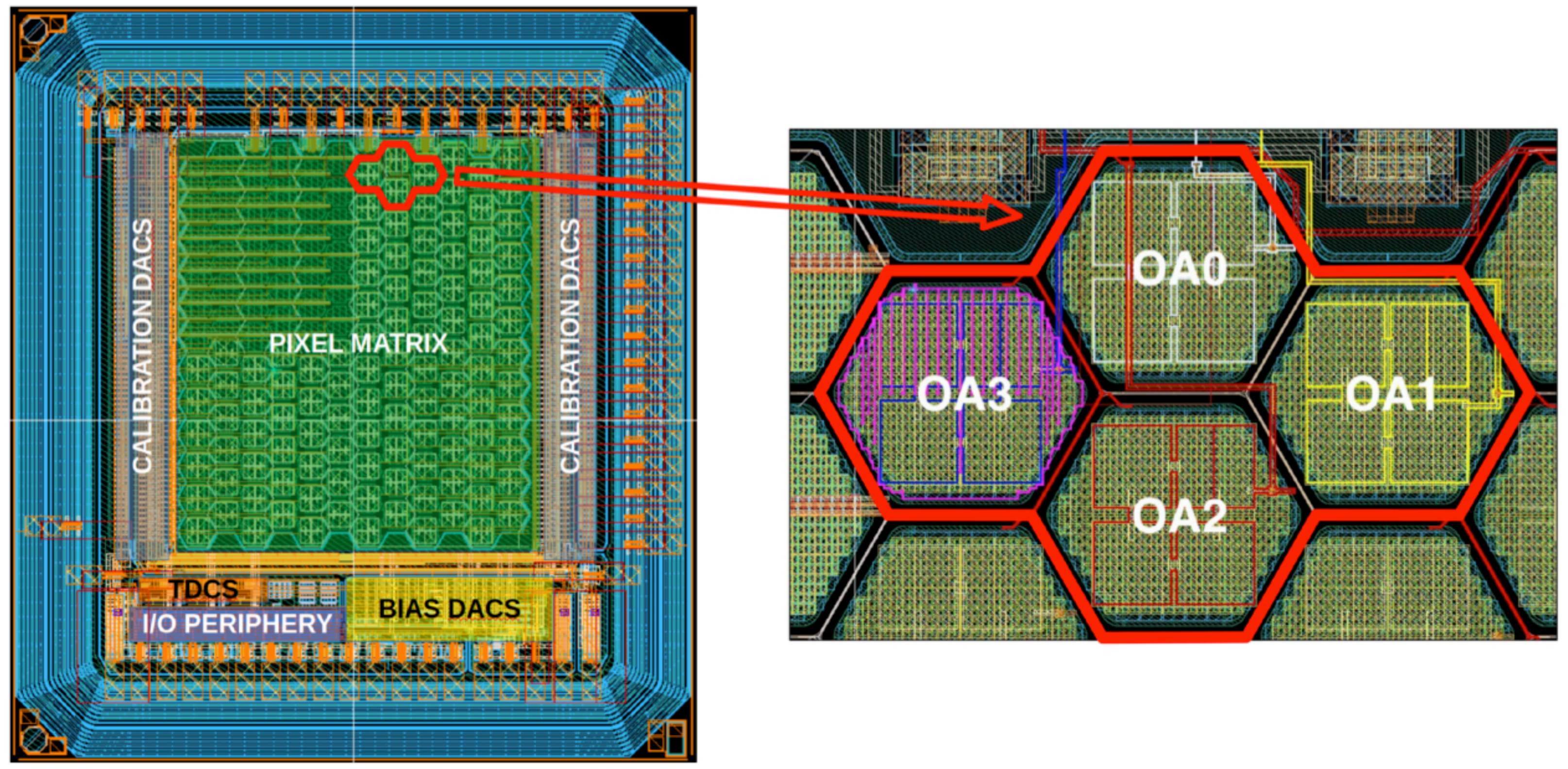
50ps
- Hexagonal pixels 65µm and 130µm side
- Discriminator output

36 ps
- Hexagonal pixels 65µm side
- 30ps TDC +I/O logic
- Analog channels

Sensor with no gain test beam results: JINST **P02019** *2022*

PicoAD Proof-Of-Concept Prototype

2021



17 ps
- **Same electronics as 2019 prototype**
- **Epitaxial layers + gain layer**
- **4 different gain-layer doses**

PicoAD proof-of-concept prototype: arXiv:2206.07952, June 2022

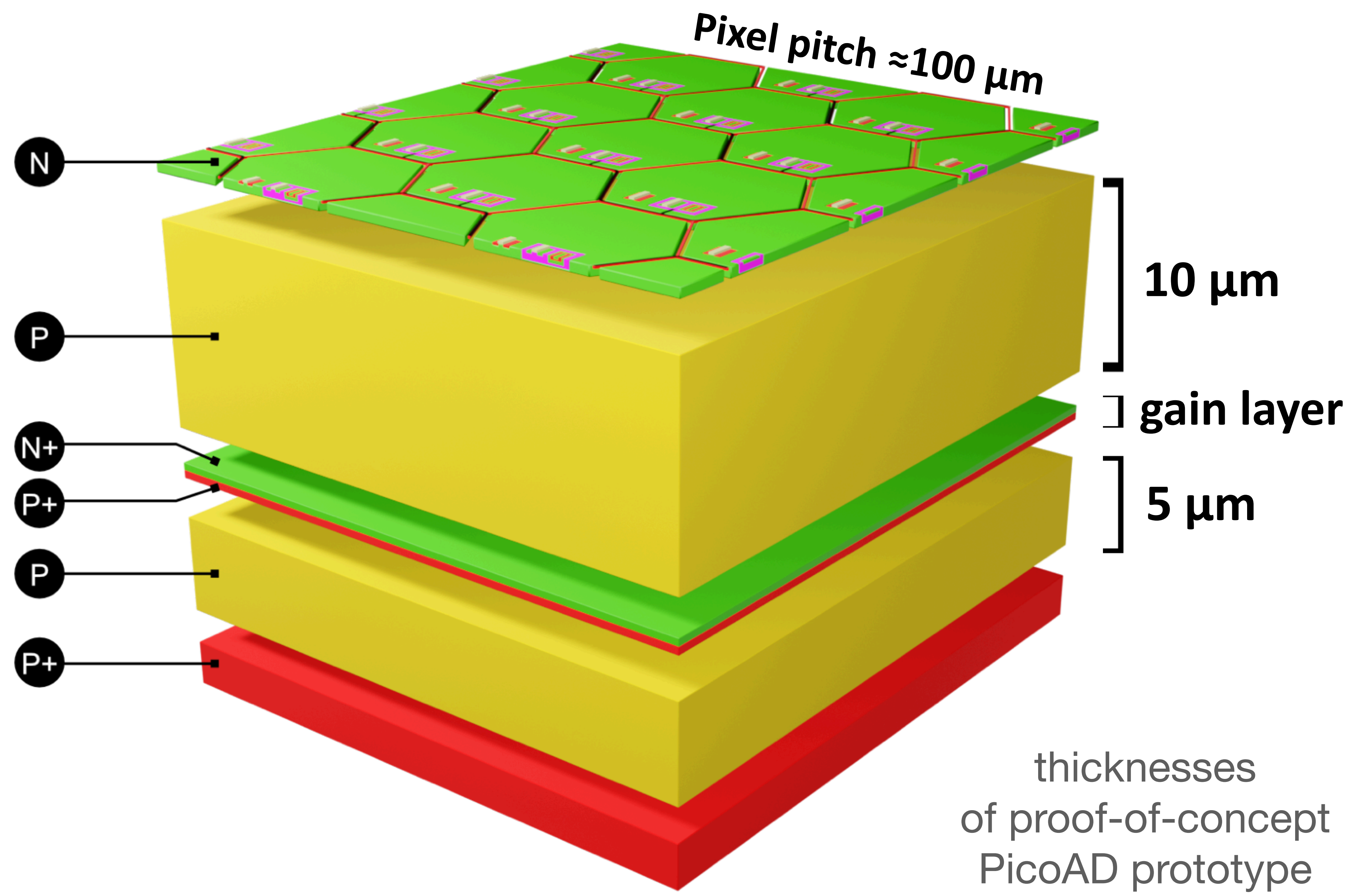
Testbeam results: arXiv:2208.11019, August 2022

PicoAD:

Multi-Junction Picosecond-Avalanche Detector[2]

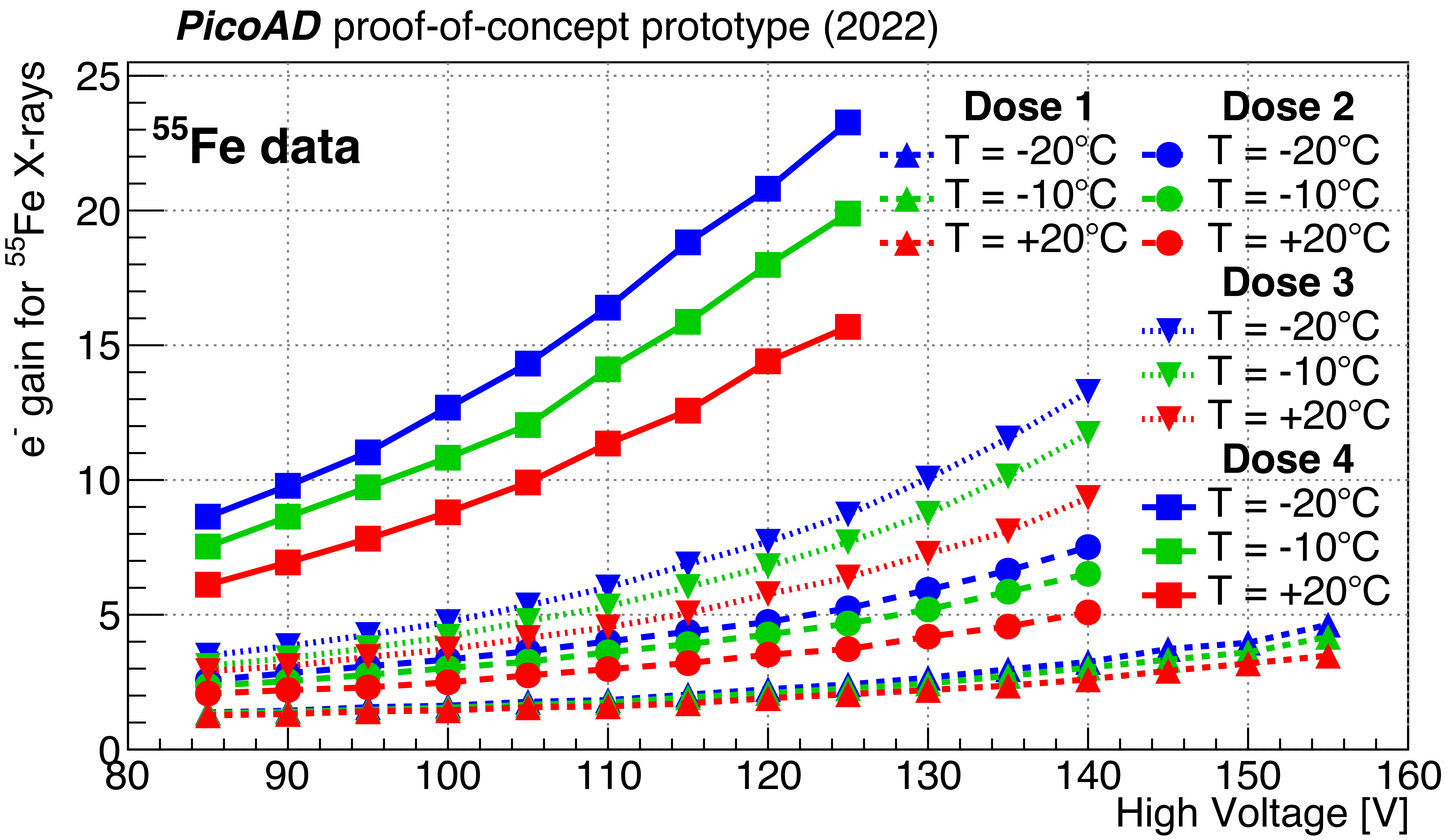
Continuous and deep gain layer

- De-correlation from implant size/geometry
  ➙ **high pixel granularity and full fill factor** (high spatial resolution)
- Only small fraction of charge gets amplified
  ➙ **reduced charge-collection noise** (enhance timing resolution)



[2] G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector; European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

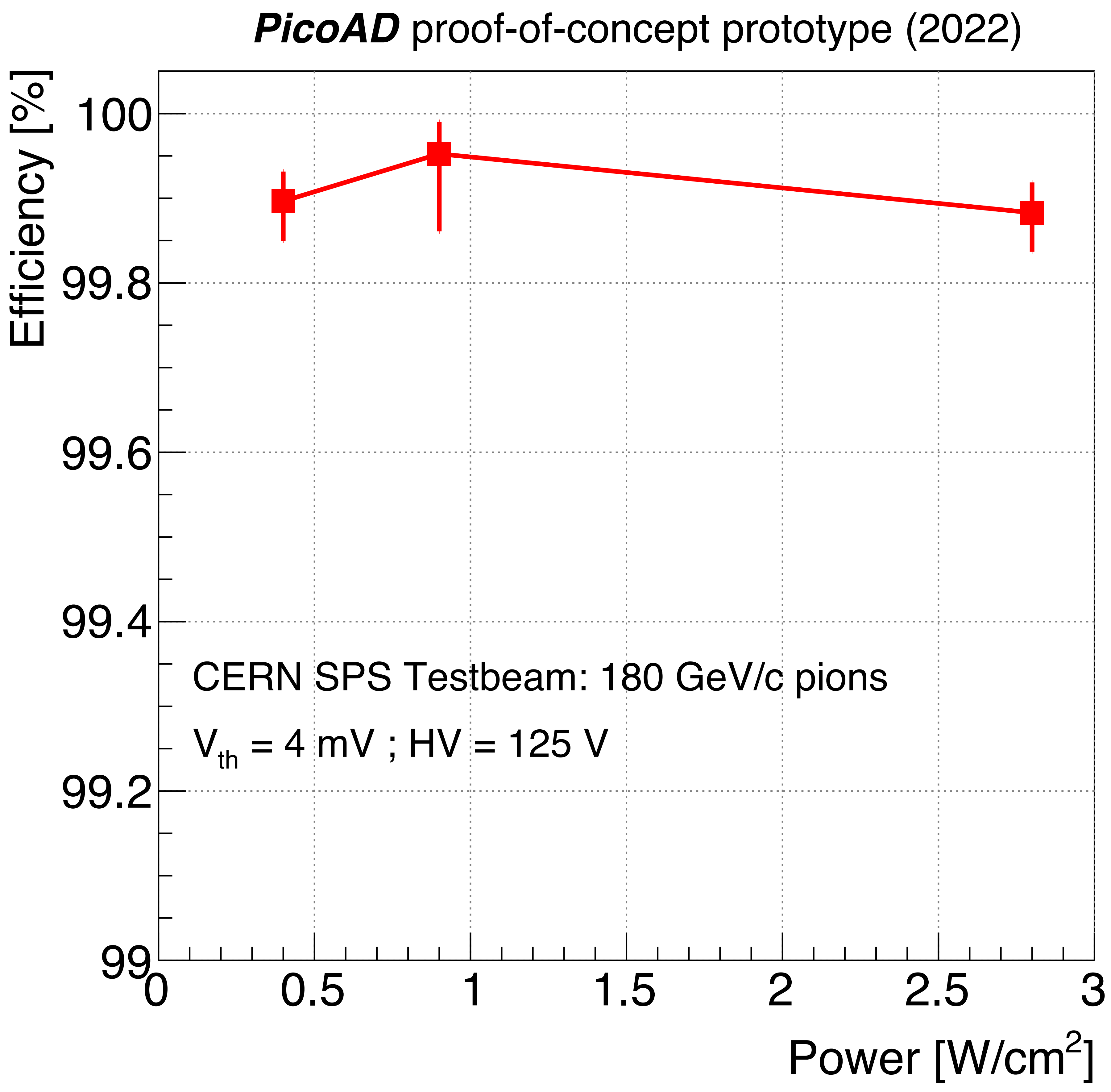
A gain of **≈20** for ^{55}Fe X-rays is reached at HV = 120 V and T = -20 °C[3]



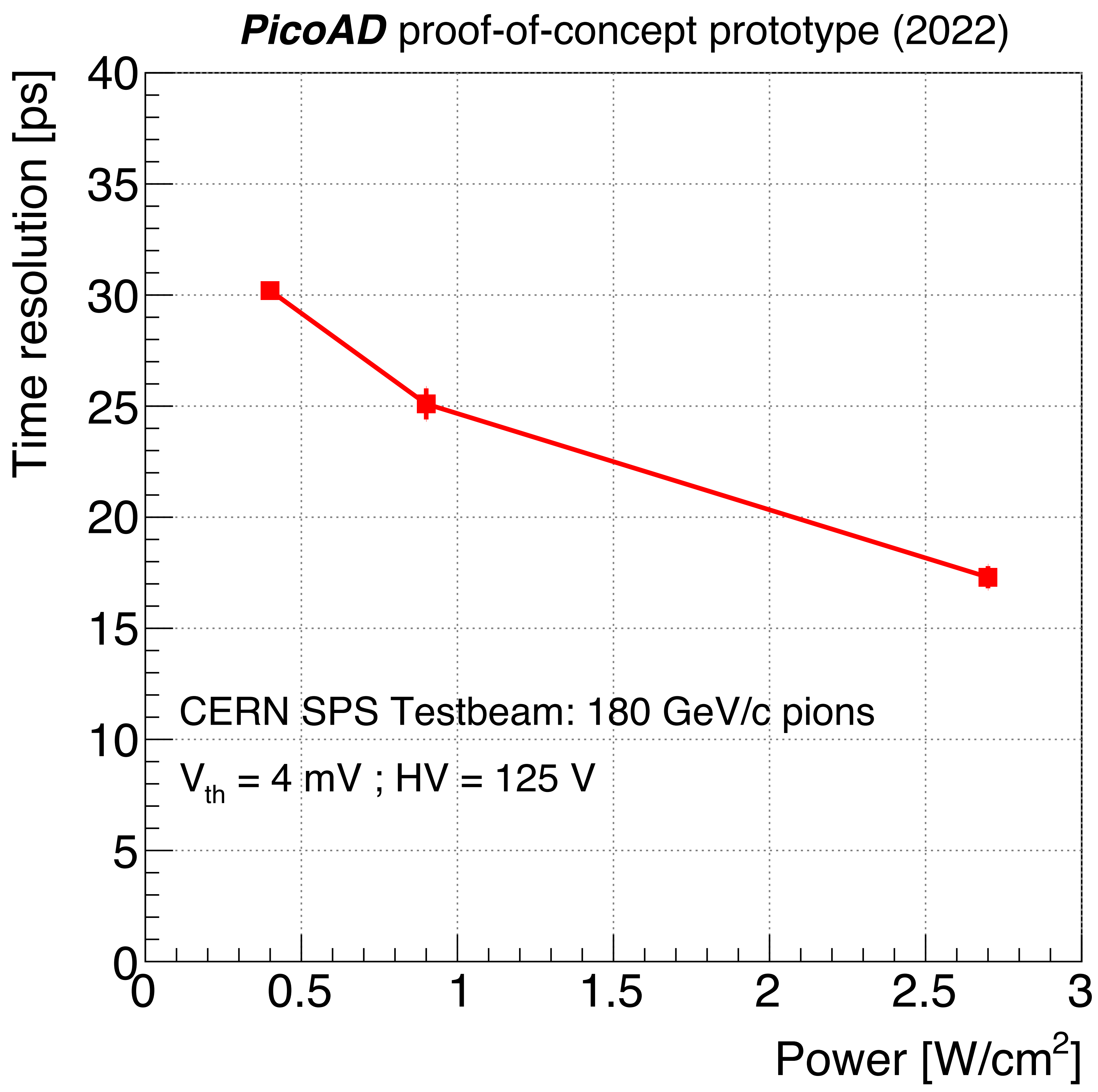
[3] L. Paolozzi et al. Picosecond Avalanche Detector - working principle and gain measurement with a proof-of-concept prototype. arXiv:2206.07952, June 2022

[4] G. Iacobucci et al., Testbeam Results of the Picosecond Avalanche Detector Proof-Of-Concept Prototype. arXiv:2208.11019, August 2022

Efficiency ≈ 99.9%
for power consumptions 0.4-2.7 W/cm²



Time resolution: 17 ps at 2.7 W/cm²
30 ps at 0.4 W/cm²



Efficiency and Time Resolution vs. Power

[4] G. Iacobucci et al., Testbeam Results of the Picosecond Avalanche Detector Proof-Of-Concept Prototype. arXiv:2208.11019, August 2022

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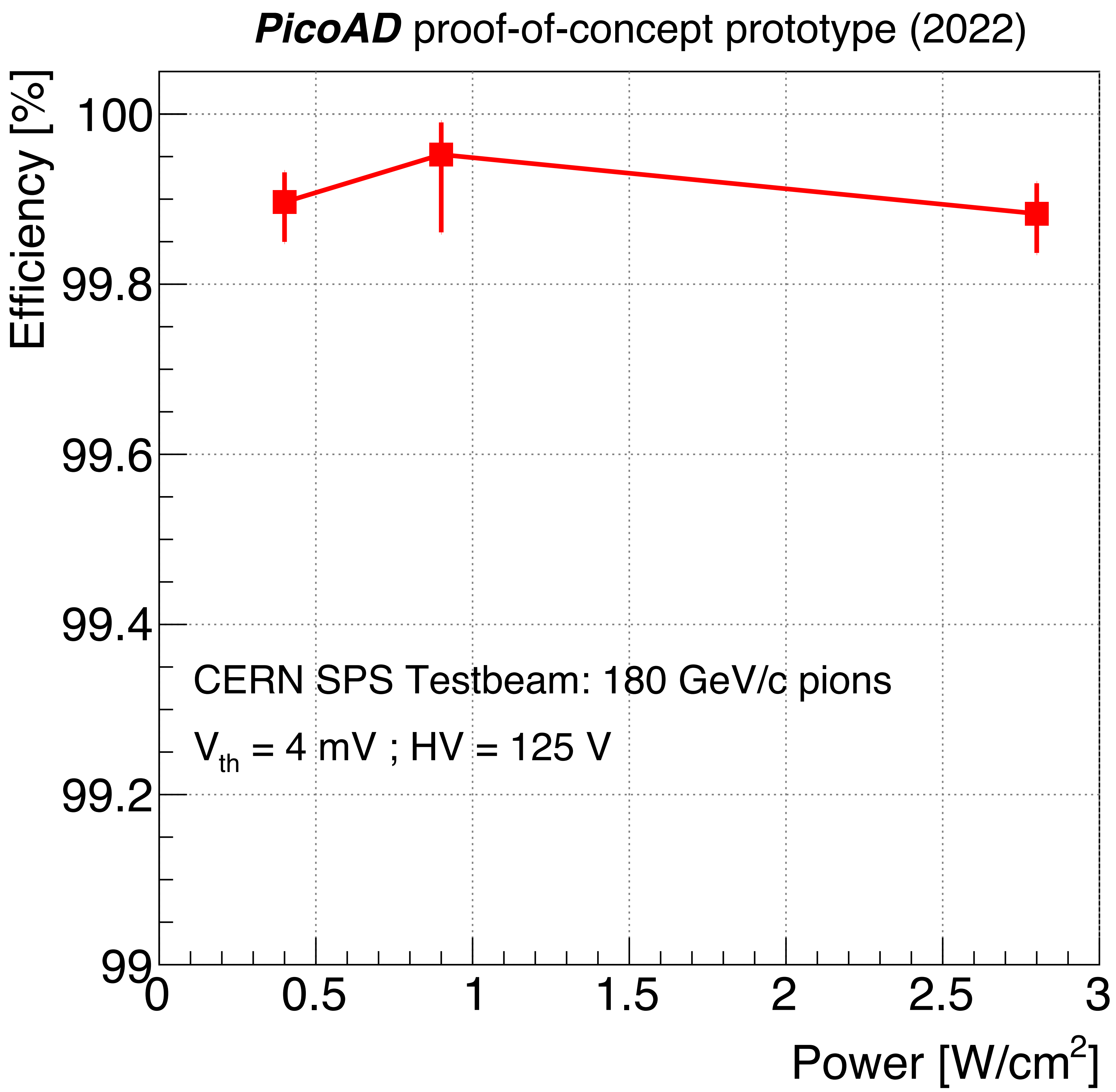
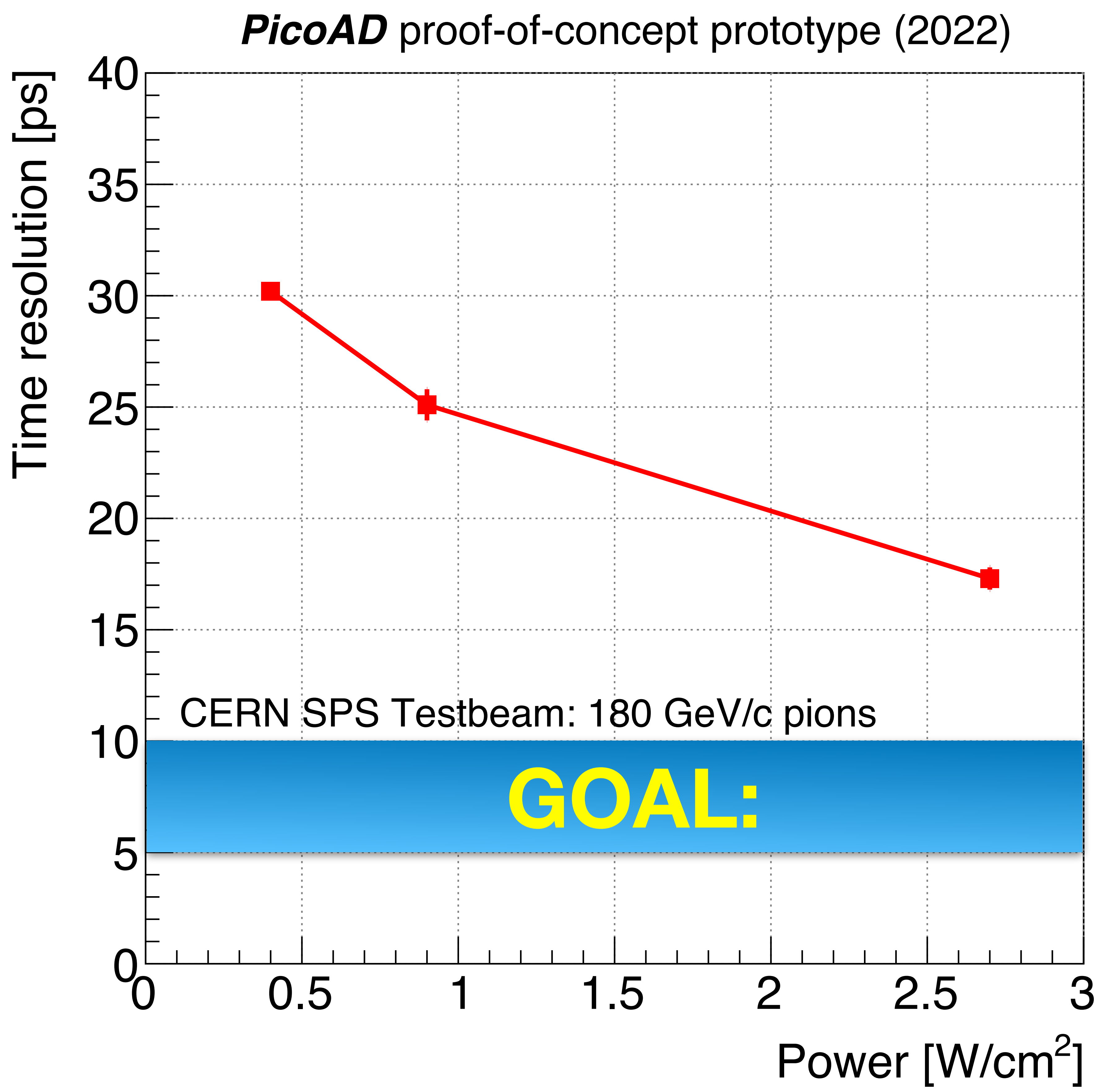
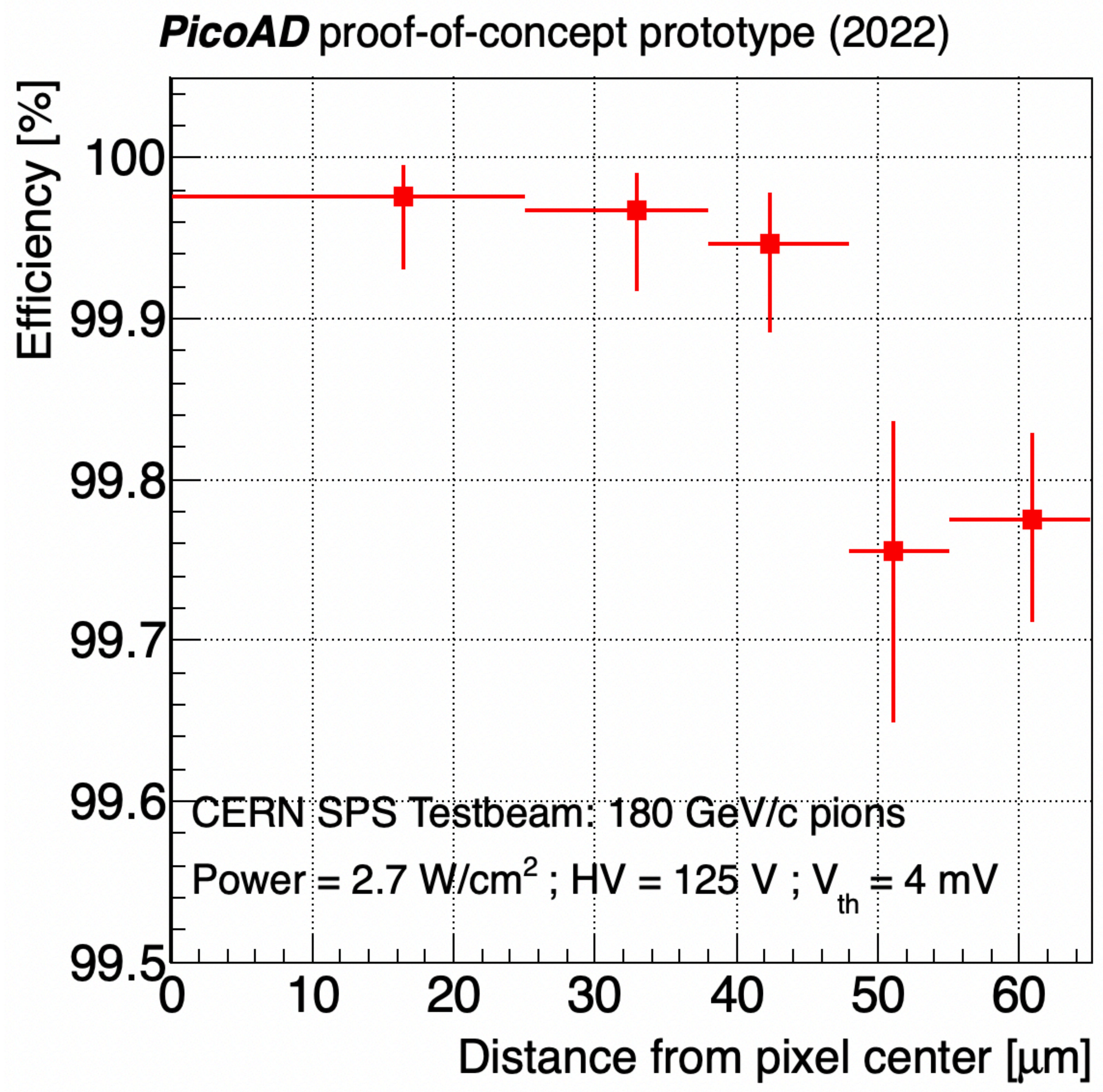




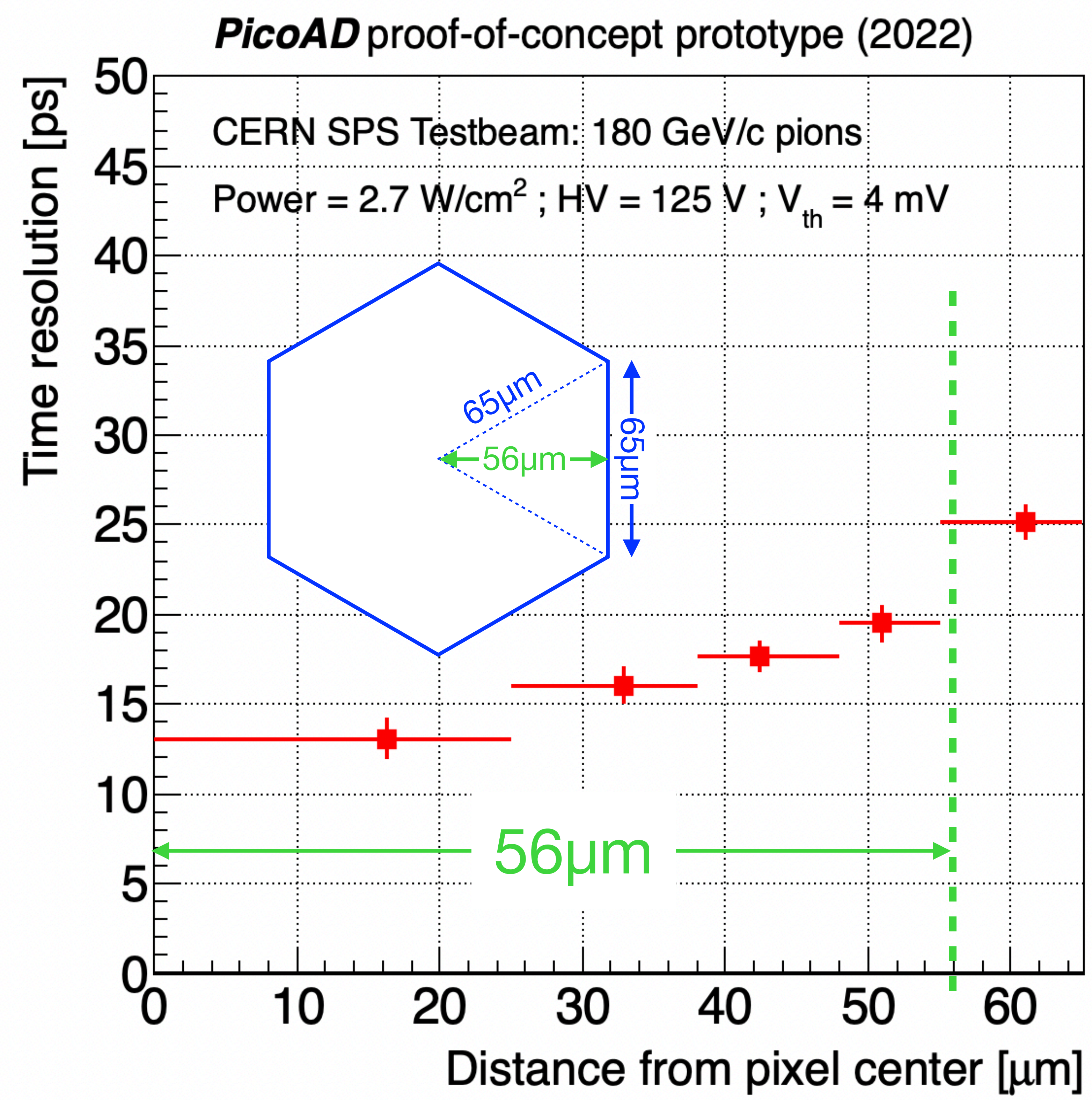
Efficiency and Time Resolution vs. position in pixel

Small performance degradation toward pixel edges

Efficiency

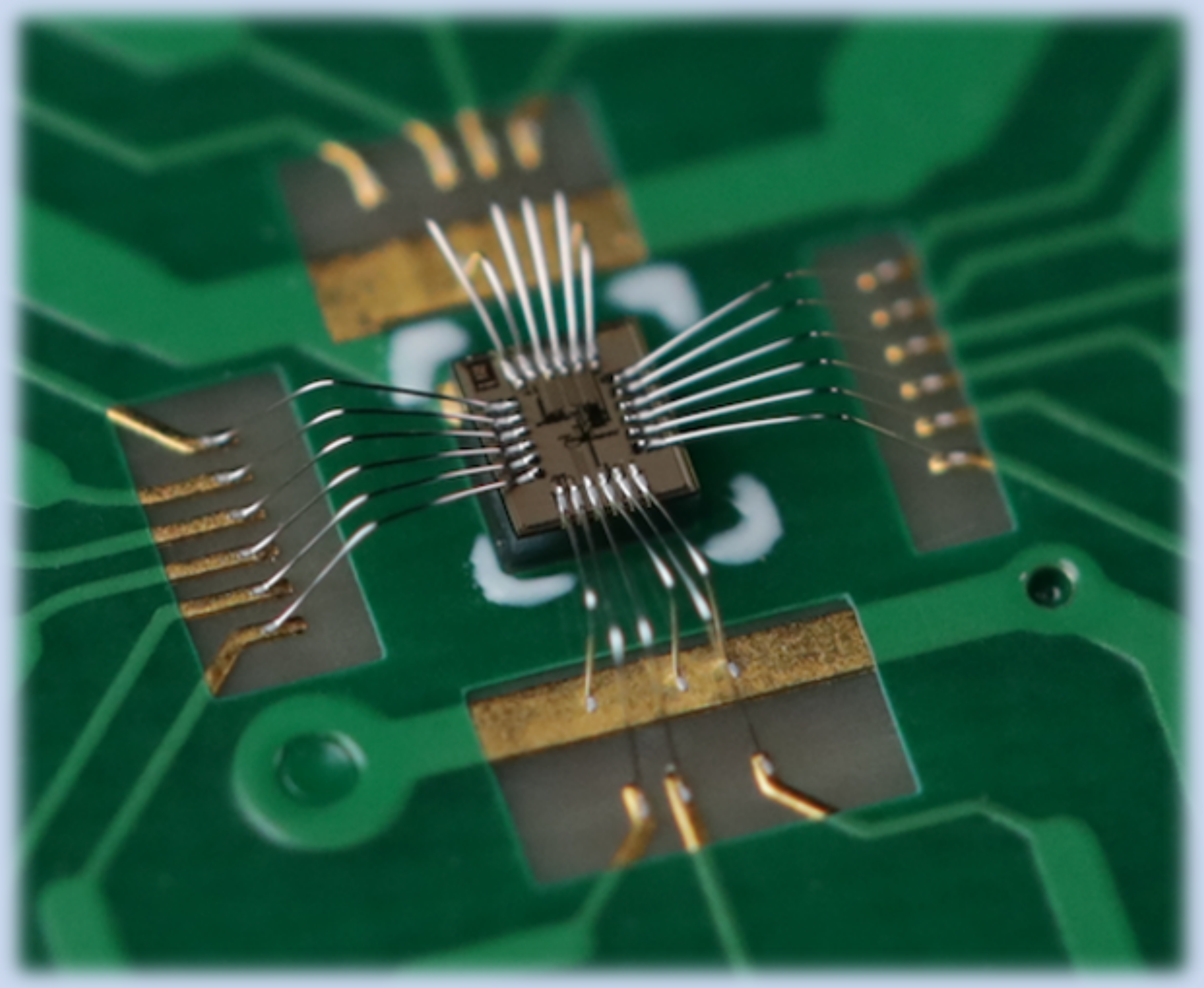


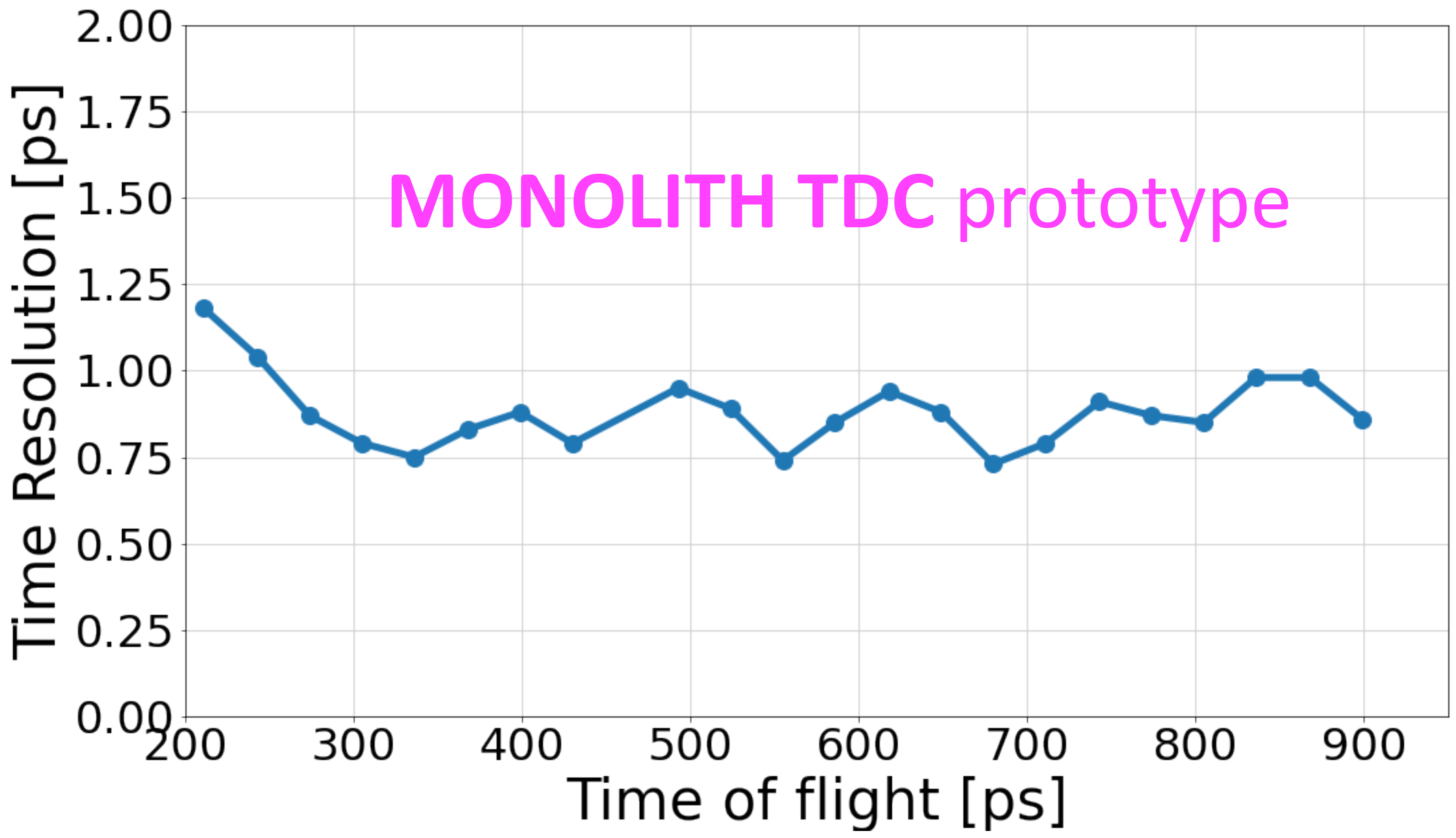
Time resolution



Sub-Picosecond TDC

We are developing a sub-picosecond TDC based on a novel design (our patent[5] & more):





Standalone prototype still under test at UNIGE.
Integrated in MONOLITH 2022 monolithic ASIC.

[5] R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.

This Workshop:

- **Spirit of the workshop: maximize exchanges in an informal environment**
  - **Short presentations**
  - **Long discussions**
  - **Extra interventions (with slides) during discussions are welcome**

- **If you really need to use internet, please use EDUROAM or register to guest-unige**

- **Coffee and lunches will be served outside the seminar room**

This Workshop: TODAY

Monday, 5 September

09:00 → 12:45 **Timing with silicon**

09:00	**Welcome — Coffee and croissants** **Speaker**: Giuseppe Iacobucci (Universite de Geneve (CH))
09:10	**Simulations + numerical calculations for fast timing sensors** **Speaker**: Werner Riegler (CERN)
09:30	**Design of fast CMOS in 65 nm TJ** **Speaker**: Walter Snoeys (CERN)
09:50	**Timespot project testbeam results and simulations** **Speaker**: Adriano Lai (Universita e INFN, Cagliari (IT))
10:10	**Discussion**
10:50	**Coffee break**
11:05	**MONOLITH project simulations and testbeam results** **Speaker**: Magdalena Munker (University of Geneva)
11:25	**Overview LGAD technology at FBK** **Speaker**: Giovanni Paternoster (Fondazione Bruno KEssler)
11:45	**AC–coupled LGAD with HPKK technology** **Speaker**: Koji Nakamura (High Energy Accelerator Research Organization (JP))
12:05	**Discussion**

12:45 → 14:00 **Lunch break**

14:00 → 15:10 **Gain layers**

14:00	**Summary on IHP experience with gain layers** **Speaker**: Mr Matteo Elviretti (IHP microelectronics)
14:20	**Gain layer performance degradation after irradiation** **Speaker**: Michael Moll (CERN)
14:40	**Discussion**

15:10 → 18:20 **Fast electronics**

15:10	**The PicoPix project** **Speaker**: Xavi Llopart Cudie (CERN)
15:30	**INFN project on fast electronics** **Speaker**: Angelo Rivetti (INFN - National Institute for Nuclear Physics)
15:50	**Coffee break**
16:00	**Group picture**
16:05	**Overview talk on HBTs** **Speaker**: Dr Holger Ruecker (IHP microelectronics)
16:25	**Fast, low noise frontend in SiGe BiCMOS** **Speaker**: Lorenzo Paolozzi (CERN)
16:45	**The FastIC project** **Speaker**: Rafael Ballabriga Sune (CERN)
17:05	**Development of novel sub-picosecond TDC** **Speaker**: Dr Roberto Cardella (Universite de Geneve (CH))
17:15	**Discussion**

This Workshop: TOMORROW

Tuesday, 6 September

09:00 → 12:20 **Applications in HEP and space experiments**

- 09:00 **The NA62 GigaTracker**
  Speaker: Mathieu Perrin-Terrin (Centre National de la Recherche Scientifique (FR))
- 09:20 **UZH plans for CMS Phase3 and in AIDAInnova**
  Speaker: Anna Macchiolo (University of Zurich (CH))
- 09:40 **LHb plans for LS4 (TBC)**
  Speaker: Paula Collins (CERN)
- 10:00 **Mu3e silicon timing upgrade**
  Speaker: Andre Schoening (Ruprecht Karls Universitaet Heidelberg (DE))
- 10:20 **Coffee break**
- 10:35 **DUNE cryogenic electronics**
  Speaker: Hucheng Chen (Brookhaven National Laboratory (US))
- 10:55 **Potential use of combined ToF-tracking sensors for Proton Computer Tomography**
  Speaker: Prof. Federico Sanchez (Universite de Geneve (CH))
- 11:15 **Discussion**

12:05 → 14:00 **Lunch break**

14:00 → 16:20 **Cryogenic applications**

- 14:00 **EPFL AQUA Lab cryogenic projects**
  Speaker: Prof. Edoardo Charbon (EPFL)
- 14:20 **IHP PDK + models for cryogenic applications**
  Speakers: Dr Anton Datsuk (IHP), Holger Ruecker (IHP microelectronics)
- 14:40 **IDQuantique projects**
  Speaker: Dr Félix Boussières (IDQuantique)
- 15:00 **Discussion**