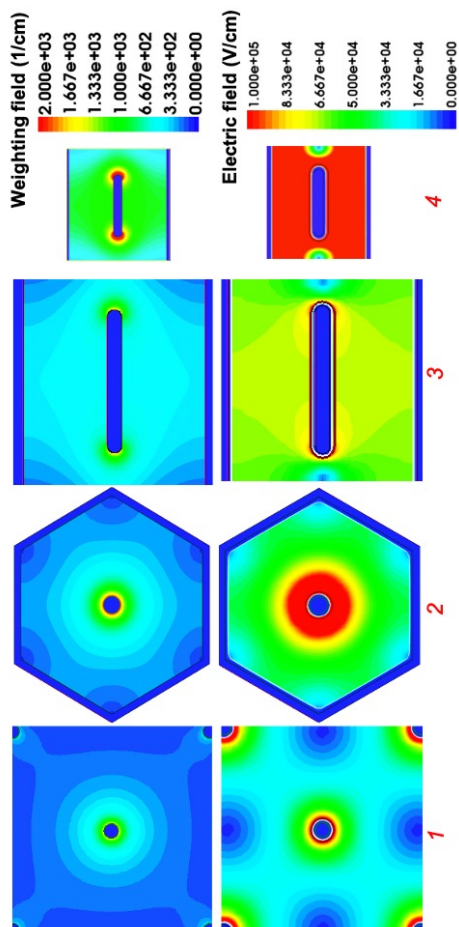




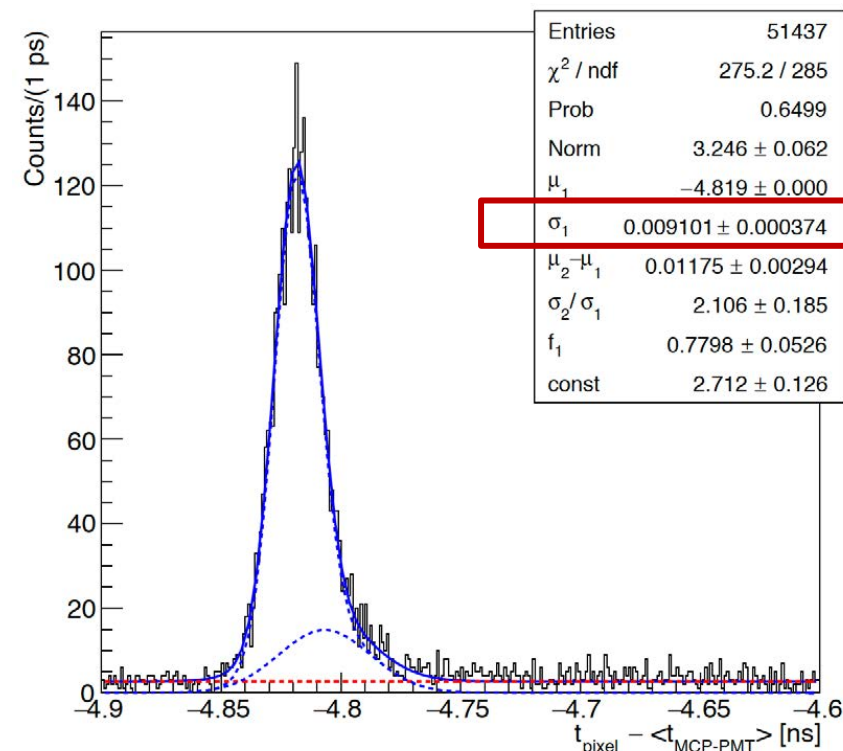
# Studies and Tests on 4D pixel sensors

Adriano Lai,  
INFN Cagliari



## Talk Outline

1. *What we mean for 4D-pixel*
2. *Experimental/System Requirements*
3. *Study of pixel properties and simulation tools*
4. *Key-role of the electronics stage*
5. *Latest test results*
6. *Perspectives*



Definition of 4D pixel  
and scope of the developments

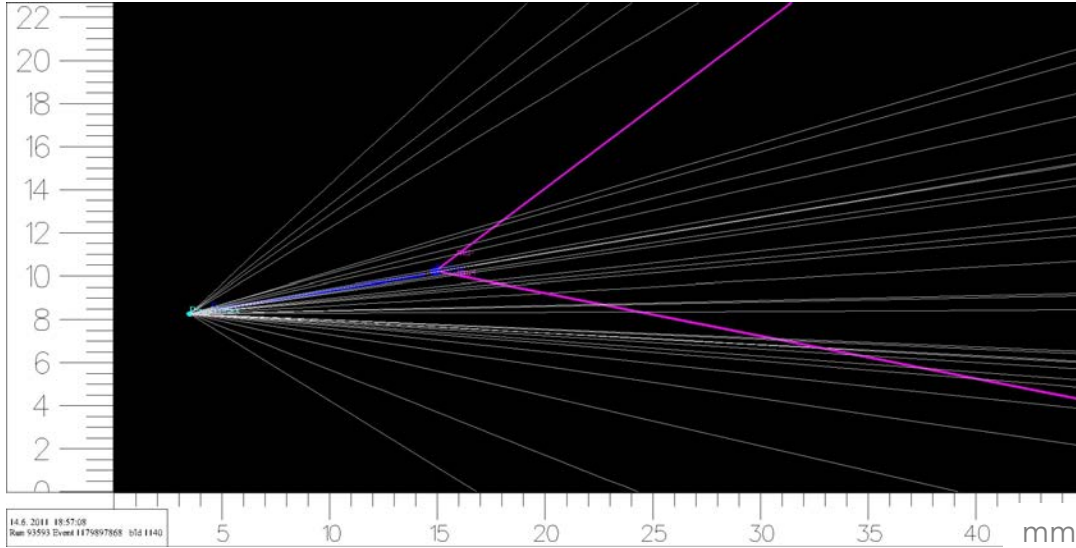
# 4D trackers/pixels: what do we mean for?

(beyond pile-up mitigation: when timing layers are not enough)



Plots from:  
 Considerations for the VELO detector at the  
 LHCb Upgrade II – CERN-LHCb-2022-001

$B_{os}$  meson decaying into a  $\mu^+$  and  $\mu^-$  pair



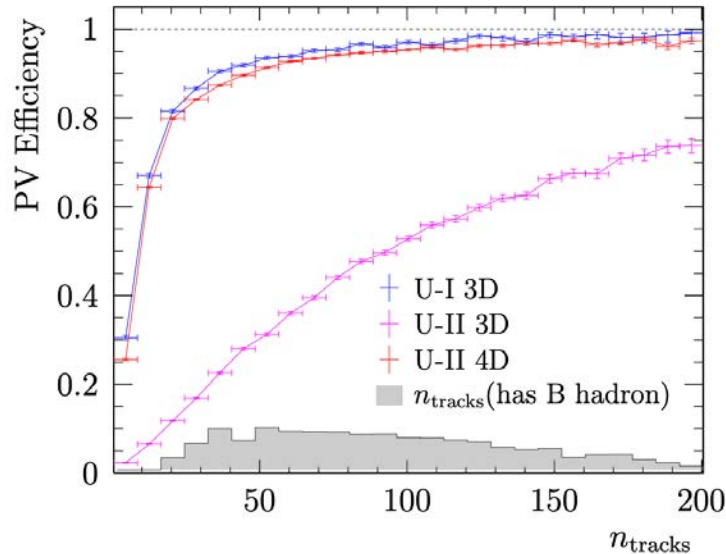
**4D pixel:**

**A solid state pixel sensor (pitch  $\approx 50 \mu\text{m}$ ) bearing time information**

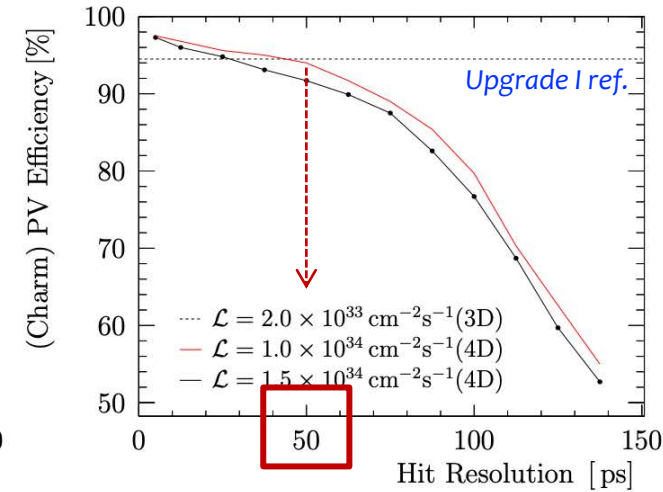
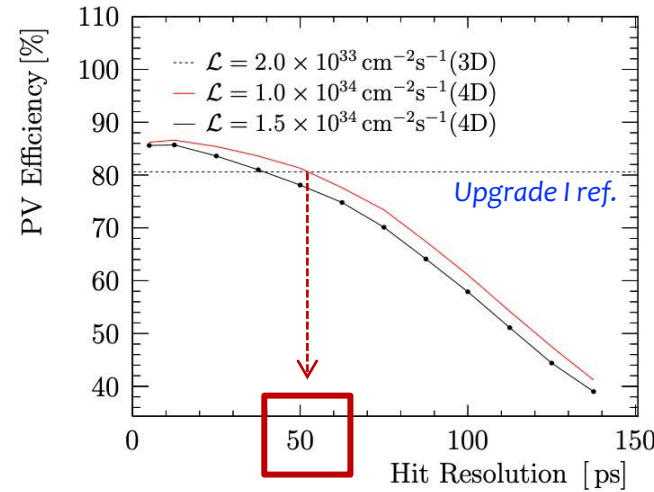
Track merging: bad Primary (and Secondary) Vertex reconstruction

Incorrect PV assigned to tracks: poorly measured lifetime  
 (dominant systematic effect for time-dependent analysis)

PV reconstruction efficiency as a function of the single hit resolution, for all vertices (left) and for vertices where at least one of the decay products is a charm hadron (right).



**Reconstruction efficiency vs the number of tracks per primary vertex, comparing the Upgrade I 3D reconstruction in both data conditions, and a variant using timing information to resolve the primary vertices**



**50 ps per hit (corresponding to 20 ps per track) are sufficient to recover the Upgrade-I efficiency**

# Technical Requirements of 4D-Tracking

*In the next generation of Upgrades*

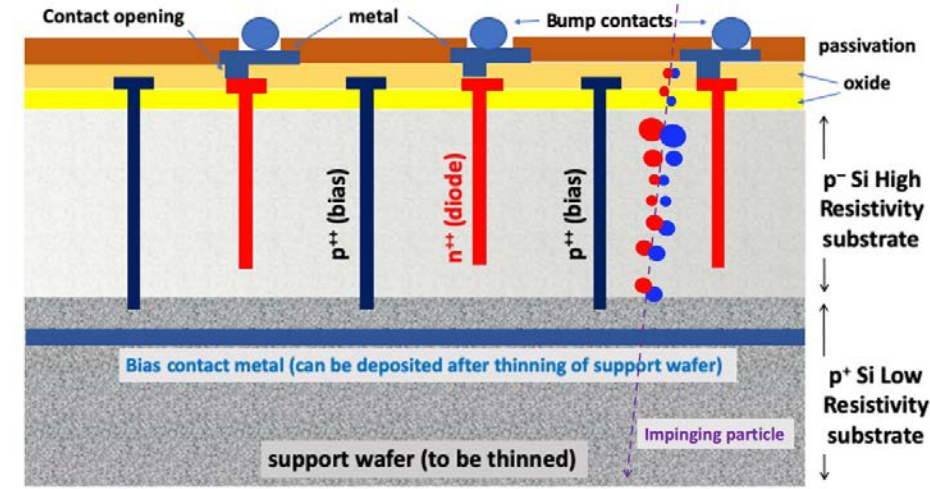
*(LHCb run5, NA62 4x, CMS-PPS & ATLAS-AFP run4 ... FCC-hh...)*

1. Space Resolution  $\sigma_s \approx 10 \mu\text{m}$  ( $\rightarrow$  pixel pitch  $\approx 40\text{--}60 \mu\text{m}$ )
2. Time Resolution  $\sigma_t \leq 50 \text{ ps}$  on the full chain ( $\sigma_t = \sigma_{\text{sensor}} \oplus \sigma_{FE} \oplus \sigma_{TDC}$ )
3. Radiation hardness to high fluences (for sensors) and high doses (for electronics).  
Fluences  $\Phi = 10^{16} \div 10^{17} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$  and Doses  $> 1 \div 2 \text{ Grad}$
4. A detection efficiency of  $\varepsilon > 99\%$  per layer is typically required (high fill factor)
5. The material budget must be kept below  $1 \div 0.5 \%$  radiation length per layer

Very challenging front-end electronics must be developed:  
high resolution @  $10\text{s } \mu\text{W}/\text{pixel}$ , huge data bandwidth  $\approx 100 \text{ Gbps}/\text{cm}^2$ .  
Today a complete solution for that is FAR from being available.  
Developments ongoing

# A different approach: 3D silicon sensors

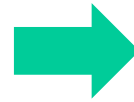
*Gain? no thanks! go... Geometric!*



Deep Reactive Ion Etching (MEMS technology)



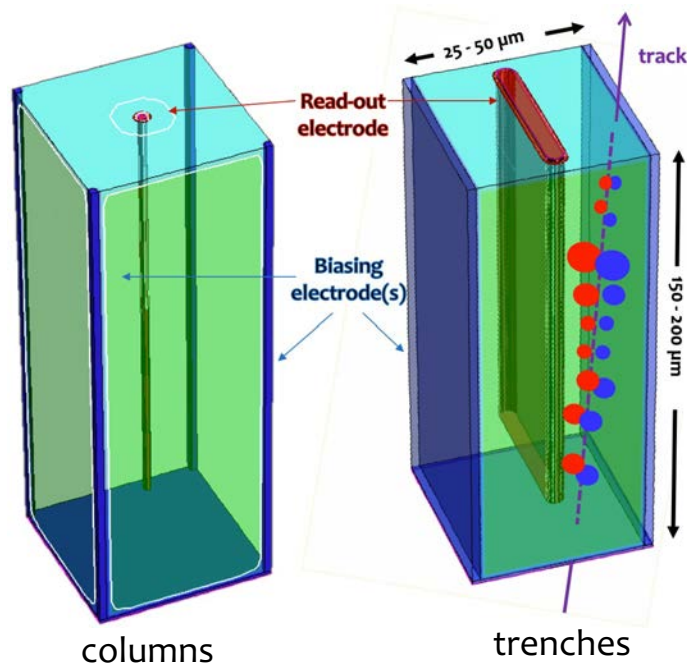
Concept (S. Parker et al., 1997):  
 Perpendicular electrodes make  
 Inter-electrode distance  $d$   
 independent of sensor thickness  $z$



Sensitive volume and electrode shapes can be designed and modeled for maximum performance

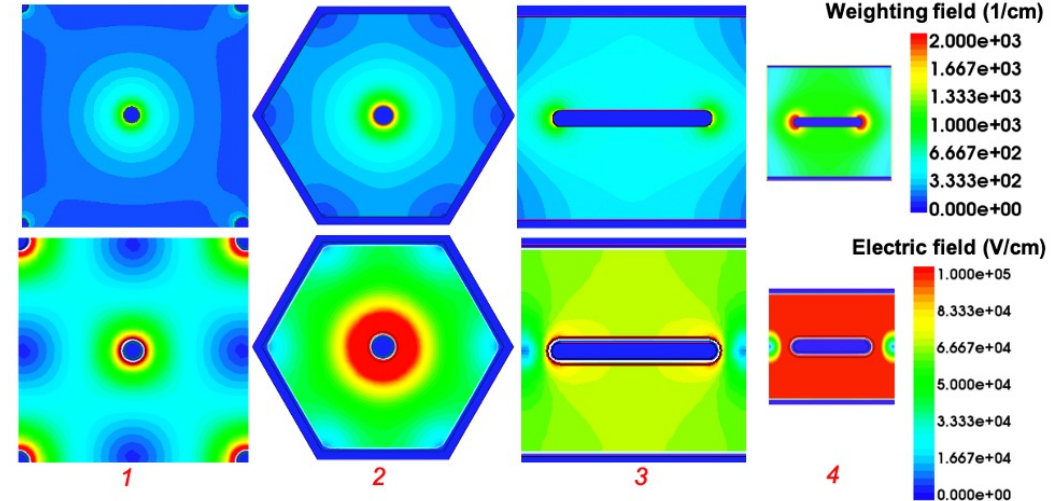


High and uniform E field



Column or trench aspect ratio  $\approx 30:1$

$$i = qE_w \cdot v$$

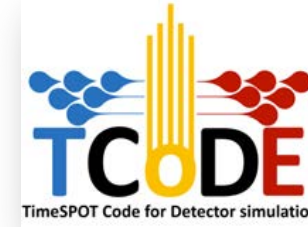


TCAD Sentaurus output: 2D model simulation of three different electrode geometries at bias voltage  $V_{bias} = -100 V$

(3D) Sensor modeling and its  
impact in sensor design and  
understanding



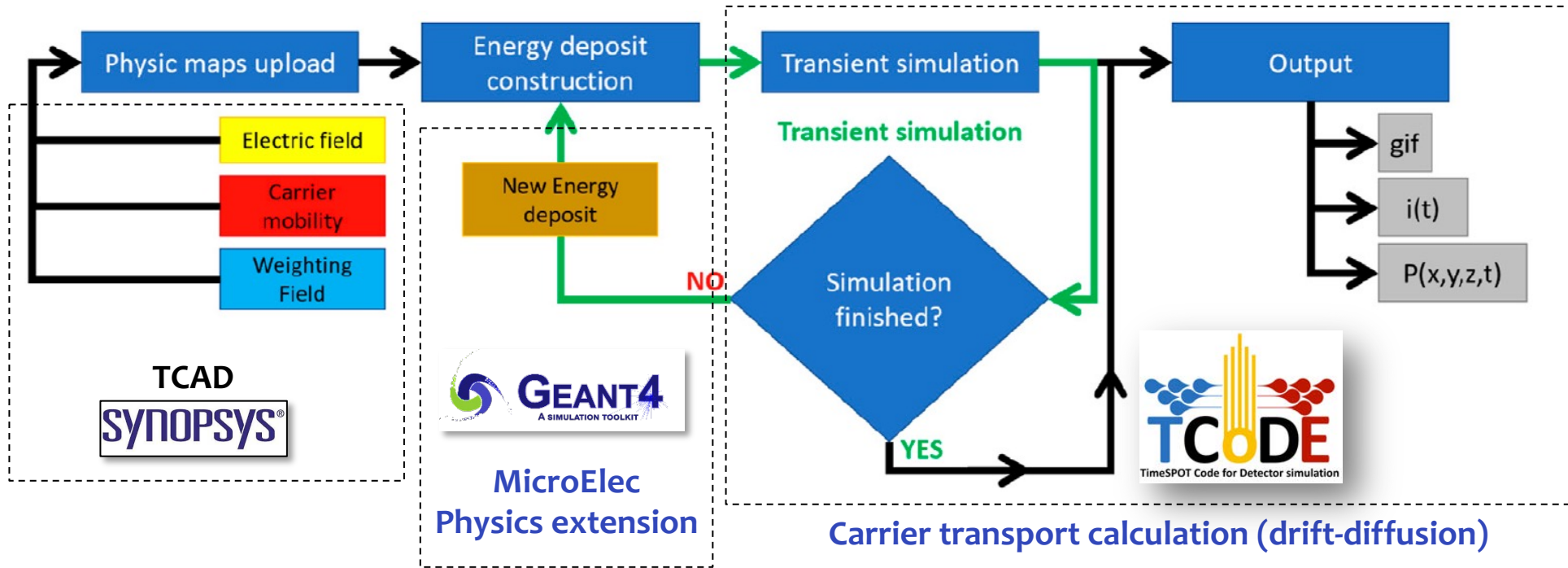
# The playground and the game CCT and current signals



<https://github.com/MultithreadCorner/Tcode>

GPL3 license

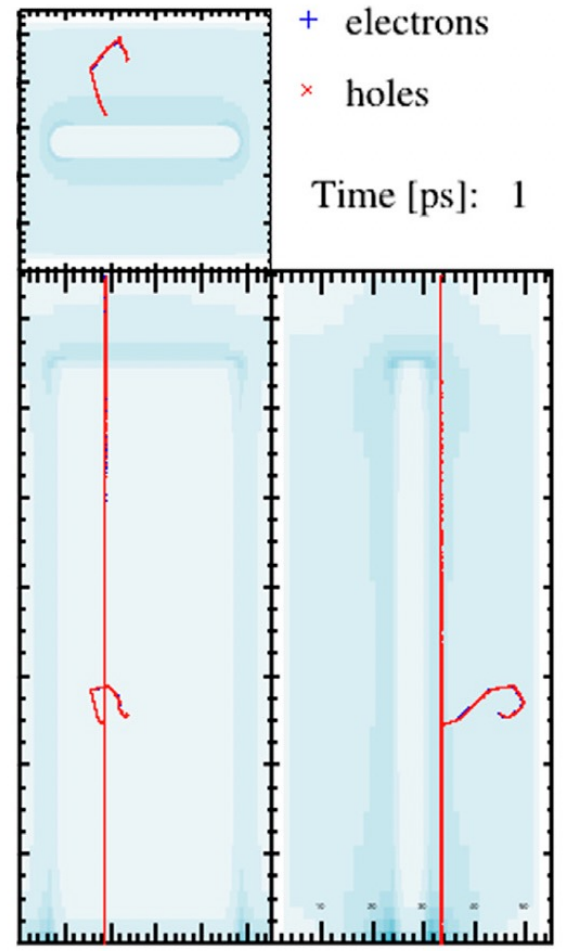
## The TCoDe simulation flow



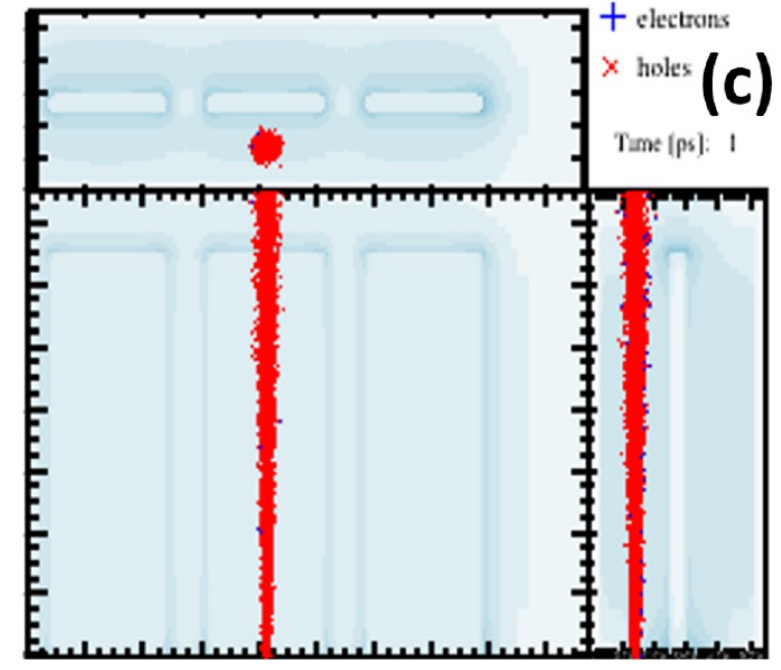
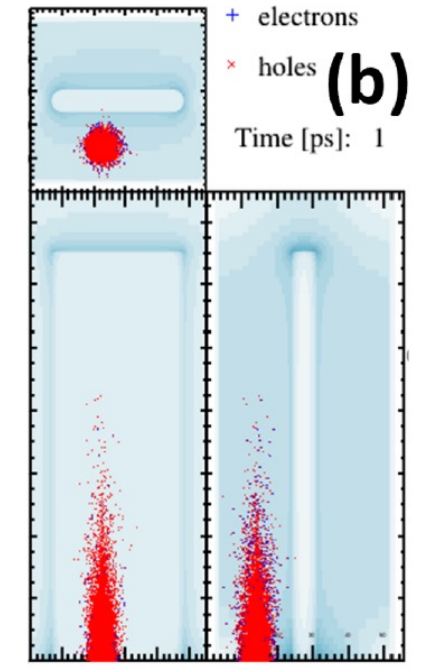
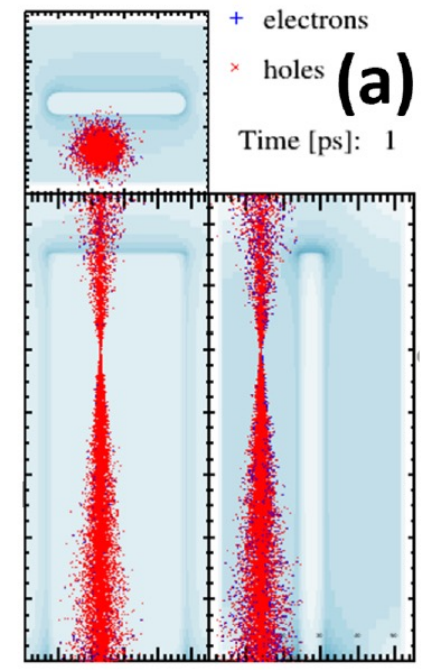
The **carrier motion** calculated using a 4<sup>th</sup>-order Runge–Kutta algorithm and the thermal diffusion equation. The contribution of each carrier to the current induced on the readout electrode is determined with the **Ramo theorem** for each time interval.

**Multi-threaded approach** (Hydra libraries): each carrier is followed independently in a separate computing thread, either in CPU or GPU.

# Energy deposits Geant4 and/or analytical



MIP deposit shape

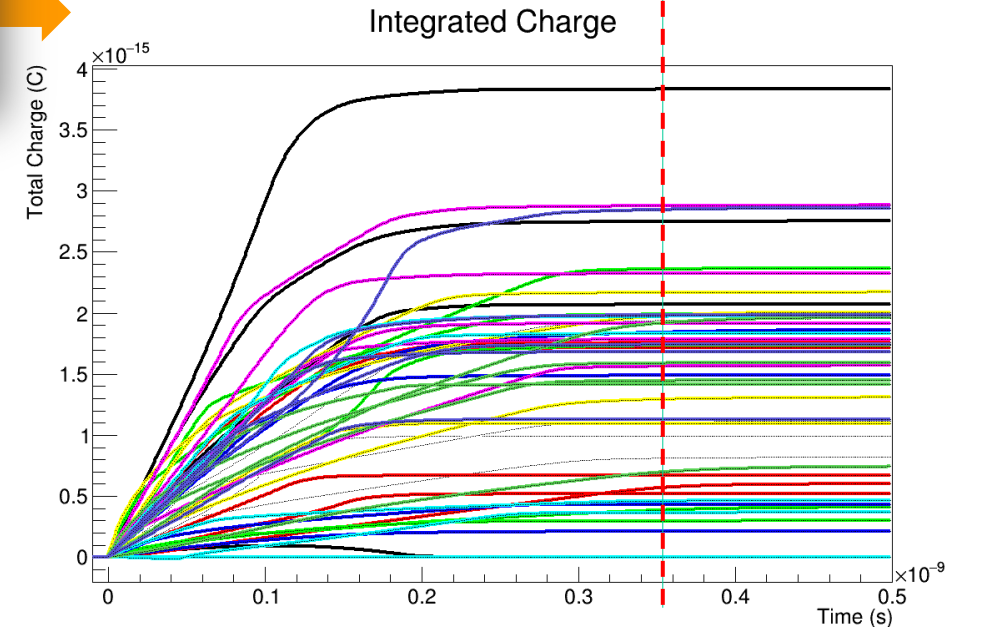
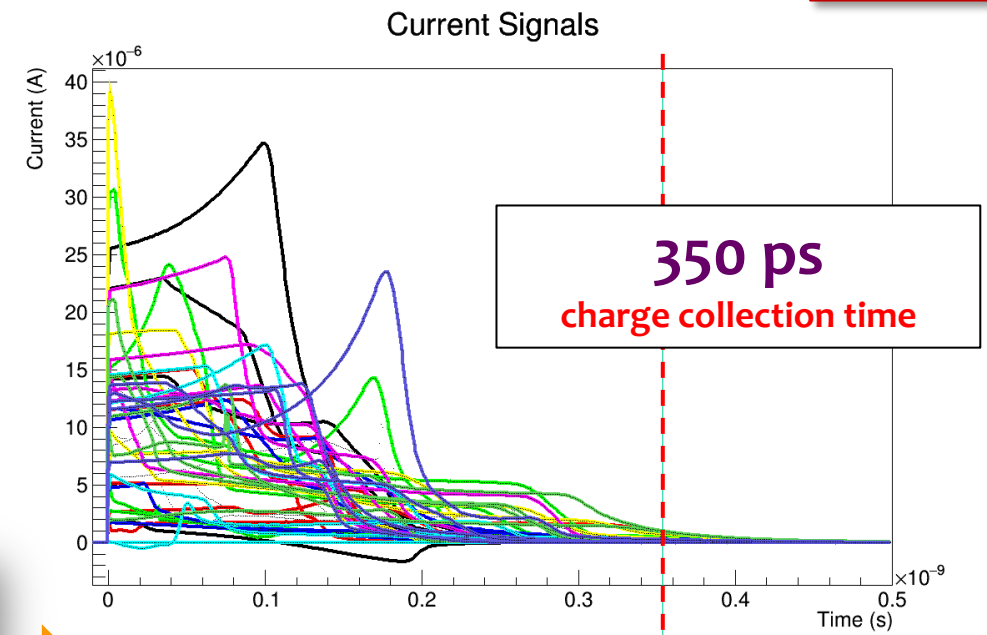
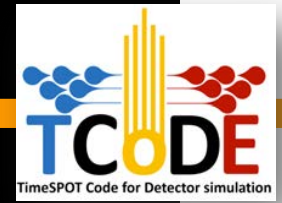
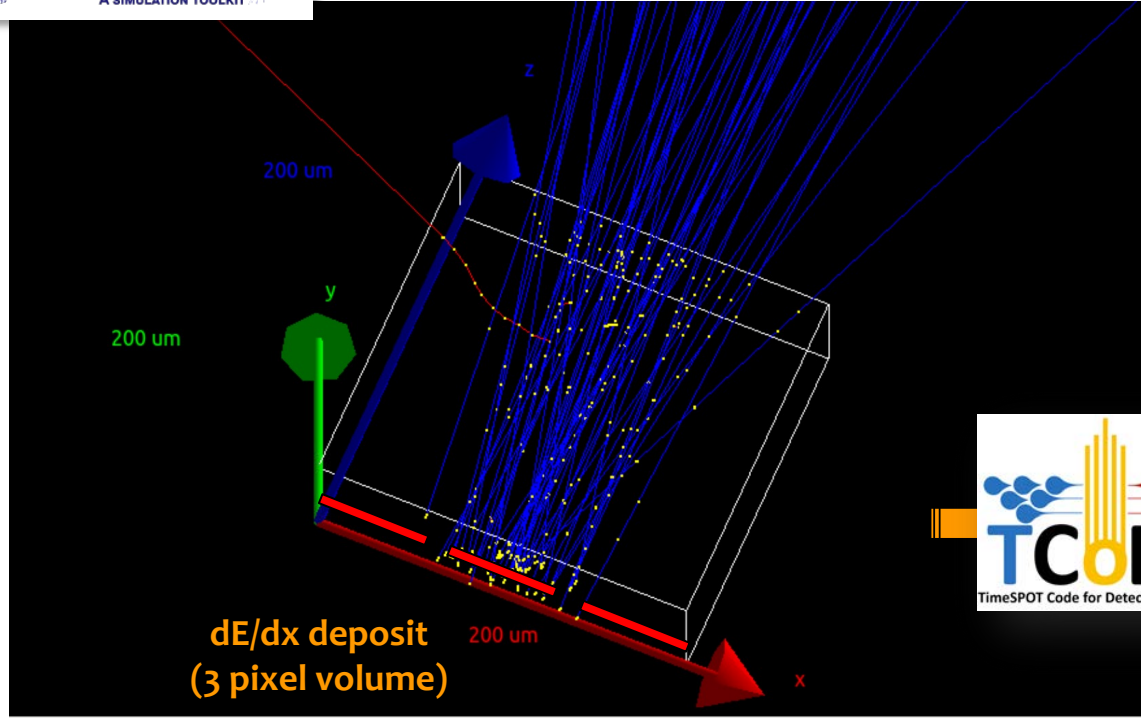


Examples of calculated energy deposit shapes **from laser sources** inside a TimeSPOT 3D-trench structure:

- (a) Deposit with focus inside the active bulk.
- (b) Deposit shape due to high absorption (655 nm wavelength)
- (c) Deposit of IR laser source (1030 nm wavelength), emulating a MIP.



# TCoDe operation and statistics



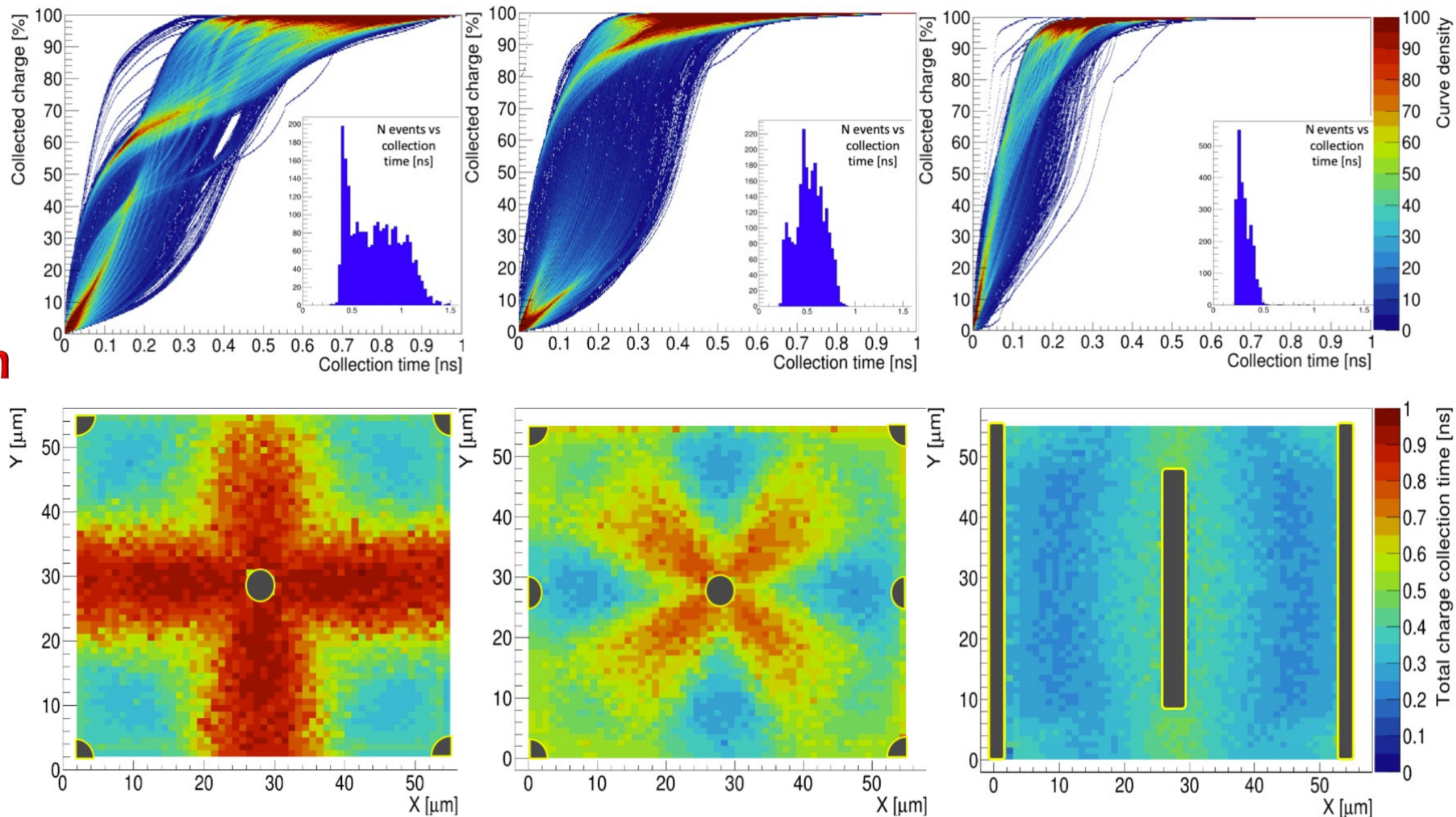
50 tracks  
 Induced current signals calculated by TCODE  
 (input to F/E electronics model)  
 1h40' in ST (Intel®Xeon®CPU X5450 – 10 GB RAM)  
 1'40'' on a gaming laptop in MT  
 2-3 months on TCAD (estimate)

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# Charge Collection

## Time Curves and maps



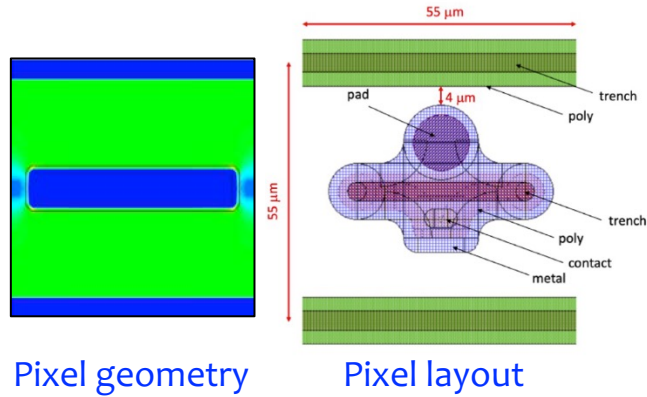
Time performance comparison among three different 3D geometries at  $V_{\text{bias}} = -100\text{V}$  (from left to right: five columns, nine columns and trench geometry). (Top) percentage of total charge collected on the electrodes versus time. (Top inserts) distribution of charge collection time for the three geometries. (Bottom) time for complete charge collection versus impact point for the same geometries. Each simulation is based on about 3 000 MIP tracks.

# Sensor fabrication @ FBK

2 batches (2019 and 2020)

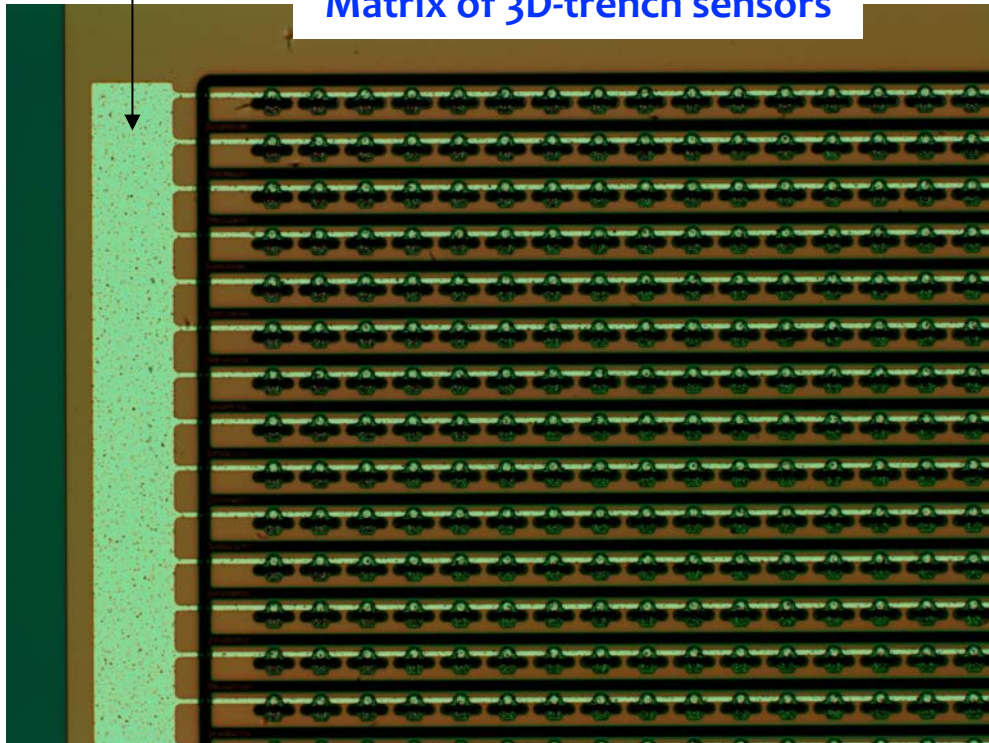
## The optimal geometry

- 3D-trench
- $5 \times 40 \times 135 \mu\text{m}^3$  trench
- $150 \mu\text{m}$  pixel depth



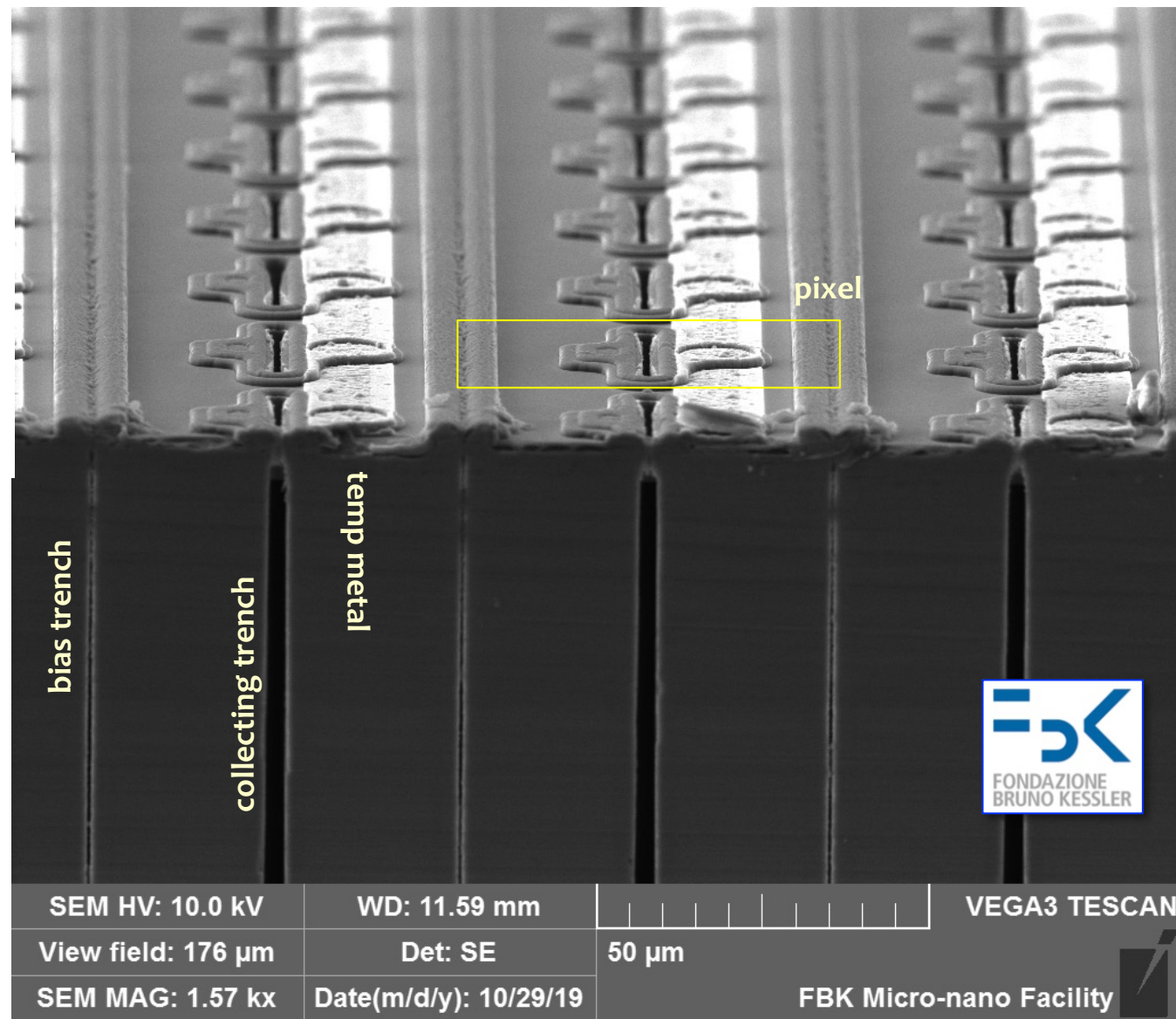
temp metal  
for static tests

## Matrix of 3D-trench sensors



← collecting trench

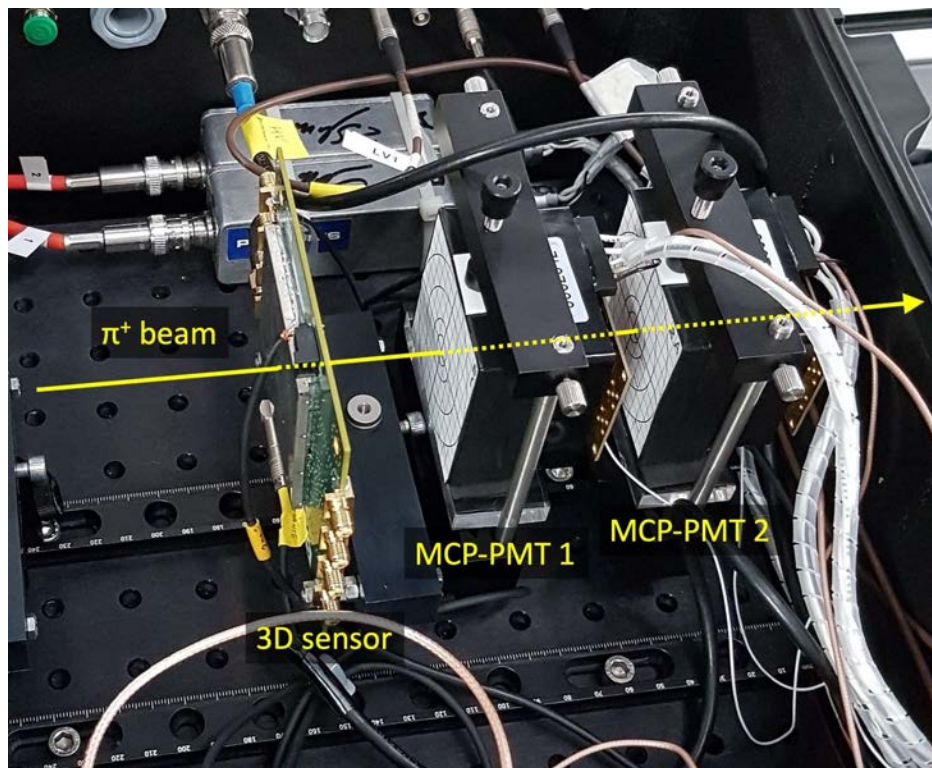
← bias trench



**Deep Reactive Ion Etching**  
 Bosch technology  
 (developed for **MicroElectroMechanicalSystem**  
 technology)

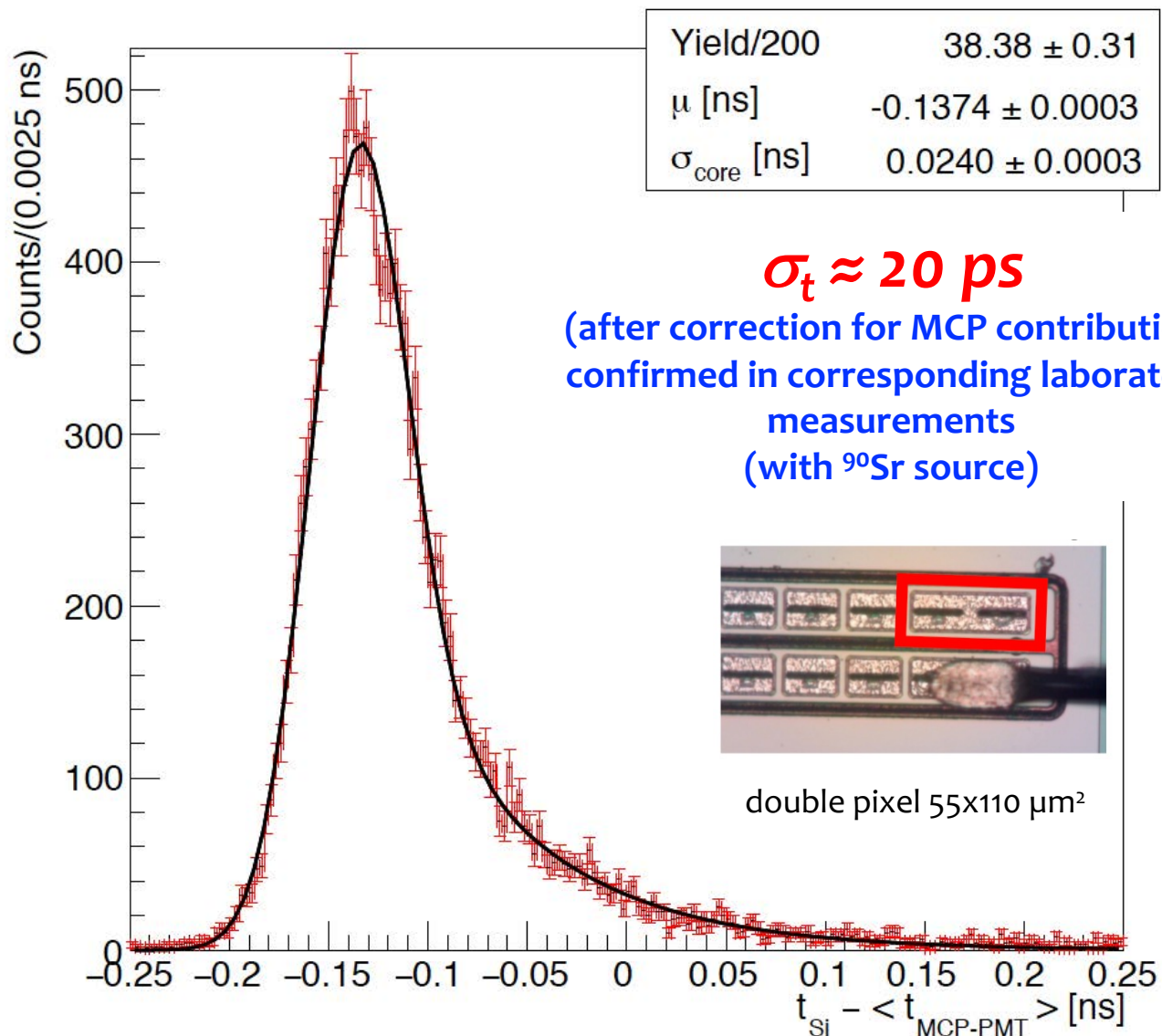
# First results on 3D-trench pixels at PSI (2019)

Time resolution of 3D-trench silicon pixels with MIPs (test-beam & lab) at room temperature  
(ref. Intrinsic time resolution of 3D-trench silicon pixels for charged particle detection, 2020 JINST 15 P09029)



PSI  $\pi M1$ ,  $\pi^+$  beam, 270 MeV/c

Fast but not optimised FE used

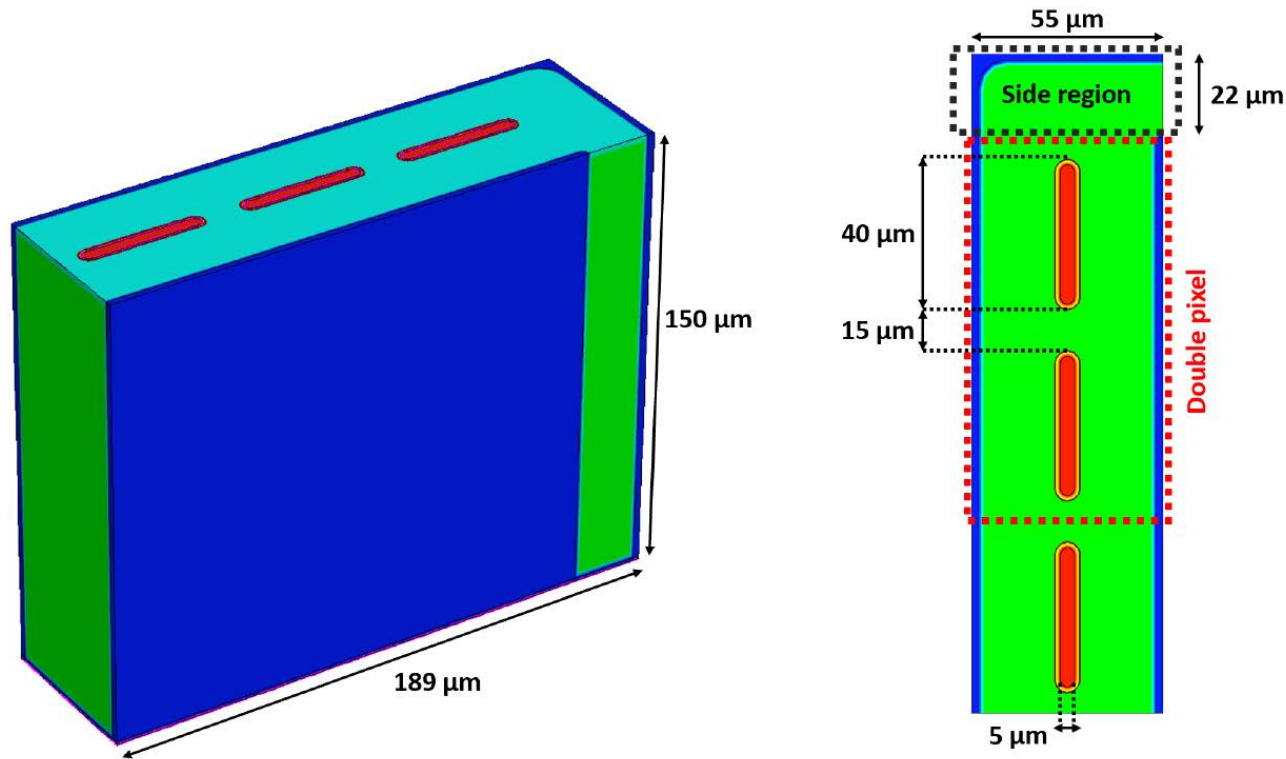




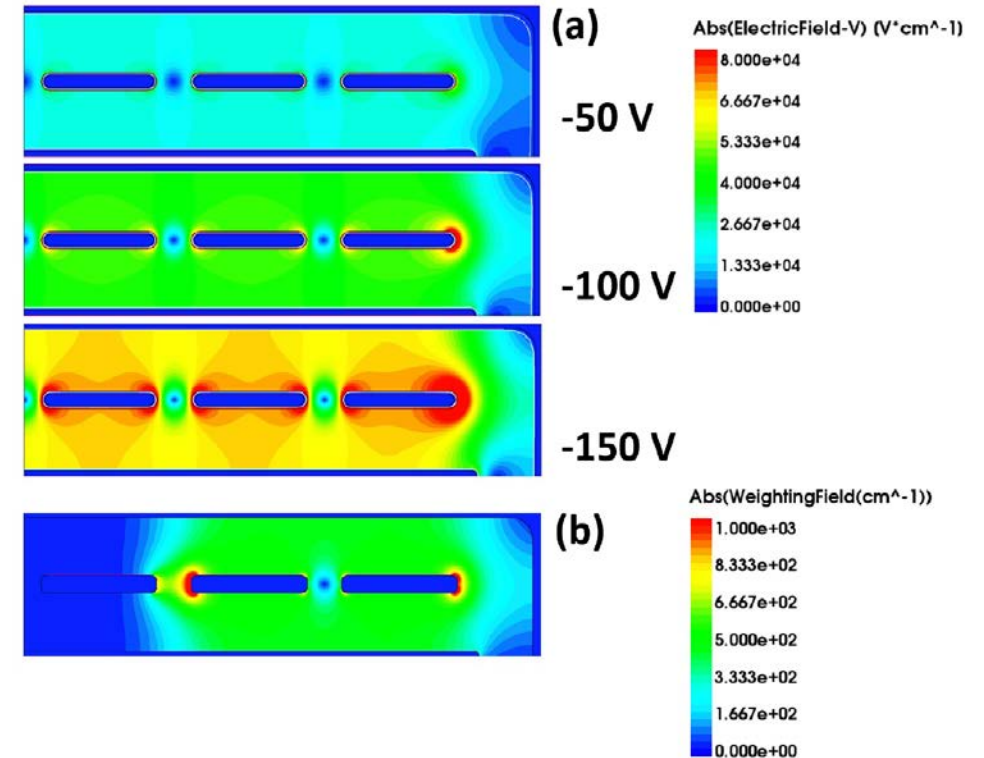
# TCAD outputs

## For detailed sensor characterization

D. Brundu et al., *Accurate modelling of 3D-trench silicon sensor with enhanced timing performance and comparison with test beam measurements.* JINST, 16, P09028, 2021



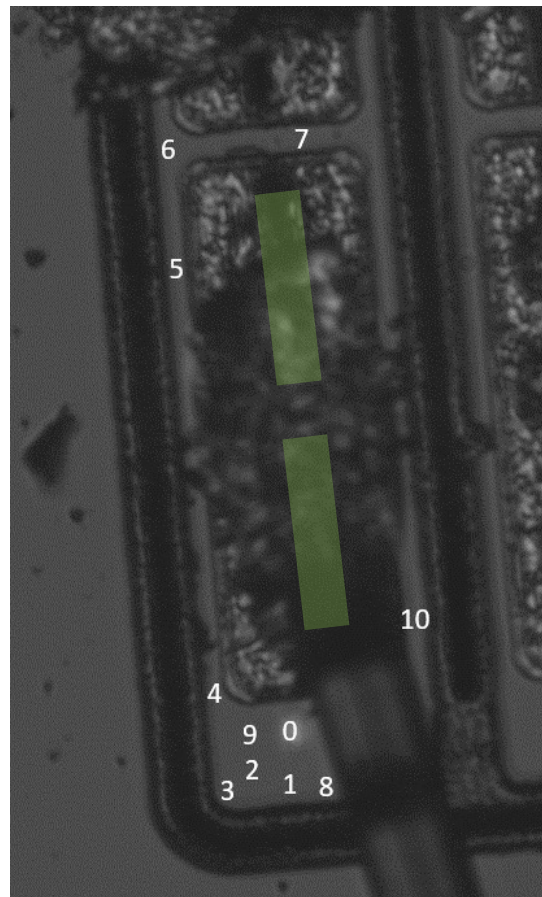
Layout of the simulated TimeSPOT test structure, including sections and sizes, designed using Sentaurus **TCAD**. The double pixel is indicated by the dotted-red line.



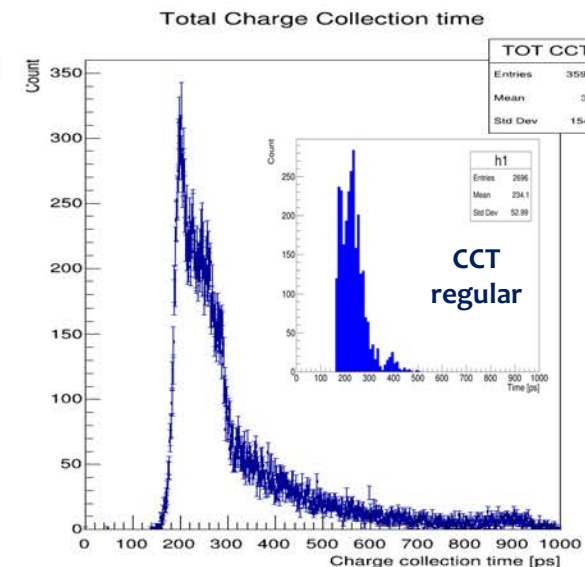
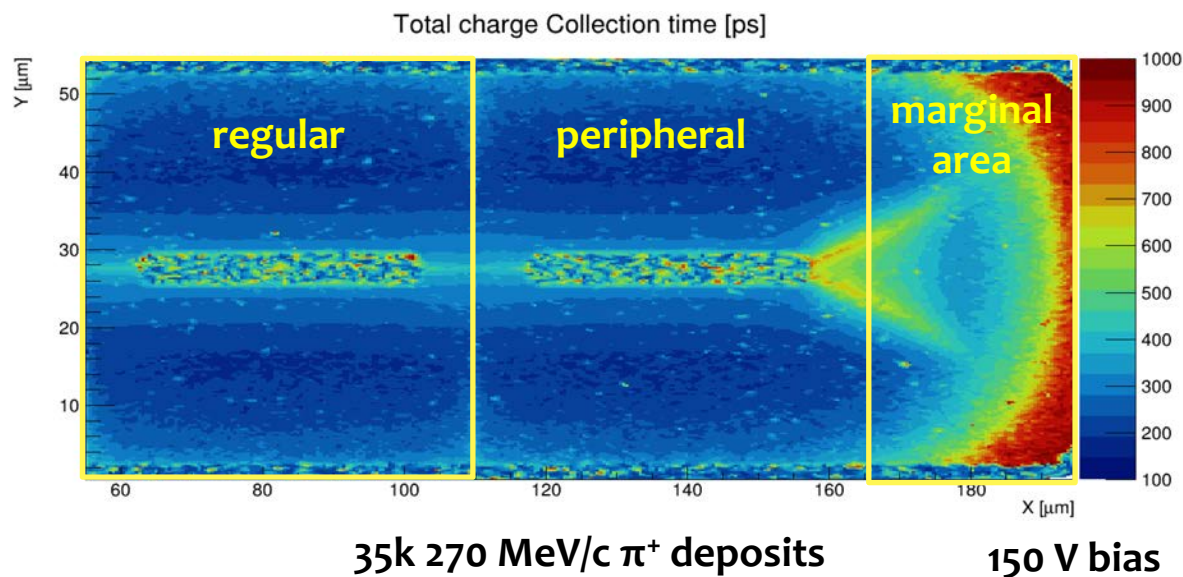
(a) Electric field amplitude at different bias voltages for the double-pixel test structure and  
(b) weighting field

# A virtual experiment on the DUT to identify tail contributions

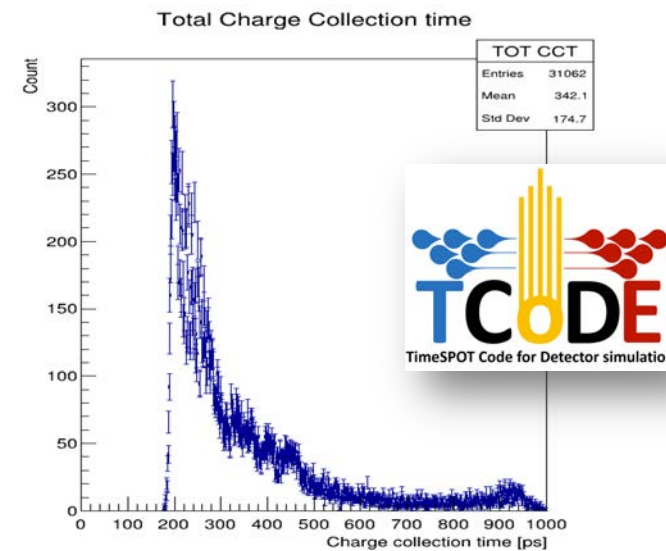
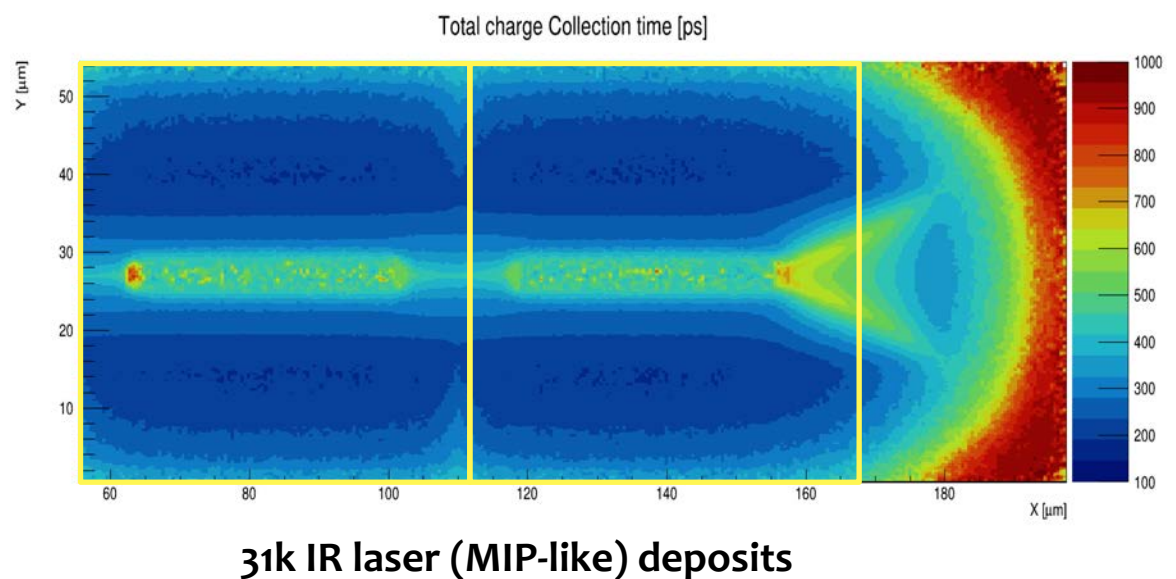
## Charge Collection Time distributions from TCoDe



Double pixel structure under test @ PSI test-beam ( $\sigma_t \approx 20$  ps + exponential tail)

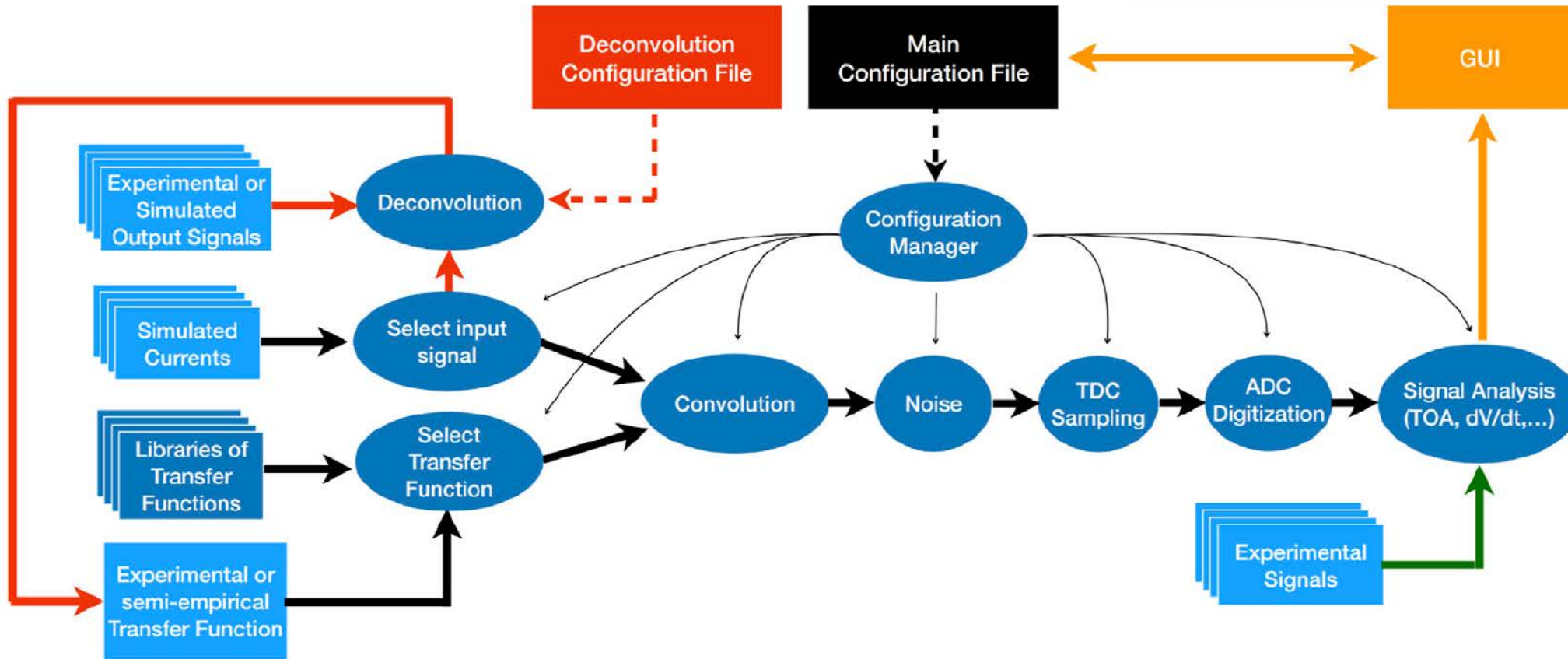


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Before convolution

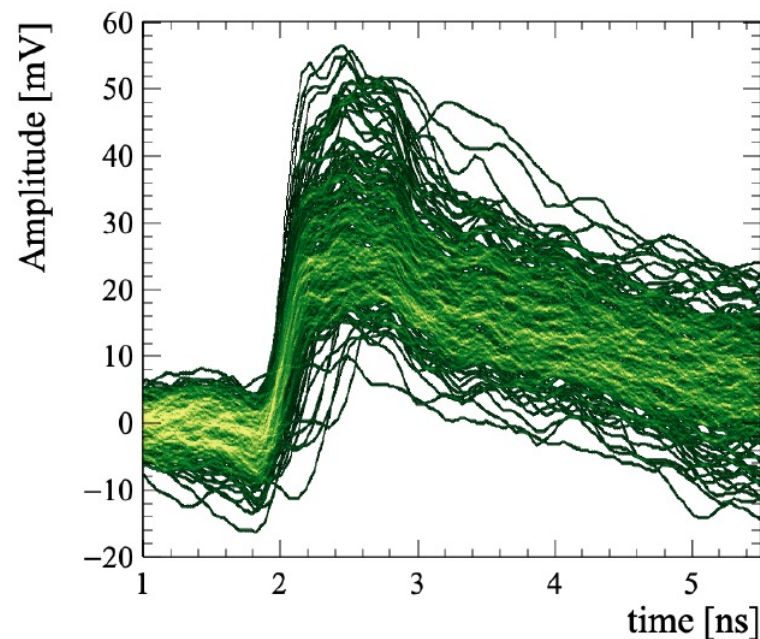
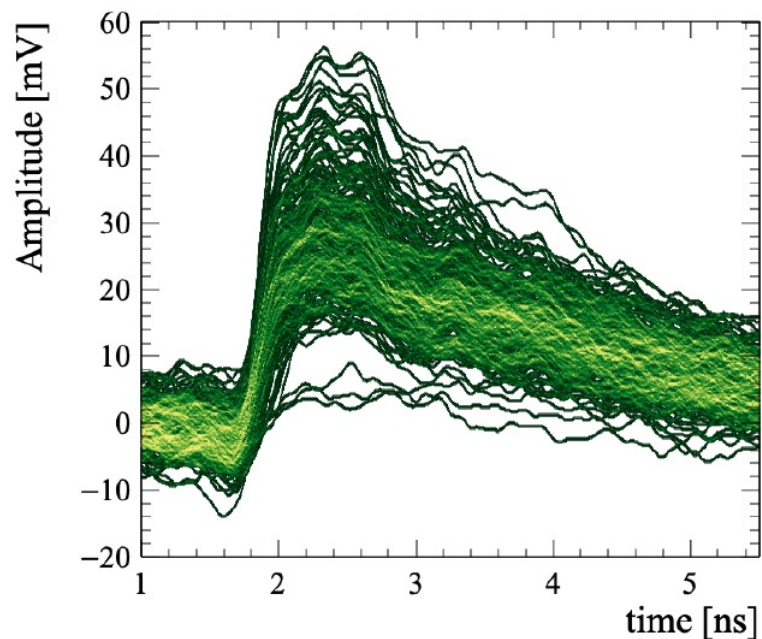
# F/E response? TFBoost!



**TFBoost simulations flow.** The black path is the main simulation in which the convolution and the signal analysis are performed. The green path is followed if TFBoost is used as a pure signal analyzer, while the red path is followed to perform the deconvolution between an input current and an output signal.

# Accurate re-analysis

## And the origin of the tails: simulation outputs



Overlap of all silicon sensor waveforms (about 200) for (left) simulation and (right) test beam data

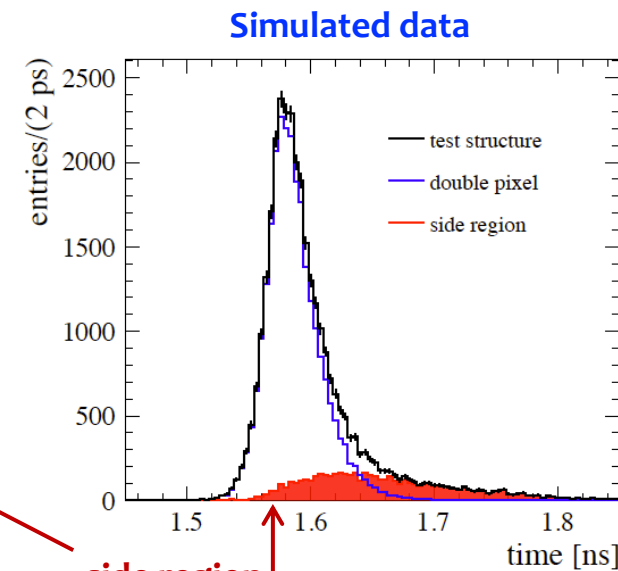
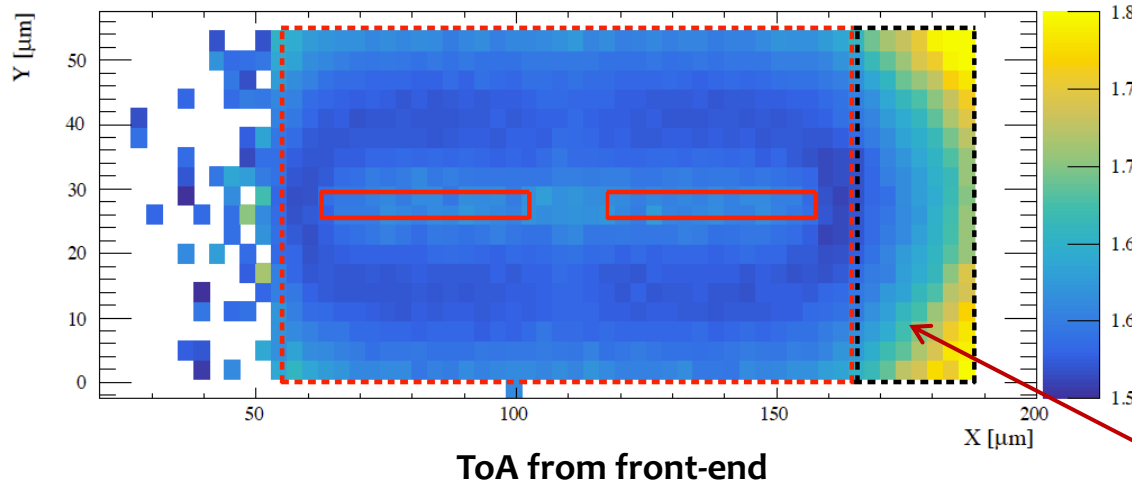
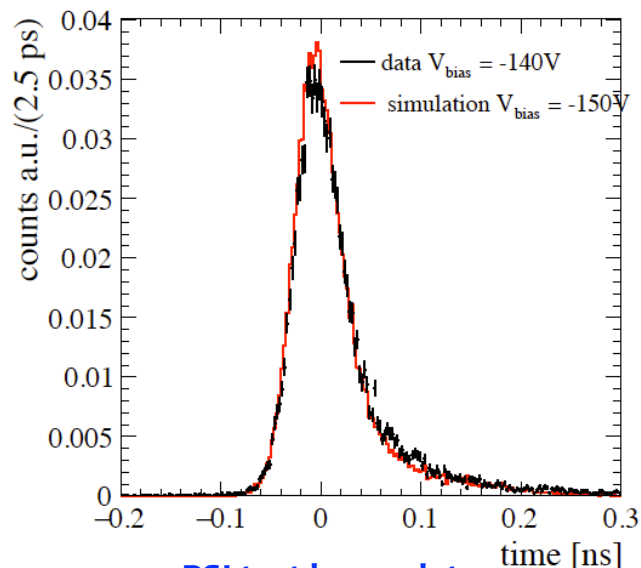
	$V_{\text{bias}}$ [V]	Amp( $P_{\text{max}}$ ) [mV]	$\langle S/N \rangle$	$\langle N \rangle$ [mV]	rise time [ps]	dV/dt [mV/ns]
Simulation	-50	25.0	14.6	2.11	247	103
	-100	24.5	14.3	2.17	224	113
	-150	24.4	14.2	2.19	217	116
Data	-50	24.1	14.3	2.19	258	111
	-110	24.4	13.9	2.30	221	123
	-140	24.7	14.2	2.29	217	126

Maximum amplitude, average signal-to-noise ratio, noise, rise time (20–80%) and slew rate (dV/dt) of the 3D-trench silicon sensor response at different values of the bias for simulation and data.  
**The statistical uncertainties are below 1%.**



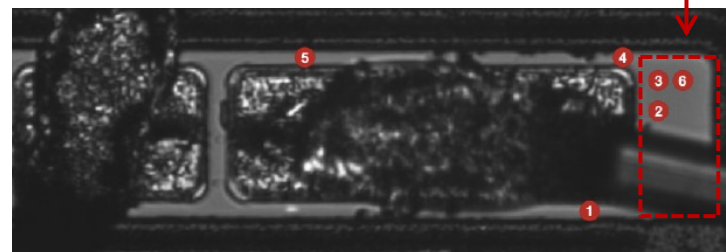
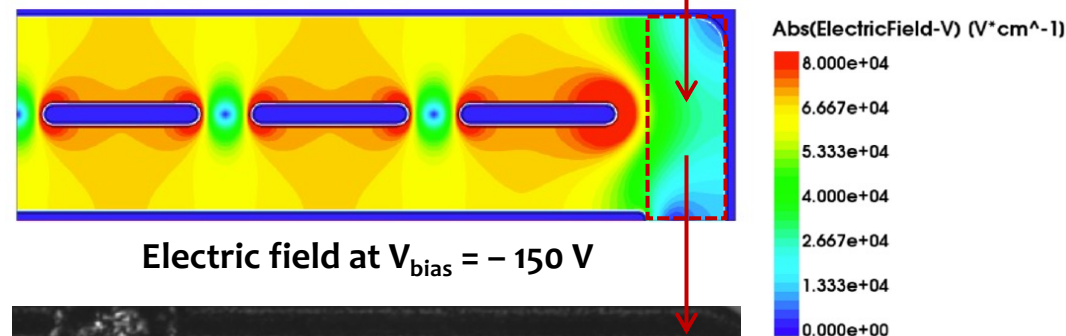
# Final response about the slow tails

The very special case of the double pixel



side region

Simulation			Measurement	
$V_{bias}$ [V]	$\sigma_{intrinsic}$ [ps]	$\sigma_t$ [ps]	$V_{bias}$ [V]	$\sigma_t$ [ps]
-50	9.6 ± 0.1	18.9 ± 0.2	-50	20.7 ± 0.3
-100	8.0 ± 0.1	16.7 ± 0.2	-110	19.8 ± 0.2
-150	7.0 ± 0.1	16.3 ± 0.2	-140	19.0 ± 0.2



Tails have been studied with **very accurate pixel modeling**, from the ionization process to the front-end output.  
 A clear assignation of the tail contribution was done to the **(out)side region** of the pixel (outside the nominal pixel area in this particular case).  
 As a by-product, simulations clearly indicate **a better intrinsic performance** of the sensor

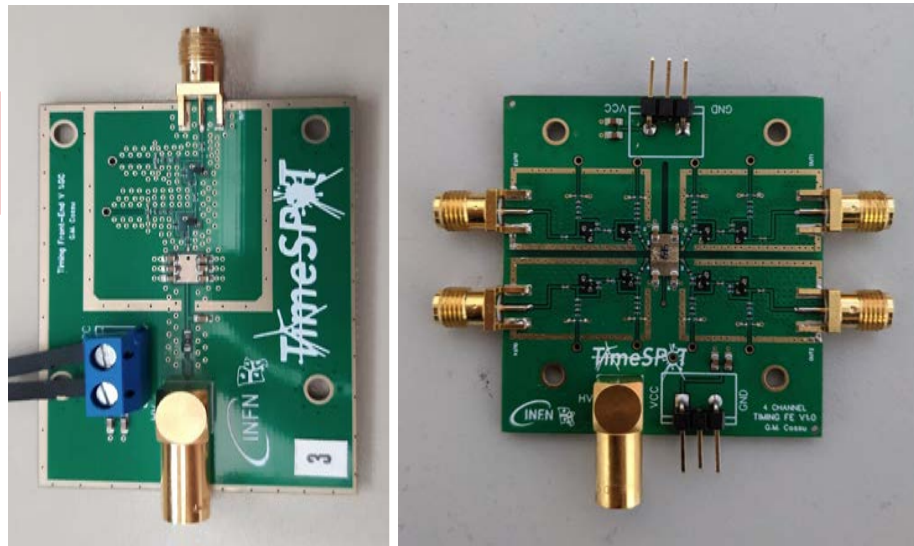
Measurements at test beams and  
3D-trench sensor characterization

# Latest results

Test-beams Nov21 & May22 @SPS/H8

**New faster dedicated front-end electronics**

Si-Ge input stages  $t_r \approx 100$  ps. Measured jitter  $< 7$  ps @ 2 fC  $\approx 70$  mW/channel



## 1. Not-irradiated:

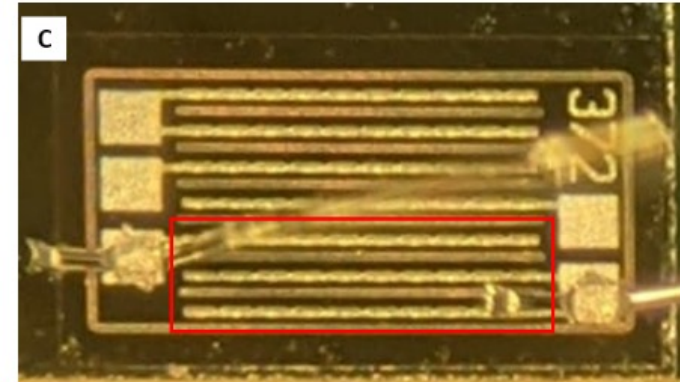
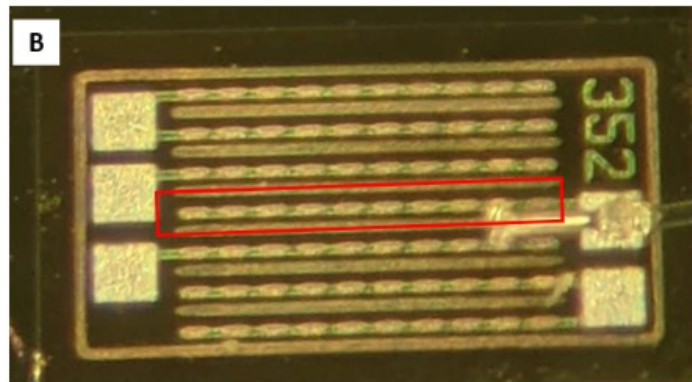
- Landau distributions vs  $V_{bias}$
- Time resolution
- Geometrical efficiency vs tilt angle
- Time resolution vs tilt angle

## 2. Same with samples irradiated @ $\Phi = 2.5 \cdot 10^{16}$ 1-MeV-n/cm<sup>2</sup>

## 3. First studies on charge sharing

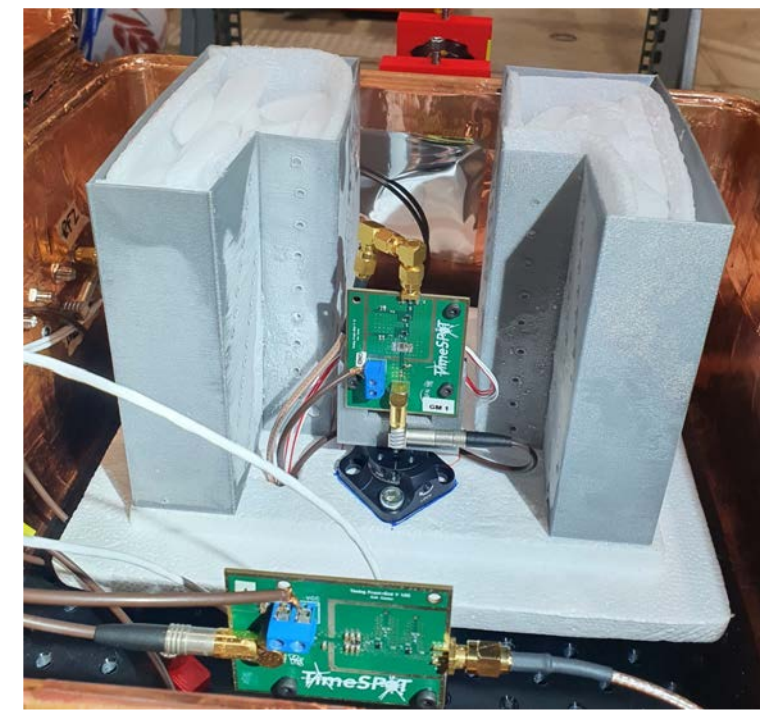
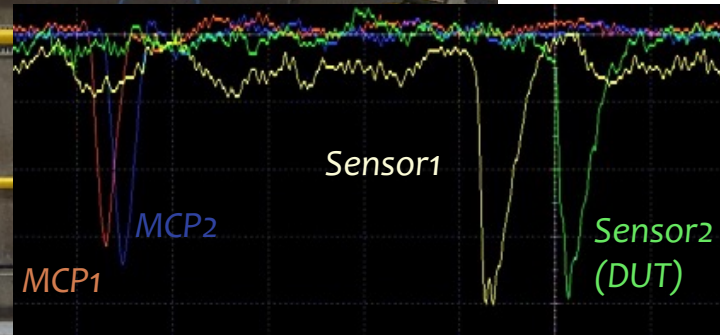
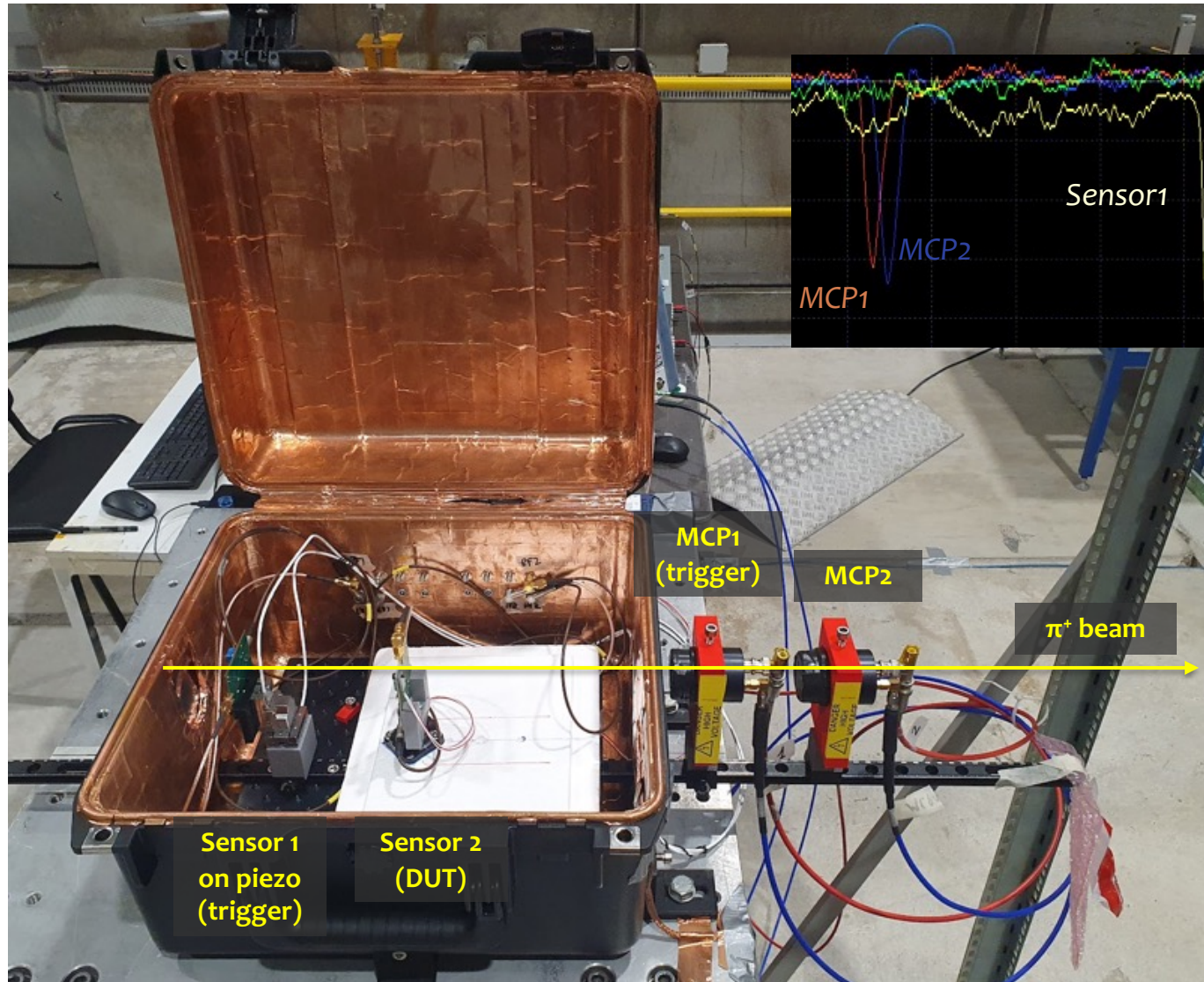
Tested structures. For each sensor the active area is shown in red.

(A) Single pixels sensor; (B) strip sensor; (C) triple strip sensor



# Experimental setup

Test-beams Nov21 & May22 @SPS/H8



180 GeV/c  $\pi^+$  beam

2 MCP-PMTs on the beam line to time-stamp the arriving particle ( $\sigma_{\text{avg}} = 5$  ps)

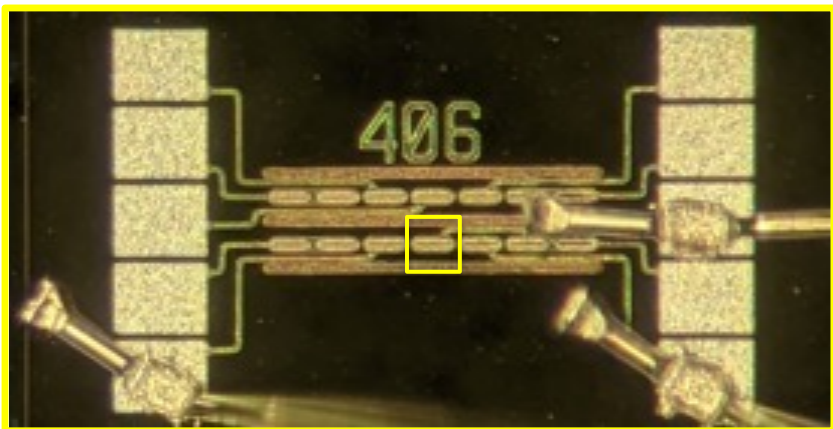
Piezoelectric stages to precisely align the two 3D structures with beam, all mounted in a RF-shielded box

Possibility of operating the fixed sensor down to  $-40^\circ\text{C}$  using dry ice to test irradiated sensors

Readout with an 8 GHz bandwidth 20 GSa/s scope: trigger on the AND of one 3D sensor and one MCP-PMT

# Amplitude distributions vs bias

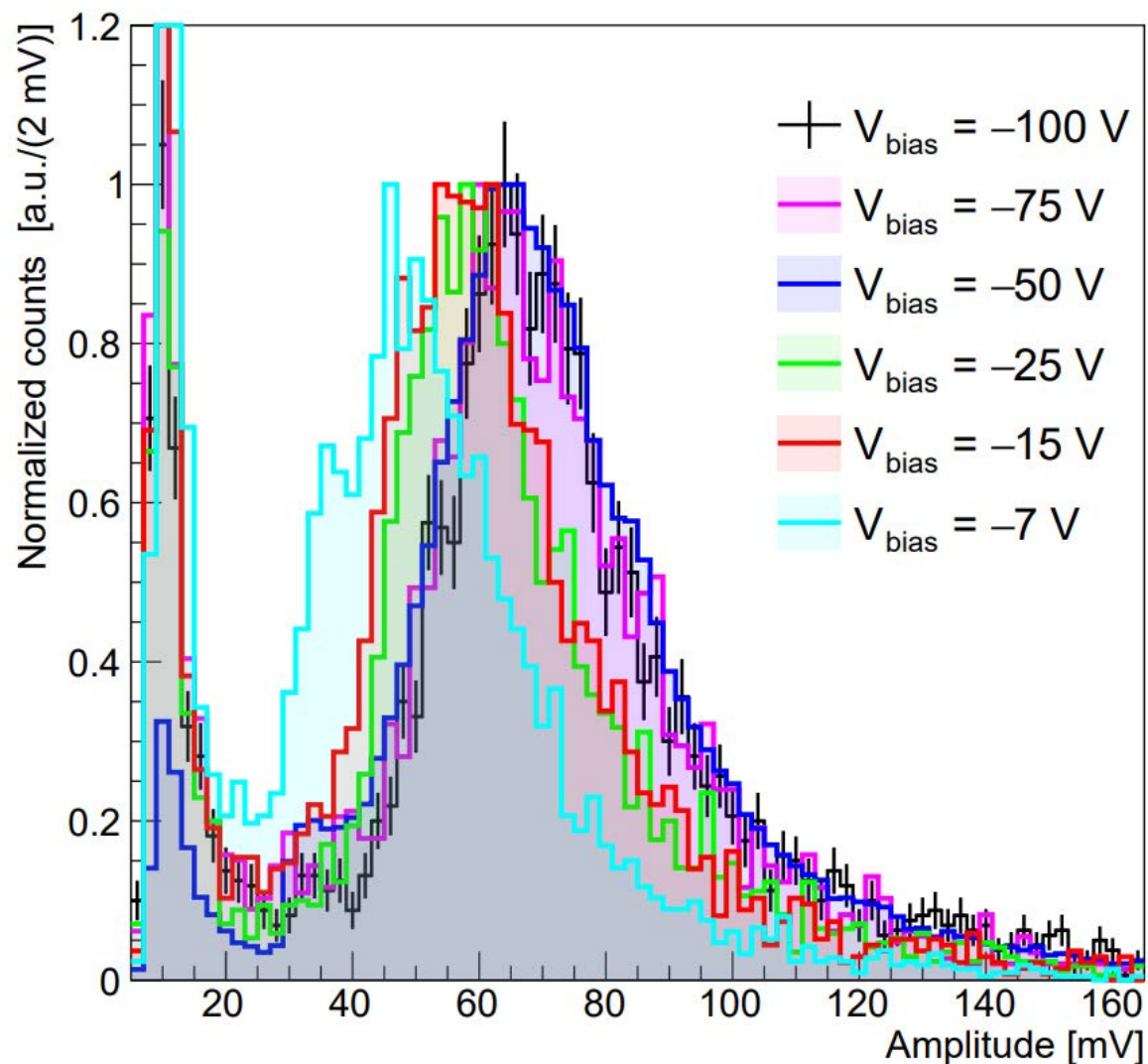
## Single pixel, not irradiated



Normal pion incidence ( $\alpha_{tilt} = 0^\circ$ )

DUT not on the trigger

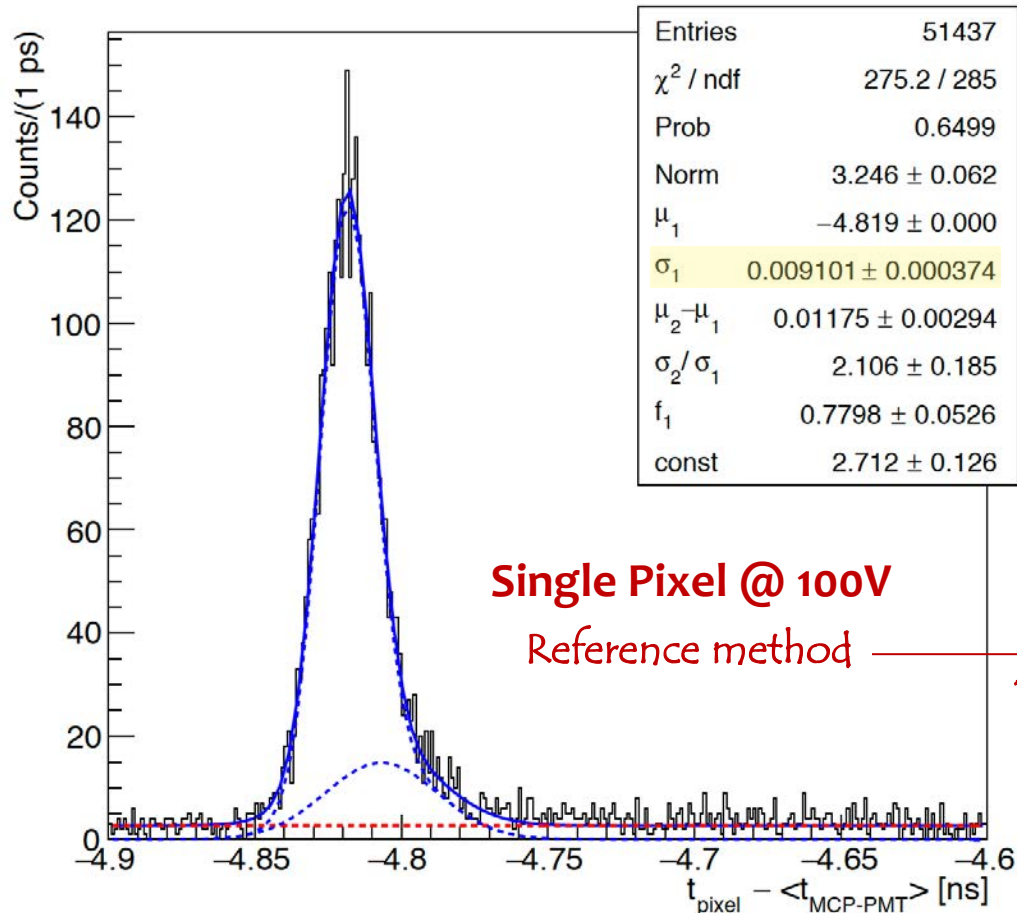
Very good sensor performance even at **low**  $V_{bias}$   
(prompt full depletion)



# Timing measurements

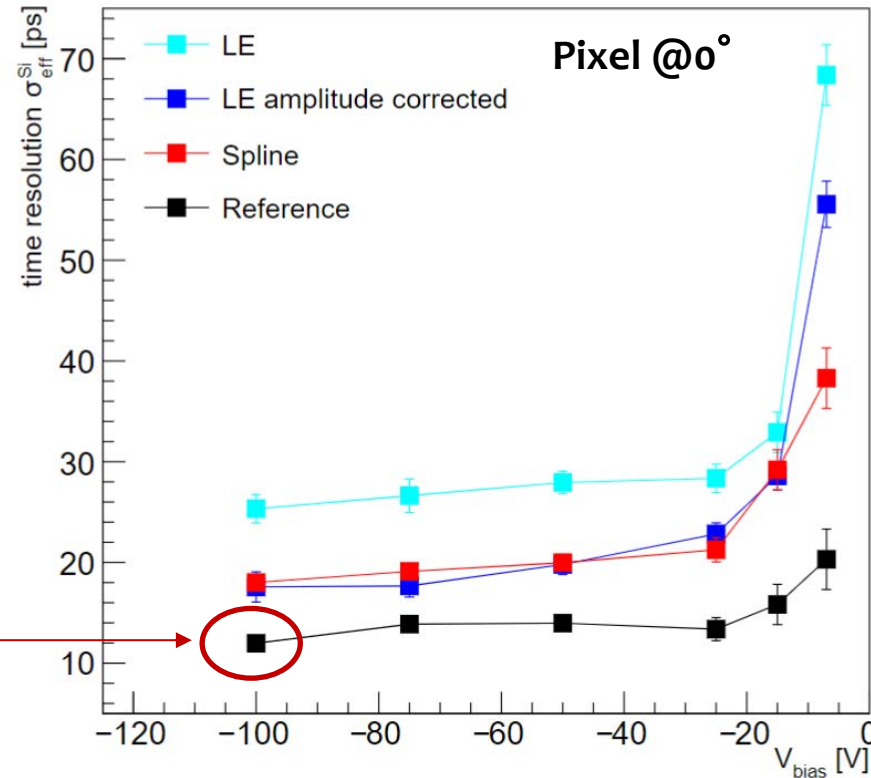
(single pixel @  $\alpha_{tilt} = 0^\circ$ , not irradi.) SPS/H8 (Nov'21)

- LE: Leading edge, NO ToT correction
- LE: Leading edge, ToT correction
- Spline: Classic CFD
- Reference: Differentiation + CFD



Single Pixel @ 100V  
Reference method

$\sigma_t^{\text{eff}}$   
11.5 ps



$$(\sigma_t^{\text{eff}})^2 = f_1(\sigma_1^2 + \mu_1^2) + (1 - f_1) \cdot (\sigma_2^2 + \mu_2^2) - \mu^2$$

Where  $f_1$  is the fraction of the core Gaussian and  $\mu$  is defined as

$$\mu = f_1\mu_1 + (1 - f_1) \cdot \mu_2$$

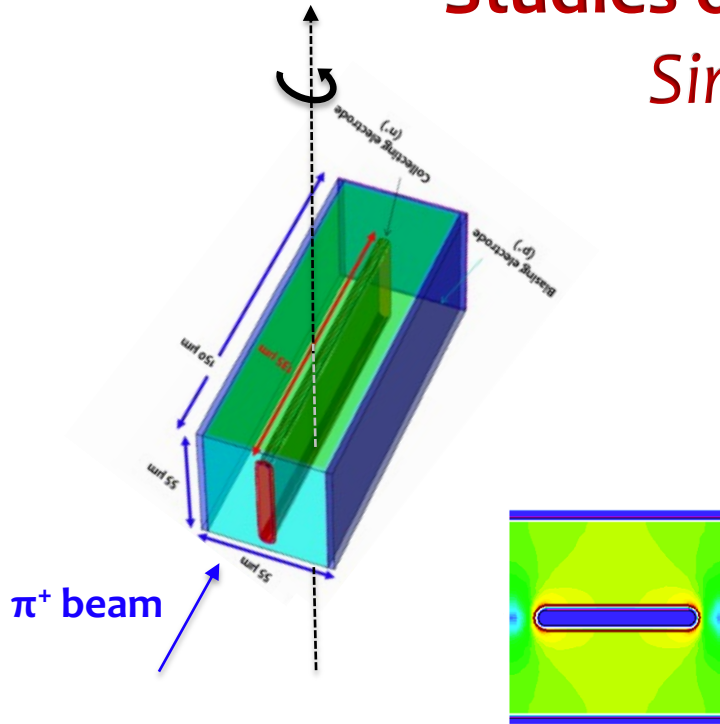
$\sigma_t^{\text{eff}}$  takes into account the two-Gaussian behaviour

Distribution of the difference between the TOA of the single pixel and the time reference,  $t_{\text{pixel}} - \langle t_{\text{MCP-PMT}} \rangle$ , for the single pixel perpendicular to the beam at  $V_{\text{bias}} = -100$  V with the reference method. The distribution is fit with the sum of two Gaussian functions (blue dashed lines) describing the signal, and a constant (red dashed line) modelling the background.

Paper to be submitted soon to Frontiers in Physics: "New results on the TimeSPOT 3D-silicon sensors from measurements at SPS"

# Studies of Geometric Efficiency: setup

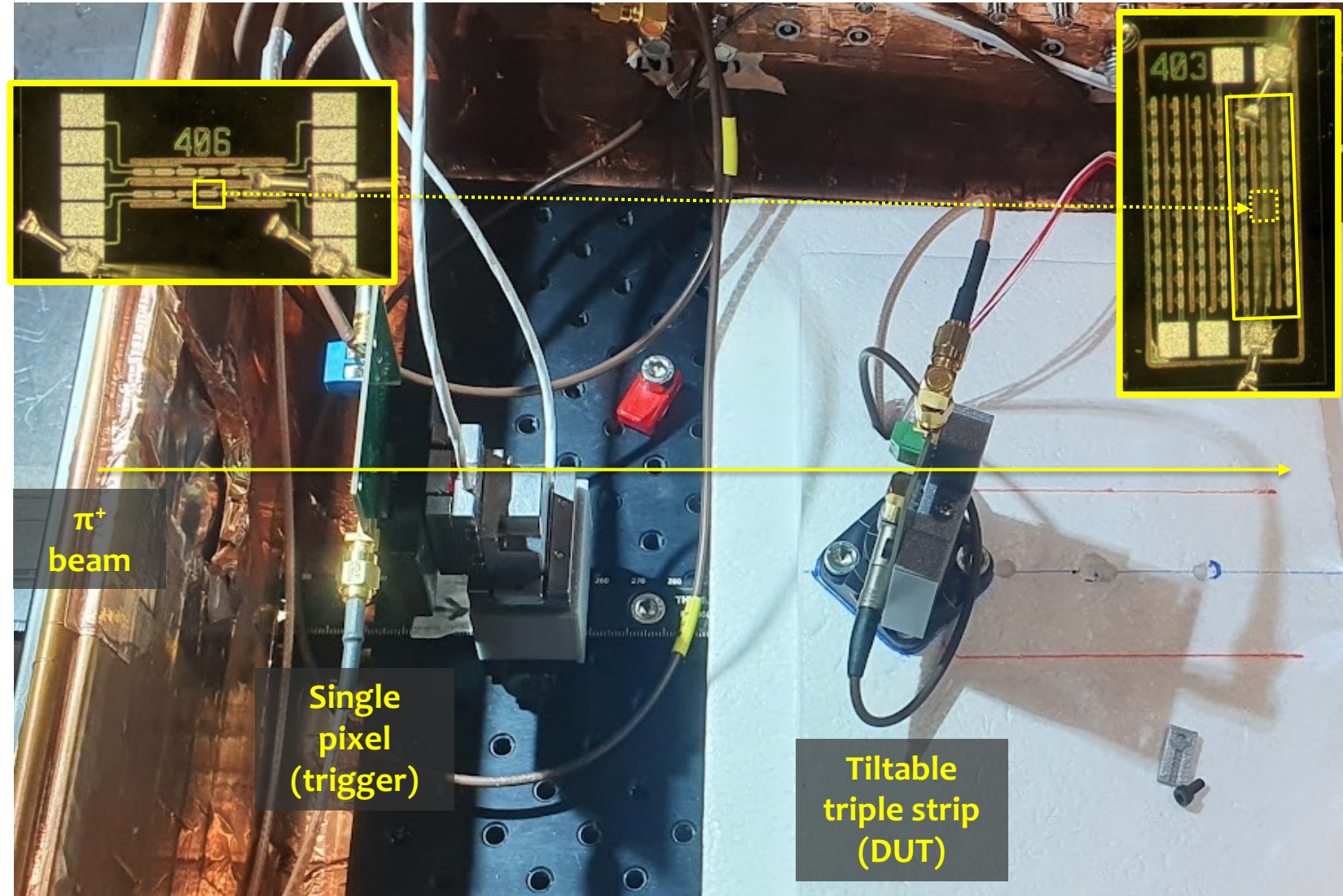
## Single pixel, not irradiated



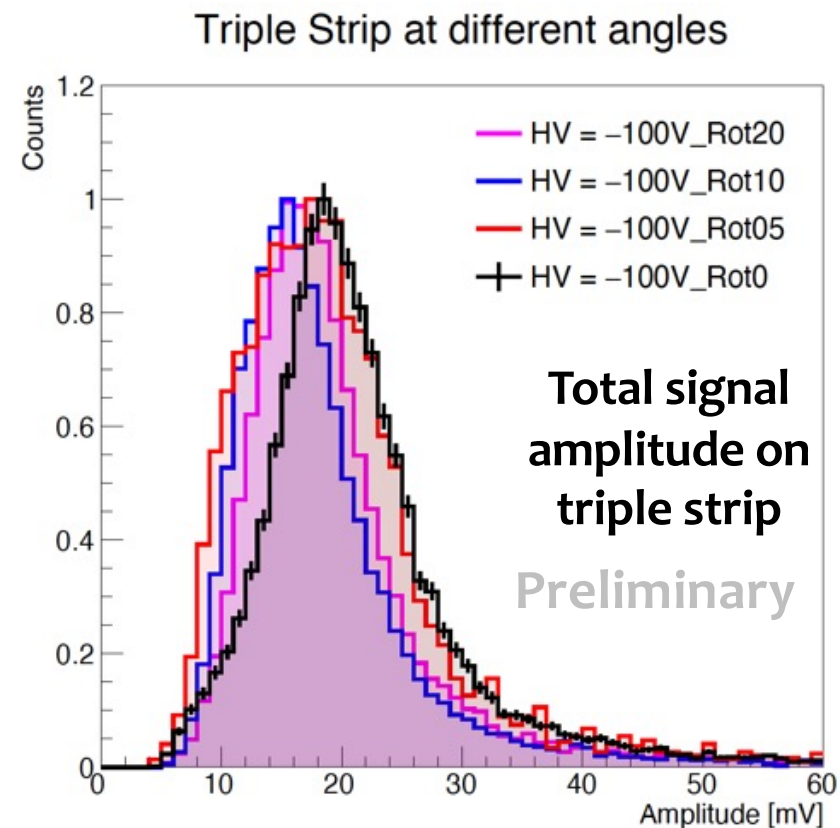
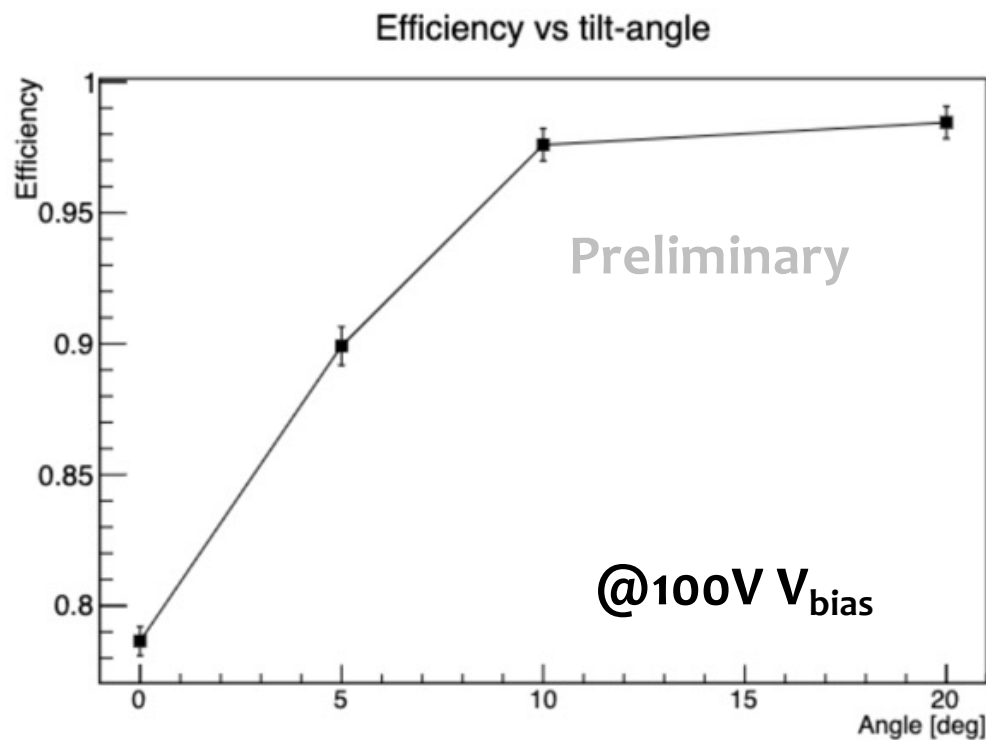
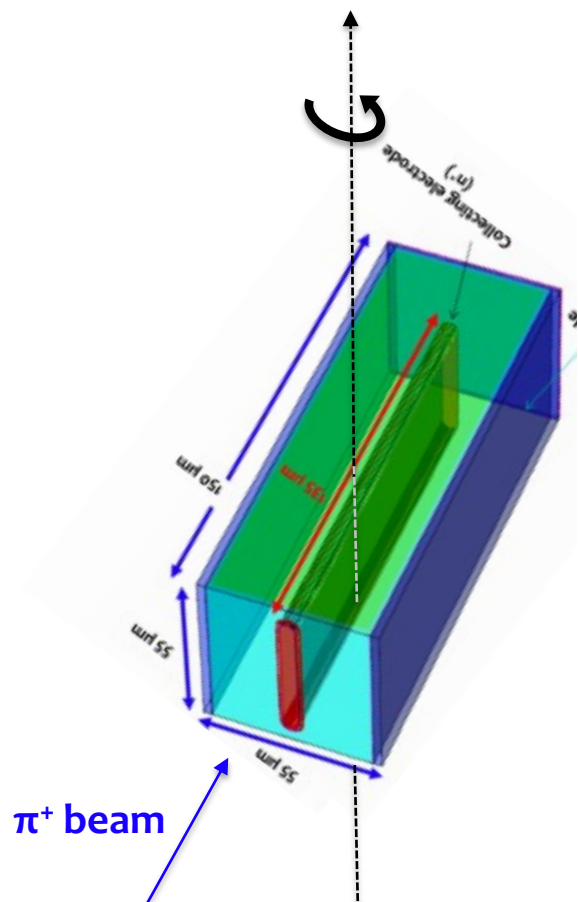
Tilting the sensors with respect to normal incidence should allow to recover geometric efficiency

Trigger on one pixel (55 μm x 55 μm, on piezos) centered on a triple strip (165 μm x 550 μm, DUT) and counting the fraction of signals seen in the triple strip (on a single FE channel)

The DUT is rotated around the trench direction



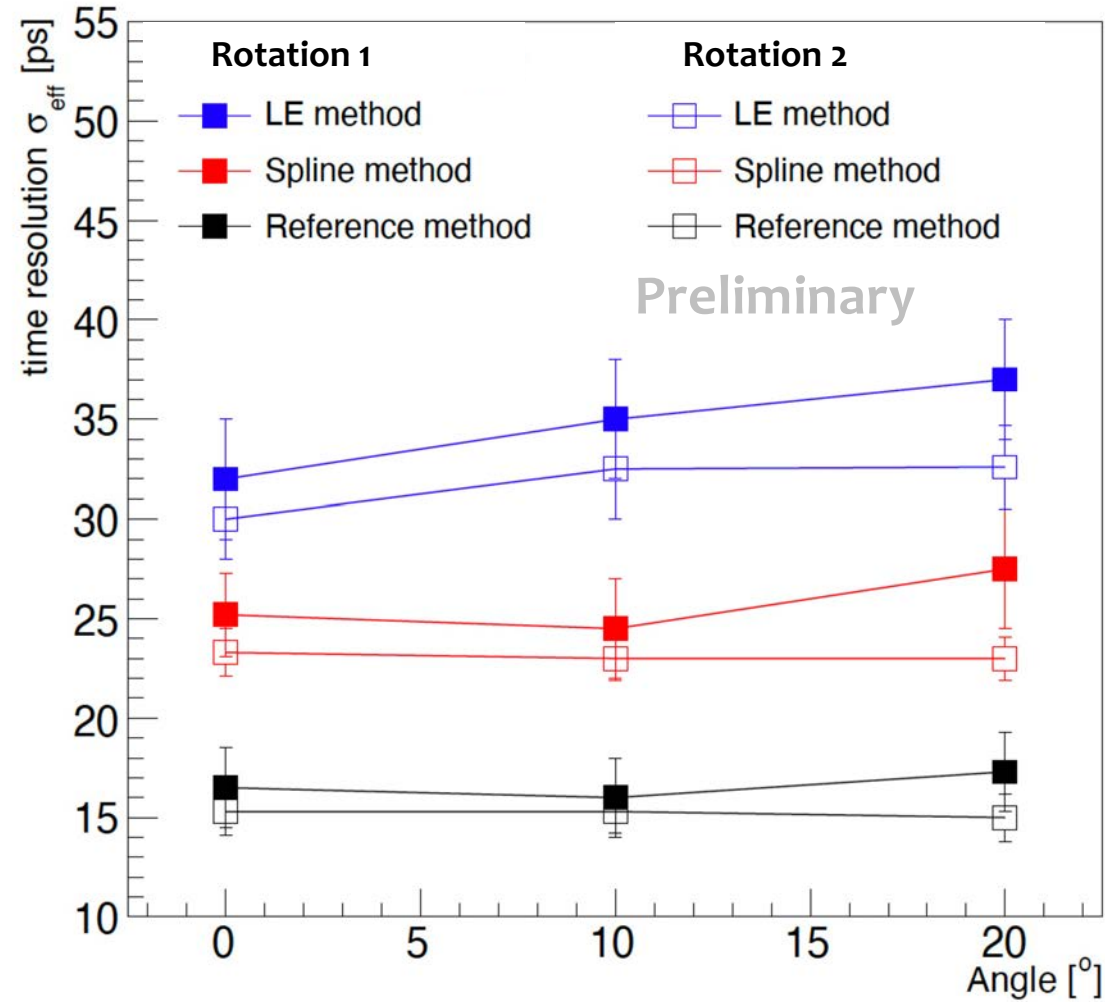
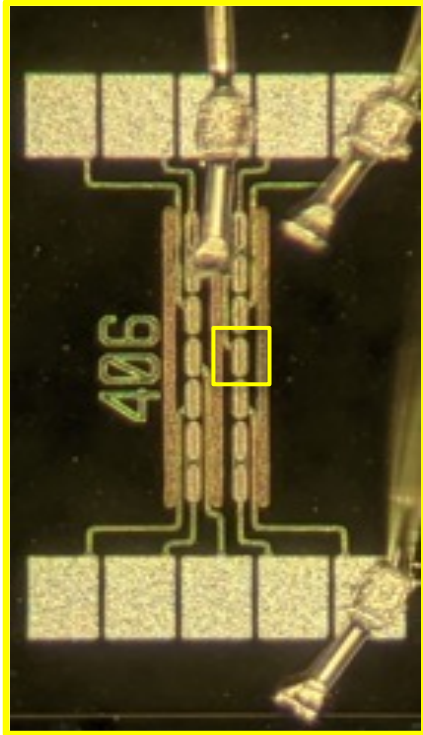
# Efficiency: results



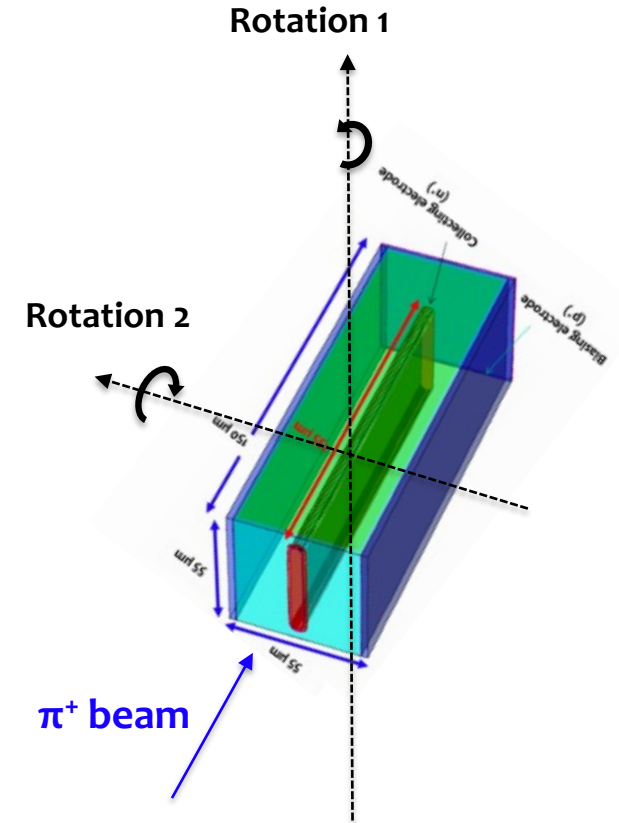
The inefficiency (at normal incidence) due to the 3D pixel dead-area of the trenches is fully recovered by tilting the sensors around the trench axis at angles larger than 10°



# Tilted sensors: timing performance



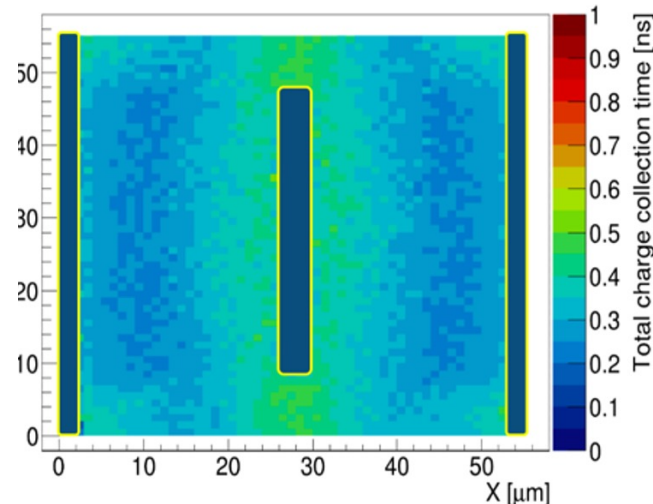
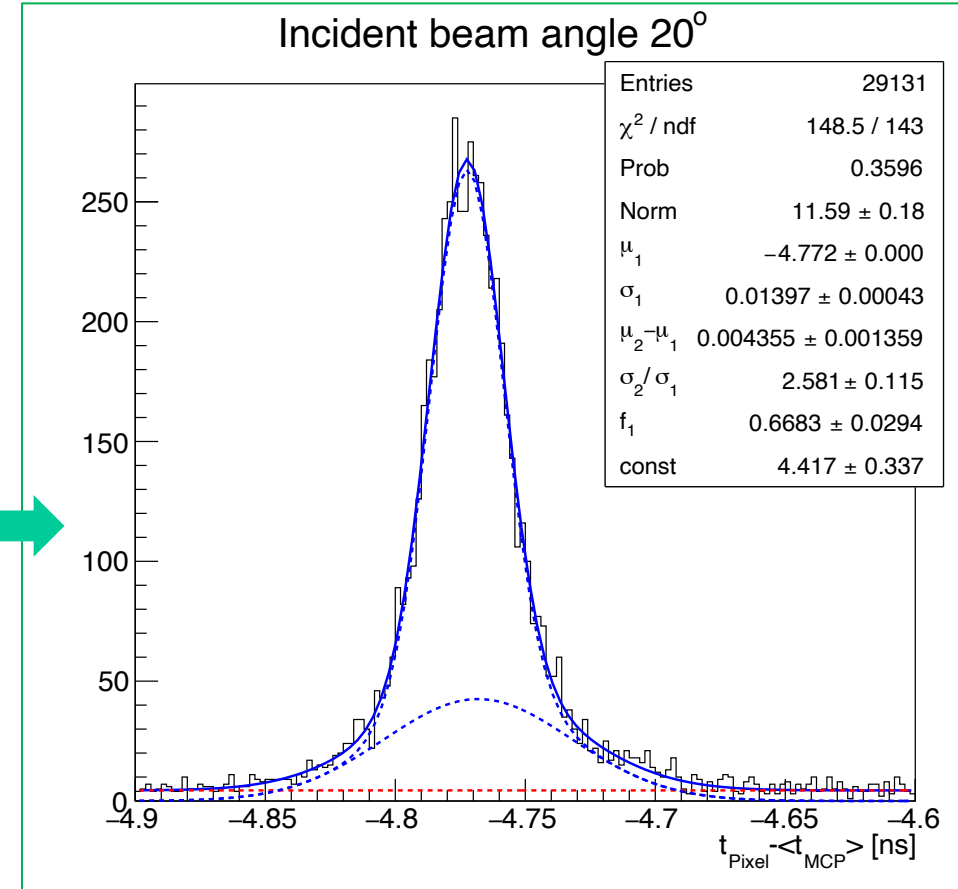
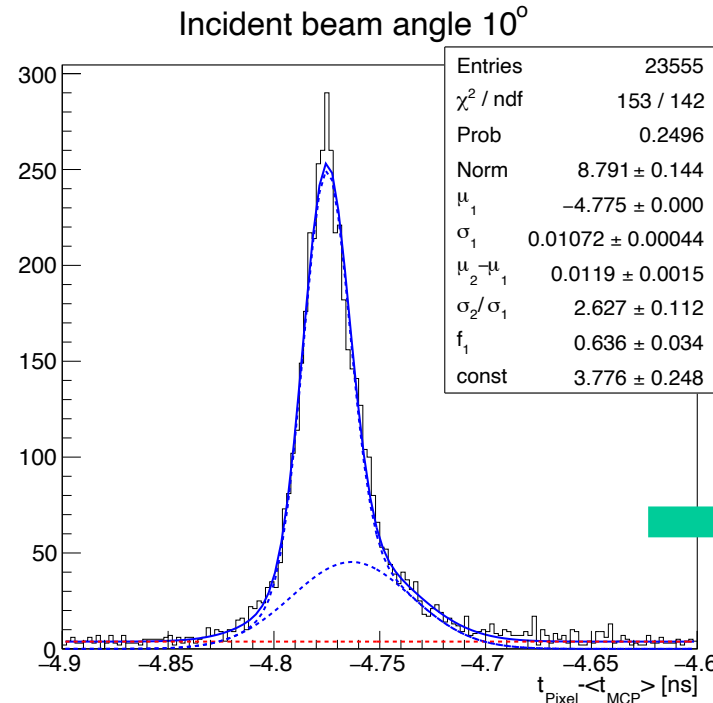
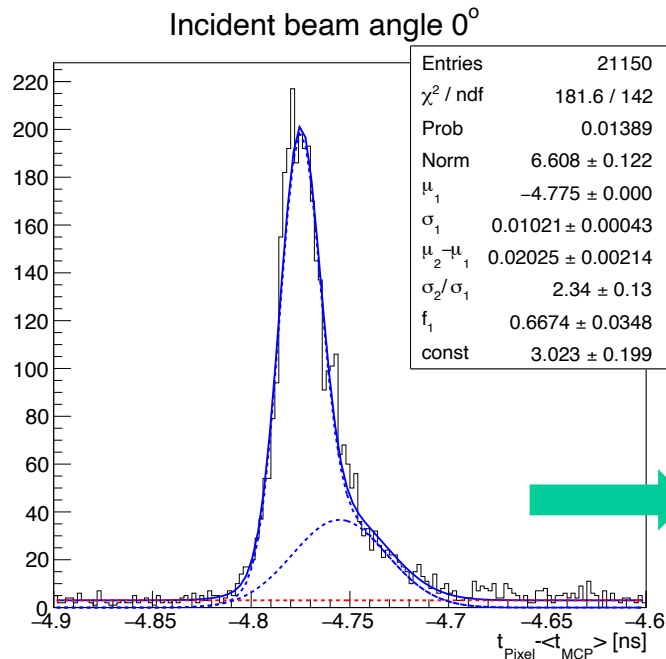
Single Pixel @ 50V



# Effect of tilting on distribution shapes

Spline method, SPS/H8 (Nov'21)

Single Pixel @ 50V

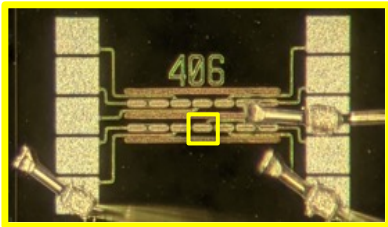


Simulated CCT map of a single 3D-trench sensor pixel scan ( $\alpha_{\text{tilt}} = 0^\circ$ )

Tilting has the effect of «mixing up» the fast and less-fast regions of the pixels, thus uniforming the timing response

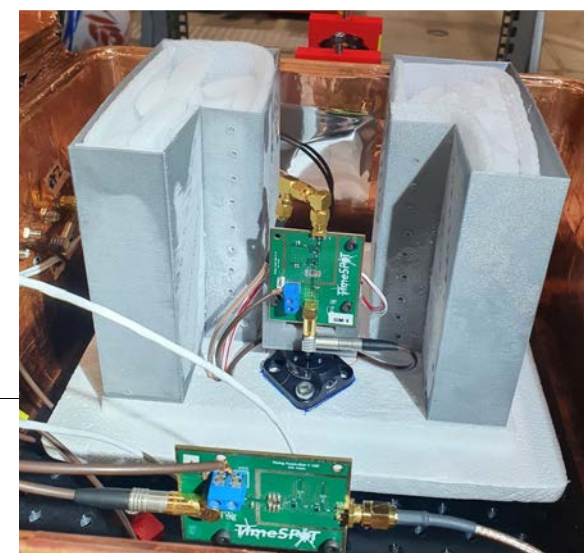
As a result, the shapes are more Gaussian at increasing  $\alpha_{\text{tilt}}$

Notice that, due to detection efficiency,  $\alpha_{\text{tilt}} = 20^\circ$  is the normal working condition of a 3D in a detecting system

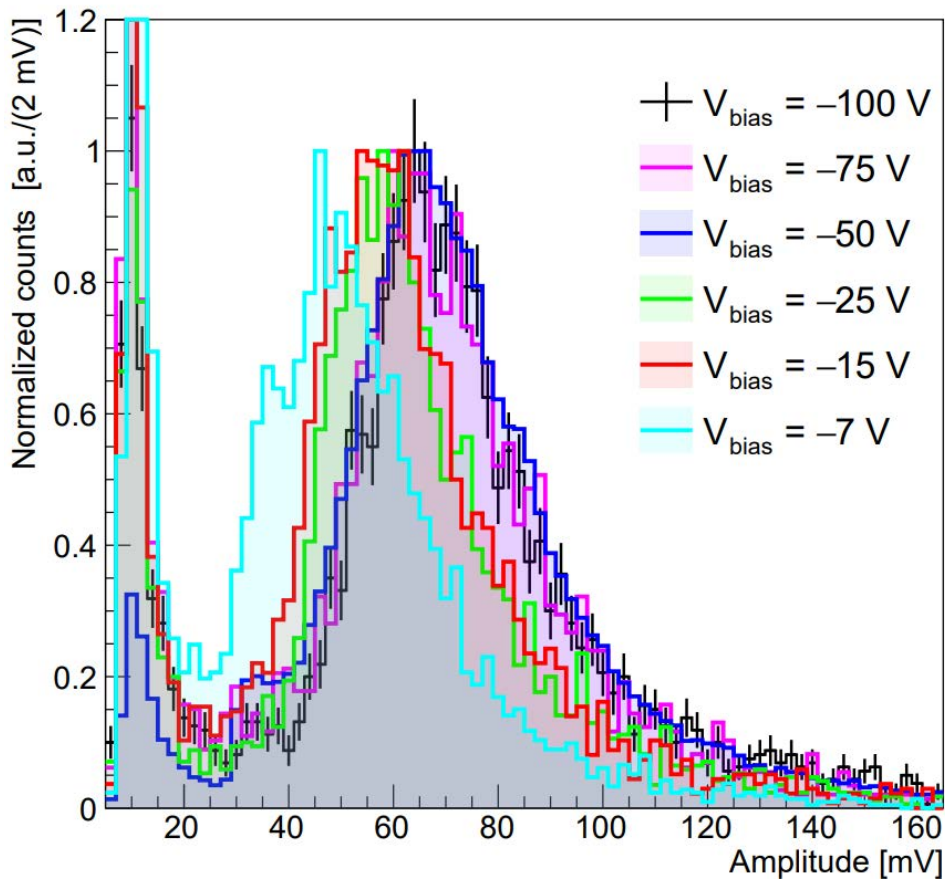


# Amplitude distributions vs bias

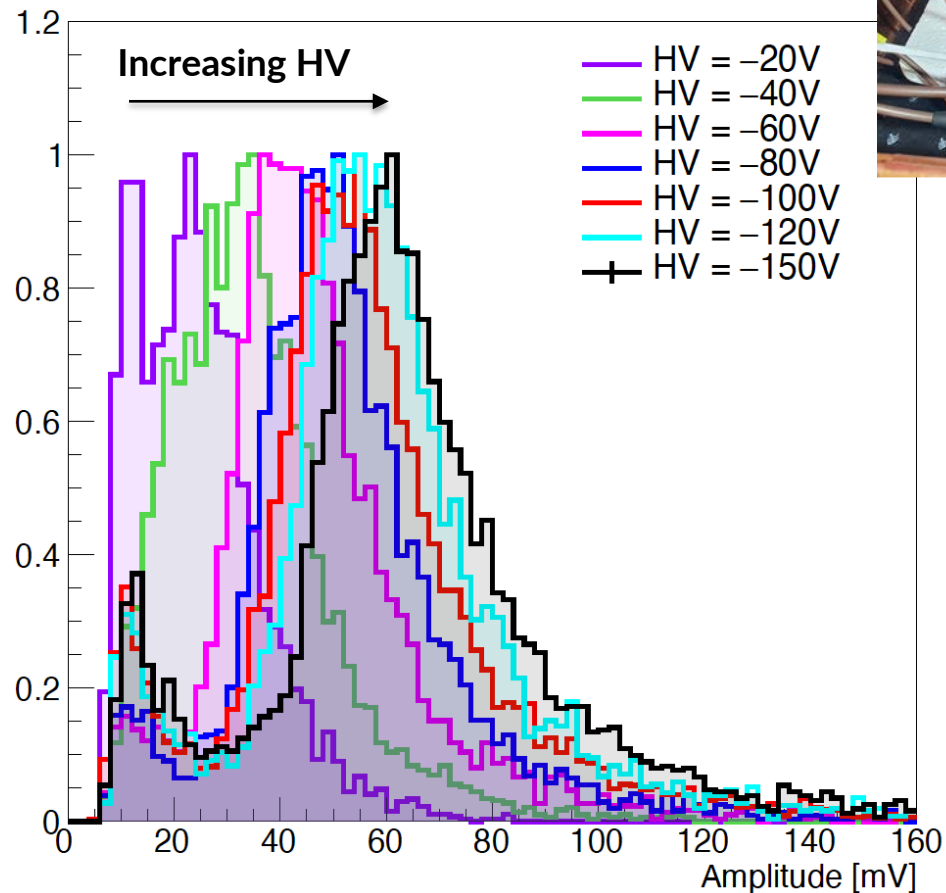
## Single pixel, irradiated



Not IRRADIATED,  $\alpha_{tilt} = 0^\circ$

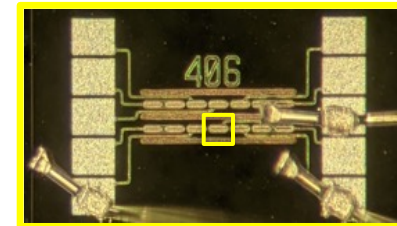


Irradiated @  $2.5 \cdot 10^{16} n_{eq}/cm^2$ ,  $\alpha_{tilt} = 0^\circ$

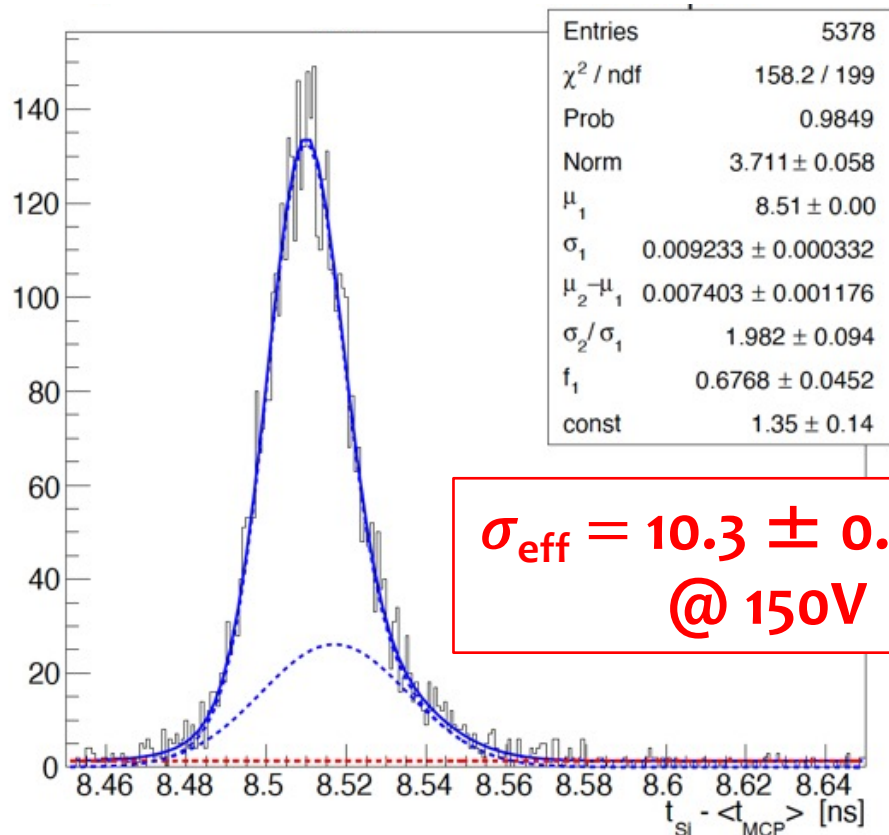


The effect of fluence is evident from the  $\Delta V_{bias}$  needed to reach the same Amplitude

# Irradiated sensors: timing performance

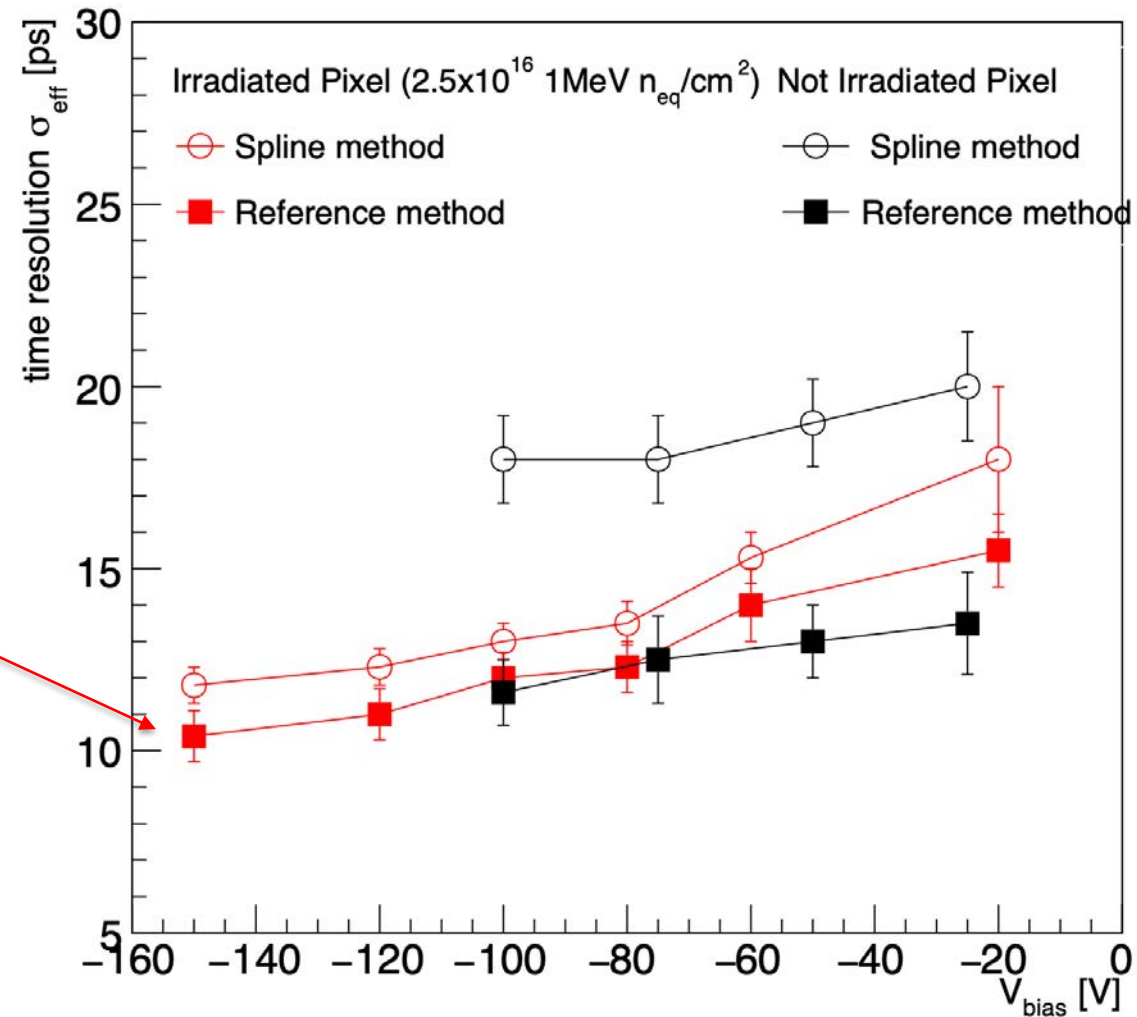


Irradiated @  $2.5 \cdot 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ ,  $\alpha_{\text{tilt}} = 0^\circ$

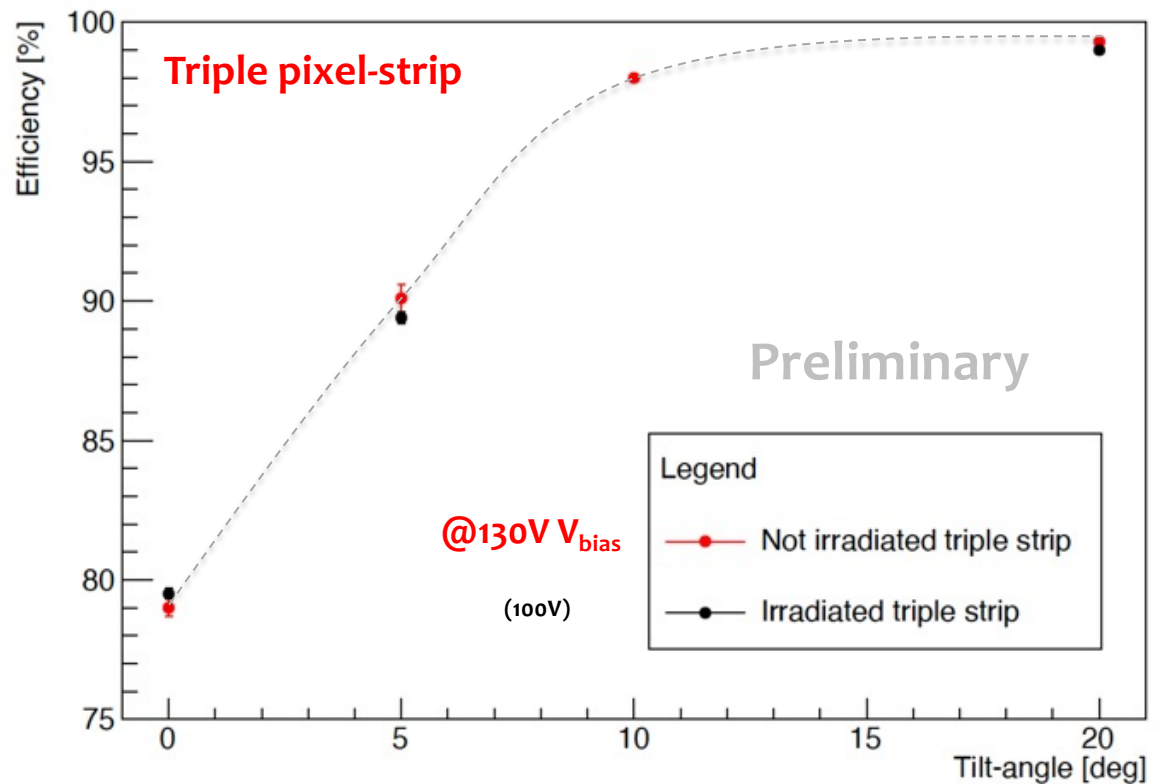
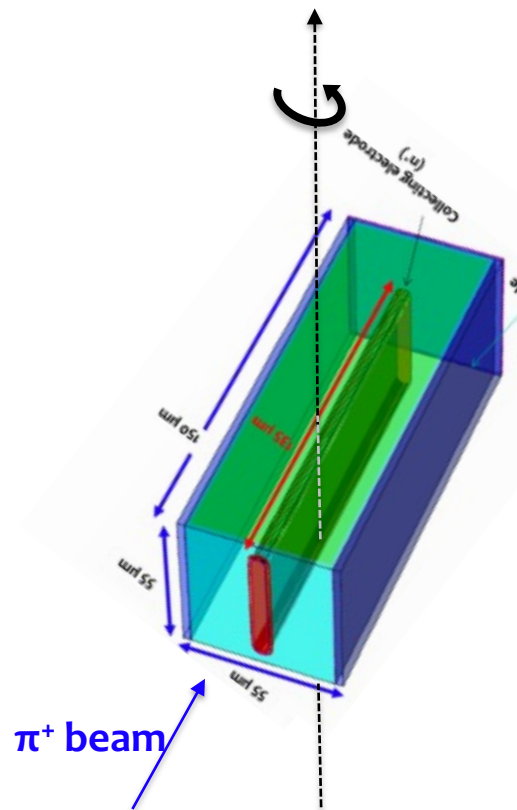
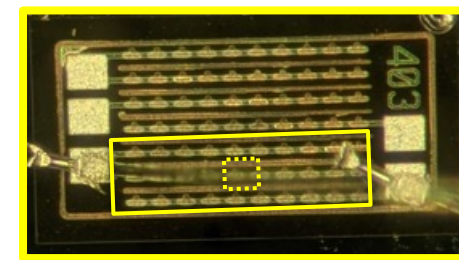


$\sigma_{\text{eff}} = 10.3 \pm 0.5 \text{ ps}$   
@ 150V

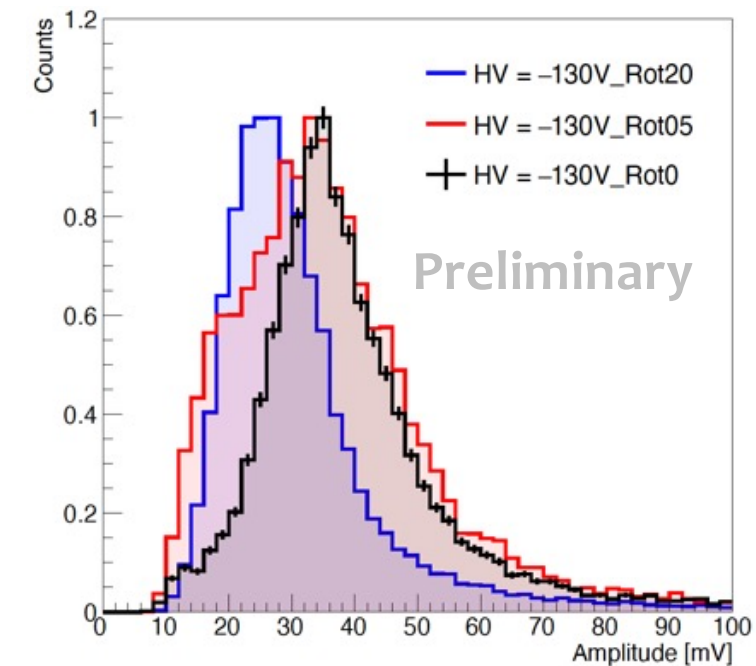
To be compared with 11 ps @ 100 V  
of the not-irradiated case



# Irradiated sensors: geometrical efficiency



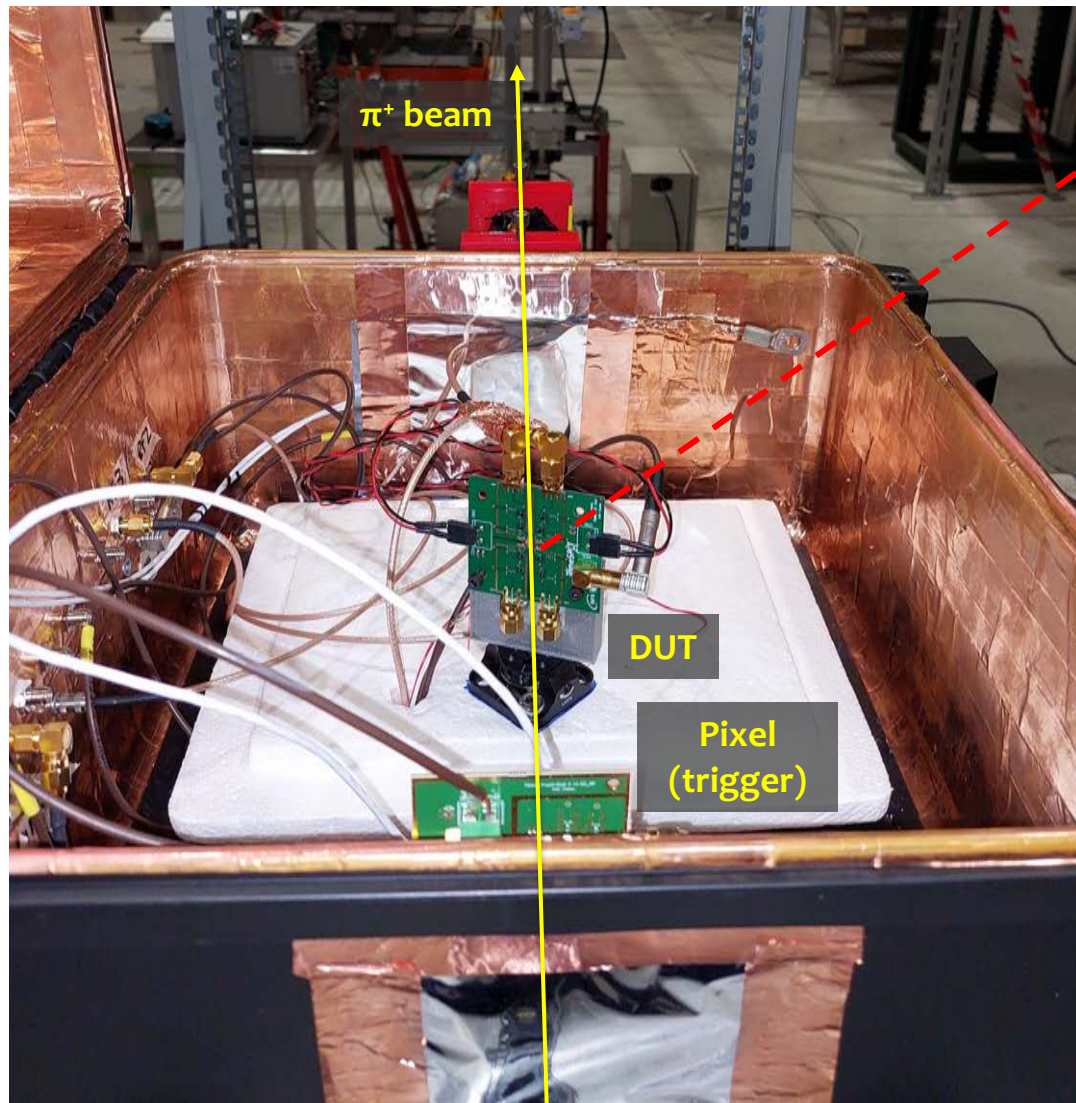
Triple strip @  $2.5 \cdot 10^{16} n_{eq}/cm^2$ ,  $\alpha_{tilt} = 0^\circ, 5^\circ, 20^\circ$



The inefficiency (at normal incidence) due to the dead-area of the trenches is fully recovered by tilting the sensors around the trench axis

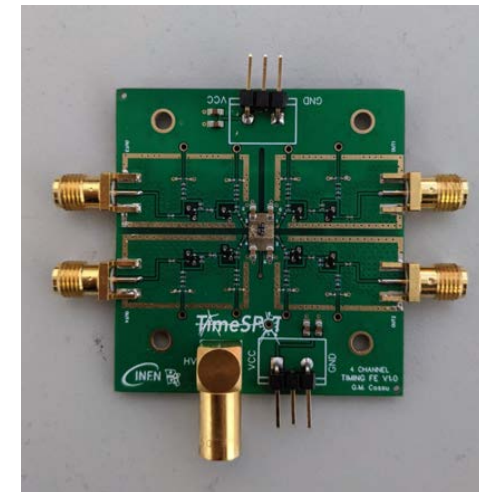
also for sensors irradiated with fluences of  $2.5 \cdot 10^{16}$  1-MeV neutron equivalent

# Charge sharing studies: setup



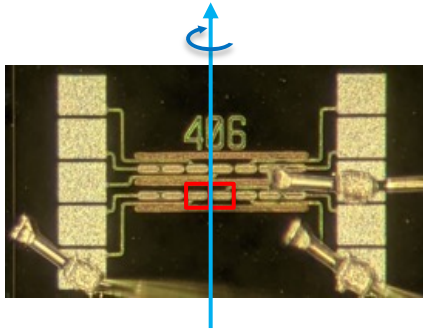
4-channel FEE board

2 adjacent pixels –  
each one read-out by  
one FEE channel



Tilting the sensor it is possible to study the  
behaviour of two pixels when a charged particle  
crosses both of them

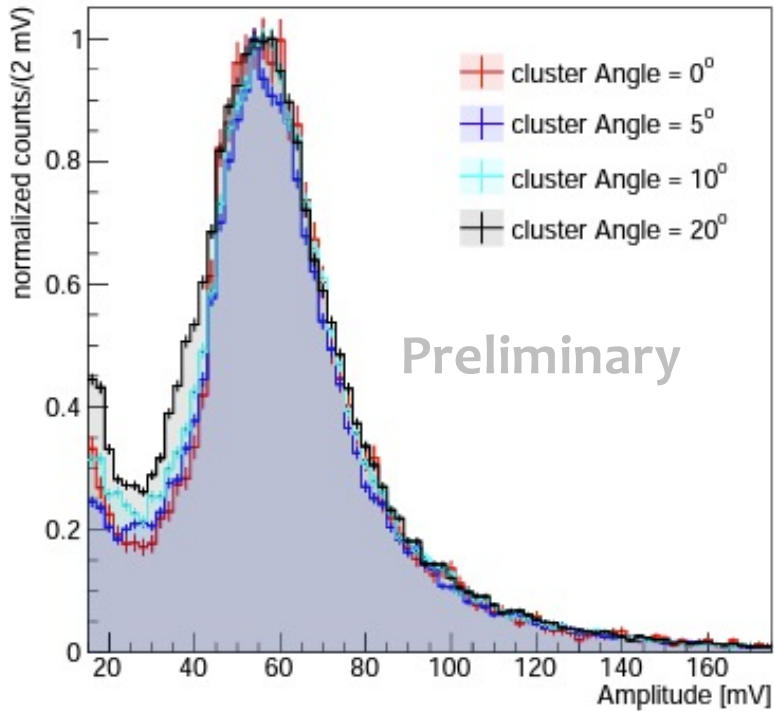
# Charge sharing studies: results



When a particle crosses two pixels:

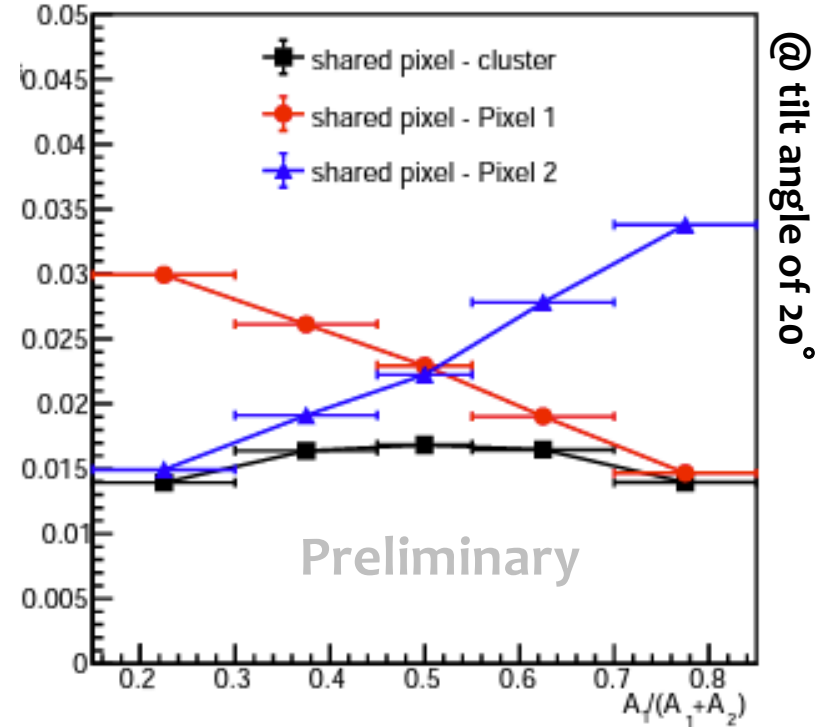
1. Amplitude = sum of the amplitudes of the two signals
2. Time of Arrival = weighted sum on amplitudes of the ToA in the two pixels

Amplitude distributions at different angles



Combining the two pixels information, it is possible to recover the amplitude distribution expected at normal incidence angle

Time resolution as a function of the fraction of sharing



Using the information of both pixels, timing performance improves

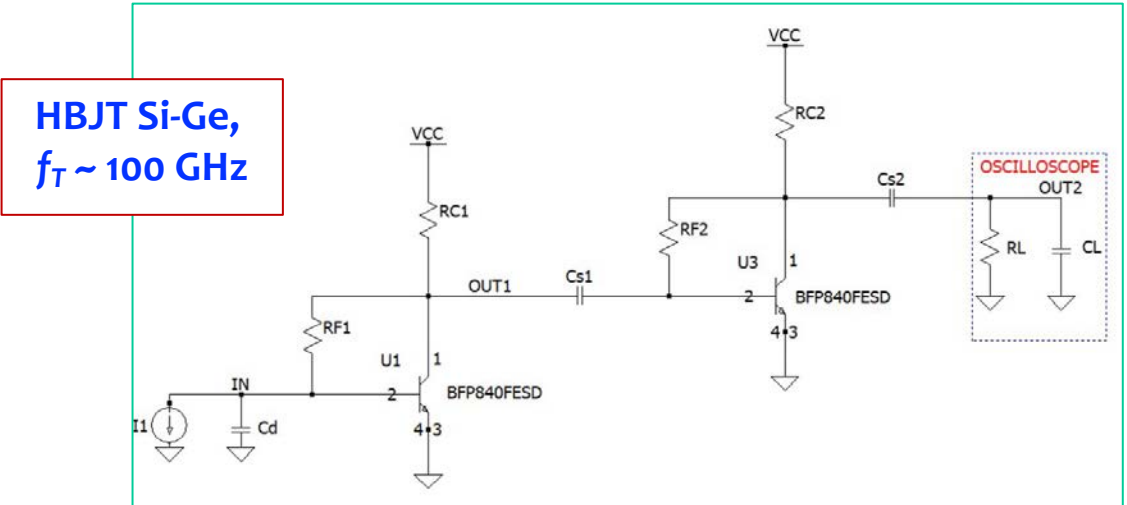
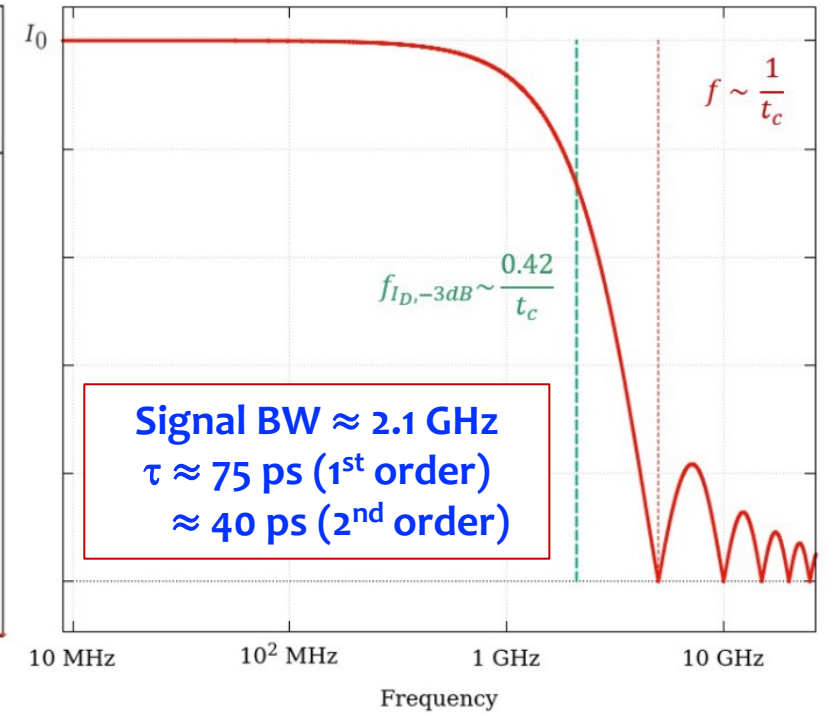
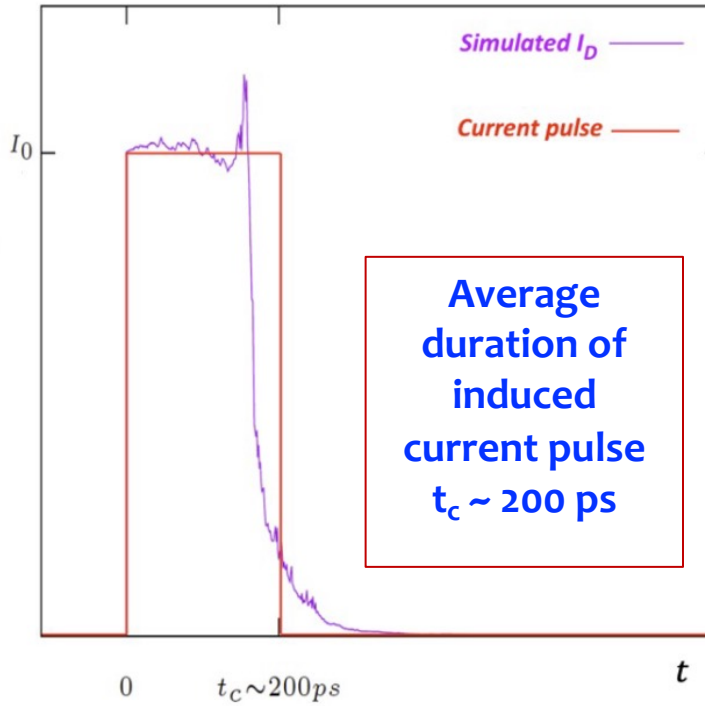
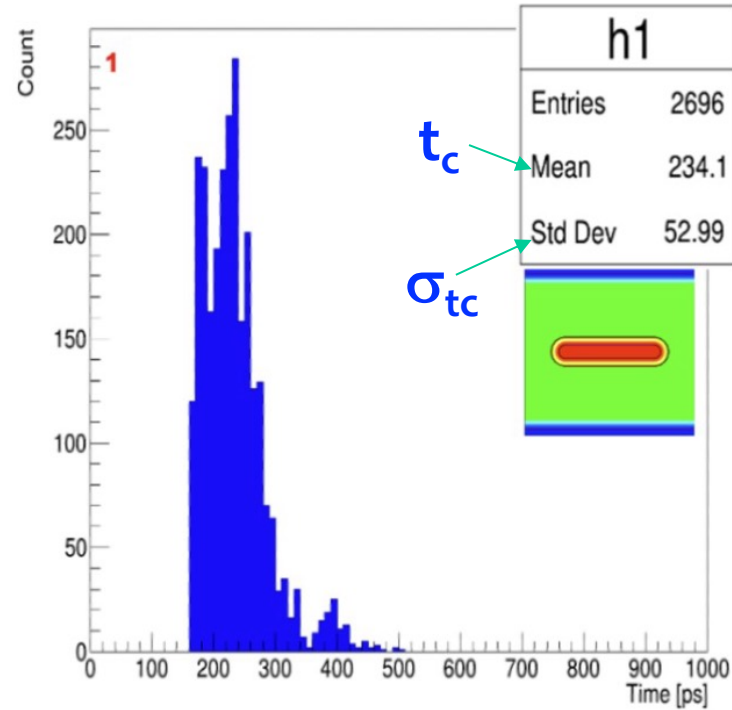
\*time resolution from histogram RMS

Electronics: the decisive stage,  
TimeSPOT developments (fast item)



# The $\approx$ ideal Front-End for 3D-trench sensors

Charge Collection Time distribution



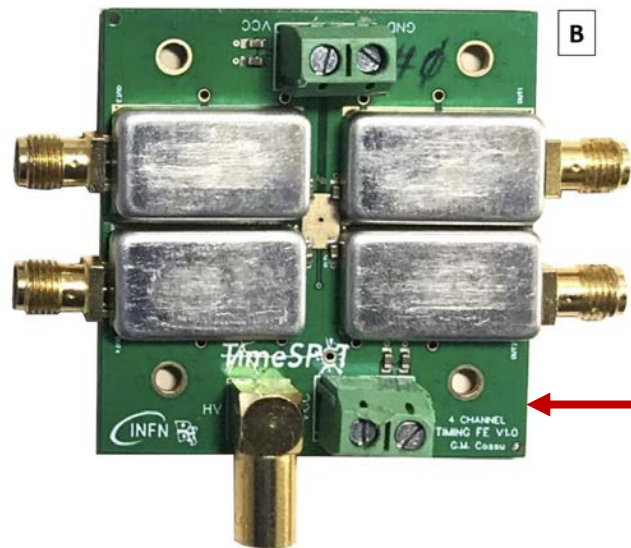
HBJT Si-Ge,  
 $f_T \sim 100$  GHz

A «quasi» current sensitive amplifier (Trans-Impedance-Amp) stage,  
with  $Z_{in} \approx 50 \Omega$  can sustain  $C_D \leq 1$  pF

G. M. Cossu and A. Lai, “Front-end Electronics for Timing with picoseconds precision using Solid State Sensors”, in preparation  
A. Lai and G. M. Cossu, “High-resolution timing electronics for fast pixel sensors”, arXiv2008.09867, 2020

# CMOS 28-nm for pixels with timing capabilities

When system constraints come into play



BUT:

Rate constraints  
Area constraints  
Data BW constraints  
Power constraints

A first complete set of  
«balanced HEP requirements»



Requirement	scenario $S_A$	scenario $S_B$
Pixel pitch [ $\mu\text{m}$ ]	$\leq 55$	$\leq 42$
Lifetime fluence [ $1 \times 10^{16} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$ ]	$> 6$	$> 1$
TID lifetime [MGy]	$> 28$	$> 5$
Sensor Timestamp per hit [ps]	$\leq 35$	$\leq 35$
ASIC Timestamp per hit [ps]	$\leq 35$	$\leq 35$
Hit Efficiency [%]	$\geq 99$	$\geq 99$
Power per pixel [ $\mu\text{W}$ ]	$\leq 23$	$\leq 14$
Pixel rate hottest pixel [kHz]	$> 350$	$> 40$
Max discharge time [ns]	$< 29$	$< 250$
Bandwidth per ASIC of $2 \text{ cm}^2$ [Gb/s]	$> 250$	$> 94$

1.5 W/cm<sup>2</sup>

LHCb-U2 specs from physics needs. VELO support document for FTDR

The toughest constraint against speed is **power budget**, originating from the (un)capabilities of our best **cooling system techniques** at present (micro-channelling)

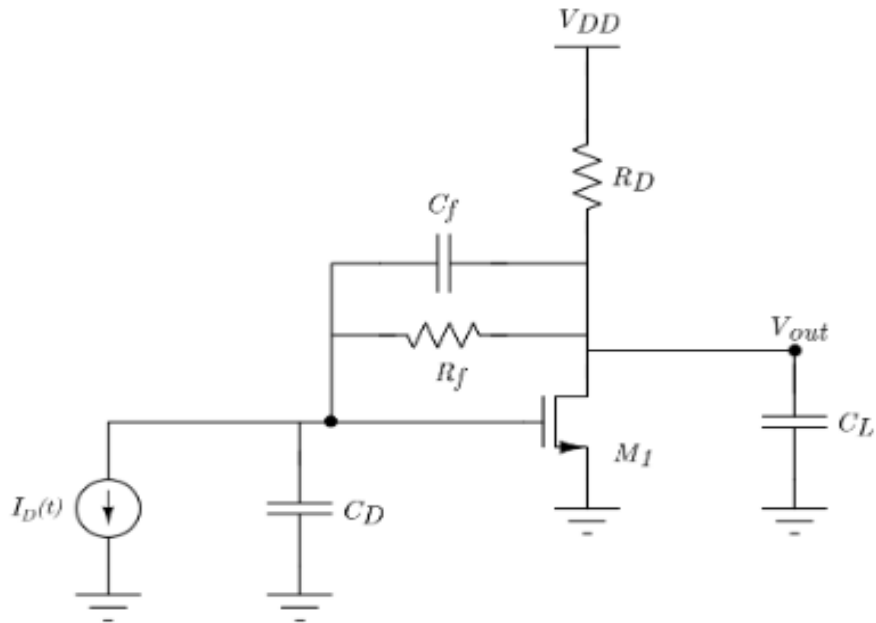
Si-Ge input stages  $t_r \approx 100 \text{ ps}$   
Measured  $\sigma_{ej} \approx 7 \text{ ps @ } 2 \text{ fC (1 MIP), } 900 \text{ fs @ } 20 \text{ fC}$

## Why CMOS 28-nm? (last “bulk” CMOS node)

1. It optimizes performance vs radiation hardness, costs, and design techniques
2. It appears to be more rad-hard than subsequent (still very expensive) finFET technologies (es. 16 nm)
3. Most groups in HEP (CERN included) have chosen (for the reasons above) to adopt it for the next 5-10 years of developments

# “Alternative” roads to front-end solutions

Trans-Impedance-Amplifier with shunt-shunt feedback (FB-TIA).



Simplified schematic of the FB-TIA amplification stage

According to the FB parameters used, this scheme can range from an integrator (Charge Sensitive Amplifier) to a fast Current-Sensitive front-end. The role of the specific transistor technology used is also decisive, especially when very high speed is pursued (Si-Ge vs CMOS).

We can consider two extreme cases as examples<sup>(1)</sup>:

A) CSA-TIA, when the amplifier peaking time  $\tau \gg t_c$

It can be demonstrated<sup>(1)</sup> that in this case

$$\sigma_t = \frac{\partial t_{thr}}{\partial t_c} \sigma_{tc} = \frac{1}{2} \sigma_{tc}$$

B) Fast-TIA, when the amplifier peaking time  $\tau \approx t_c$

It can be demonstrated<sup>(1)</sup> that in this case

$$\sigma_t = \frac{\partial t_{thr}}{\partial t_c} \sigma_{tc} \approx \frac{\tau}{2} \sqrt{\frac{V_{th}}{I_0 R_m}} \frac{\sigma_{tc}}{t_c} \approx \left( \frac{1}{2} \frac{\tau}{t_c} \sqrt{\frac{N}{S}} \right) \sigma_{tc}$$

<sup>(1)</sup> A. Lai and G.M. Cossu, *High-resolution timing electronics for fast pixel sensors*, arXiv:2008.09867

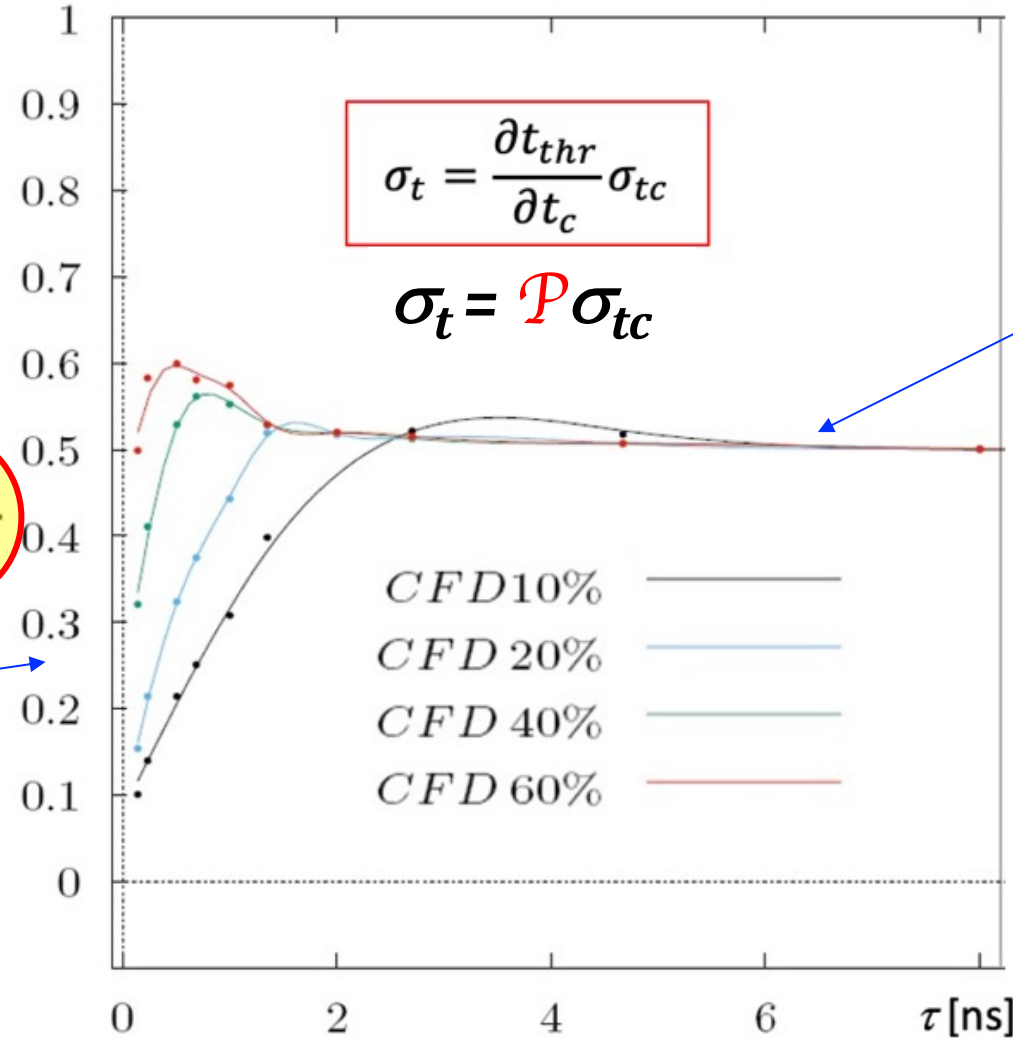
# Front-end solutions: theoretical limits

Timing propagation coefficient  $\mathcal{P}$   
 ( $\sigma_t/\sigma_{tc}$  ratio)  
 or  
 fraction of CCT standard deviation propagated to  $\sigma_t$

$$\frac{\partial t_{thr}}{\partial t_c}$$

Fast-TIA  
 For  $\tau \ll t_c$   
 $\mathcal{P}$

can be considerably less than 1  
 Resolutions below 10ps can be theoretically reached <sup>(1)</sup>



CSA-TIA  
 For  $\tau \gg t_c$   
 $\mathcal{P}$

Approximates  $\frac{1}{2}$ .  
 In the case of a 3D-trench pixel, this corresponds to  $\approx 20-25$  ps (with a 55  $\mu$ m pitch)

To reach  $\tau \approx 100$  ps, the choice of feedback parameters is not sufficient. High performance transistor stages and high power are mandatory as well

$\mathcal{P}$  (= Derivative of time at threshold  $t_{thr}$  with respect to average CCT  $t_c$ , aka time centroid) vs the amplifier peaking time  $\tau$ , at  $t_c = 250$  ps for various CFD fractions.

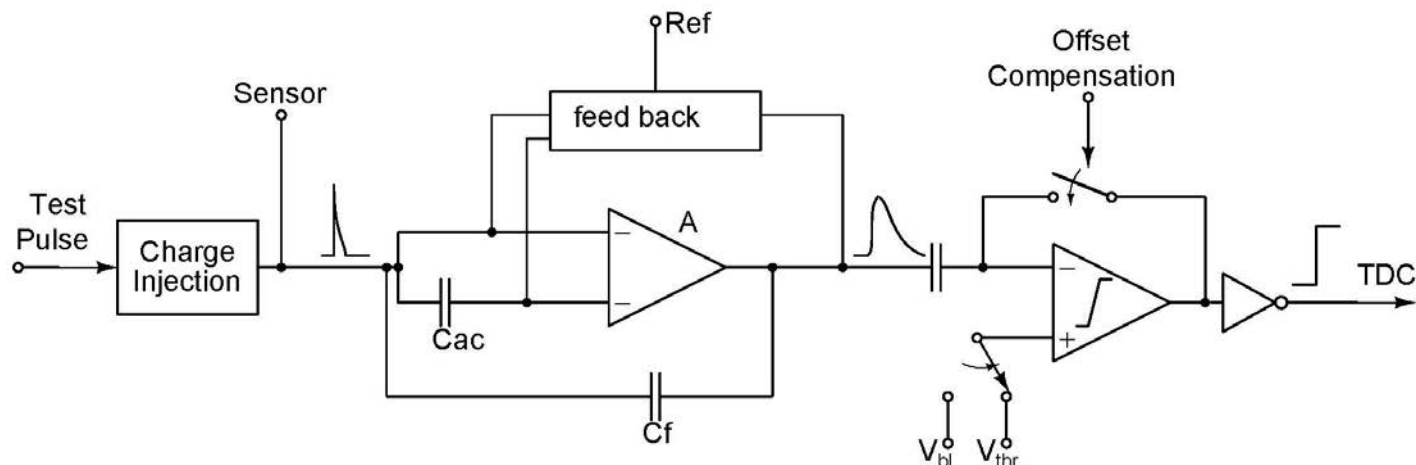
<sup>(1)</sup> A. Lai and G.M. Cossu, *High-resolution timing electronics for fast pixel sensors*, arXiv:2008.09867

# Timespot1: Analog Front End

## Inverter core amplifier with double Krummenacher FB

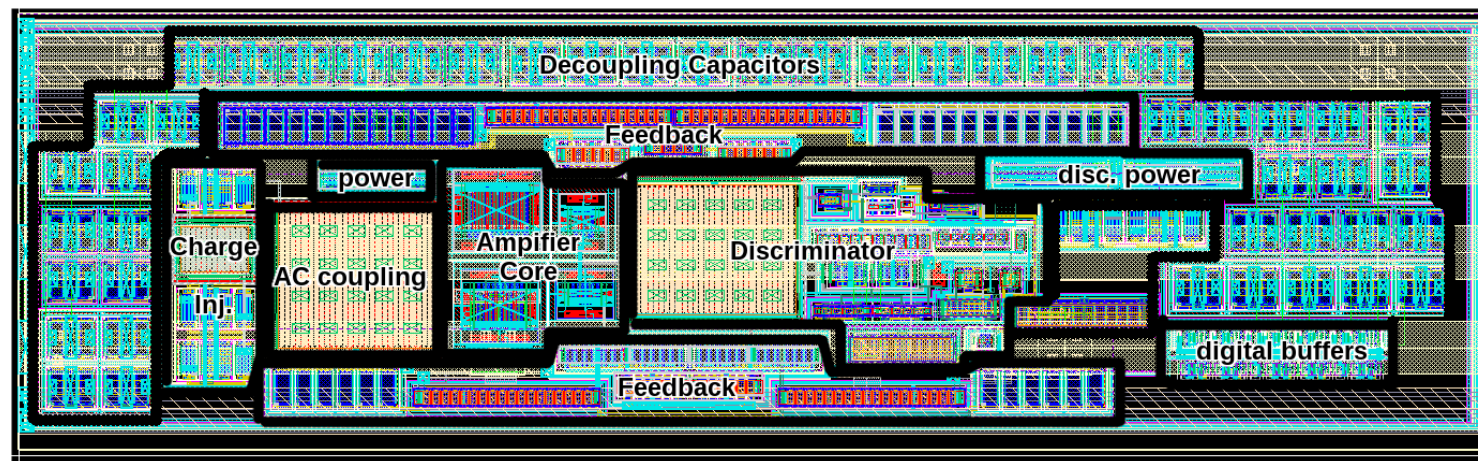
Inverter-based Charge Sensitive Amplifier (CSA)  
with DC current compensation.

Leading Edge Discriminator with Discrete-time  
Offset-Compensation for threshold uniformity  
OC procedure: 250 ns every  $\leq 800 \mu\text{s}$



Pwr regime	nominal	high
Pwr/channel [ $\mu\text{W}$ ]	18.6	32.9
Slew rate [ $\text{mV/ns}$ ]	250	360
$Z_{in}$ [ $\Omega$ ] in BW	23k	23k
Gain [dB]	93	93
RMS noise [mV]	3.9	3.8
BW [MHz]	311	455
Jitter [ps]	15.6	10.5

Expected performance @ 2 fC  
(post-layout simulation)



50x15  $\mu\text{m}^2$



# Timespot1: TDC

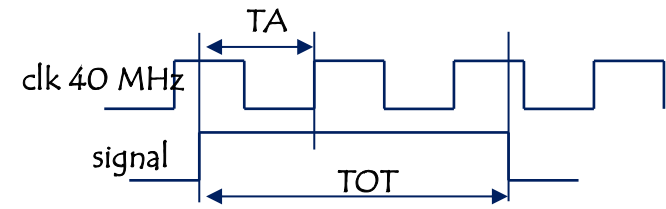
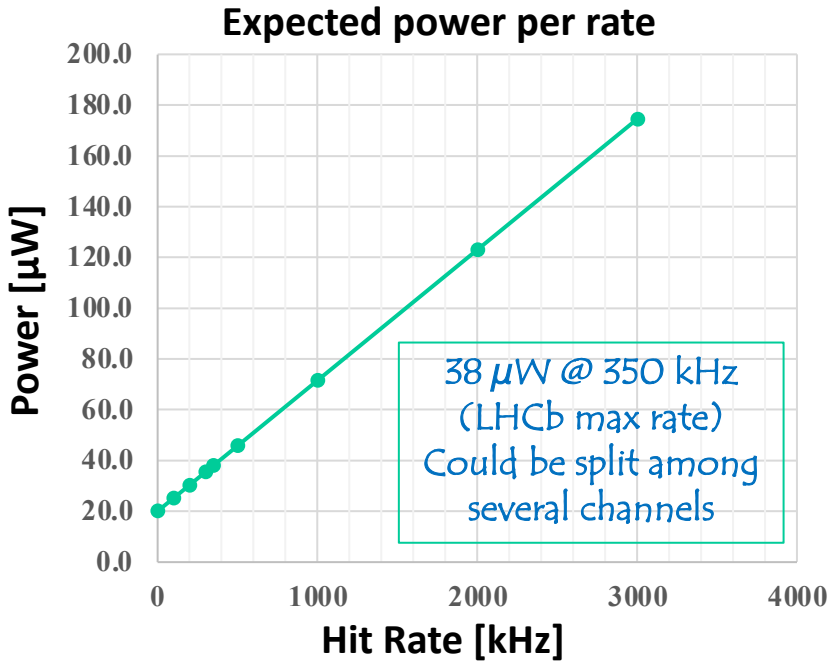
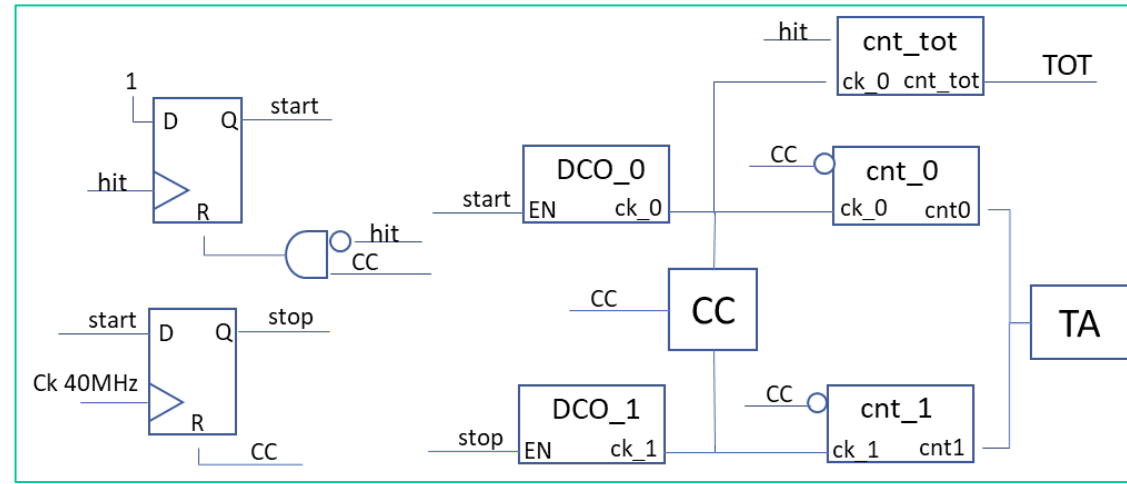
Fully digital design, standard-cell based



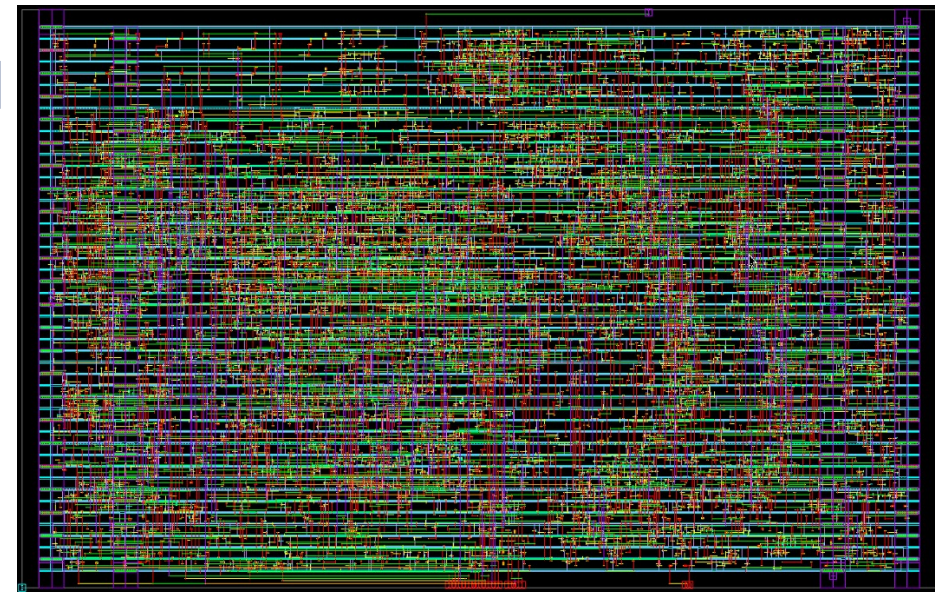
To maximize sustainable rate, 1 TDC per pixel channel has been integrated

Max input rate = 3 MHz  
23 bits output word (ToA + ToT)  
ToT resolution  $\approx$  1 ns

High resolution, “low” consumption TDC based on 2 DCOs and a Vernier architecture



The TDC gives the phase of the signal wrt the 40MHz BX clock  
The TDC and the counter use the same DCO-generated Clk ( $\sim$ 1 GHz)  
4 levels of Vernier precision ( $\Delta$ f in DCOs) can be programmed.  
Typical LSB 12 ps





# Timespot1 ASIC

## 28-nm CMOS

- Reduced size (1024 pixels, 6 mm<sup>2</sup>)
- HPC flavour
- Complete set of functionalities for pixel readout
- Slow read-out (demo-test purpose)

640 MHz master clock

→ Digital row: 16x2 TDC  
+ Controls, Conf. registers, I<sup>2</sup>C I/F

→ Analog row (16x2 AFE)

→ Analog (service) column.  
Each contains:

- 1 Band-Gap circuit
- 5x  $\Sigma$ - $\Delta$  DACs (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

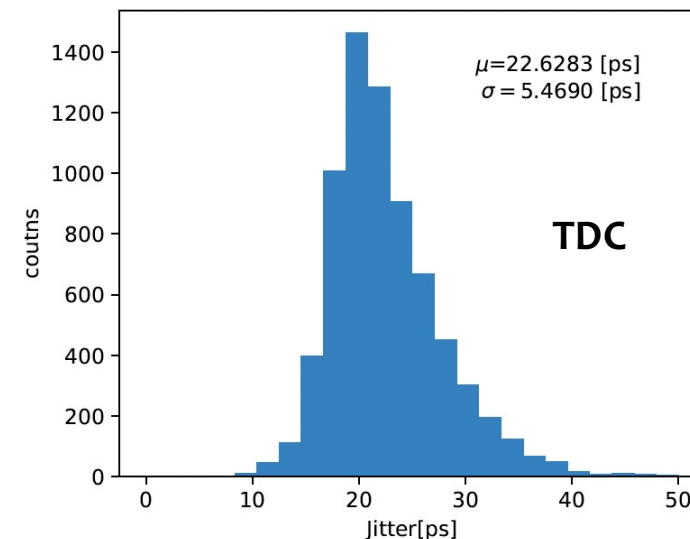
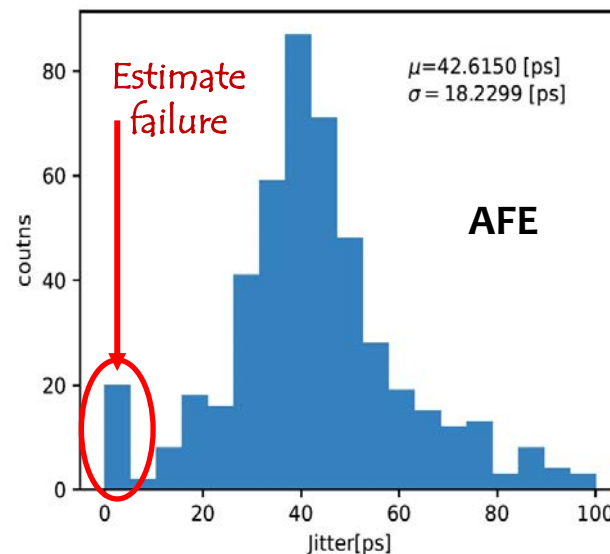
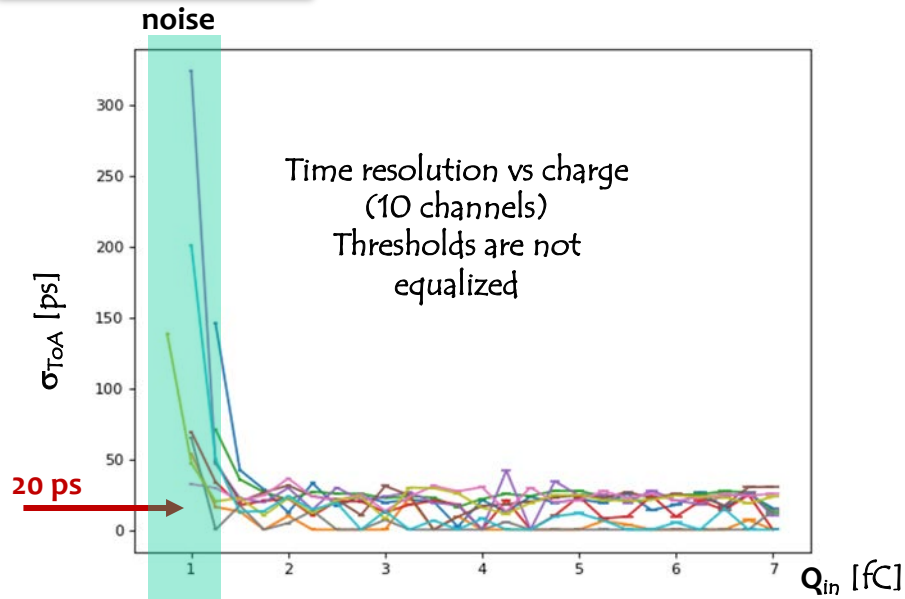
→ 4x Read Out Trees

→ 8x LVDS driver  
(each @1.28 Gbps)

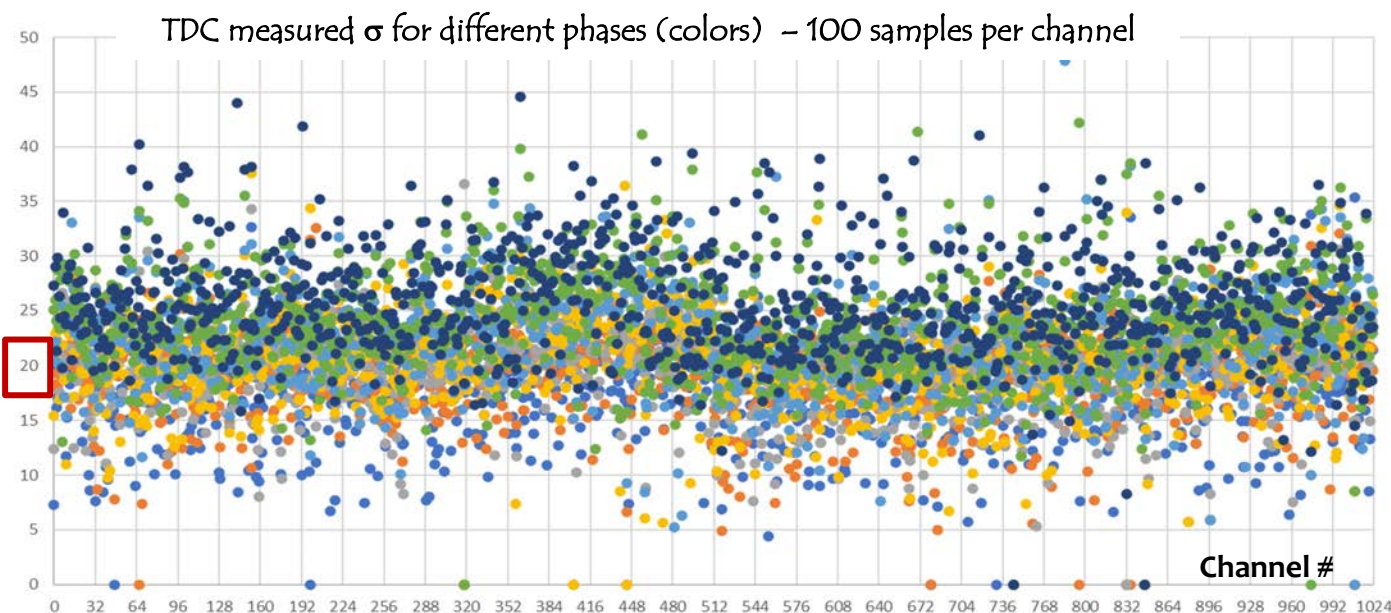


# Timespot1 ASIC operation

## Time of Arrival Resolution

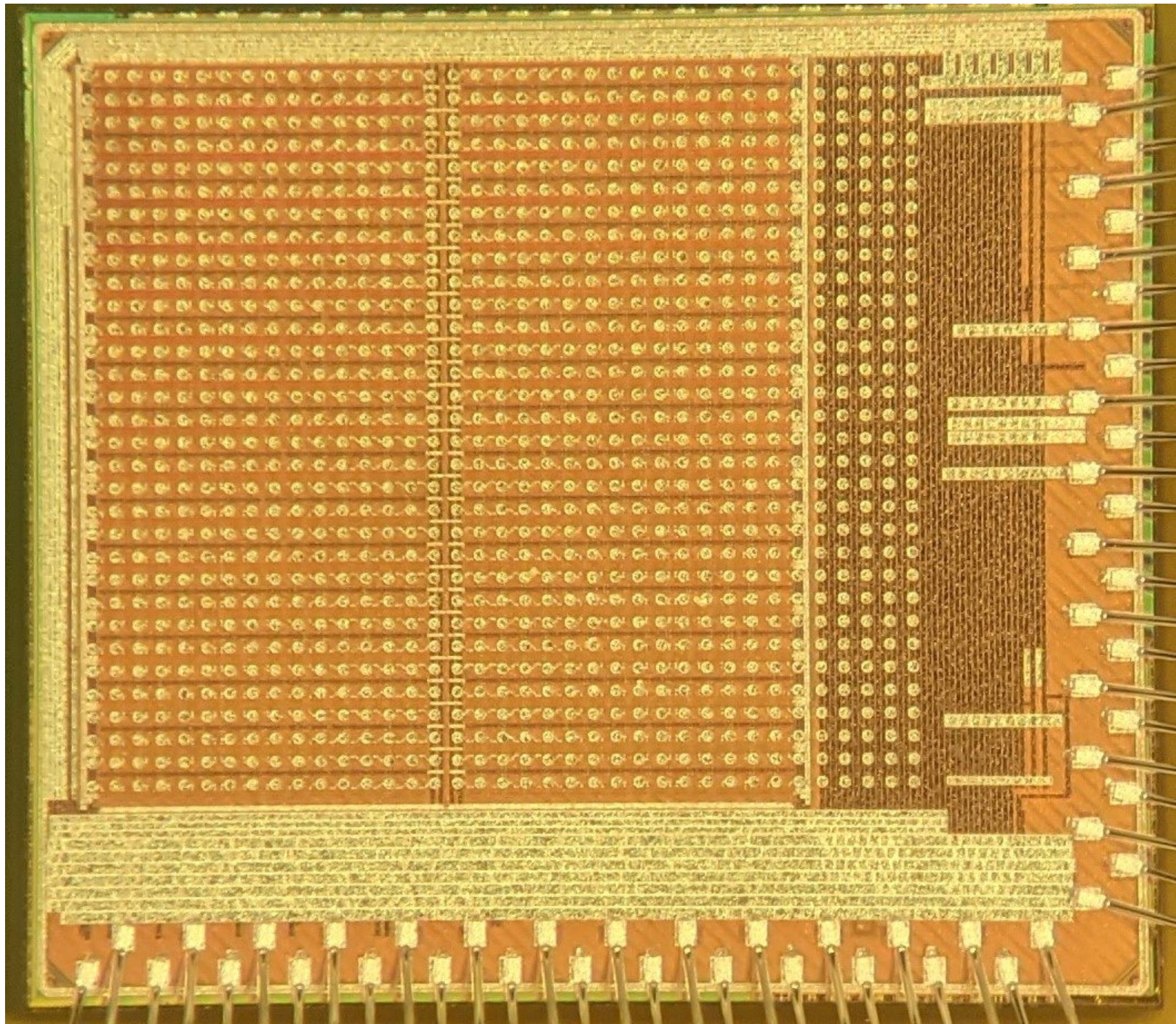


Distribution of the TA standard deviation across 1024 channels and 7 phases. Each point is computed from 100 repeated measurements.

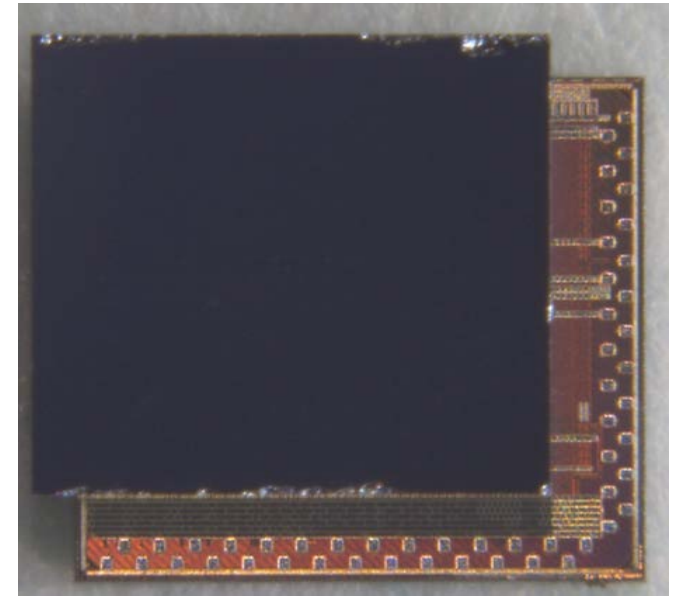


- In brief:**
- The TDC has a typical  $\sigma_t \approx 20$  ps, with relatively wide dispersion (5 ps) and is limited by the system clock jitter
  - The AFE  $\sigma_t$  is intrinsically below 20 ps but an identified bug in the discriminator spoils  $\sigma_t$  in most of the channels. The bug is easily amendable.
  - In general, global (digital) clock distribution issues limit the very good resolution at the pixel level.
  - Maximum care is mandatory in global layout and final verification procedures

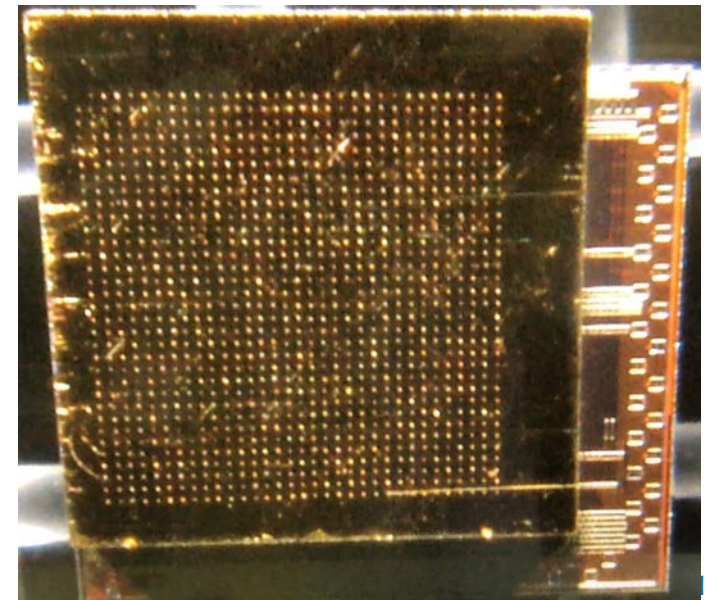




Timespot1 on 3D-trench silicon matrix



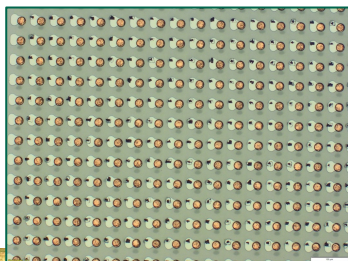
Timespot1 on 3D-column diamond matrix



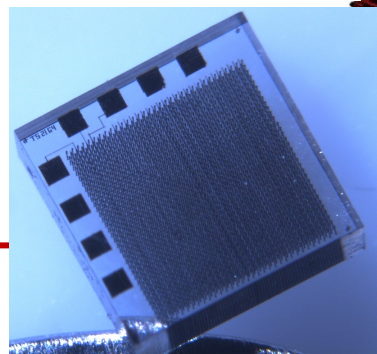
# The Timespotter<sup>®</sup> demonstrator

A mini-tracker, under beam in autumn 2022

8 samples of each «flavour» are under preparation at IZM

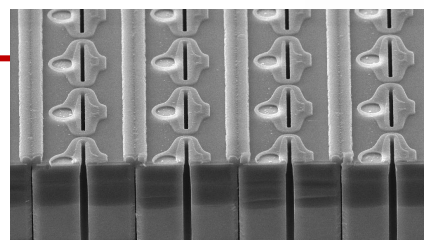
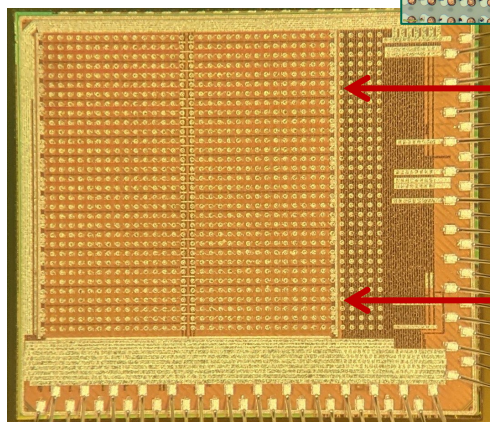


Diamond (Firenze)



32x32 matrix

Hybridized @IZM



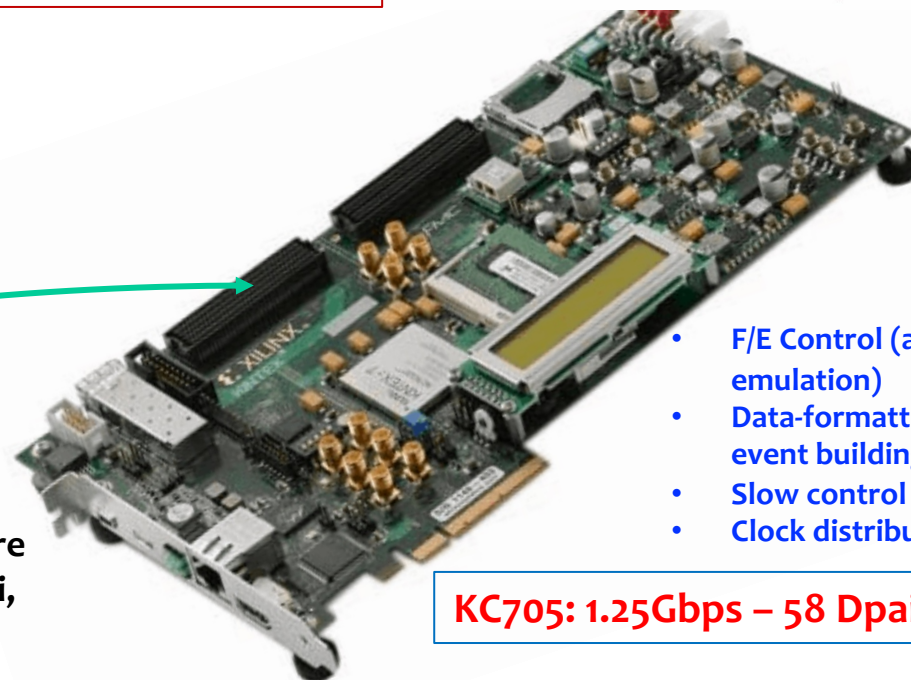
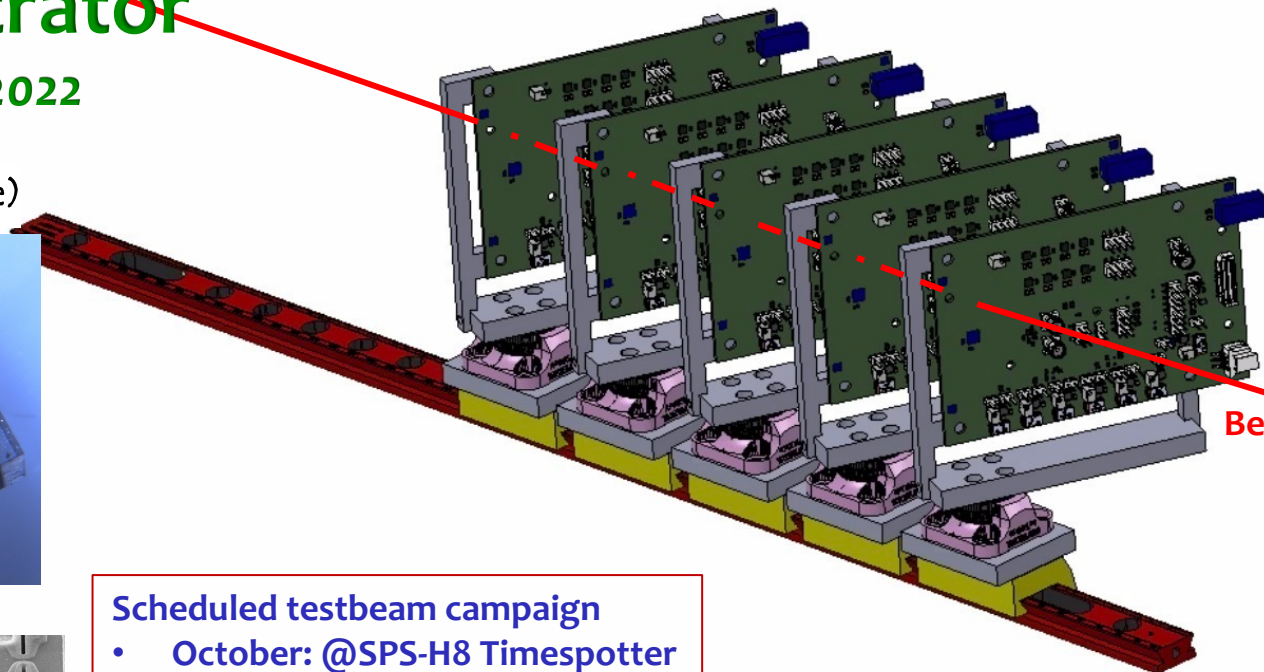
Silicon (FBK)

Hi-speed, Hi-density Samtec twinax



TS1-PCB 120x80 mm<sup>2</sup> (Cagliari, Milano, Torino)

Scheduled testbeam campaign  
• October: @SPS-H8 Timespotter



- F/E Control (and emulation)
- Data-formatting, event building
- Slow control (I<sup>2</sup>C)
- Clock distribution

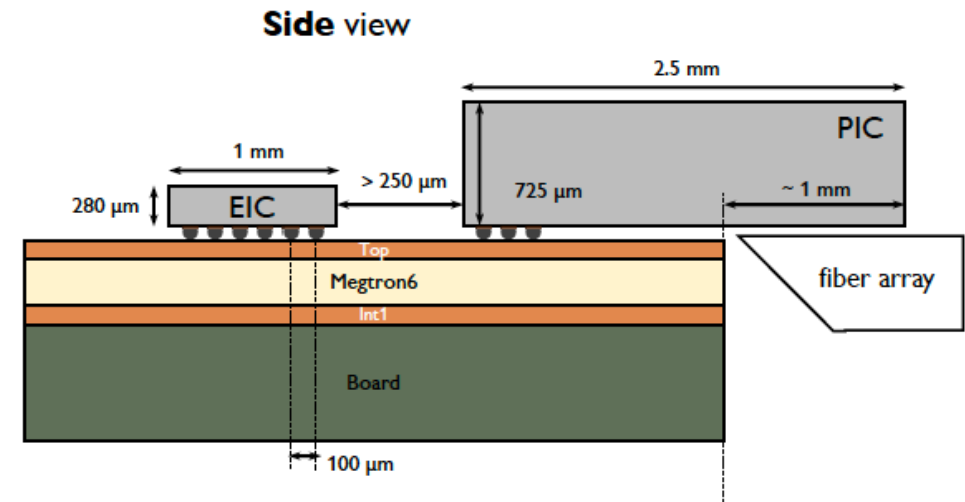
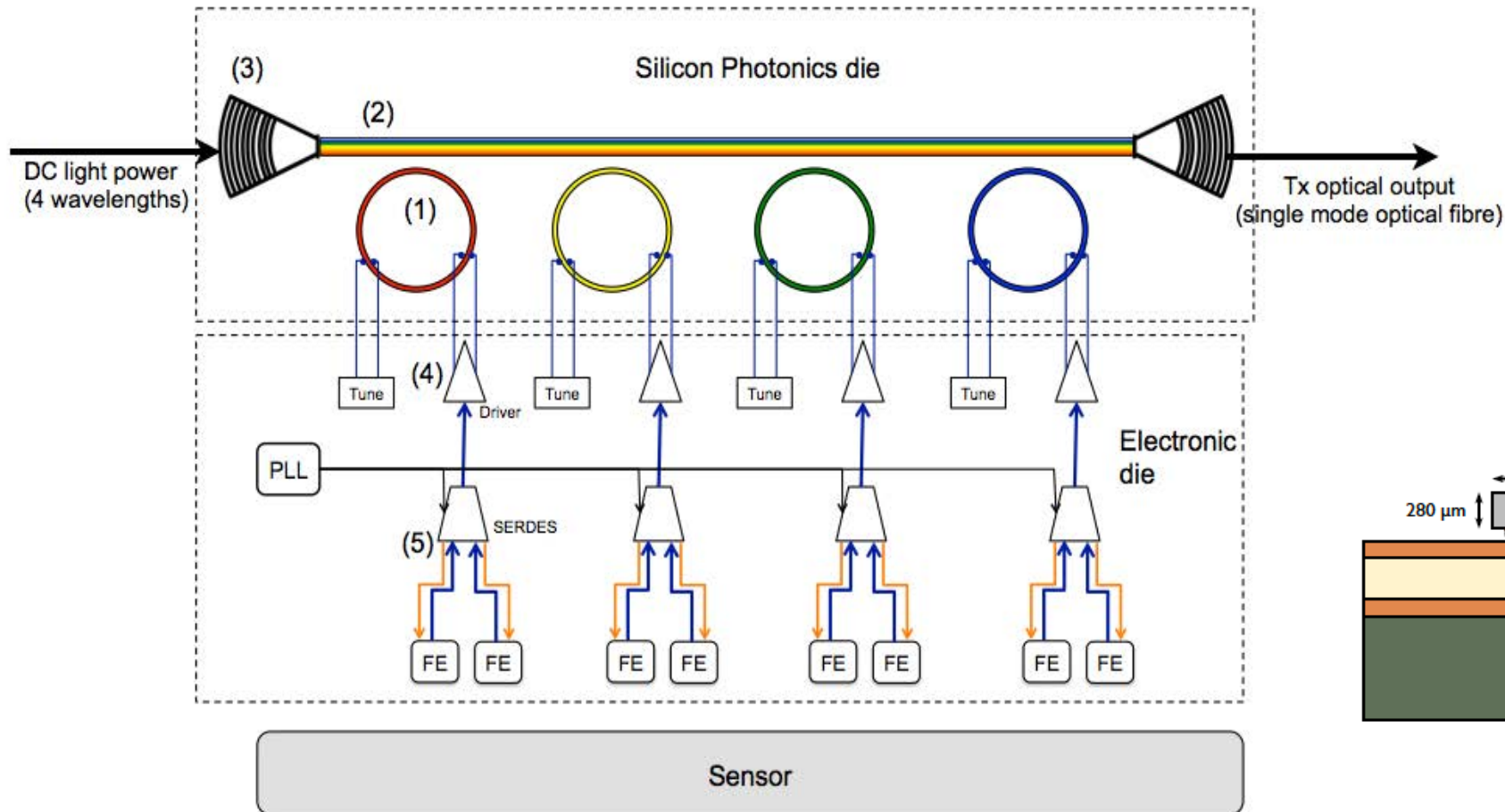
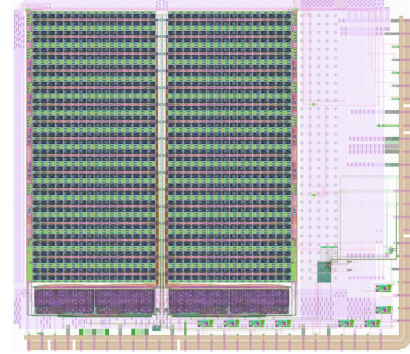
**KC705: 1.25Gbps – 58 Dpairs**

# Conclusions

1. 3D-trench (geometric) sensors show excellent performance in timing **even at extreme fluences** → the limit must still be reached
2. **Electronics is by far the weak ring of the chain**
3. Reaching  $\approx 20$  ps time resolution in 28-nm CMOS can be «easily» achieved as far as the pixel circuit is concerned within a low-moderate power budget
4. 4D timing is mainly not a matter of sensors or single devices, **it is a matter of system constraints** (power in primis, cooling, stable clock distribution, interconnectivity, data BW, material budget)
5. The timing **problem size scales dramatically with the area** (and volume) of the system
6. A **system-level** development has to be launched soon

A glimpse into the (immediate)  
future

# TimeSPOT meets Photonics (Falaphel *project and* **IGNITE**)



Schematics of the PIC and EIC assembly (FALAPHEL demonstrator). Ring resonators (1) with different and tunable resonator wavelengths are located along horizontally drawn bus waveguides (2) which are connected to optical glass fibers by efficient and robust focusing grating.

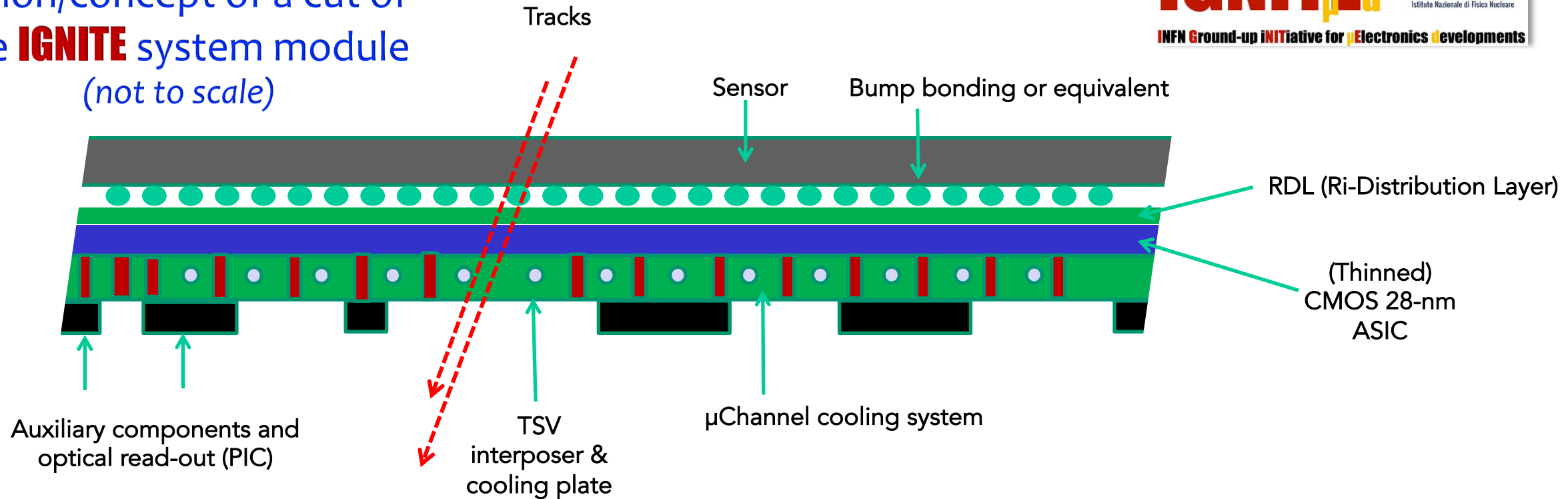
Interposer-free flip-chip integration  
using a high-speed PCB

# Electronics and Technologies for fast (high density) timing

(in the «hybrid approach»)



Vision/concept of a cut of the **IGNITE** system module  
(not to scale)



Target deliverable of the **IGNITE** project:

- A complete module (sensor, read-out ASIC, vertical IC, photonic circuit for data links, cooling system)
- The module development as a route to optimize material budget issues and High Density Interconnectivity between the device stages
- The whole thing below 0.8 (LHCb) ÷ 0.5 (NA62) % X<sub>0</sub>

# INFN Institutes and Organization

Bologna LNF Perugia  
Bari Milano Pisa  
Cagliari Milano B. Torino  
Genova Padova TIFPA  
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- 14 INFN Institutes
- Involvement of researchers from ATLAS, CMS, LHCb, NA62
- 20 FTE + dedicated Research Contracts on project funds
- 4 year project
- **Funds:** 2.4 M€ for developments and ASIC submissions
- Additional specific budget for HR (amount still under definition)
- **Starting 2023**



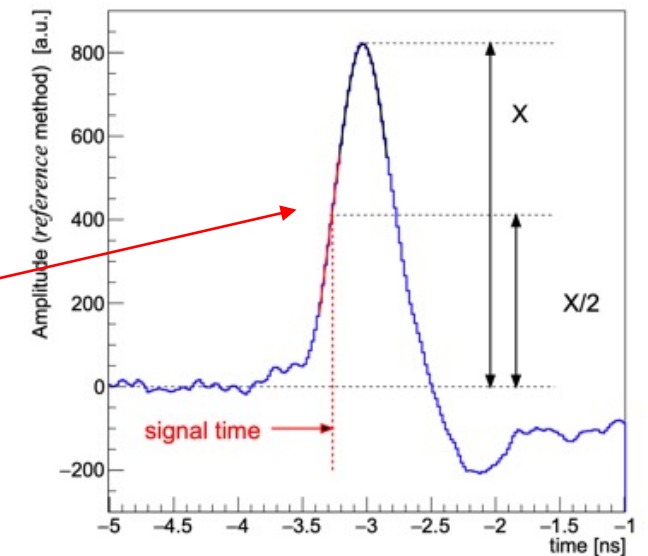
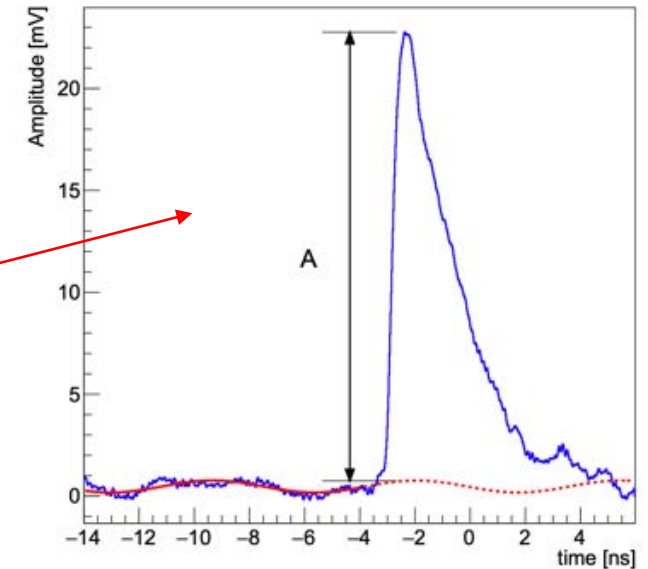
**INSIGHTS**



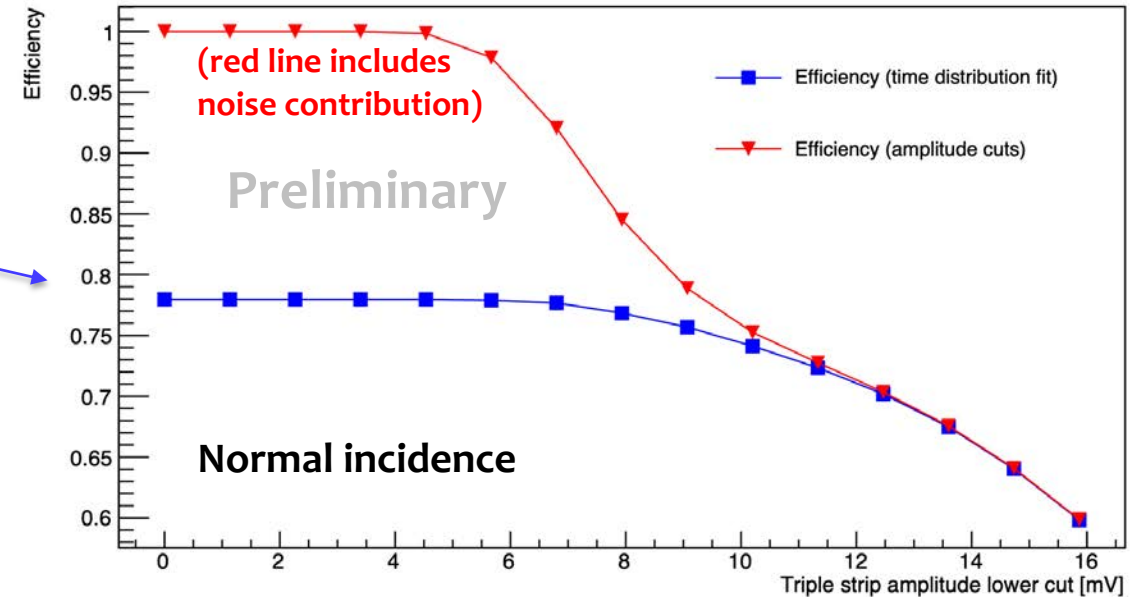
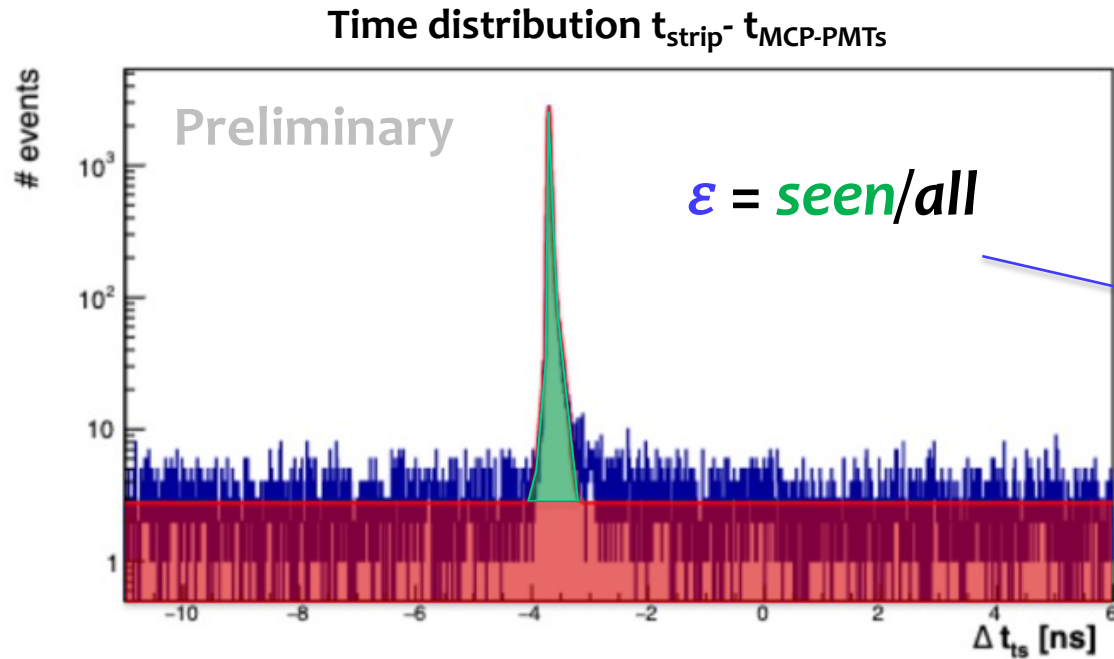
# Waveform processing

For each sensor's waveform:

- Signal baseline (red-dashed line) is evaluated on an event-by-event basis
- The signal amplitude **A** is measured (w.r.t. to the event baseline)
- Signal time of arrival evaluated with various methods:
  - **Leading-edge**: time at 15 mV signal amplitude, linear interpolation around threshold (time-walk effect is present)
  - **LE corrected for the amplitude** to suppress the time-walk effect
  - **Spline**: a classic CFD at 20% with rising edge interpolated with a spline
  - **Reference**: subtract each waveform from a delayed (by about half of the signal rise time) copy of itself, then on the resulting signal we **trigger at X/2 height**



# Efficiency: method



- Time distribution of **all triple-strip signals** w.r.t. MCP-PMTs and count as ‘seen’ the ones under the peak (the flat background corresponds to undetected hits)
- 3D pixel detection (geometrical) efficiency at normal incidence is **in agreement with** calculated fraction of active area ( $\sim 80\%$ )