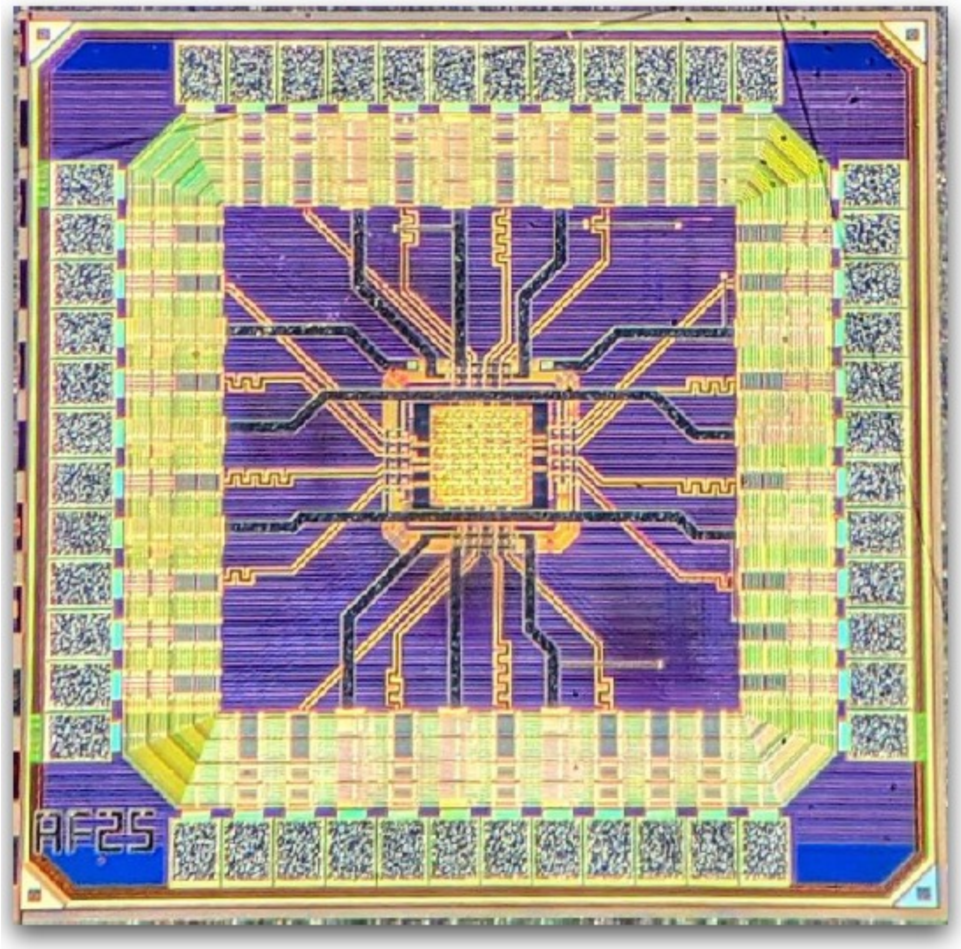
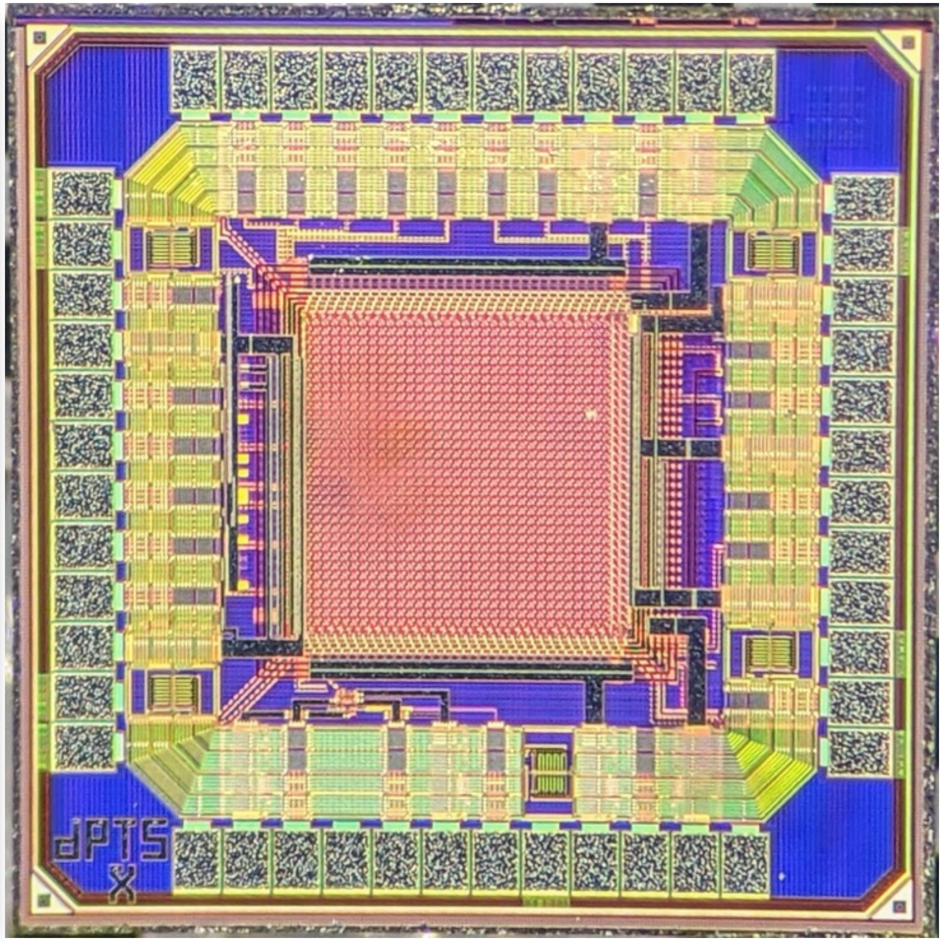
Timing in monolithic sensors in 65 nm





Analog pixel test structure (APTS) and Digital pixel test structure (DPTS) in TPSCo 65 nm ISC

W. Snoeys

Geneva, Switzerland

MONOLITH workshop Uni Geneva Sept. 5th, 2022

Acknowledgements

- The workshop organizers

and colleagues from CERN, the ALICE ITS and ITS3 upgrade, ATLAS Itk, EP R&D WP1.2 …

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

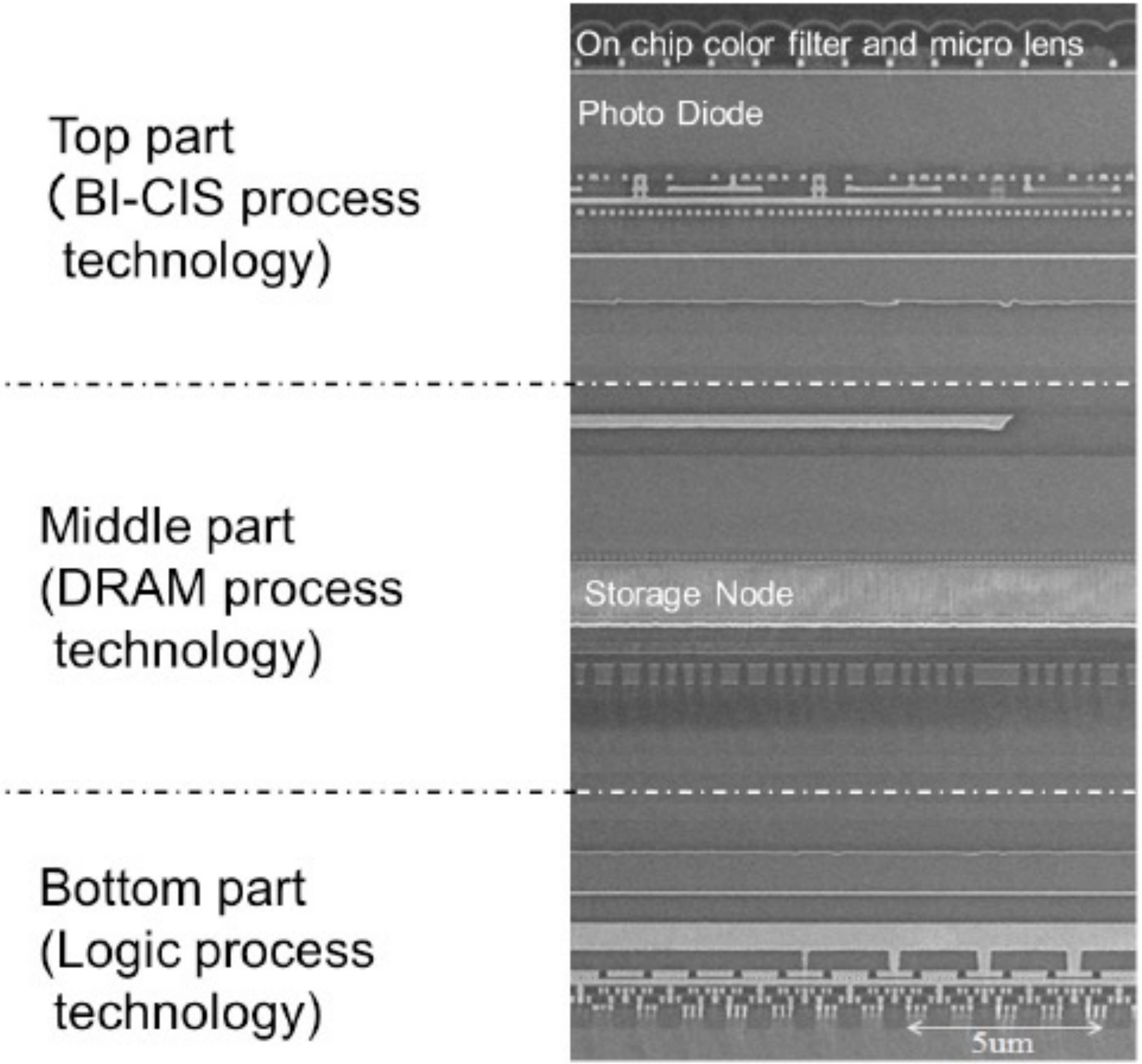
reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …

Silicon has become the standard in tracking applications both for sensor and readout

… and now CMOS MAPS make their way in High Energy Physics !

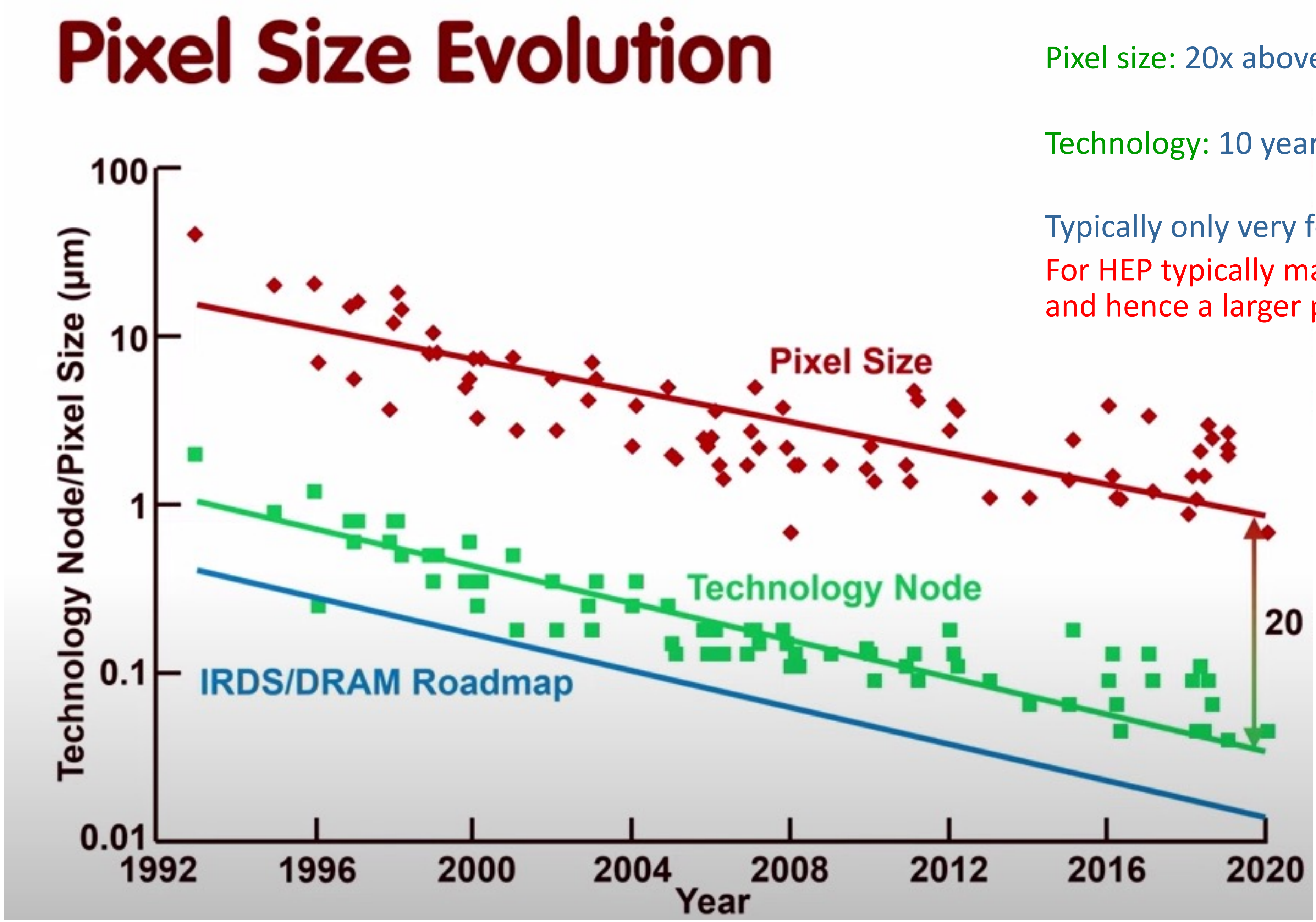
Hybrid still in majority in presently installed systems



Sony, ISSCC 2017

New technologies (TSV's, microbumps, wafer stacking…) make the distinction more vague.

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel,

For HEP typically many more transistors per pixel, and hence a larger pixel.

Albert Theuwissen, ISSCC 2021

Requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	0.01	10^{-3}
LHC	1	0.1…0.3
HL-LHC 3ab^{-1}	5	1.5
FCC	10-350	3-100

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

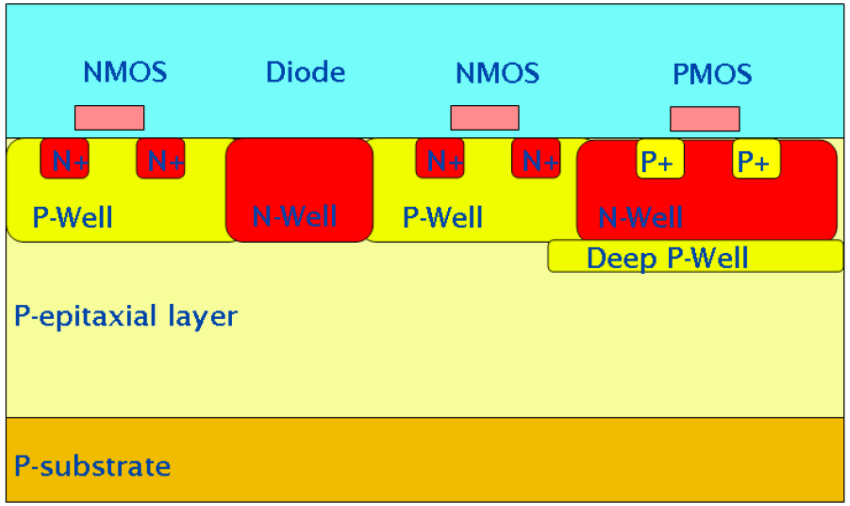
Time resolution

- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

Larger and larger areas

- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

The INMAPS process: quadruple well for full CMOS in the pixel



STFC development, in collaboration with TowerJazz **180nm**

Additional deep P-well implant allows complex in-pixel CMOS and 100 % fill-factor

New generation of CMOS sensors for scientific applications (TowerJazz CIS 180nm)

Also 5Gb/s transmitter in development

Sensors 2008 (8) 5336, DOI:10.3390/s8095336

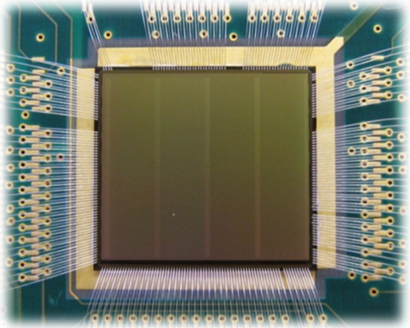
https://iopscience.iop.org/article/10.1088/1748-0221/7/08/C08001/meta

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01006/meta

http://pimms.chem.ox.ac.uk/publications.php …

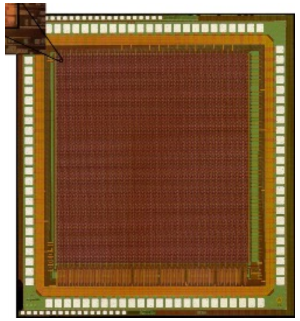
courtesy of N. Guerrini, STFC

TPAC
ILC ECAL (CALICE)



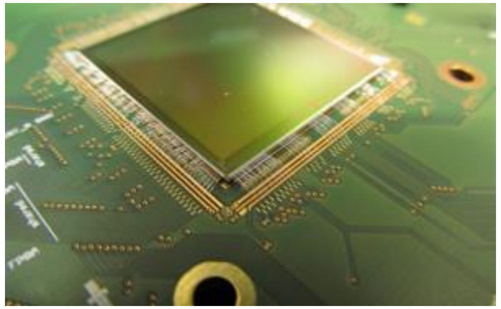
50μm pixel

DECAL
Calorimetry



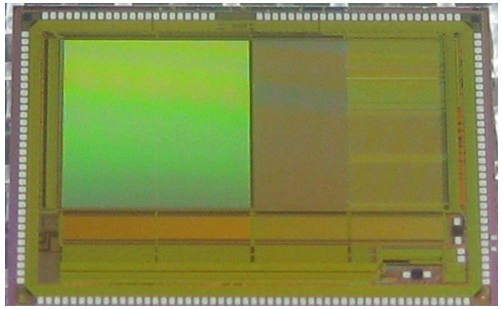
50μm pixel

PIMMS
TOF mass spectroscopy

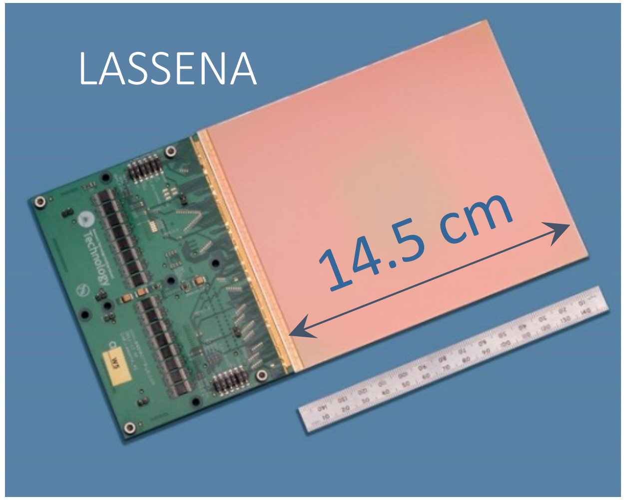


70μm pixel

CHERWELL
Calorimetry/Tracking



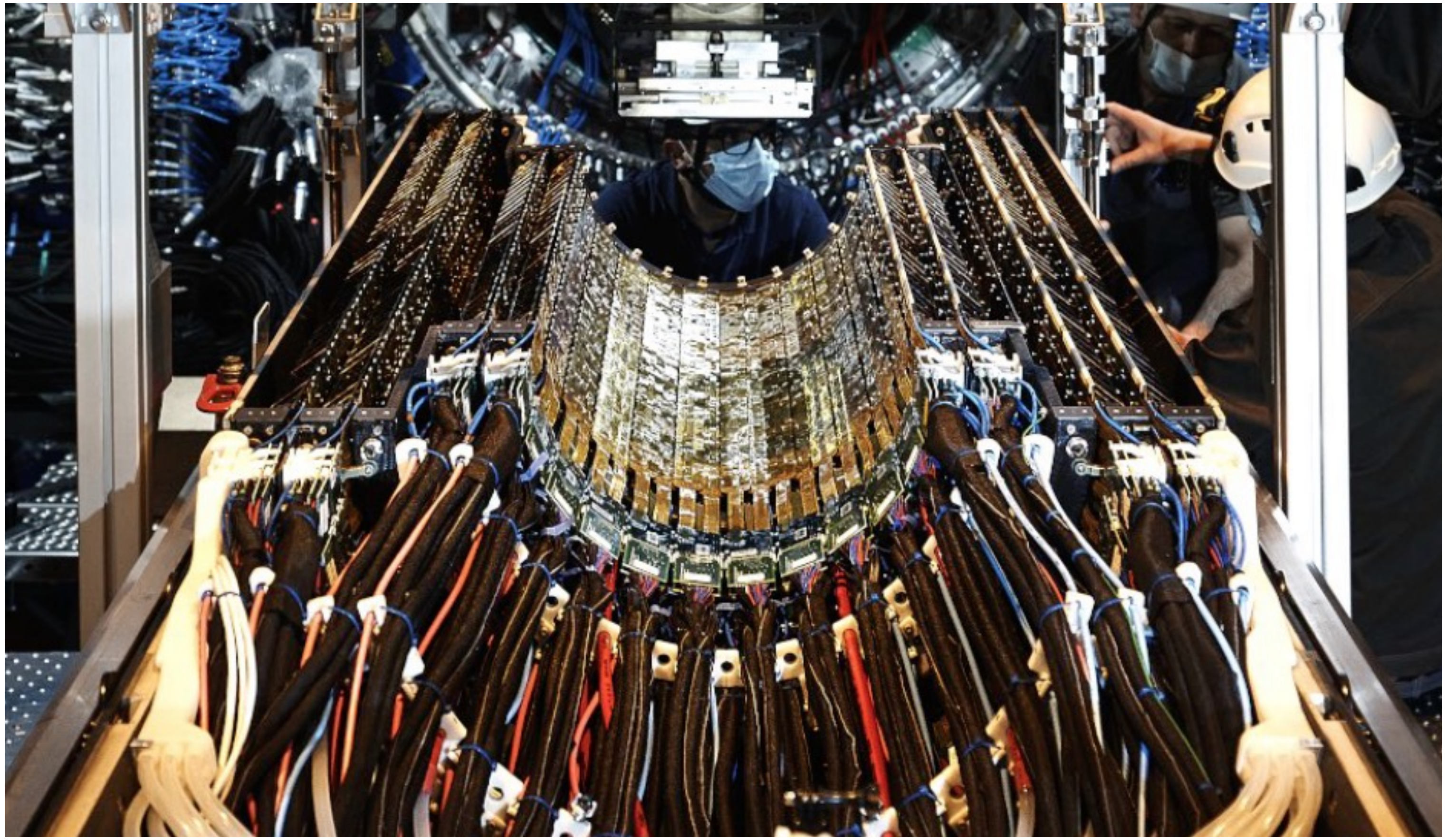
48 μm x 96 μm pixel

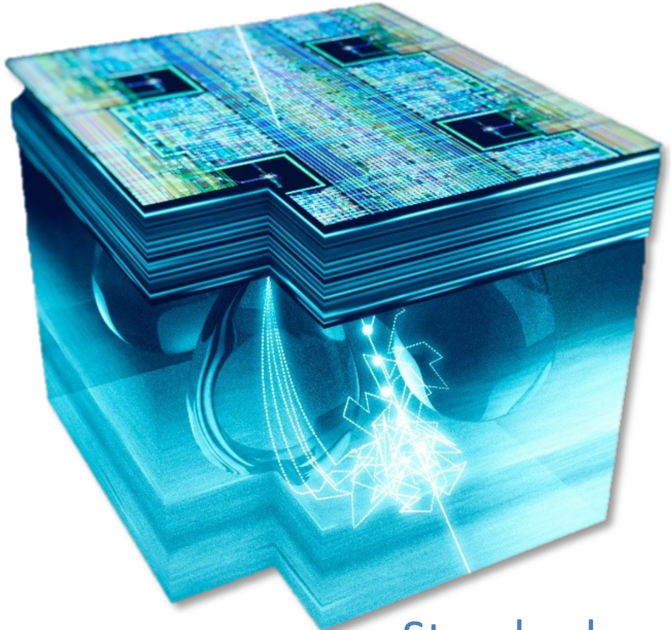


50μm pixel, waferscale

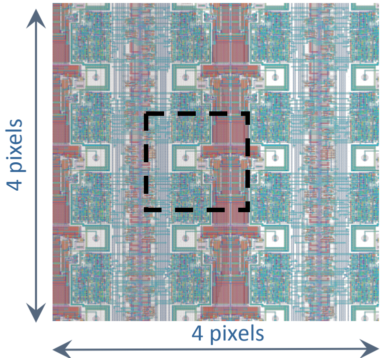
Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

State of the art: ITS2 and ALPIDE in ALICE: 10 m^2, 12.5 Gpixels

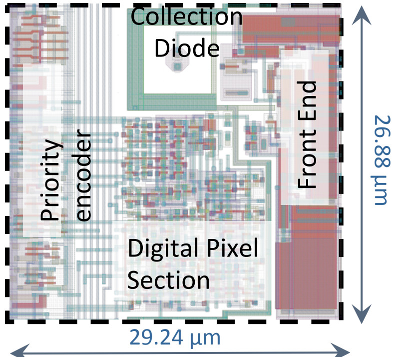


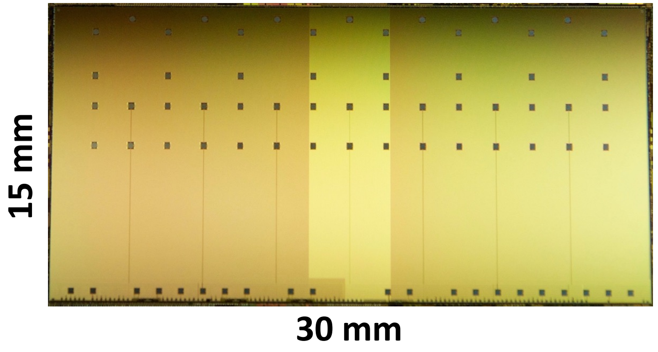


Matrix layout

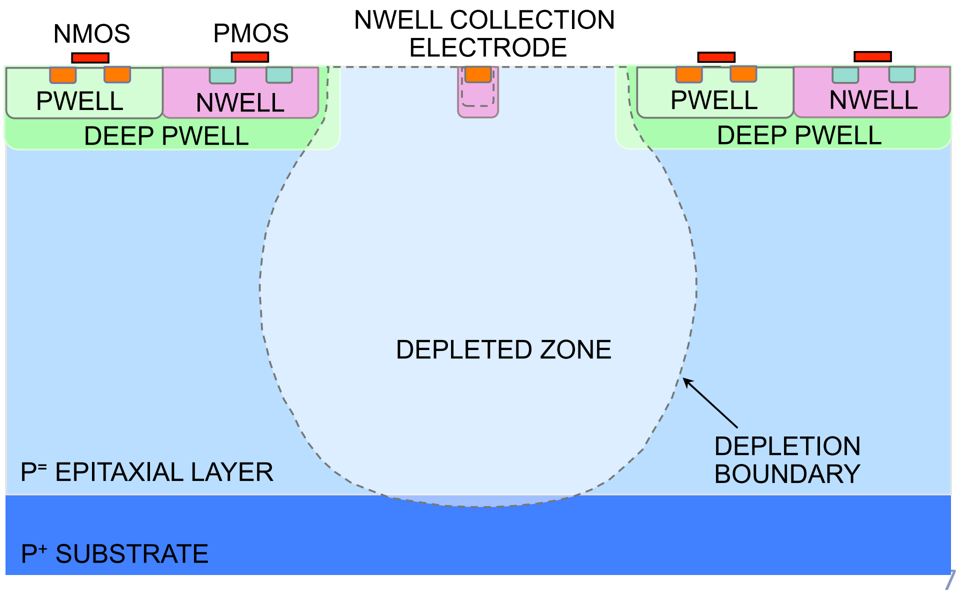


Pixel layout



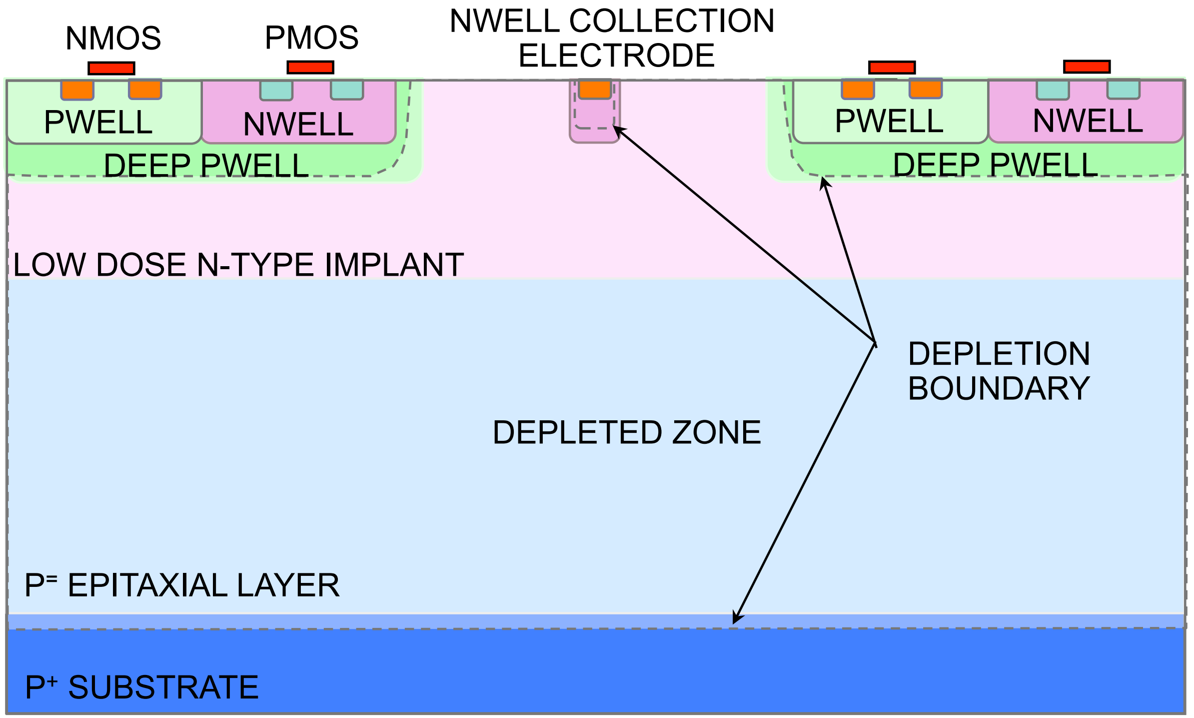


Standard process

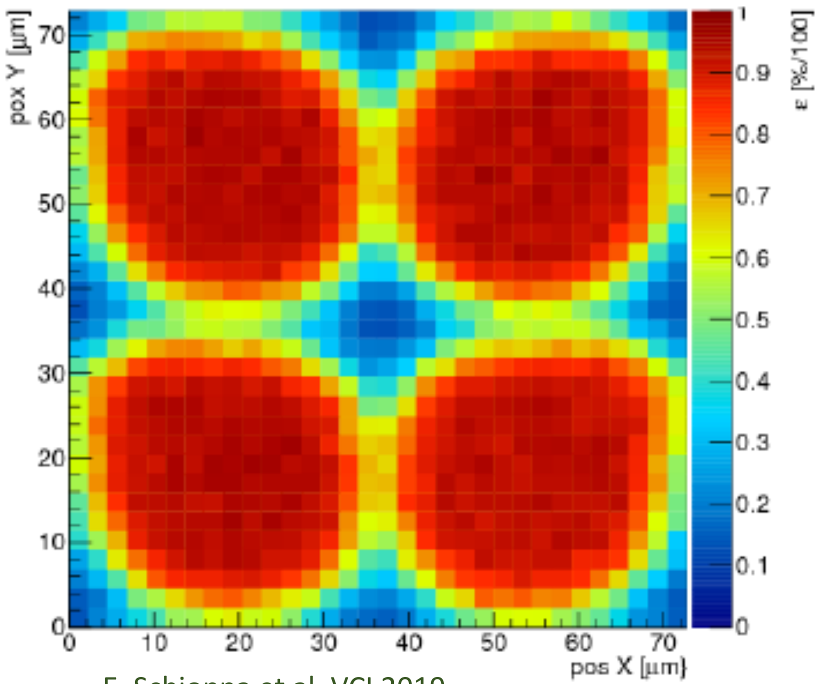


Sensor optimization

TowerJazz 180nm imaging CMOS technology



https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

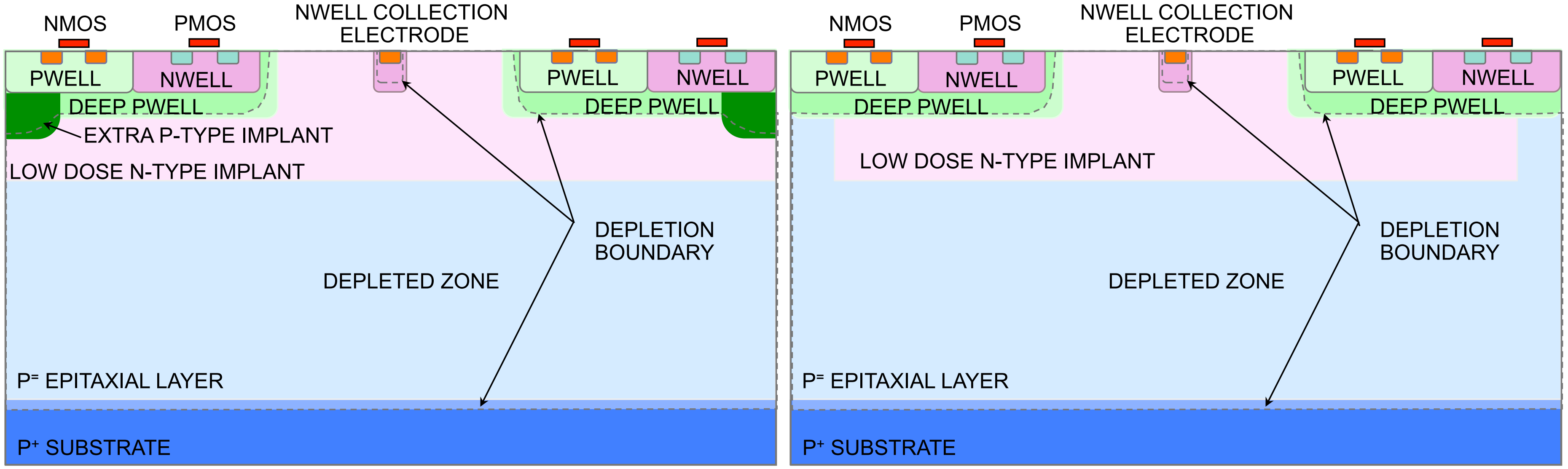


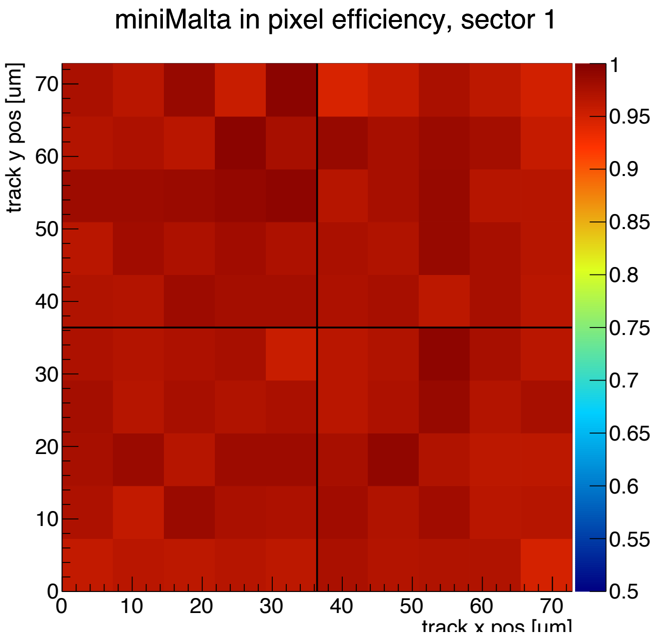
E. Schioppa et al, VCI 2019

- Side development in ALICE: move junction away from the collection electrode to deplete epitaxial layer
  - add deep low dose n-type implant -> radiation tolerance improved by an order of magnitude.
- After interest from ATLAS: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)
- However, efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2 on the pixel edges and corners due to a too weak lateral field

TCAD simulations and sensor optimization

TowerJazz 180 nm imaging CMOS technology



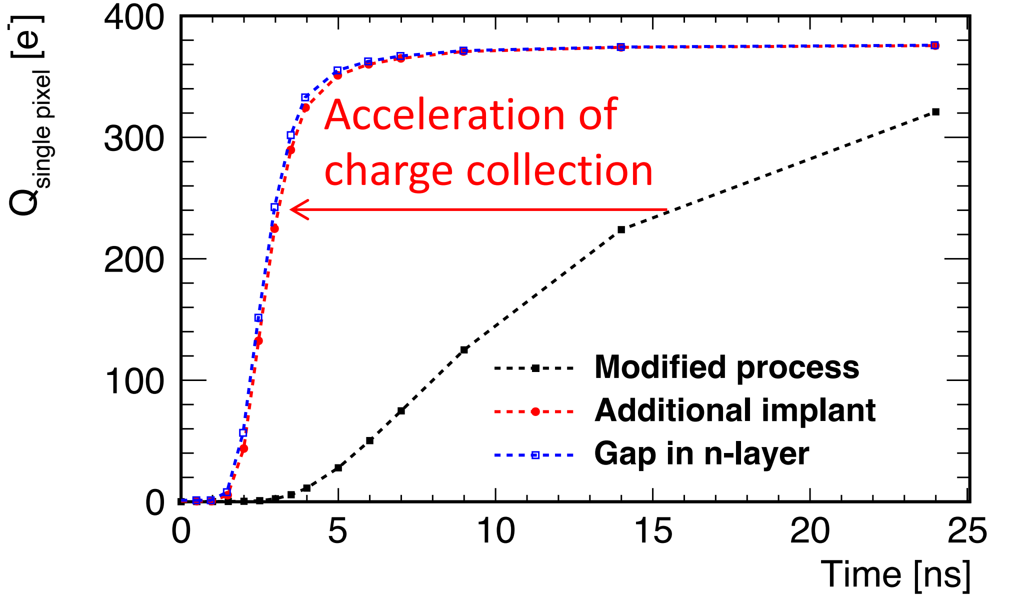


3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Extra deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode. This yields:

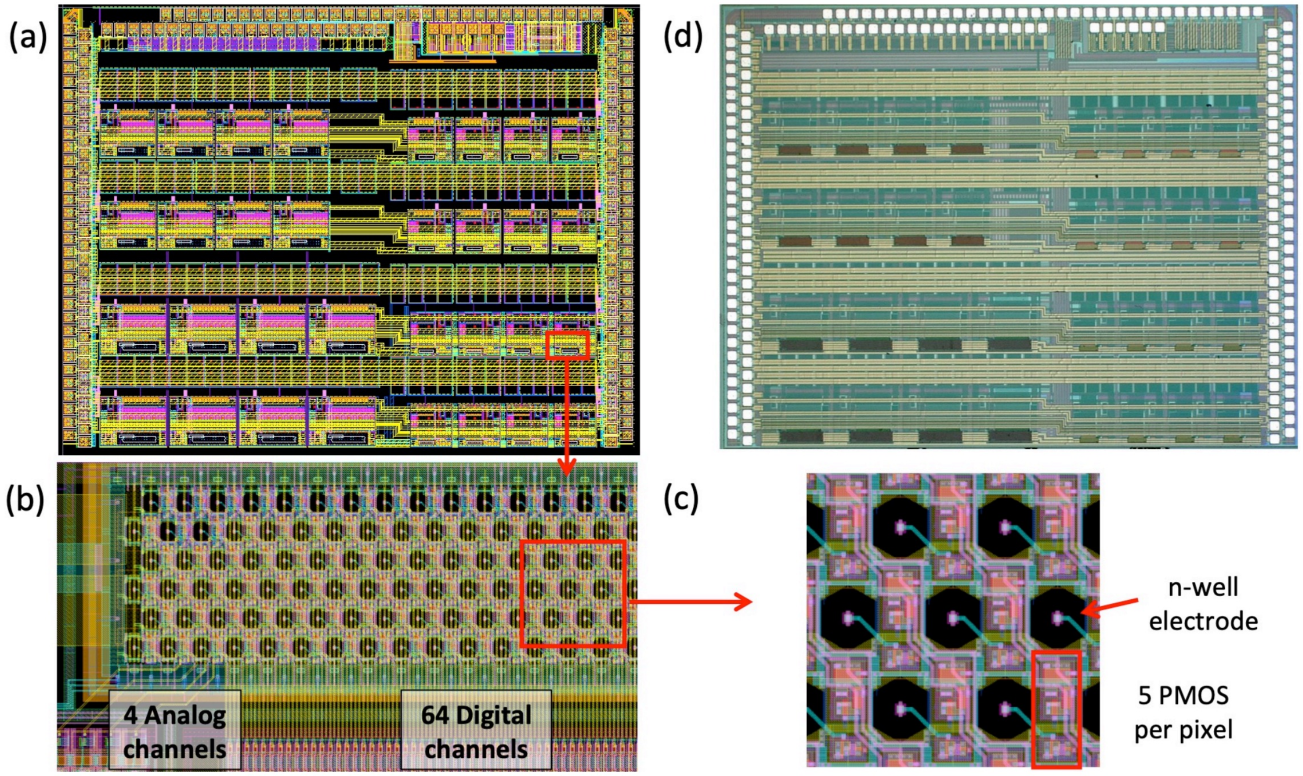
- recovered efficiency at 10^{15} n_{eq}/cm^2
  H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200
- more operating margin even before irradiation
- better sensor timing

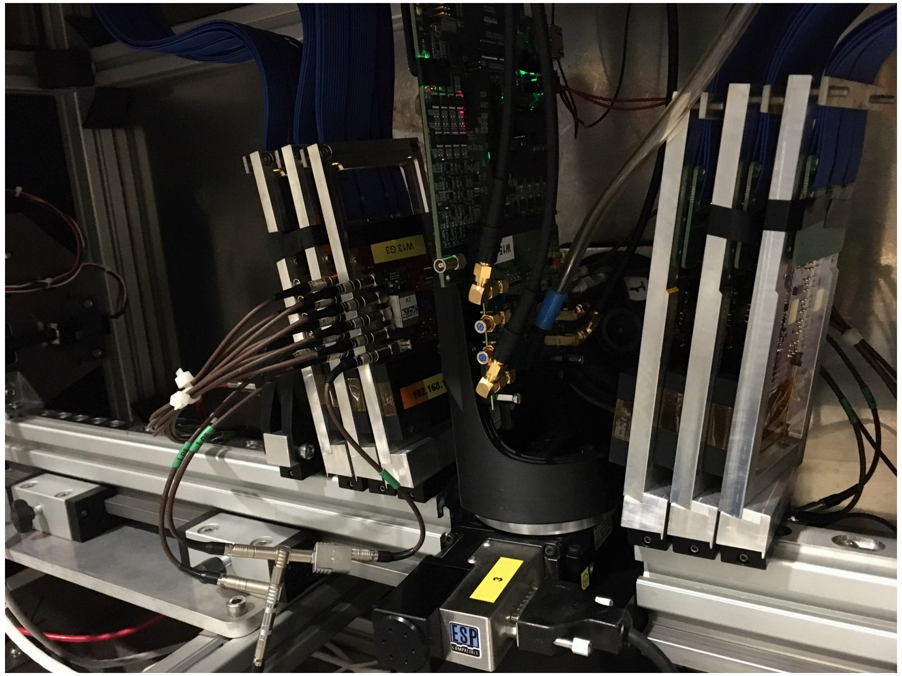
- Monte Carlo using Garfield and Allpix² can generate distributions with reduced computation time compared to full TCAD



walter.snoeys@cern.ch

FASTPIX ATTRACT project: focused on fast timing





Direct relation between charge collection and process variant (TowerJazz 180nm)

Significant impact even at very small pixel pitch

Hexagonal pixels

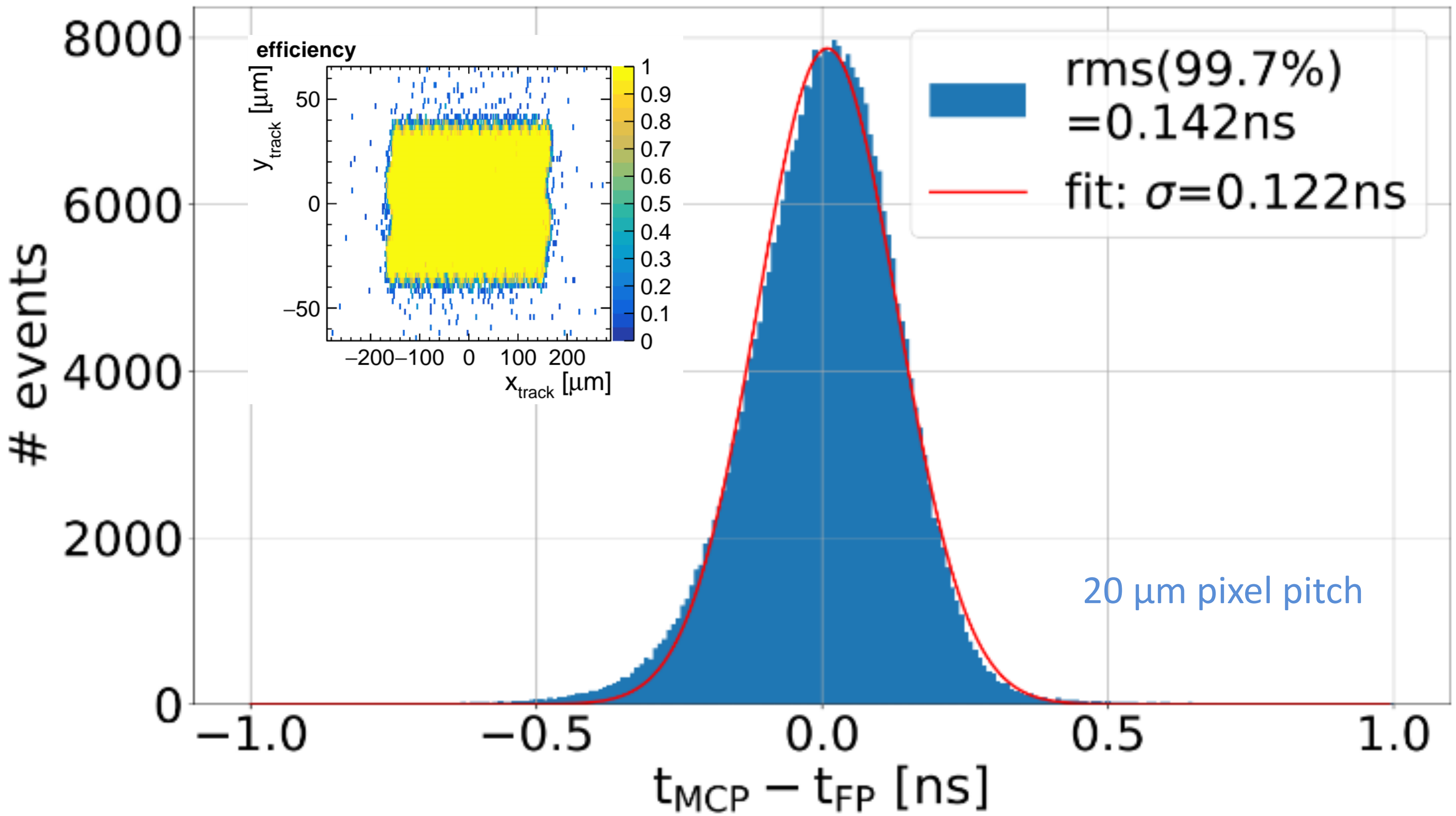
- better approximation of a circle
- charge sharing in the corners between 3 pixels instead of 4 -> more margin
- collection electrodes on hexagonal grid, circuit remains on Manhattan layout

T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461

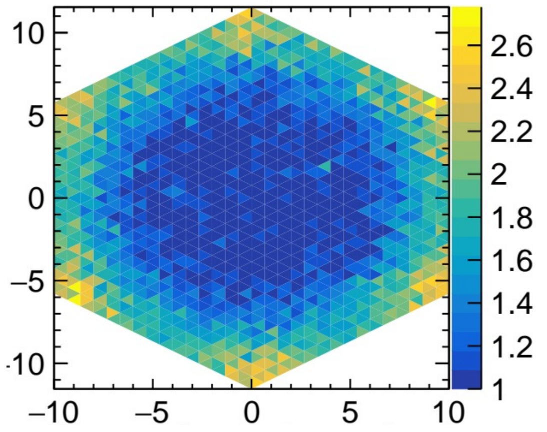
FASTPIX started as an ATTRACT project funded by the EC Grant Agreement 777222, with INFN, Ritsumeikan U. and CERN

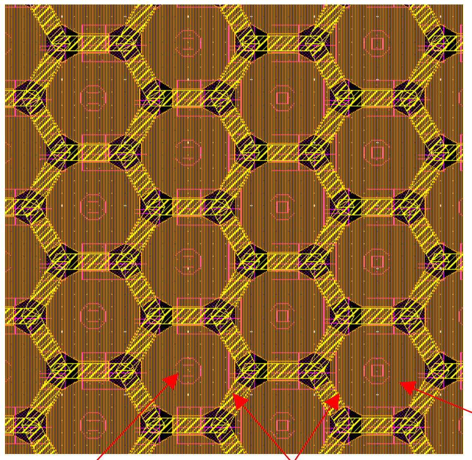
FASTPIX: sensor optimization for hexagonal pixels

EP R&D



Cluster size





- 8.66, 10, 15 and 20 µm pixel pitch
- Time resolution better than 150 ps at full efficiency, TOT corrected

https://www.mdpi.com/2410-390X/6/1/13

J. Braach, E. Buschmann, D. Dannheim, K. Dort, T. Kugathasan, M. Munker, M. Vicente

Moving to deeper submicron CMOS: CERN EP RD and the ALICE experiment

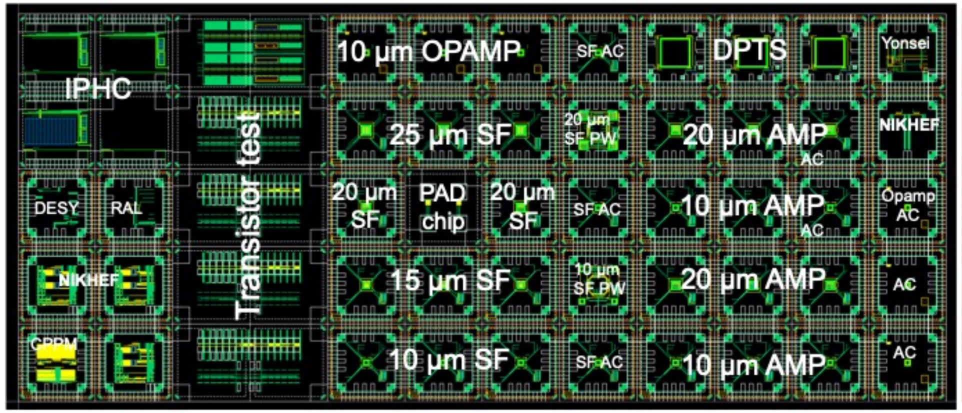
EP R&D

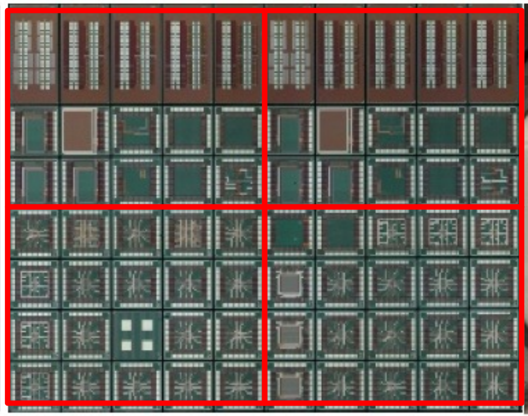
First technology selected: TPSCo 65 nm ISC

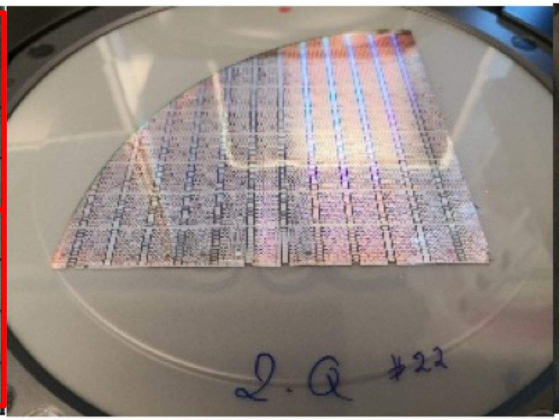
- TPSCo (joint venture TJ & Panasonic): several 65 nm flavors: high density logic, RF, and imaging (ISC)
- ISC preferred: 2D stitching experience, special sensor features, different starting materials, lower defect densities, etc
- Initially 5 metal layers, now 7 metals
- NDA (M. Campbell, L. Pocha & M. Ayass) for participating groups
- Finance Committee approval for stitched runs

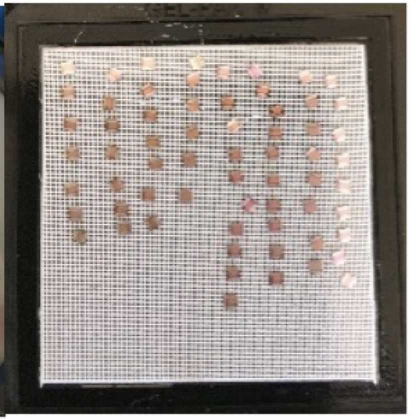
First submission: Multi Layer per Reticle MLR1

- Significant contribution from outside groups (from ALICE but not only) to design and test (!), also financially
- Many test chips of 1.5 x 1.5 cm^2 or twice that size.
- GDS submitted Dec 1, 2020, chips ready to test, Sept, 2021









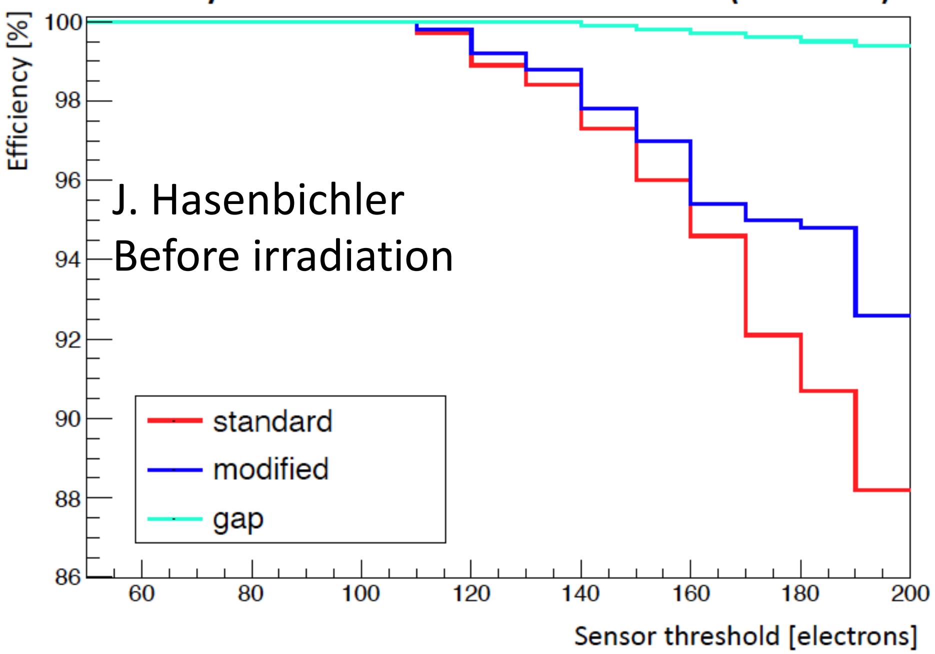
SPLITS for Multi Layer per Reticle MLR1

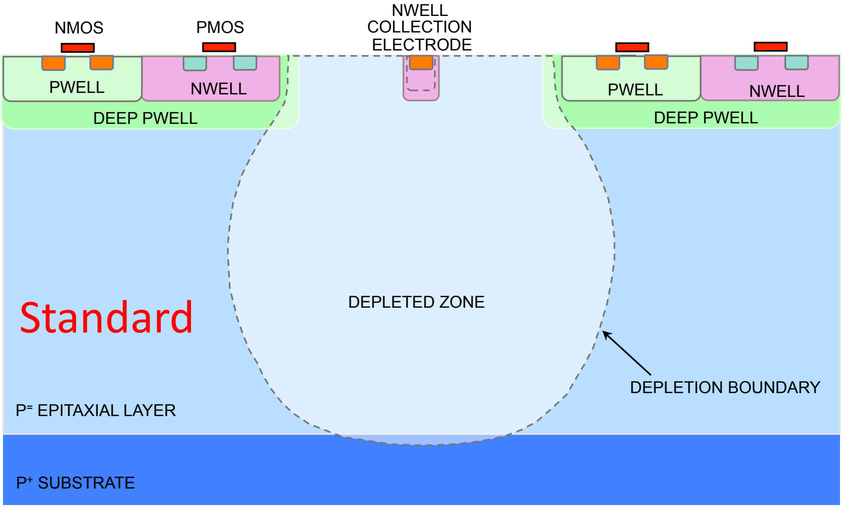
applying same optimization principles to 65 nm as in 180 nm

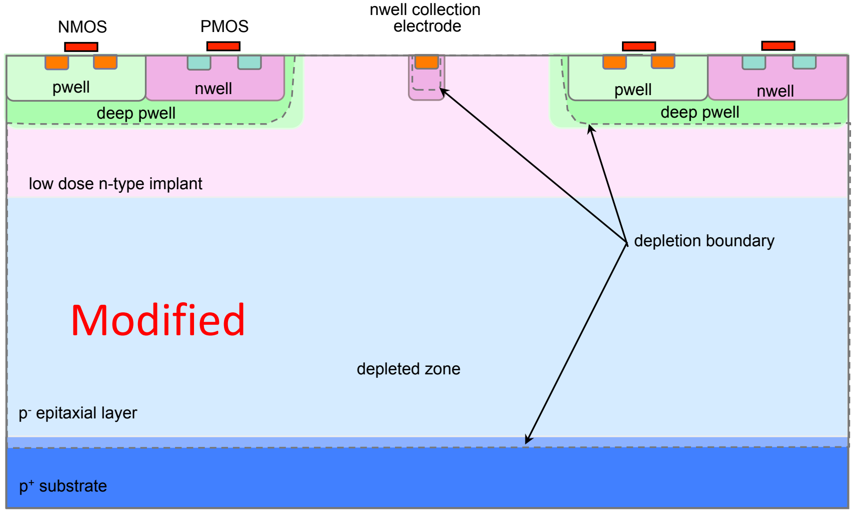
- 4 process splits, 3 wafers each
  - **Split 1: default process**
  - Split 2: first intermediate process
  - Split 3: second intermediate process
  - **Split 4: optimized process**
- 3 main pixel designs implemented in all splits
  - Standard similar in all splits, Modified, Gap

modifications more needed in 65 nm for good charge collection.

Efficiency vs. sensor threshold from TCAD + MC(Garfield++):







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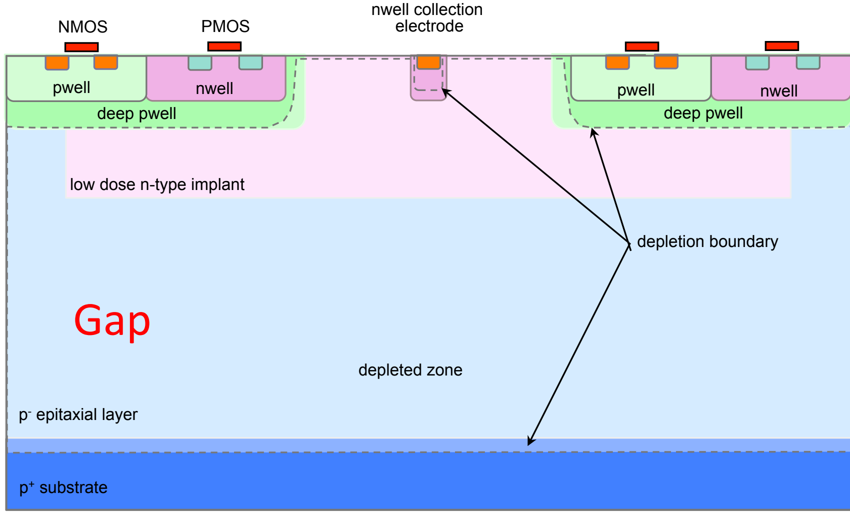
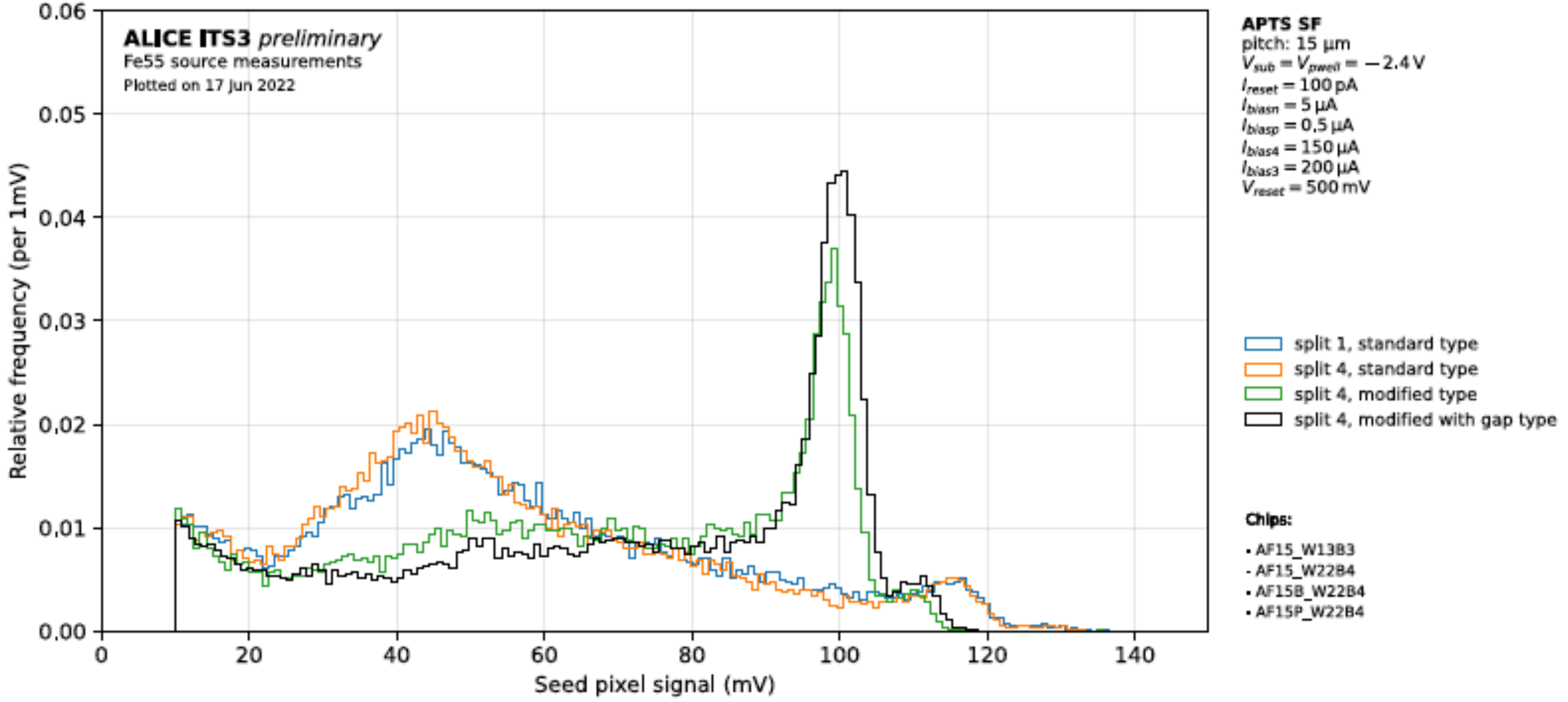


https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed →

← Charge sharing

Different pixel flavors exhibit very significantly different behaviour

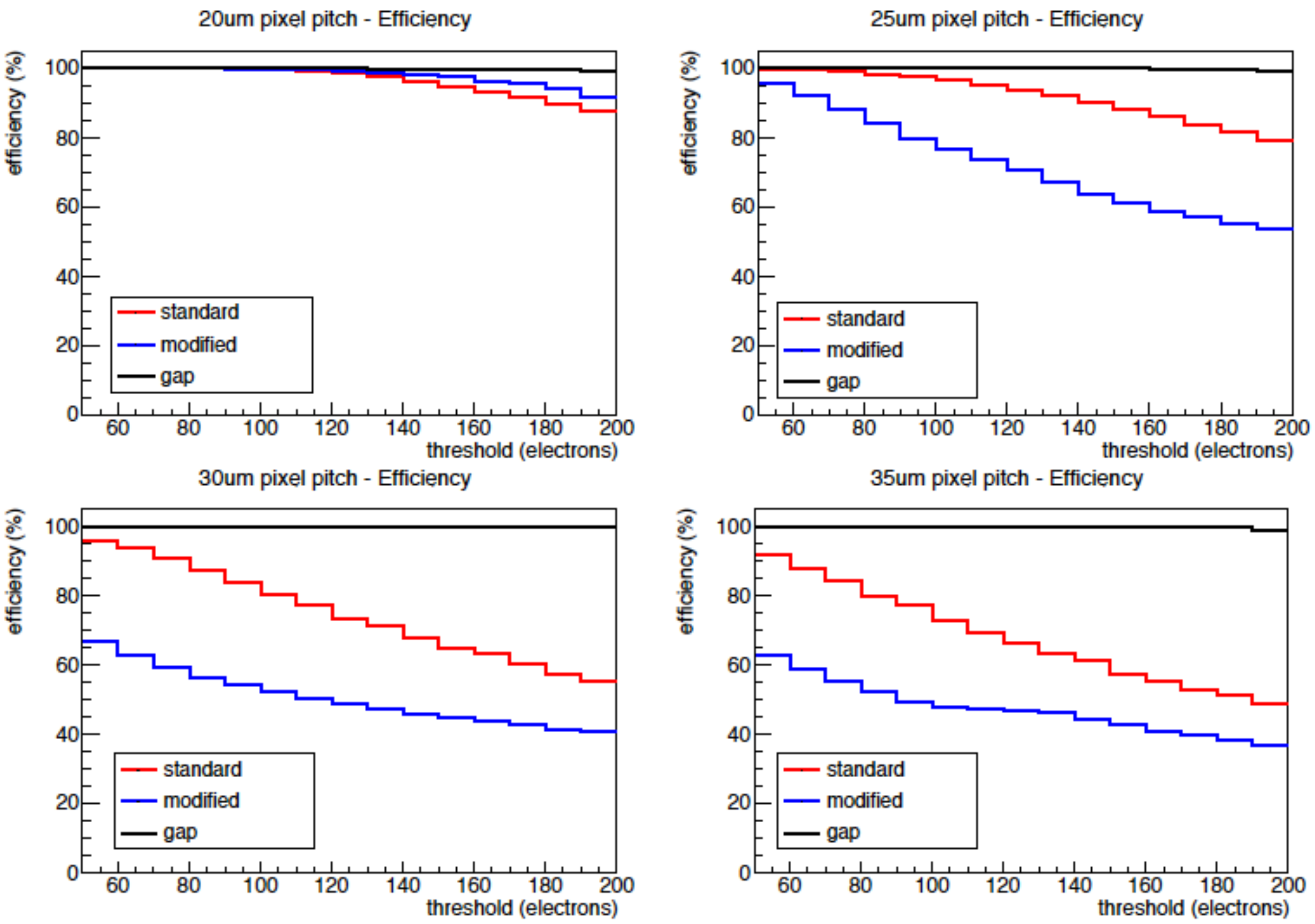


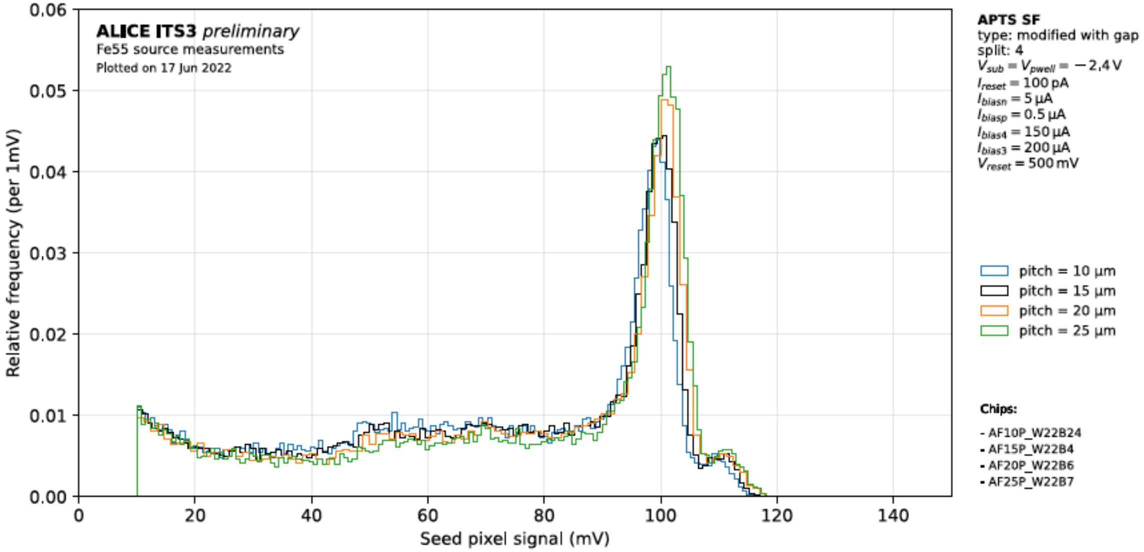
Standard process exhibits quite some charge sharing, modified concentrates charge much more on single pixel

Measurement by ALICE ITS3

Different pixel flavors at larger pixel pitches

Only gap maintains reasonable efficiency





^{55}Fe for pitches for 10, 15, 20 and 25 µm, all with gap

Remarkable result !

Measurement by ALICE ITS3

Simulations by J. Hasenbichler

Further experimental verification in testbeam in progress

MAIN RESULTS MLR1 65 nm

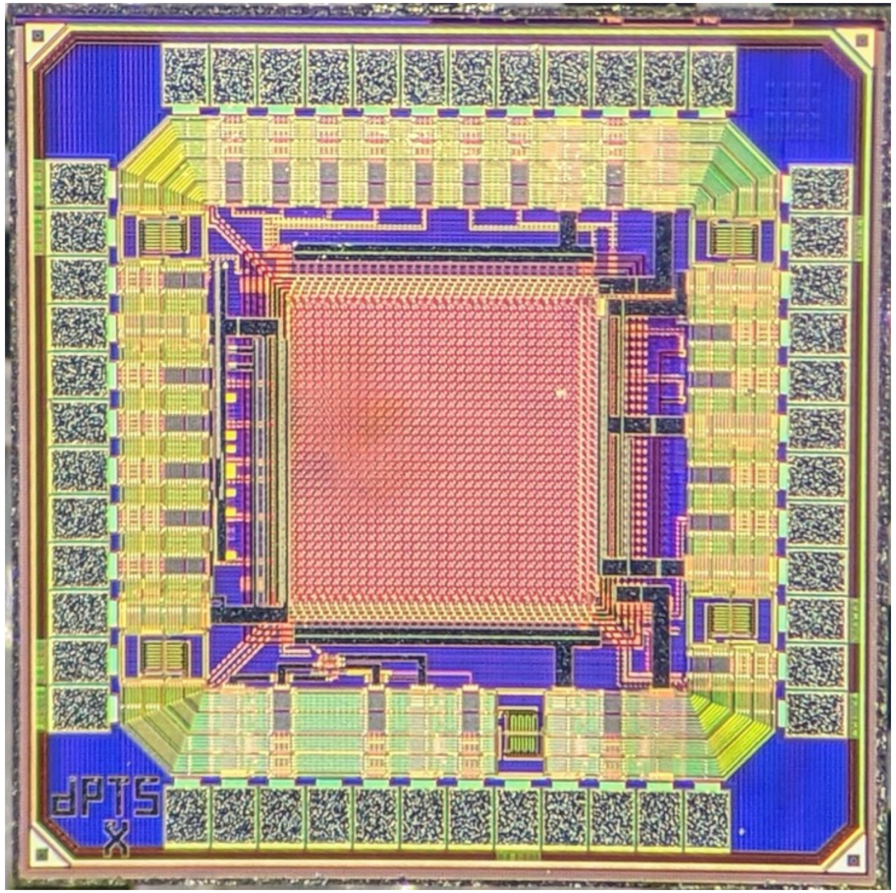
EP R&D

Functionality

- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 μm^2 pixel (DPTS) including sensor optimization
- Sensor optimization clearly accelerates charge collection
- Frontend tunable from 10 nA to 5 μA (power – time resolution tradeoff)
- Measurements at 100 nA, time resolution ~7.5 ns

Radiation effects

- Single event upset cross-section according to expectations
- Circuit radiation tolerance TID in line with other 65 nm technologies
- Sensor radiation tolerance NIEL: analysis in progress:
  - ~ 99% efficiency after 1e15 n_{eq}/cm^2 and 10 Mrad at room temperature
  - higher fluencies to be investigated, also at lower temperature



Building knowledge about this technology for general interest

- Very significant contribution from the ALICE experiment
- Towards full technology validation for our applications

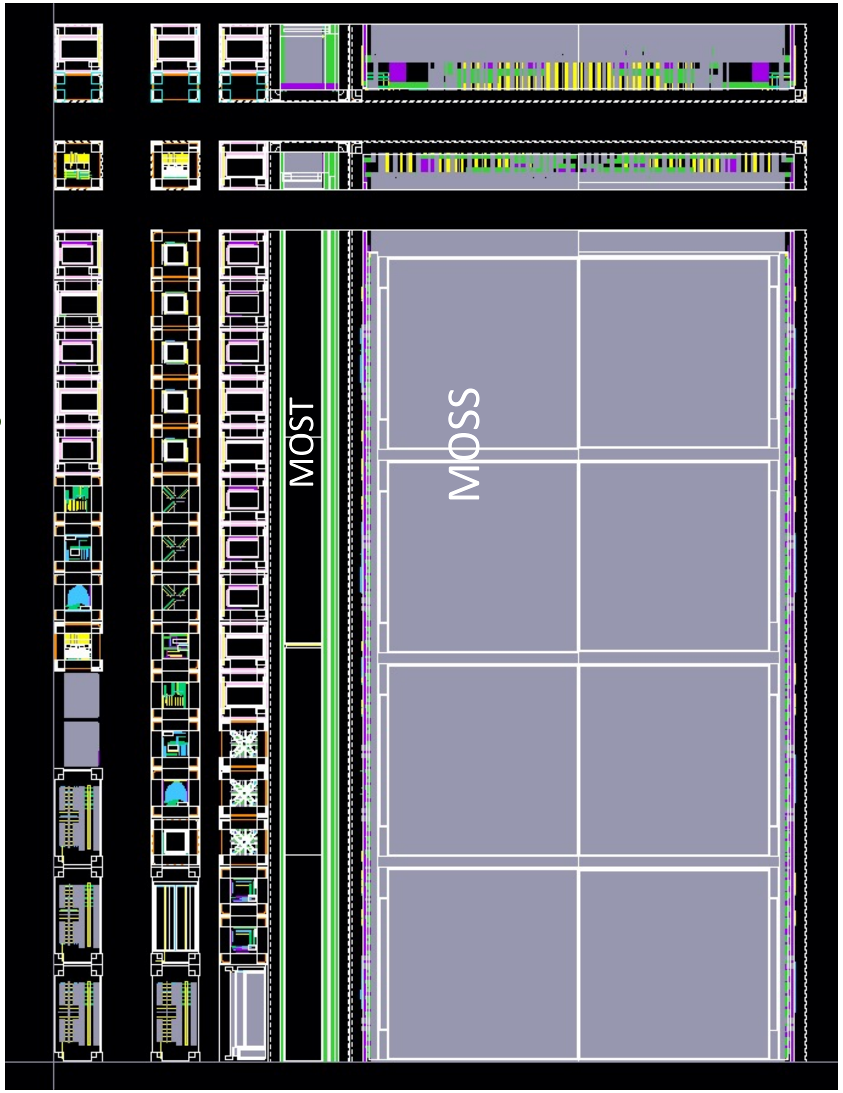
Next submission Stitched Engineering Run ER1

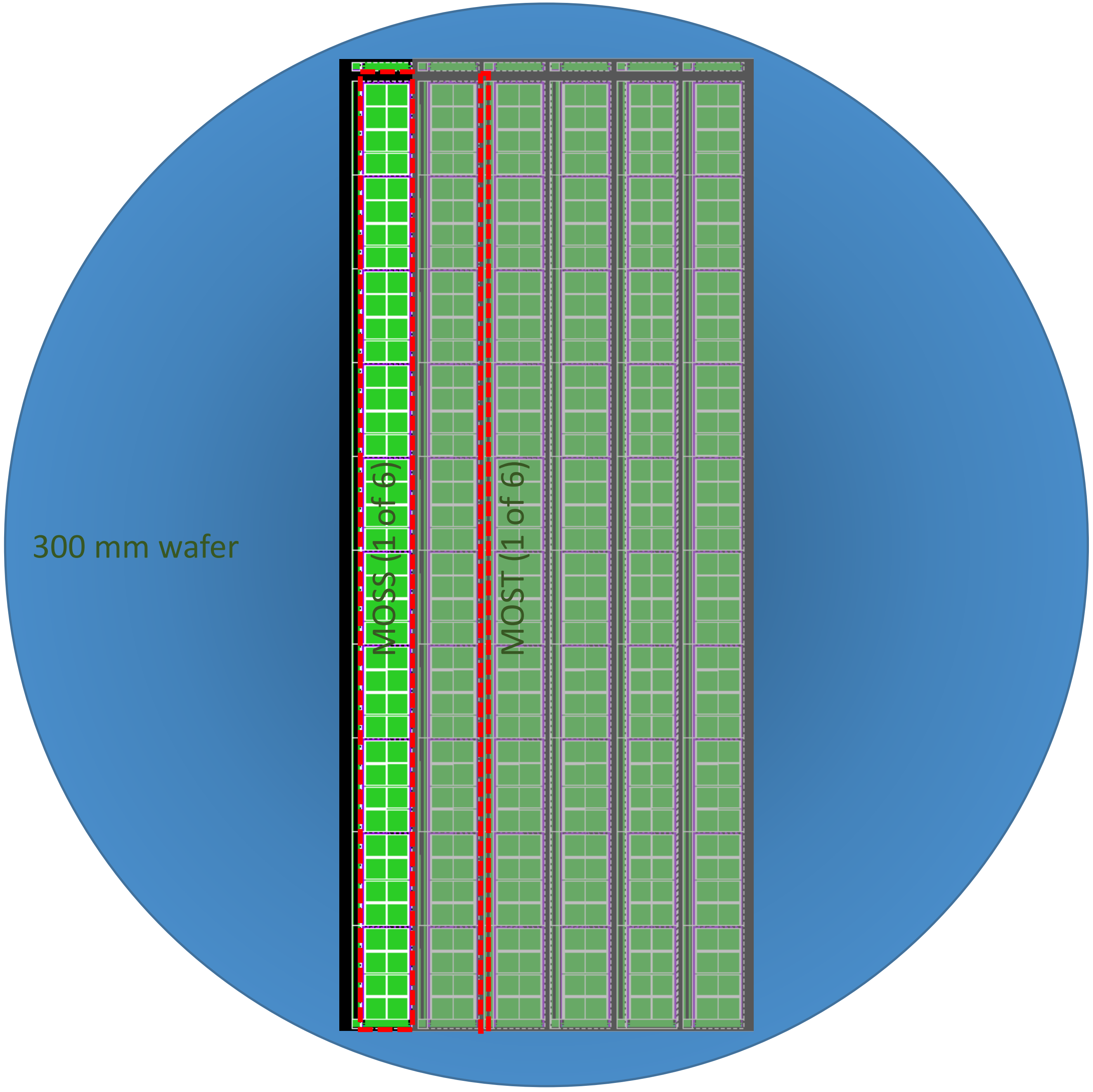
- Learning about stitching and continue learning about the technology

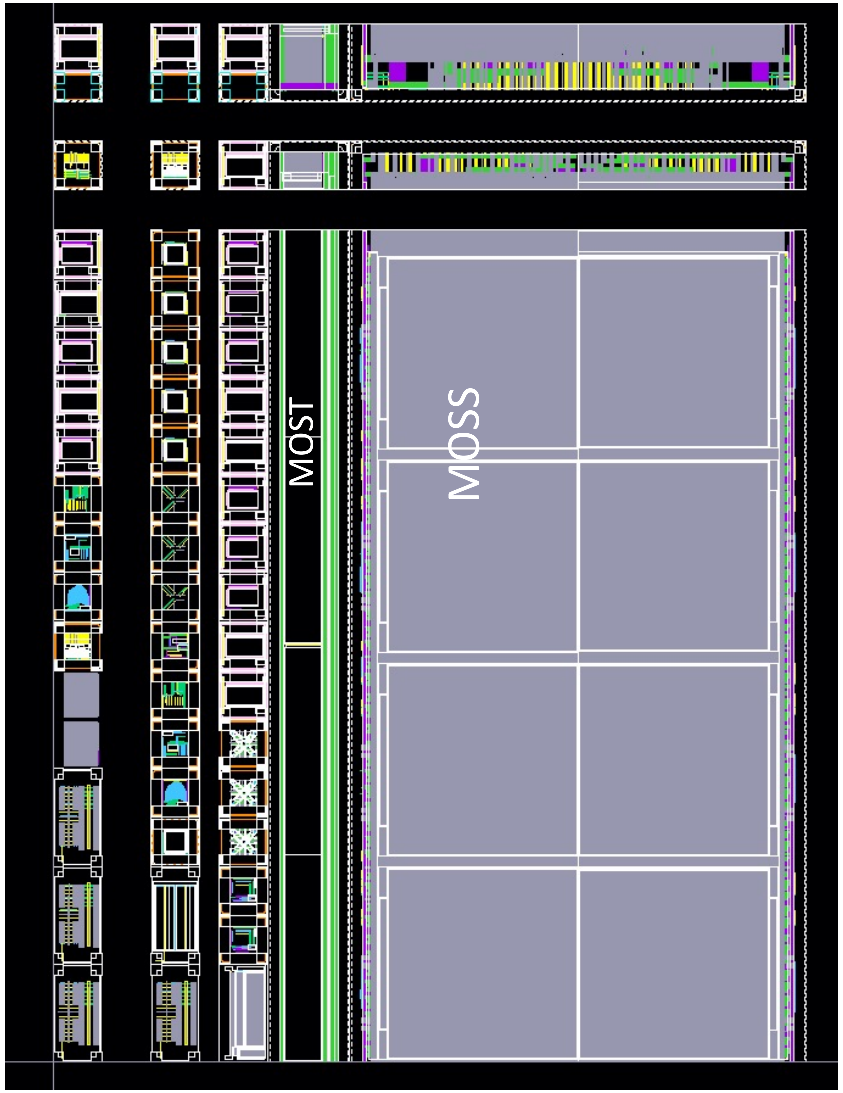
ER1 Submission

- Learn and prove **stitching**
- Two large *stitched* sensor chips (MOSS, MOST)
  - Different approaches for resilience to manufacturing faults
- Multiple small *Test Chips*
  - Pixel and Circuit Prototypes
  - Fast Serial Links
- Technology and Support
  - New metal stack, new I/O libraries, new PDKs
  - Specific features of kits and libraries

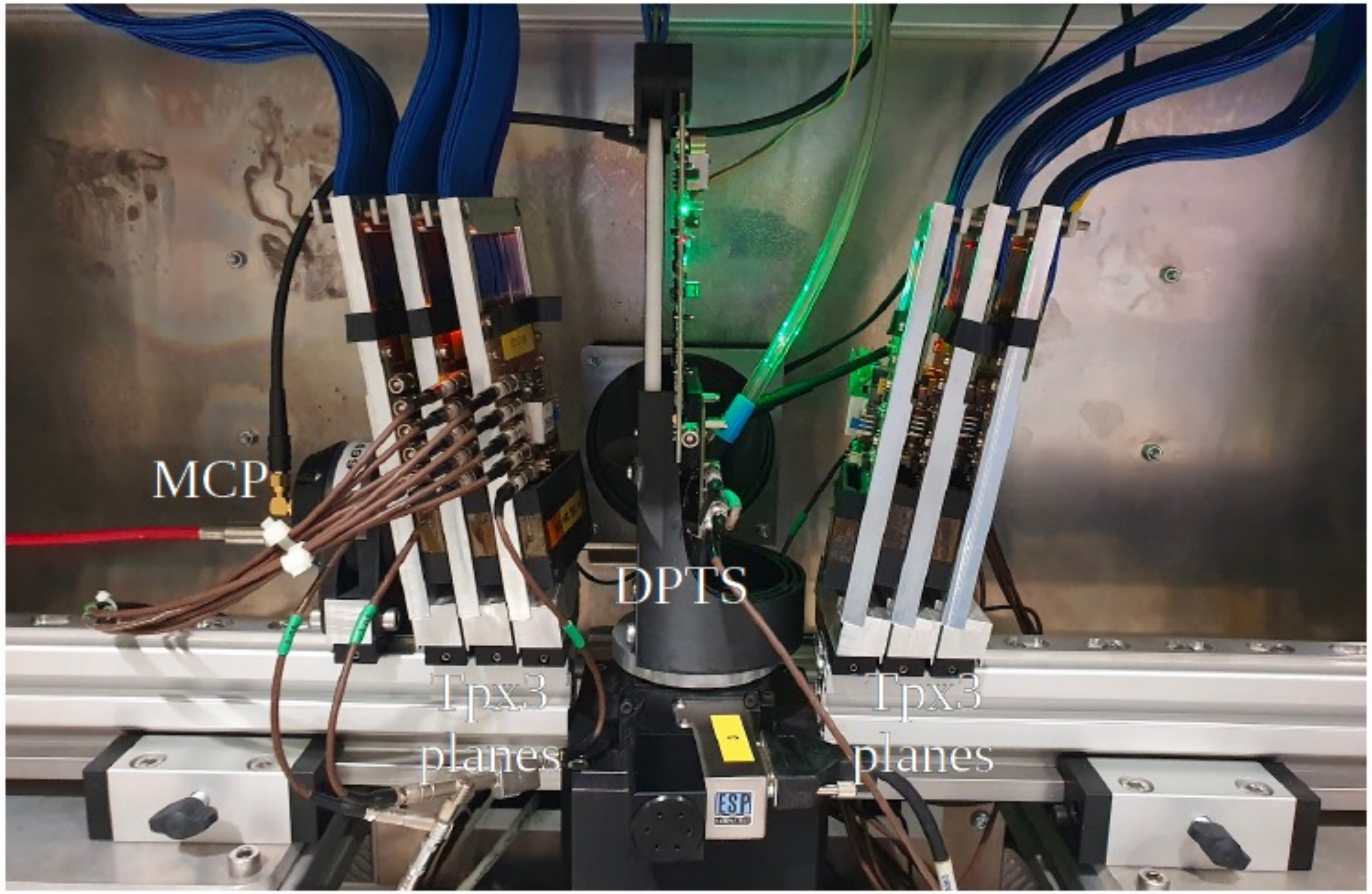
Design Reticle




300 mm wafer
MOSS (1 of 6)
MOST (1 of 6)

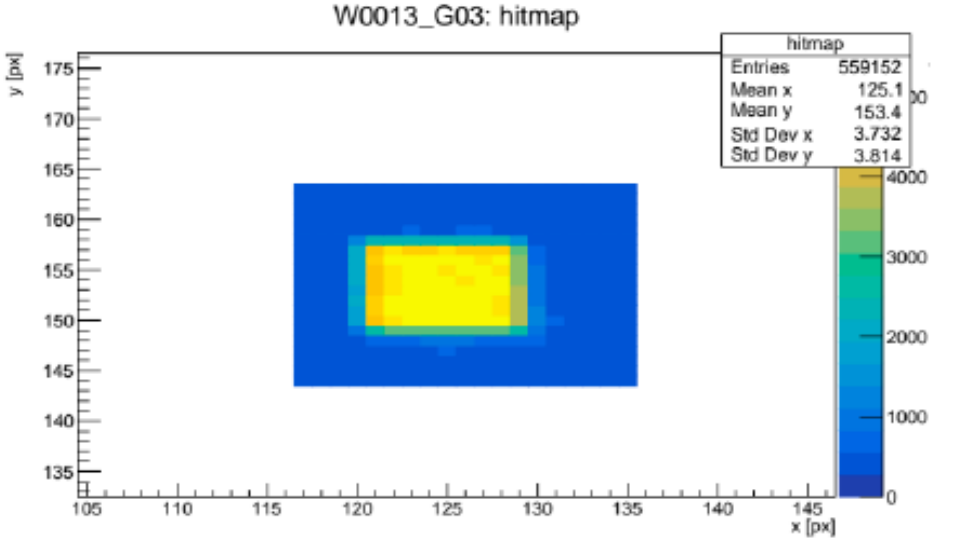

MOST
MOSS

DPTS timing measurements at higher currents



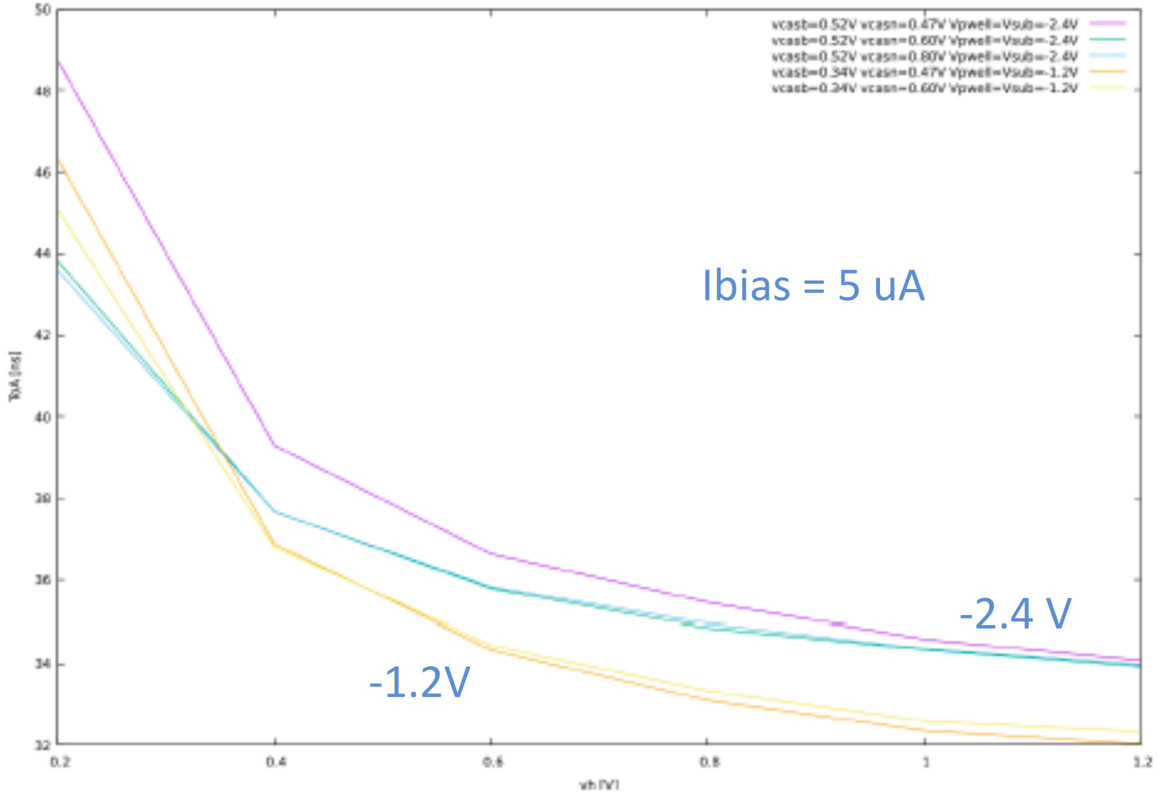
Measurements: E. Buschmann et al.

- Setup: Timepix3 telescope with Hamamatsu R4809U-50 MCP-PMT as time reference (< 10 ps RMS at 3.2 kV), Caribou readout
- Very preliminary results



Time of Arrival

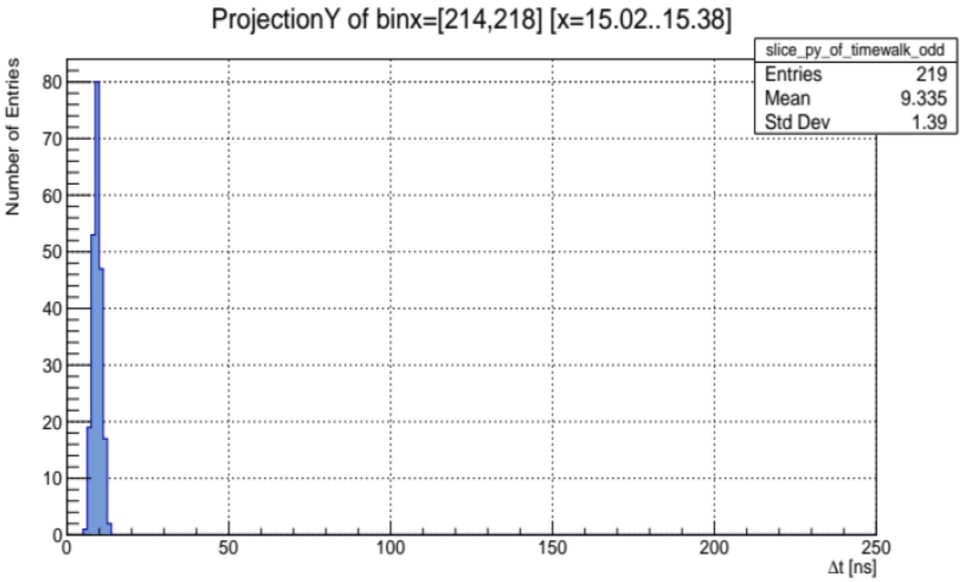
EP R&D



Work in progress

Measurements: E. Buschmann et al.

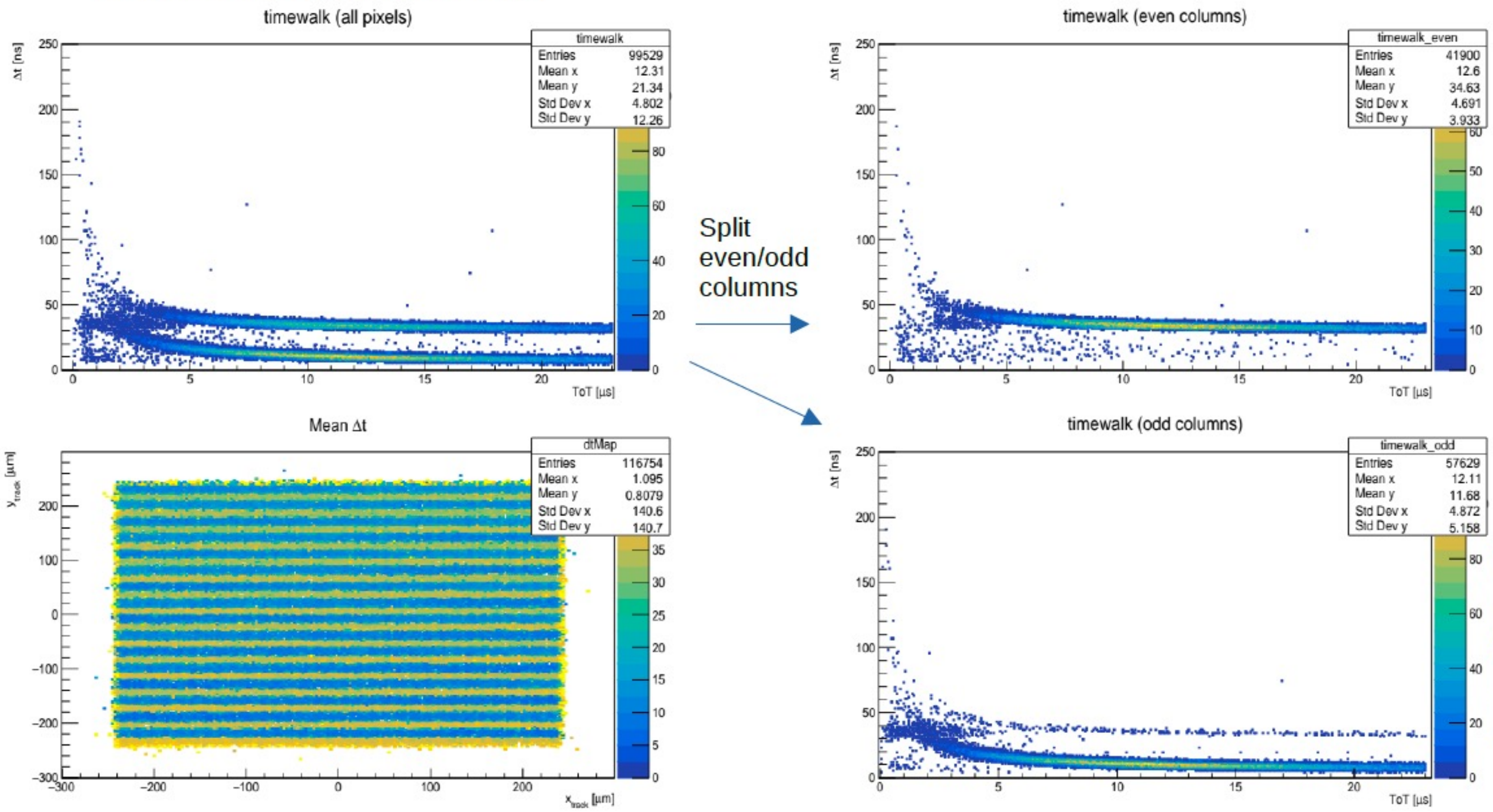
- Influence of reverse substrate bias: higher TOA at -2.4 V compared to -1.2 V (due to slow down of digital circuit), but for correct operating point better slope
- Timing around 1 ns, limited more by the front end than the sensor.



Slice for ToT=12µs

Analysis in progress, here for -1.2 V, -2.4 V to be done

EP R&D



Still some issues with decoding

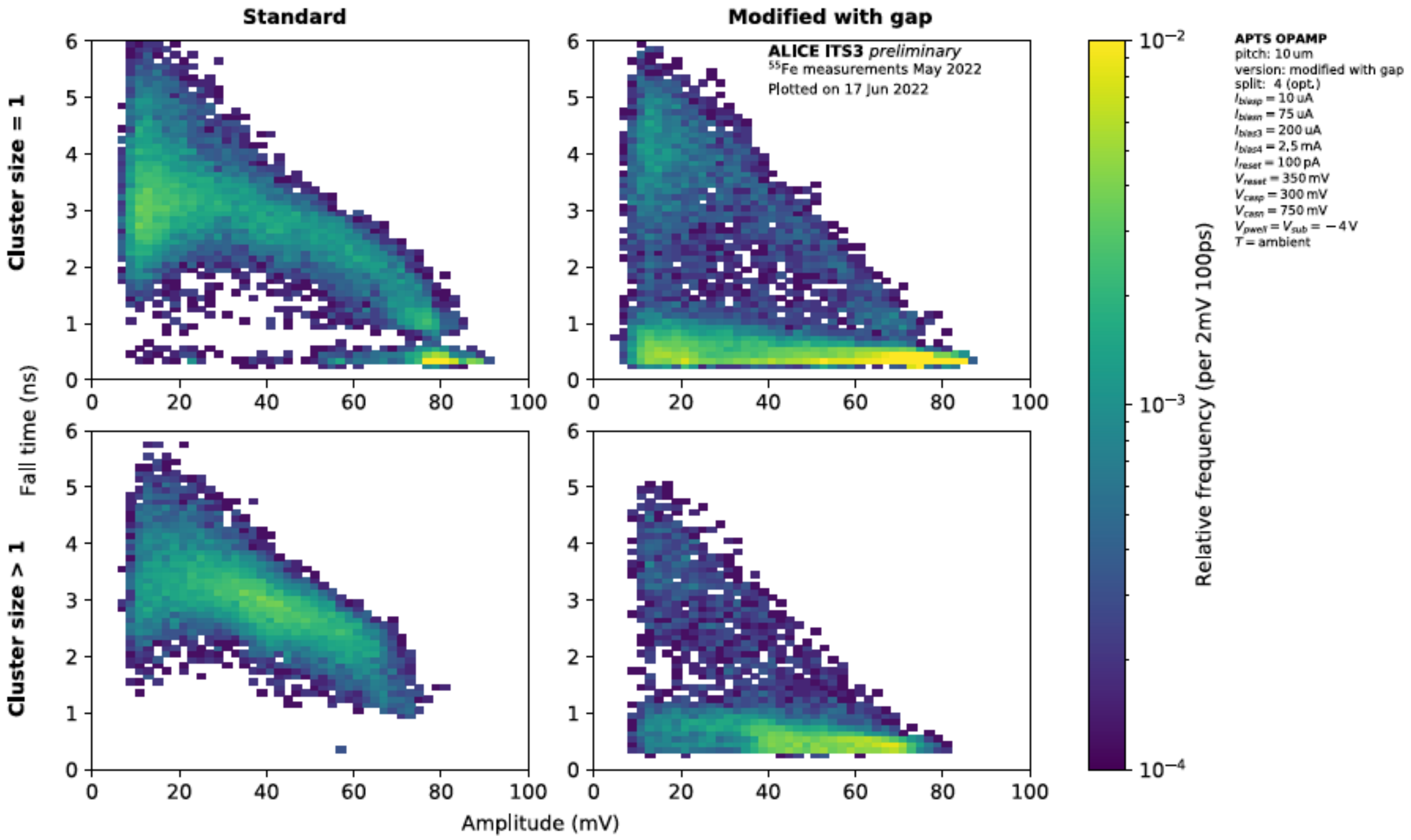
Sample 1, chip #40
Ibias=5uA
Ibiasn=500nA
Vcasb=370mV
Vcasn=470mV
Ireset=10pA
Idb=300nA
Vsub=Vpwell=-1.2V

5

Work in progress, different delay from pixels in odd and even rows here

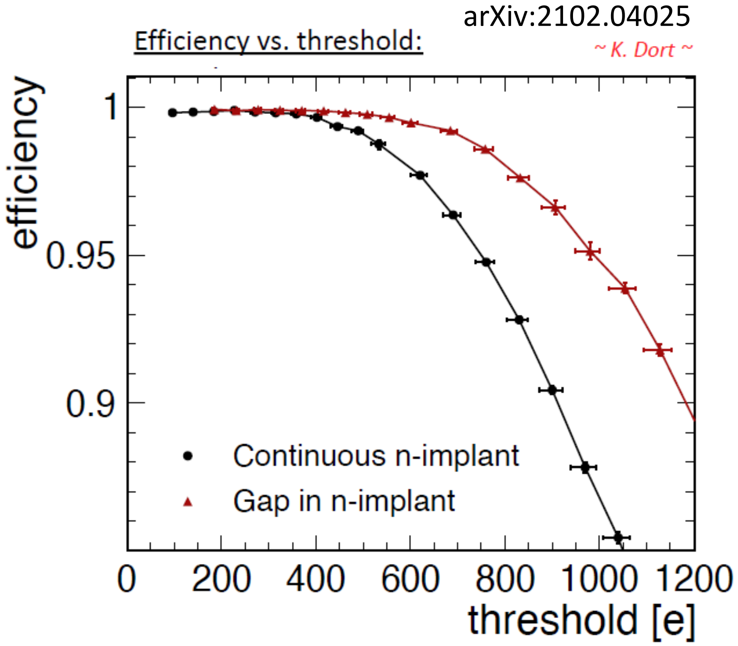
Analog pixel test structure, faster circuit

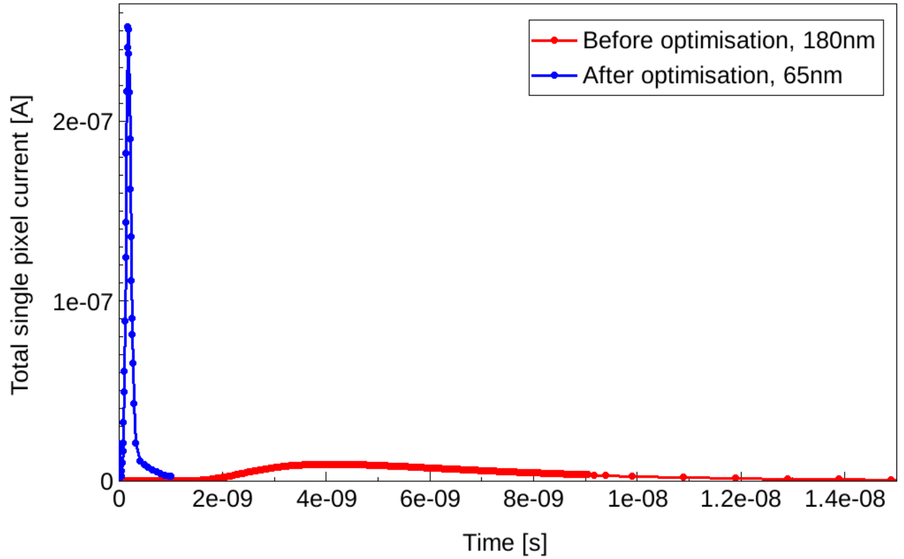
- Clusters of different sizes show distinct fall time and amplitude distributions
- Nice demonstration of the change in charge collection
- Test beam is underway to measure the timing performance

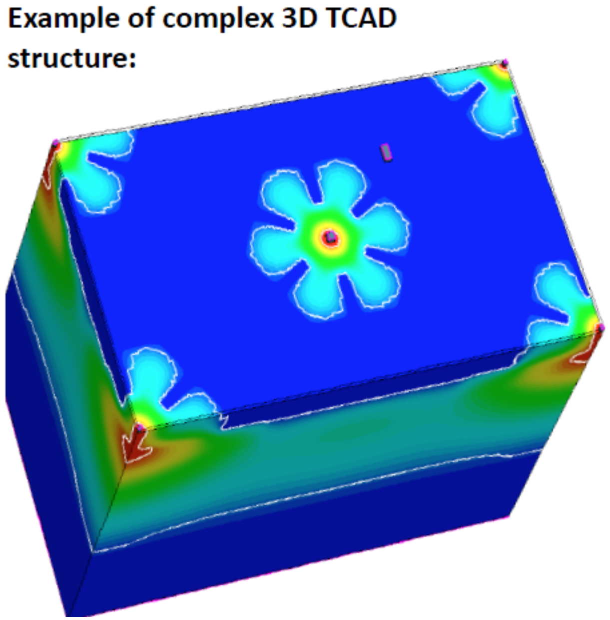


Acceleration of charge collection evident, detailed analysis ongoing, measurements by ALICE/INFN Torino

Process optimizations for small collection electrode







- Efficiency improvement is not only simulated but also measured, even before irradiation (see top left: efficient operating window is almost doubled)
- The optimization over different pixel pitches and flavors, and technologies has improved the timing by several orders of magnitude. Simulations of even more complex structures bring peak-to-peak variations in the order of 50 ps at the moment
- These techniques have now been applied to several chips, and technologies and are generally applicable.

See M. Muenker's CERN EP detector seminar

Concluding remarks

Sensor radiation tolerance, precision timing and improved efficiency can be obtained from optimization for fast charge collection using techniques based on general principles applicable to different technologies.

~ 150 ps on small collection electrode demonstrated in 180nm

Expect better on 65 nm with present process and sensor modifications, analysis in progress.

Decreasing technology feature size or special imaging sensor features can increase the voltage excursion on a small collection electrode and ultimately reduce analog front end power to zero and allow precision timing.

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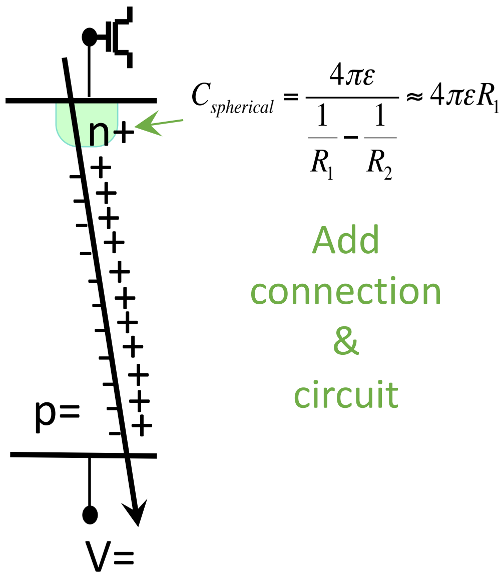
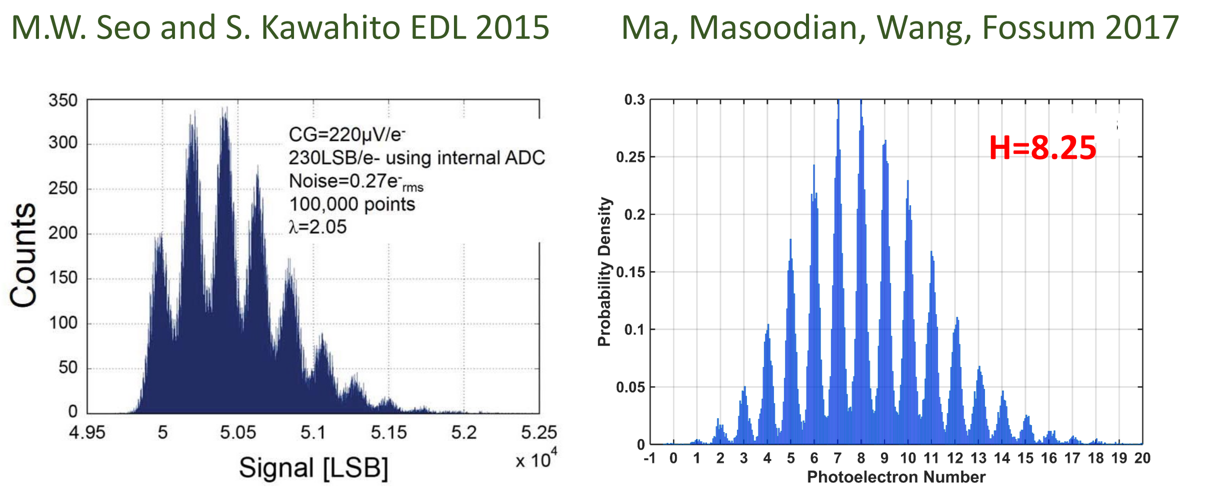
THANK YOU !

Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)

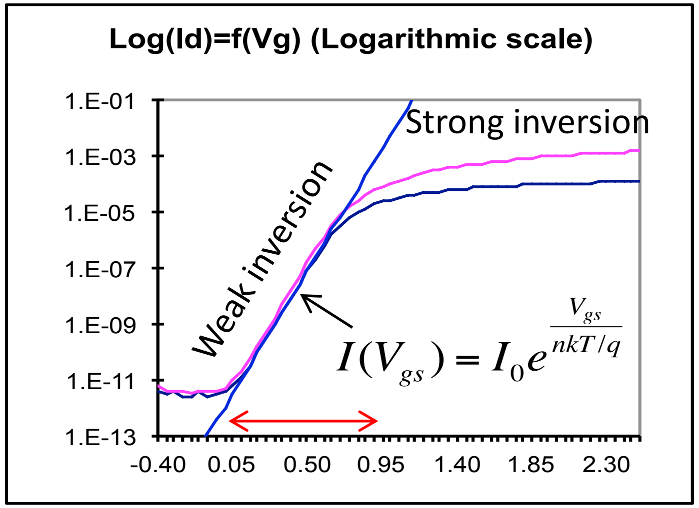




220 µV/e- in 0.11 µm, C=0.73 fF

350 µV/e- in 45 nm, C=0.46 fF

Non-linearity in weak inversion



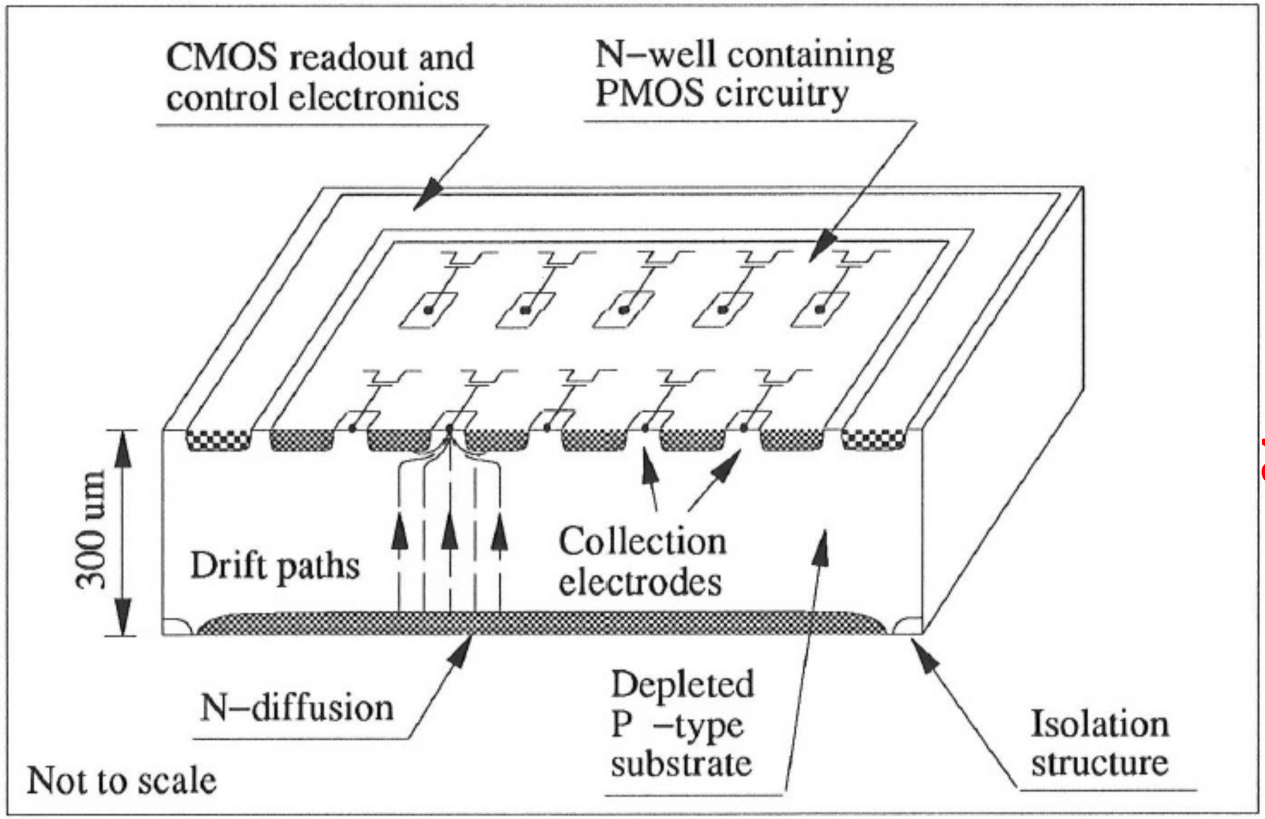
- Q/C several 10's of mV in 180 nm
- "Conventional" approach
  - ITS3 estimate ~ 10-15 nW front end for about 10 mW/cm^2 (ALPIDE in 180nm ~ 40 nW), 5x area reduction
  - Increase power and speed for better timing, µW for < 1 ns

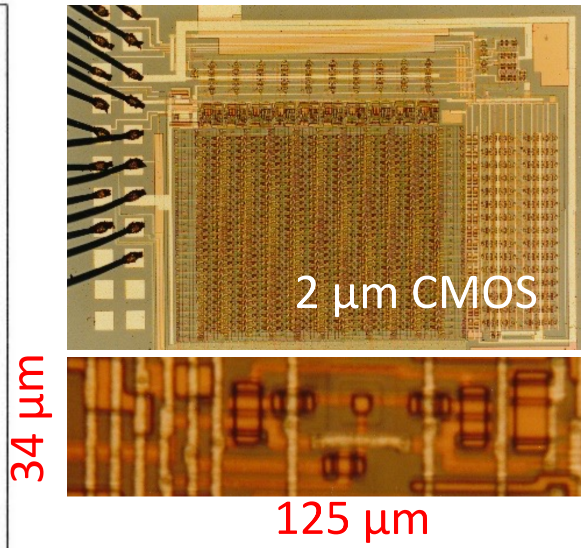
Analog power often dominant !

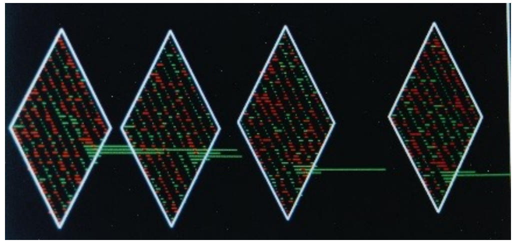
F. Piro

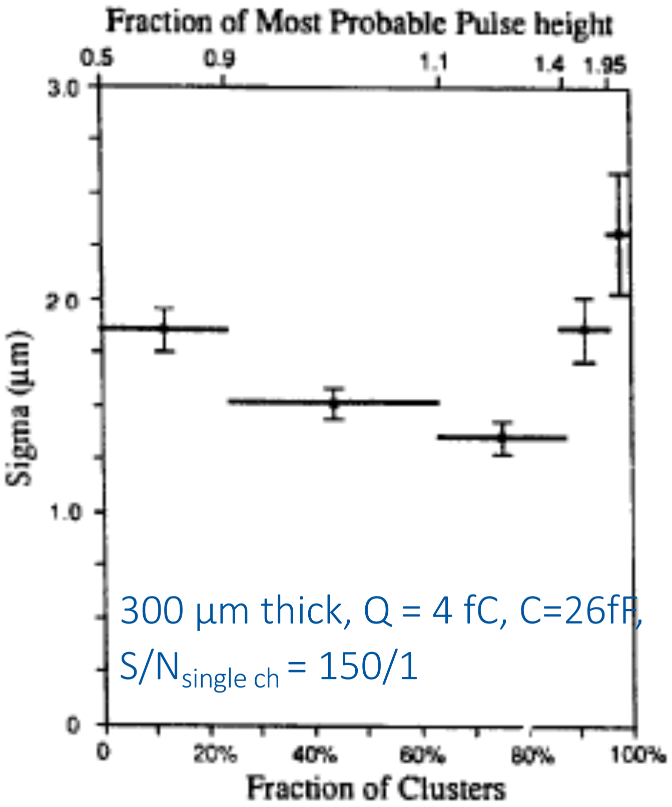
- Reduce capacitance further, using:
  - tricks from imaging technology, at present not yet explored?
    - now very conventional nwell collection electrode…
    - Still need to extract signal charge from underneath the readout circuit !
  - deeper submicron: 2500 e- to switch inverter in 65 nm, 850 e- in 28 nm, 100 e- in 5 nm A. Marchioro 2019 CERN EP seminar
- Gain layers in the sensor
- Holy Grail: For Q/C > 400 mV, analog power consumption goes to zero.

Towards standard technology, but double-sided processing

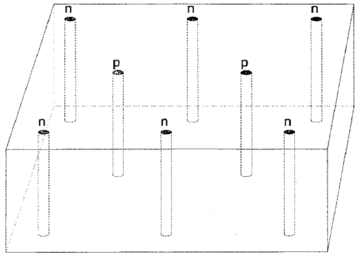








- Separation of junction from collection electrode
- Better than 2 µm position resolution even at large pitch due to good S/N
- Improved back side isolation with trenches lead to sensors with 3D electrodes (S.Parker) →



C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

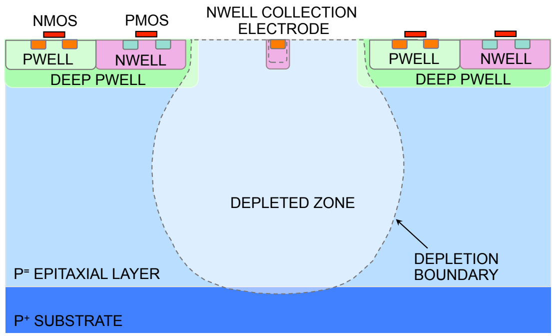
Other examples: ~ 1 µm resolution: SOI sensor, pitch 13.75 µm *M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53*

Position resolution: good S/N for interpolation Junction separation and back side processing: see below

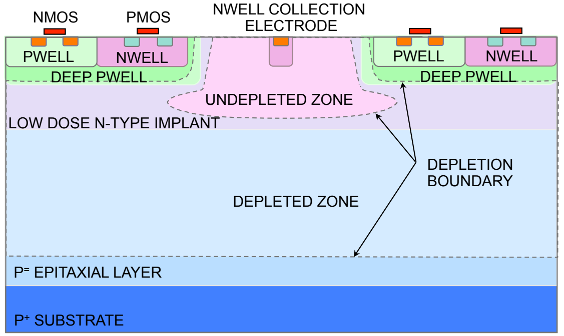
Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors

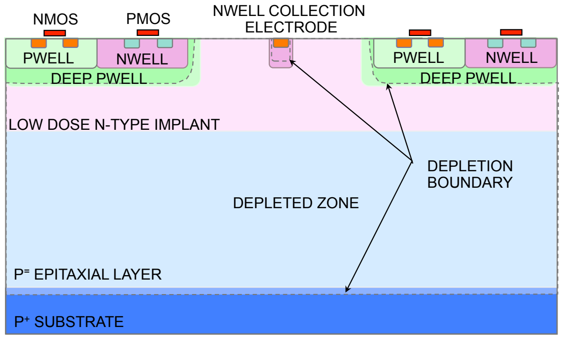
Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…



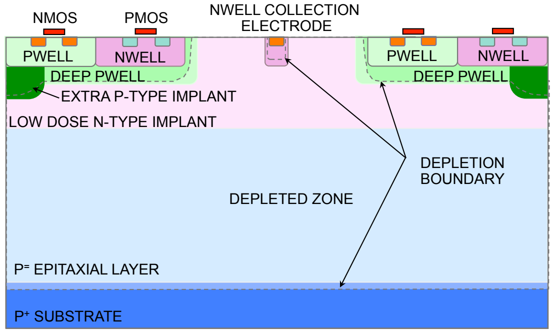
Standard, not fully depleted (ALPIDE)



Not fully depleted at low reverse bias



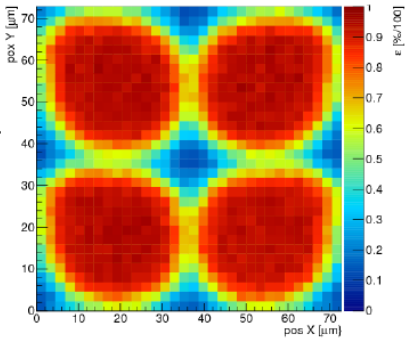
Depletion at higher reverse bias (MALTA1, MONOPIX)



Further improvements by influencing the lateral field

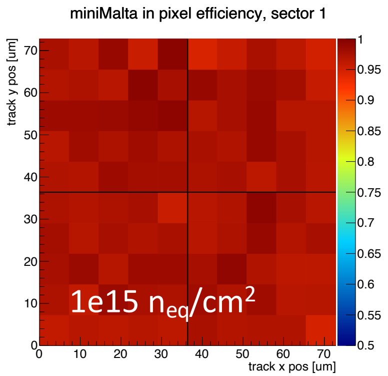
Additional implant for full depletion
=> order of magnitude improvement
Side development of ALICE for ALPIDE
NIMA 871 (2017) pp. 90-96
Triggered development in ATLAS
H. Pernegger et al, 2017 JINST 12 P06008

Efficiency drop at pixel edges after irradiation for 36.4 x 36.4 μm^2 pixel needs improvement
E. Schioppa et al, VCI 2019



3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987



Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027…
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
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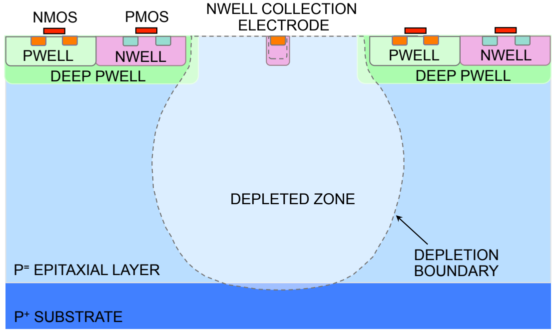

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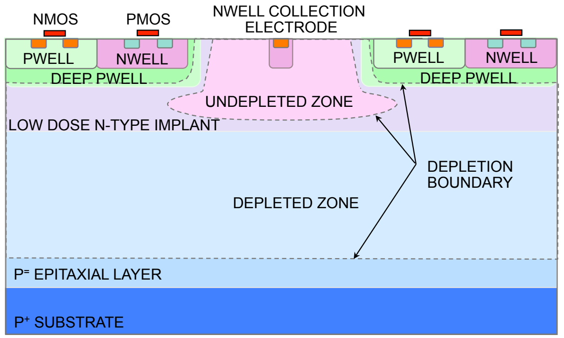
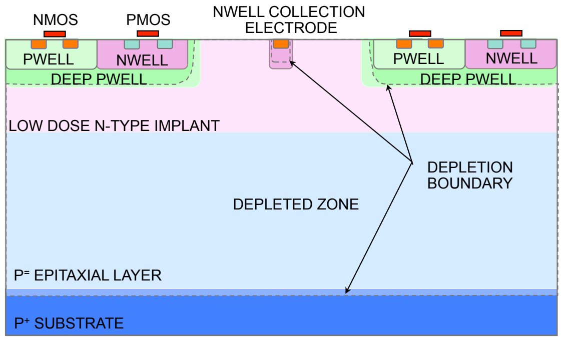


Not fully depleted at low reverse bias



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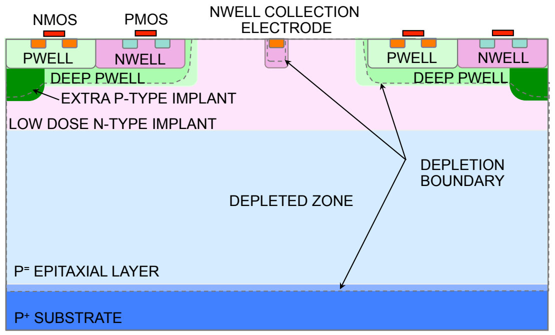
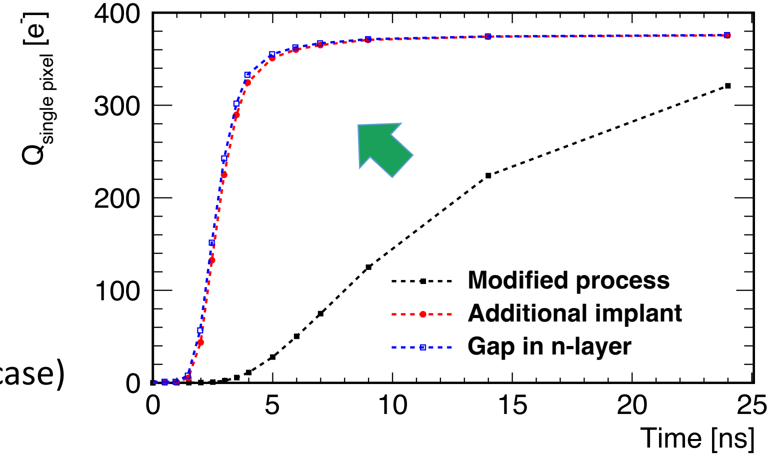


Further improvements by influencing the lateral field

Hit in the pixel corner (= worst case)



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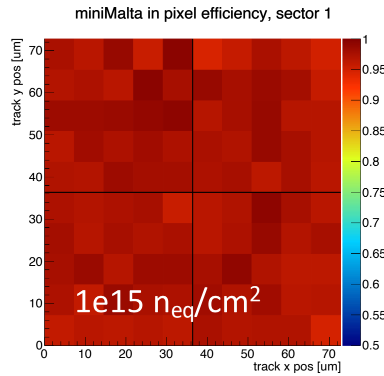

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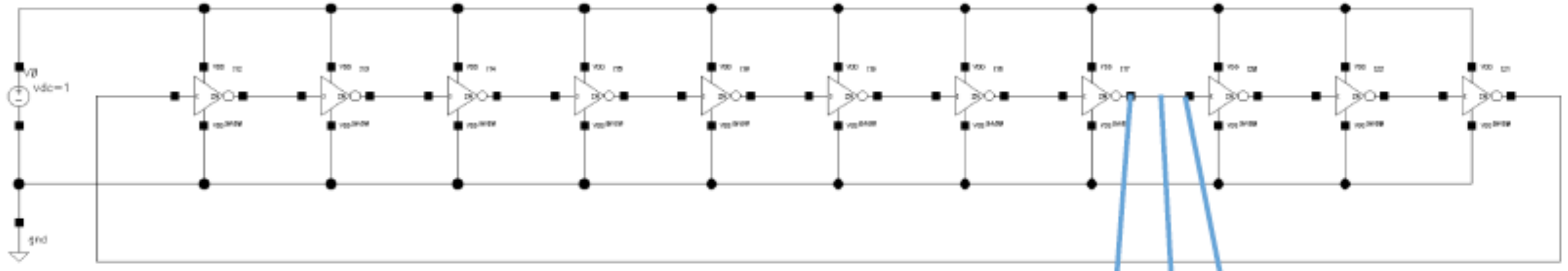
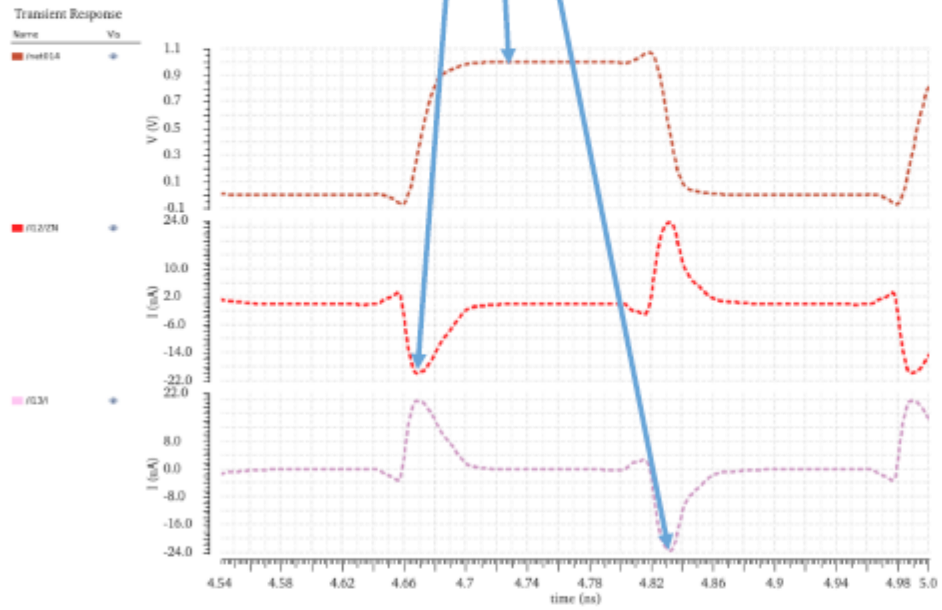
How many electrons are needed to switch a logic gate ?



- **65 nm: ~ 2500 e⁻**
- **28 nm: ~ 850 e⁻**



A. Marchioro, 2019 CERN-EP seminar