Gain Layer fabrication

For Picosecond Avalanche Detectors (PicoAD) implemented in Monolithic Active Pixel Sensors (MAPS)

Elviretti, Matteo

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IHP – Leibniz-Institut für innovative Mikroelektronik

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Agenda

1 Introduction

2 Processing

3 Experiments

4 Conclusion

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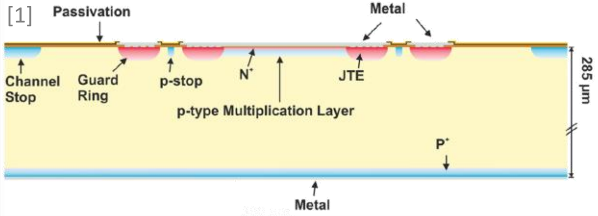
1 Introduction

Avalanche Diodes

[1]



Description

- «Reach-through» structure with p-type layer just below n+ electrode
  - Multiplication layer underneath the pixel
  - Lightly-doped absorption layer

Challenges

1. Strong variation of electric field at pixel edge
   - Requirement of introducing discontinuities in multiplication layer
2. Charge-collection noise
   - Intrinsic time jitter

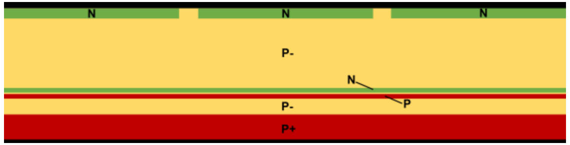
Solutions

1. Increasing pixel size
2. Thinning the avalanche diode

1 Introduction

PicoAD

[2]



Description

- Multi –junction monolithic silicon pixel detector
- $(NP)_{pixel}(NP)_{gain}$ structure
  - 1st epitaxial layer: Primary absorption region;
  - Gain Layer: Uniform deep NP junction;
  - 2nd epitaxial layer: Drift region

Advantages

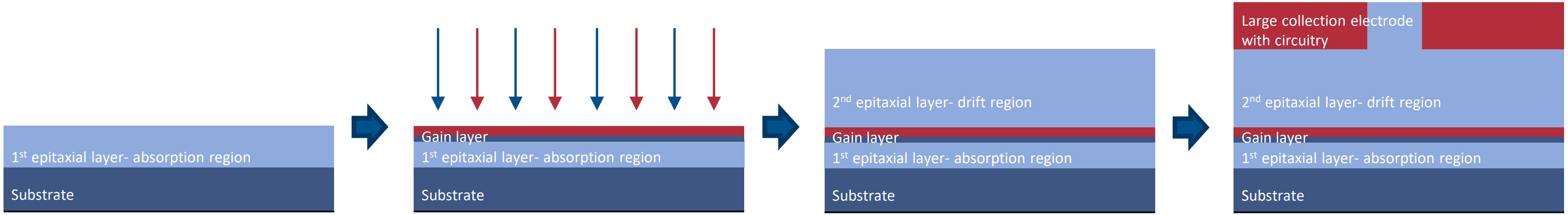
- Gain layer far from the pixels
  - Less subject to strong variation of the electric field
    - Continuous gain layer
      - It removes the inter-pixel zones of degraded time resolution
- Absorption region arbitrarily thin
  - Reduces charge-collection noise
  - Does not increase significantly pixel capacitance

2.2 Processing

Current concept

1st epitaxy on low ohmic substrate | Gain layer implantation | 2nd epitaxy | SG13G2 IHP process

[3]



3 to 5 µm epitaxy

B and As implantation

15 to 25 µm epitaxy

Challenges/issues:

Wafer flatness after 2nd epi might be not sufficient for litho processes of 130nm CMOS

Non-negligible risk of introducing defects on the surface of the thicker epitaxial drift layer

Time consuming when done with IHP dichlorsilane-based process at 850°C

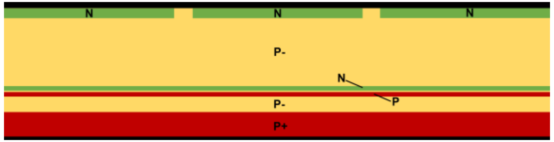
3 Experiments

ATTRACT

FASER

MONOLITH

[2]



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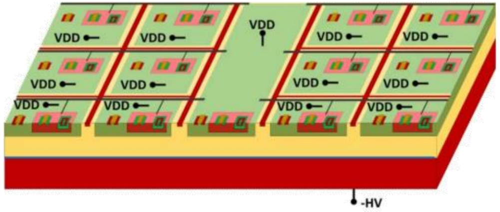

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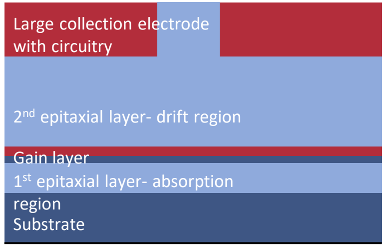

Large collection electrode with circuitry

2^{nd} epitaxial layer- drift region

Gain layer

1^{st} epitaxial layer- absorption region

Substrate

IHP contribution

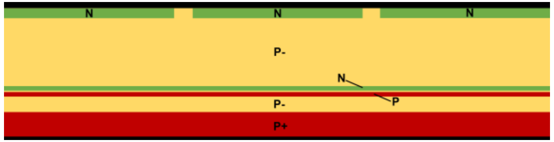
1^{st} and 2^{nd} epitaxies (low T tool at IHP)
Gain layer implantation
SG13G2 BiCMOS process

50 µm epi layer (Globitech)
Pre-process polishing
SG13G2 BiCMOS process

1^{st} and 2^{nd} epitaxies (Globitech)
Masked gain layer implantation
SG13G2 BiCMOS process (yet to be started)

3.1 Experiments

ATTRACT MONPicoAD

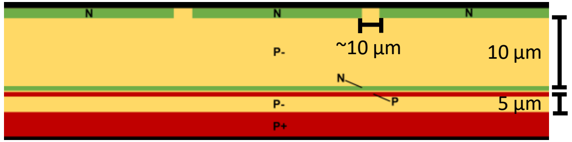


Structure

- Heavily p-doped substrate (0.1 Ωcm)
- 5 µm thick epitaxial layer (absorption region)
- Masked gain Layer (with litho marks)
- 10 µm epitaxial layer (drift region)
- IHP 130 nm SiGe BiCMOS front-end electronics and pixels
- Metallization

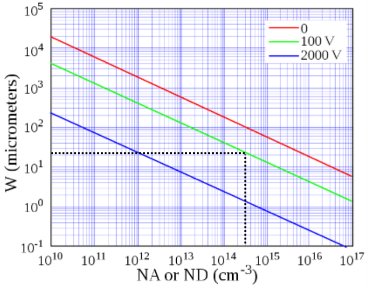
3.1 Experiments

ATTRACT MONPicoAD: Epitaxies



Dichlorsilane-based epitaxy:

- 1^{st} epitaxy on a low resistivity B-doped substrate
  - 5 µm B-doped ($3x10^{14}$ cm^{-3}) layer
- 2^{nd} epitaxy after gain layer implantations
  - 10 µm B-doped ($3x10^{14}$ cm^{-3}) layer

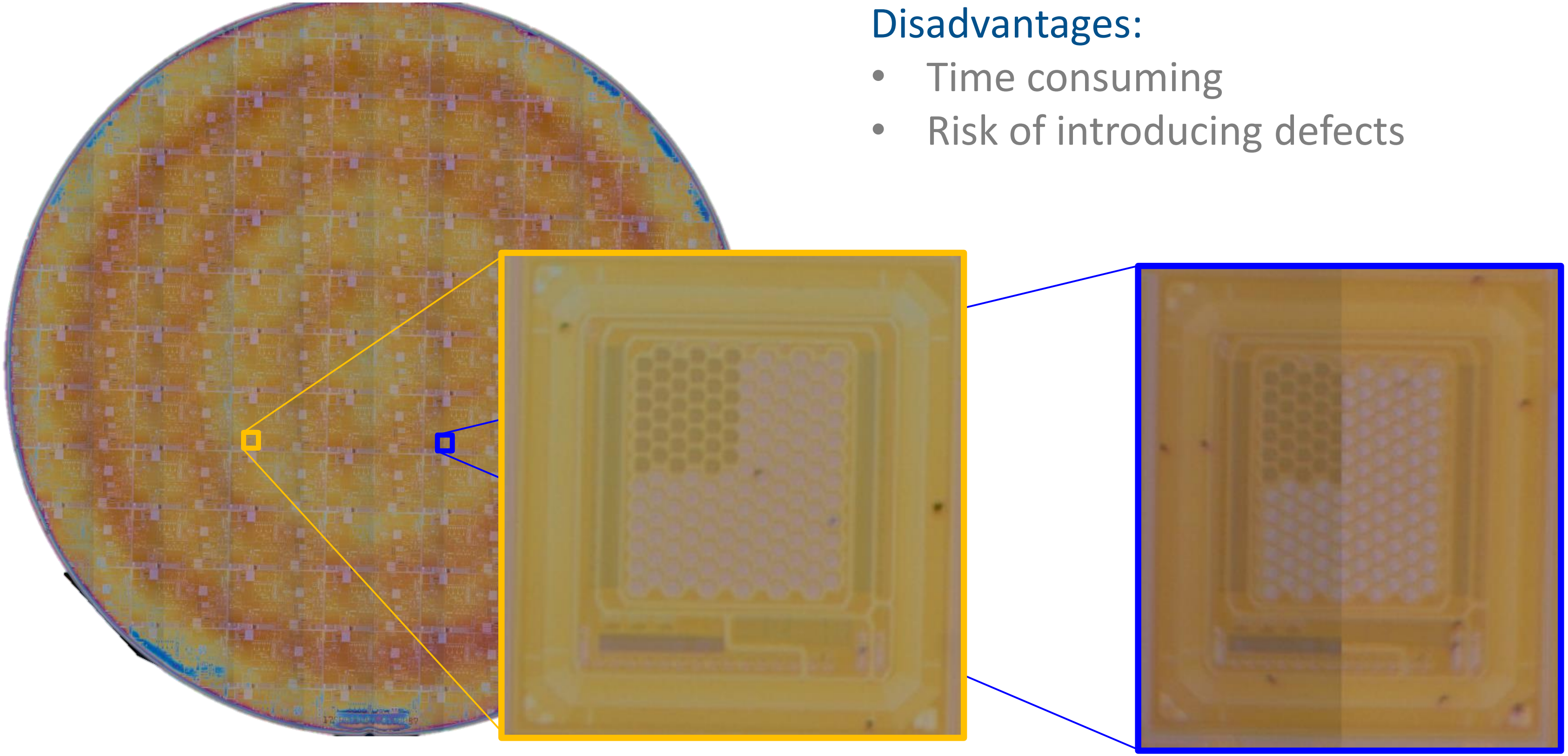


$$W_d \approx \left[\frac{2\epsilon_r\epsilon_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi-V})\right]^{1/2}$$

ATTRACT MONPicoAD: Epitaxies

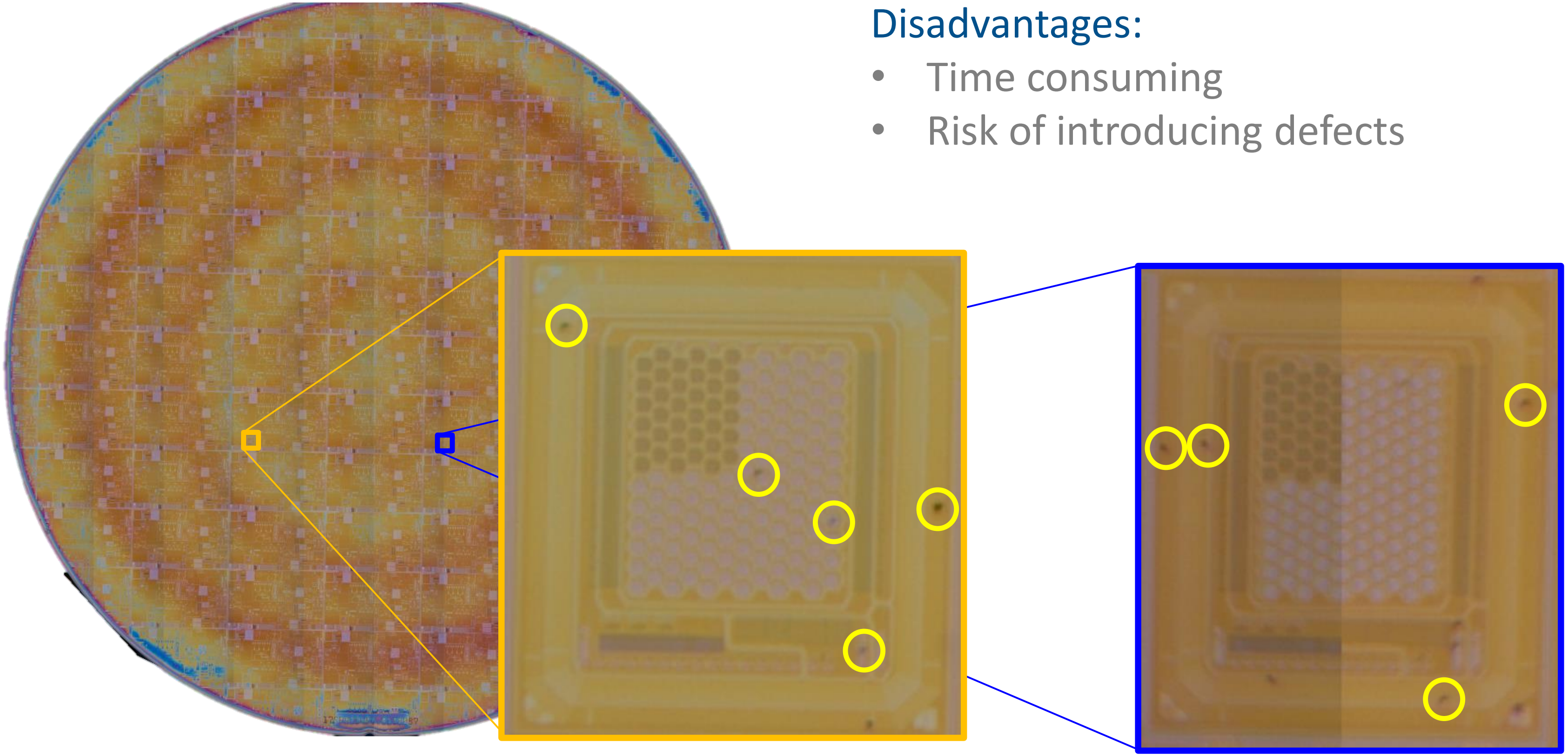
Disadvantages:

- Time consuming
- Risk of introducing defects



3.1 Experiments

ATTRACT MONPicoAD: Epitaxies

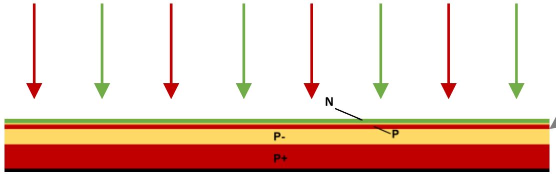


Disadvantages:

- Time consuming
- Risk of introducing defects

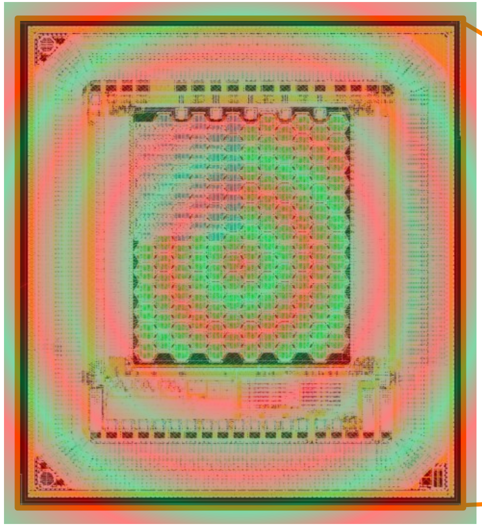
3.1 Experiments

ATTRACT MONPicoAD: Gain Layer



Gain layer implantation at the edge of the sensor

Cross section

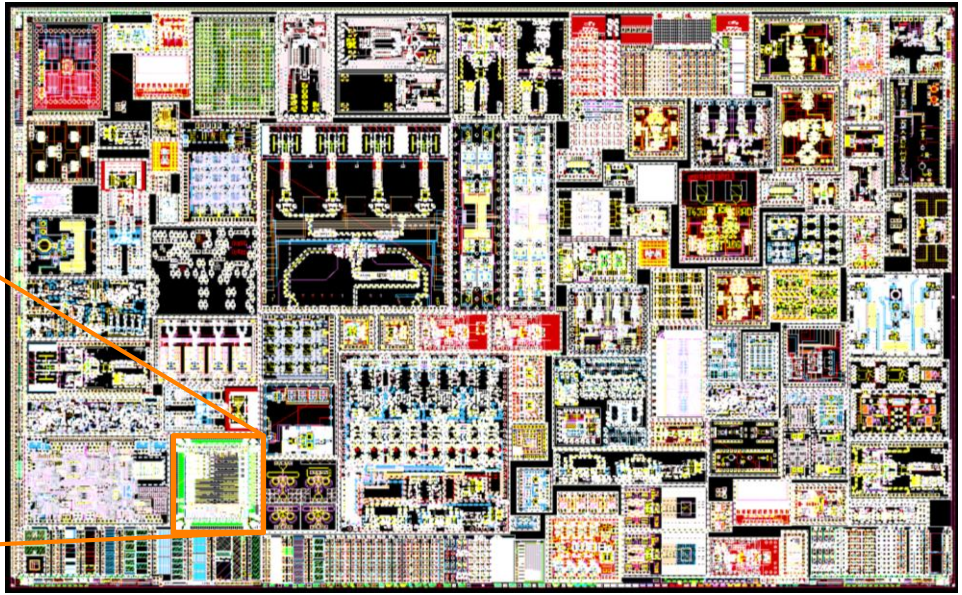


Top view

🟥 Implanted area

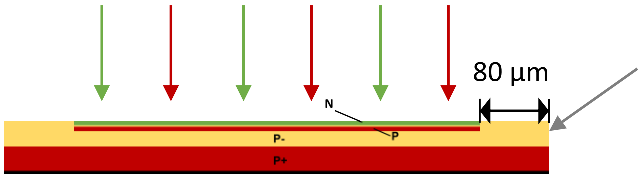
Challenges

- Direct junction between drift and gain region
  - Excess current in device may be produced



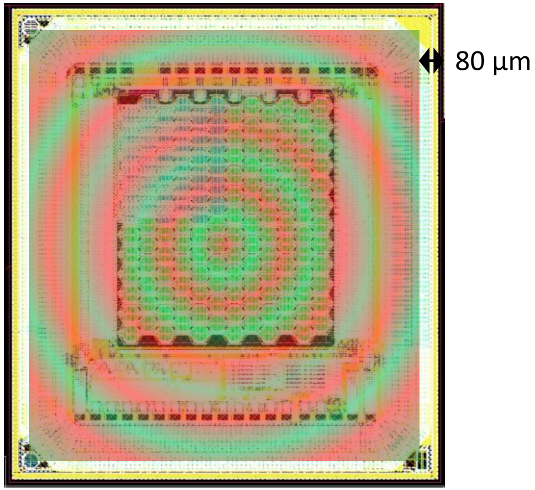
3.1 Experiments

ATTRACT MONPicoAD: Gain Layer



Gain layer implantation 80 µm far from edge of sensor

Cross section



Top view

▨ Implanted area

Challenges

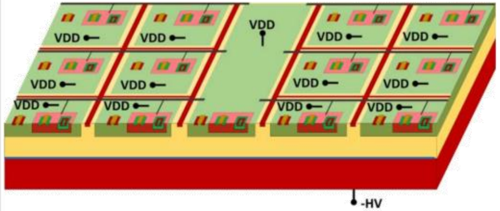
- Direct junction between drift and gain region
    - Excess current in device may be produced

Solution

- A mask is used for implantation
    - Gain layer ends 80 µm far from chip edge
    - Dedicated litho marks processed after 1st epi

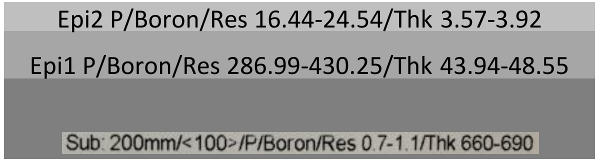
3.2 Experiments

FASER monolithic pixel sensor



Structure

- Heavily p-doped substrate
- ~46 µm thick epitaxial layer (ρ=200÷500 Ωcm)
- ~4 µm thick epitaxial layer (ρ=15÷25 Ωcm)



Epi2 P/Boron/Res 16.44-24.54/Thk 3.57-3.92

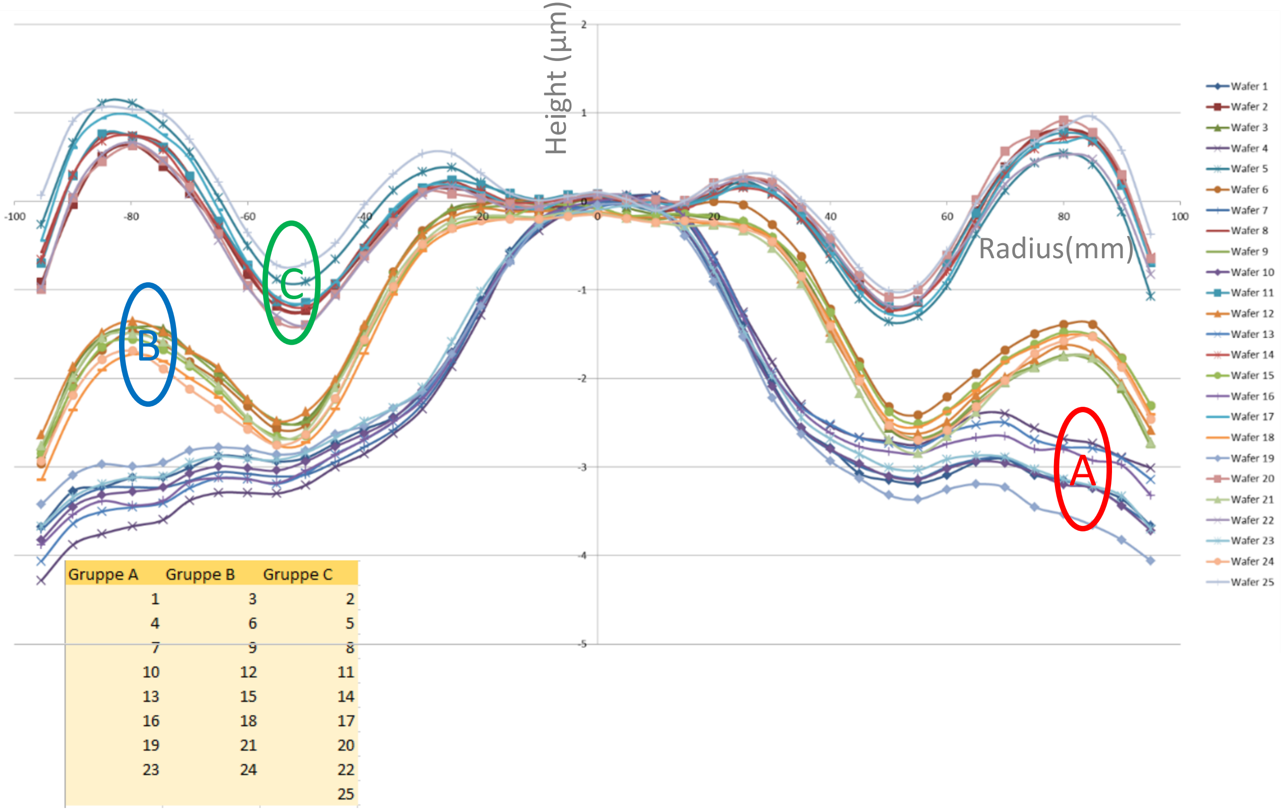
Epi1 P/Boron/Res 286.99-430.25/Thk 43.94-48.55

Sub: 200mm/<100>/P/Boron/Res 0.7-1.1/Thk 660-690

- Front-end electronics and pixels
- Metallization

3.2 Experiments

Challenges



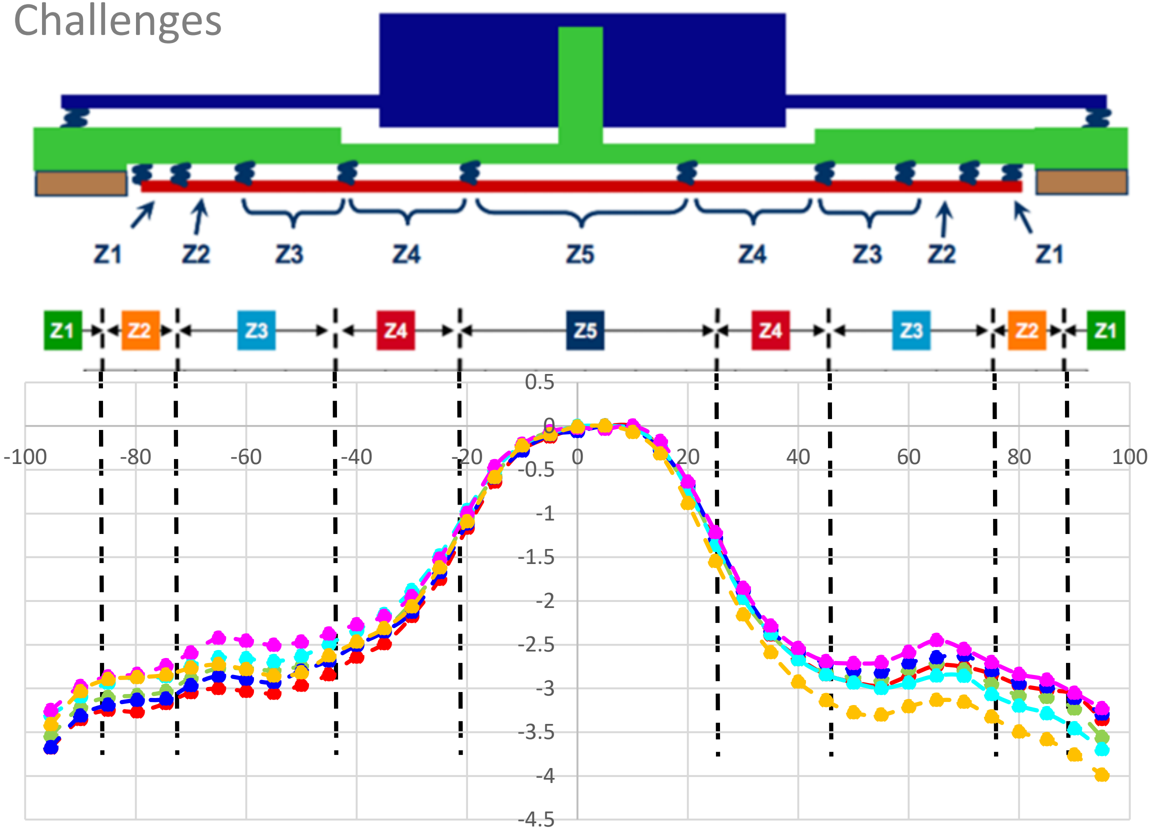
Gruppe A	Gruppe B	Gruppe C
1	3	2
4	6	5
7	9	8
10	12	11
13	15	14
16	18	17
19	21	20
23	24	22
		25

Global Wafer flatness

- measured through autofocus feature of Nikon litho tool
- 3 profile groups individuated
  - 3 AMAT Centura epi reactor chambers
- Not sufficient for litho processes of 130nm CMOS

3.2 Experiments

Challenges

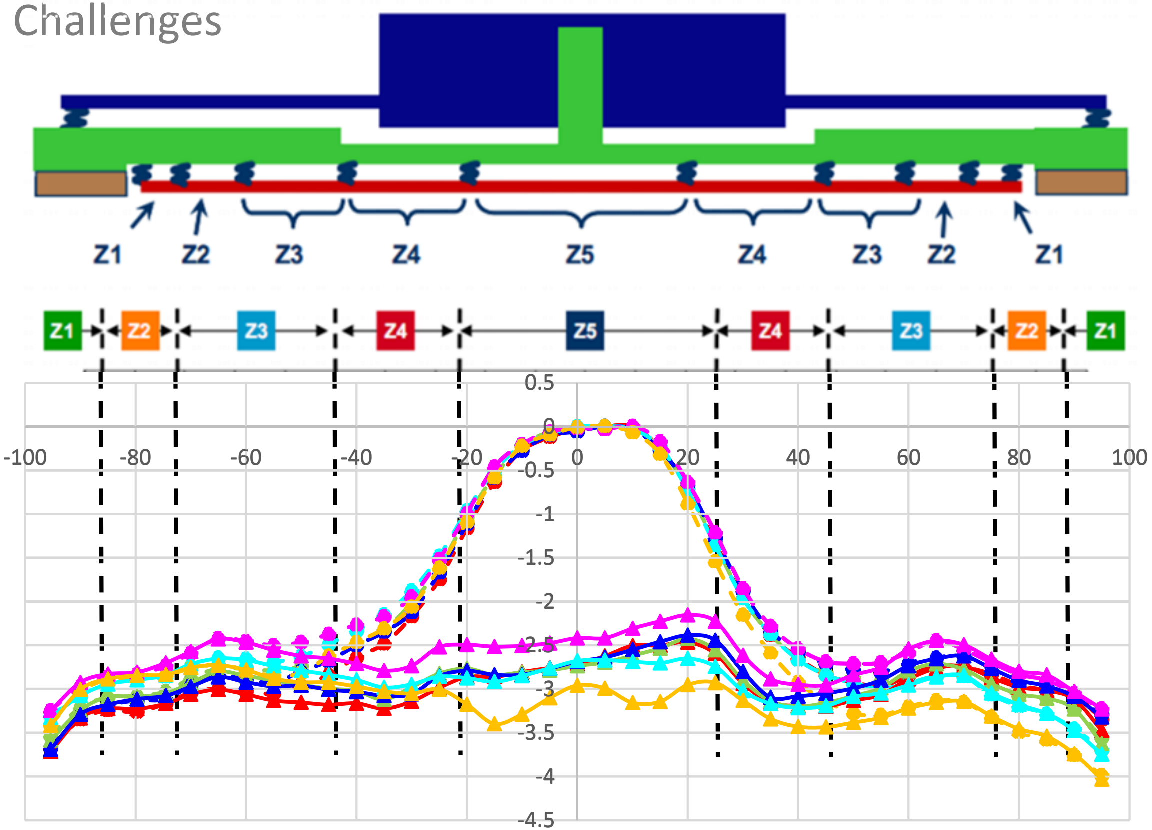


Chemical Mechanical Polishing

- Mirra Mesa from AMAT
  - 5 different pressure zones
  - Proper recipes for each zone

3.2 Experiments

Challenges



Outcome

- PCM Measurements in spec

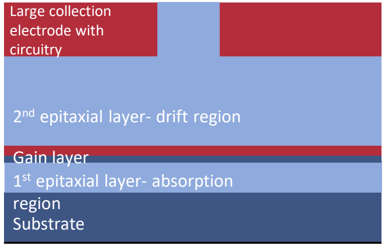
Solution

- Better epi homogeneity
  - wafer-to-wafer
    - only one chamber
  - across-wafer
    - Thinner epi layer

3.3 Experiments

MONOLITH

PicoAD sensor



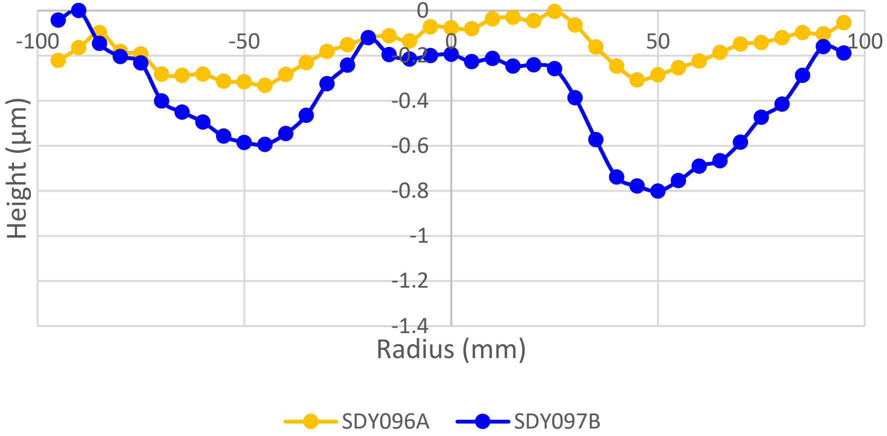
GLOBITECH
DESIGNING EPI SOLUTIONS

Structure

- Heavily p-doped substrate
- 3÷5 µm thick epitaxial layer (absorption region)
- Masked gain Layer (no litho marks)
- 15÷25 µm epitaxial layer (drift region)
- IHP 130 nm SiGe BiCMOS front-end electronics and pixels
- Metallization

3.3 Experiments

PicoAD sensor: Epitaxies



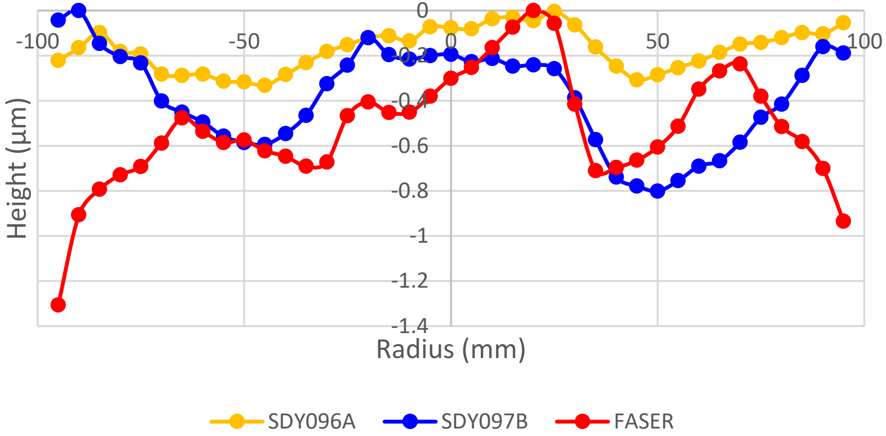
1^{st} Epi (µm)	2^{nd} Epi (µm)	Name
3	15	SDY096A
	25	SDY096B
5	15	SDY097A
	25	SDY097B

Global Wafer Flatness

- Thinnest epitaxies (1^{st}=3µm; 2^{nd}=15µm)
  - Most critical slope of 18.2 nm/mm
- Thickest epitaxies (1^{st}=5µm; 2^{nd}=25µm)
  - Most critical slope of 49.6 nm/mm

3.3 Experiments

PicoAD sensor: Epitaxies



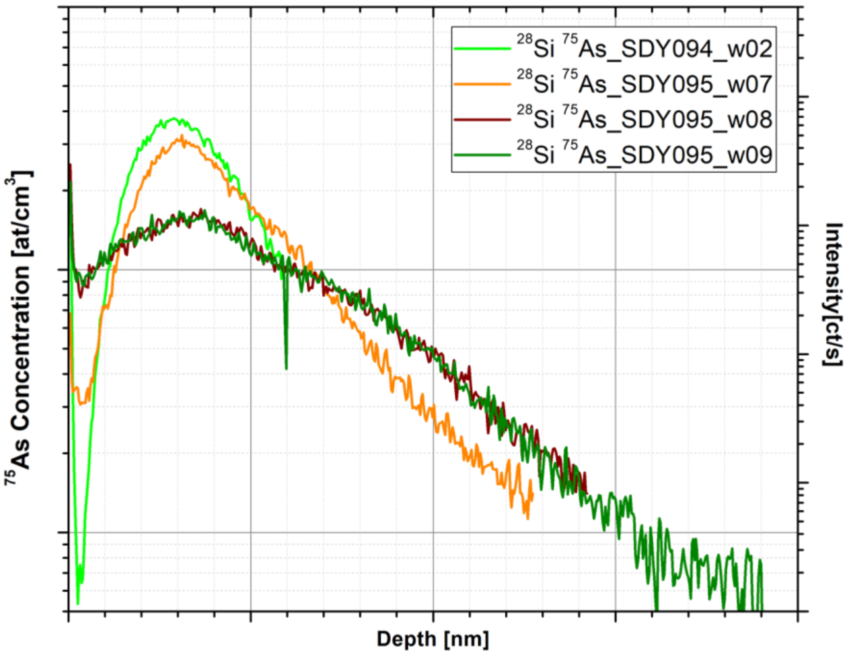
1st Epi (µm)	2nd Epi (µm)	Name
3	15	SDY096A
	25	SDY096B
5	15	SDY097A
	25	SDY097B
50	--	FASER

Global Wafer Flatness

- Thinnest epitaxies (1st=3µm; 2nd=15µm)
  - Most critical slope of 18.2 nm/mm
- Thickest epitaxies (1st=5µm; 2nd=25µm)
  - Most critical slope of 49.6 nm/mm
- FASER succesfully processed wafer
  - Most critical slope of 65.9 nm/mm

3.3 Experiments

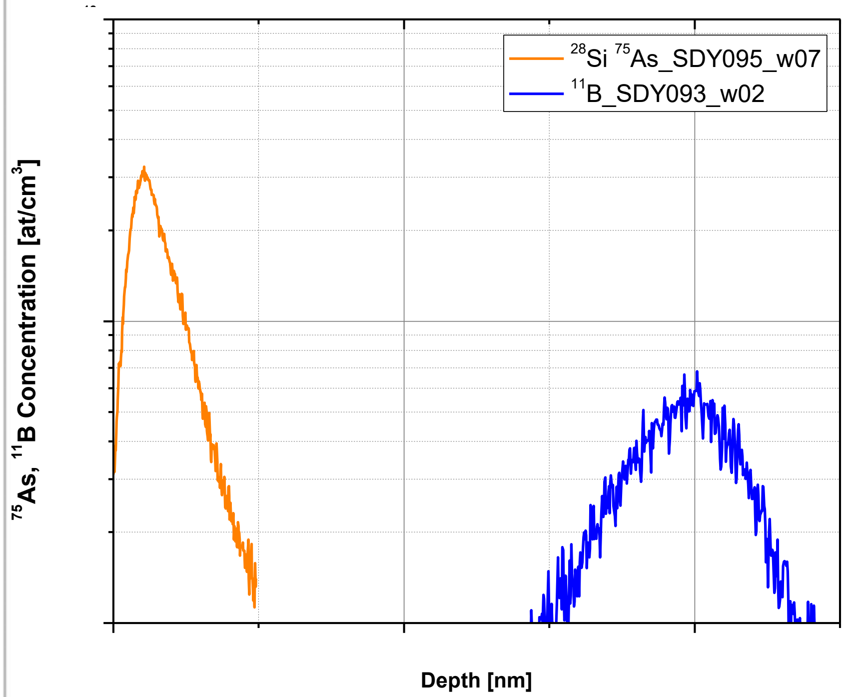
PicoAD sensor: Gain Layer



Constraints

- As surface concentration
  - Upper limit
    - Globitech requirement (reactor chamber contamination)
  - Lowest possible
    - To minimize outdiffusion

PicoAD sensor: Gain Layer



Constraints

- As surface concentration
  - Upper limit
    - Globitech requirement (reactor chamber contamination)
  - Lowest possible
    - To minimize outdiffusion
- Upper limit in energy for the B implantation

3.3 Experiments

PicoAD sensor: Gain Layer

15um 2nd epi:

Thickness 2nd epi	Thickness 1st epi	As gain layer doses name	Lot	Slots (as processed)	Zeilen
15um (25 w)	3um (12 w)	3	SDY096	W01-06	1,4,7,10
		3.5			2,5,8,11
		4 (6 w)			3,6,9
		2.5		W07-12	1,4,7,10
		2.5			2,5,8,11
		4.5 (6 w)			3,6,9
	5um (13 w)	3	**SDY097**	**W01-07**	**1,4,7,10**
		3.5			**2,5,8,11**
		4 (7 w)			**3,6,9**
		2.5		**W08-13**	**1,4,7,10**
		2.5			**2,5,8,11**
		4.5 (6 w)			**3,6,9**

25um 2nd epi:

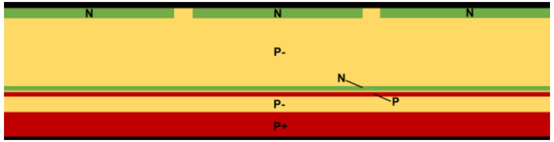
Thickness 2nd epi	Thickness 1st epi	As gain layer doses name	Lot	Wafers	Zeilen
25um (24 w)	3um (12 w)	4	SDY096	W13-18	1,4,7,10
		4.5			2,5,8,11
		5 (6 w)			3,6,9
		3.5		W19-24	1,4,7,10
		3.5			2,5,8,11
		4.75 (6 w)			3,6,9
	5um (12 w)	4	SDY097	W14-19	1,4,7,10
		5			2,5,8,11
		5 (6 w)			3,6,9
		3.5		W20-25	1,4,7,10
		3.5			2,5,8,11
		4.75 (6 w)			3,6,9

49 Wafers

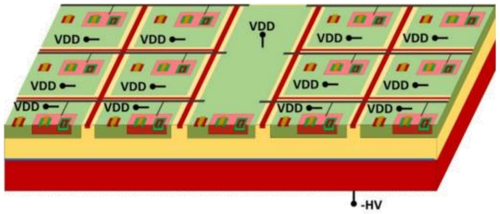
- 25 wafers -> 15 µm 2nd epi
    - 12 wafers -> 3 µm 1st epi
    - 13 wafers -> 5 µm 1st epi
        - 3 gain layer variants each wafer
- 24 wafers -> 25 µm 2nd epi
    - 12 wafers -> 3 µm 1st epi
    - 12 wafers -> 5 µm 1st epi
        - 3 gain layer variants each wafer

4 Conclusion

[2]



[4]



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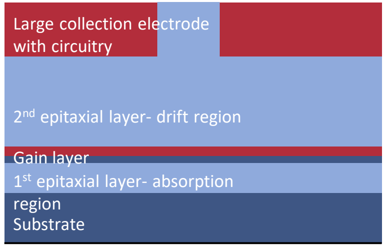

Outcomes

1st prototype fabrication

Functional chips delivered

Very promising results [2, 5]

Functional chips delivered

Manually controlled CMP needed

Measurements ongoing

Currently tested in a particle beam

Globitech epitaxy can be exploited up to 25 µm

Alignment accuracy limited to ~100 µm

BiCMOS process yet to be started

Thank you for your attention!

Elviretti, Matteo

IHP – Leibniz-Institut für innovative Mikroelektronik
Im Technologiepark 25
D – 15236 Frankfurt (Oder)
Phone: +49 (0) 335 5625 346
Fax: +49 (0) 335 5625
e-mail: elviretti@ihp-microelectronics.com

www.ihp-microelectronics.com

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Bibliography

[1] – Carulla, M., et al. "50µm thin Low Gain Avalanche Detectors (LGAD) for timing applications." Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 924 (2019): 373-379.

[2] – Paolozzi, L., et al. "Picosecond Avalanche Detector--working principle and gain measurement with a proof-of-concept prototype." arXiv preprint arXiv:2206.07952 (2022).

[3] – Münker, M. on behalf of the MONOLITH team «Picosecond time stamping in fully monolithic highly granular silicon pixel detectors” – TRENTO workshop, March 2022

[4] – Paolozzi, Lorenzo, Giuseppe Iacobucci, and Pierpaolo Valerio. "Fast pixel sensors for ionizing particles integrated in SiGe BiCMOS." 2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). IEEE, 2020.

[5] – Iacobucci, G., et al. "Efficiency and time resolution of monolithic silicon pixel detectors in SiGe BiCMOS technology." Journal of Instrumentation 17.02 (2022): P02019.

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