Angelo Rivetti

Some INFN projects on fast electronics…

…in which I'm (marginally) involved!

Overview

- Fast timing electronics for
  - Hybrid pixels
  - LGAD
  - SiPM
  - CMOS sensors

Front-end for LGADs - 1

The FAST project

In the past 5 years, the Torino UFSD group has been working on the development of ASIC tailored to readout UFSD sensors with about 2 pF of capacitance.
The first two ASICs have been:

1. ABACUS [1] (Asynchronous logic Based Analog Counter for Ultra fast silicon Strips)
2. TOFFEE [2] (Time Of Flight Front End readout Electronics).

Leveraging on these first 2 ASICs, the family of FAST (Front-end Amplifiers for Silicon detectors in Timing applications) ASICS was designed.

N. Cartiglia, F. Fausti, J. Olave, A. Martinez

Front-end for LGADs - 2

The FAST Architecture

FAST is designed in **a commercial 110 nm CMOS technology**, specifically optimized for UFSD of 3-6 pF in a temperature range between -30 and +50 Celsius degrees. FAST has been developed with particular attention to **reducing the power consumption** by a factor 10 compared with the previous ASICs.

The channel architecture consists of a Trans-Impedance Amplifier (TIA) and a second amplification stage based on a common source amplifier (CS). This first part is followed by a two stages leading edge discriminator with Pulse Width Regulator (PWR) to tune the digital output duration and an LVDS driver.

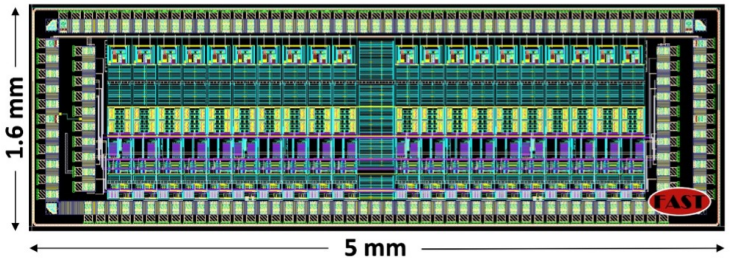
The latest version, FAST3, comes in 3 flavours (delivery Q4/2022):

- FAST3_A: A 16 channels ASIC, with analogue output (no discriminator stage)
- FAST3_D: A 20-channel ASIC with an amplifier and discriminator stage, with discriminated output
- FAST3_ALCOR: A 32-channel ASIC, includes the optimized front-end stage used in FAST3_A, a discriminator stage, time to digital converter (TDC), and a digital control unit reaching a time resolution lower than 40 ps.

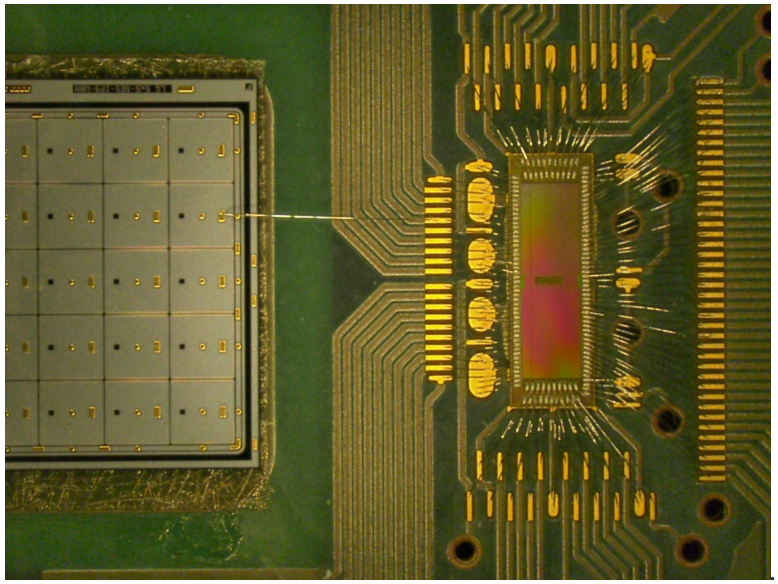
Single channel details:

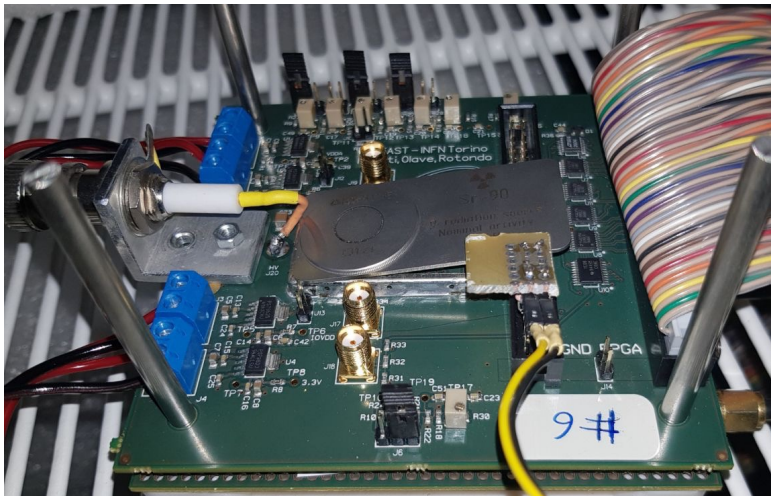
- Power limited to 1.5 mW/ch
- Designed for 1 proton MIP in 50 µm thick UFSD sensor
- Sensor cap: 1 pF – 6 pF
- bandwidth: ~ 400 MHz
- Gain: ~ 31mV/fC(8 regulations)
- Noise: ~ 640e-
- SNR(MIP): ~ 75
- Max hit rate: 300 MHz

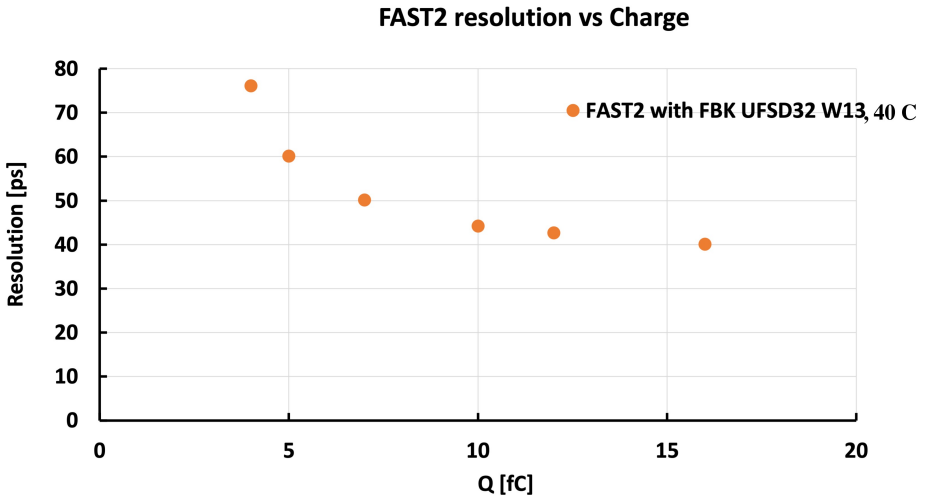
FAST3_A and FAST3_D



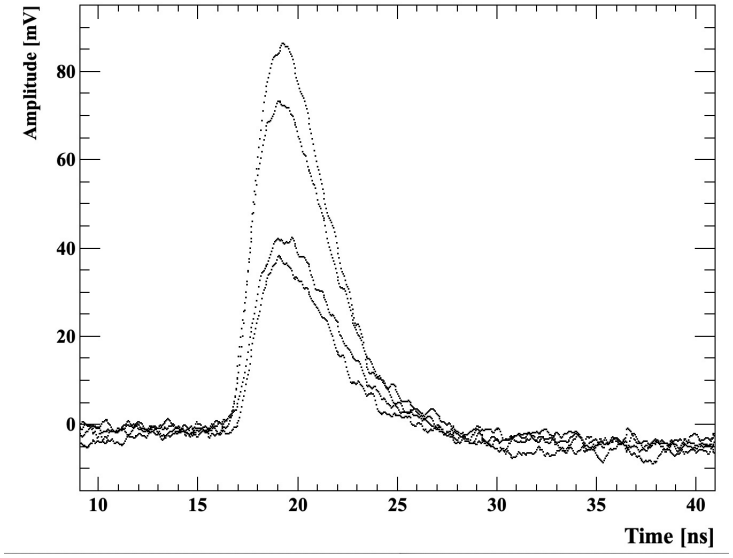
Front-end for LGADs - 3



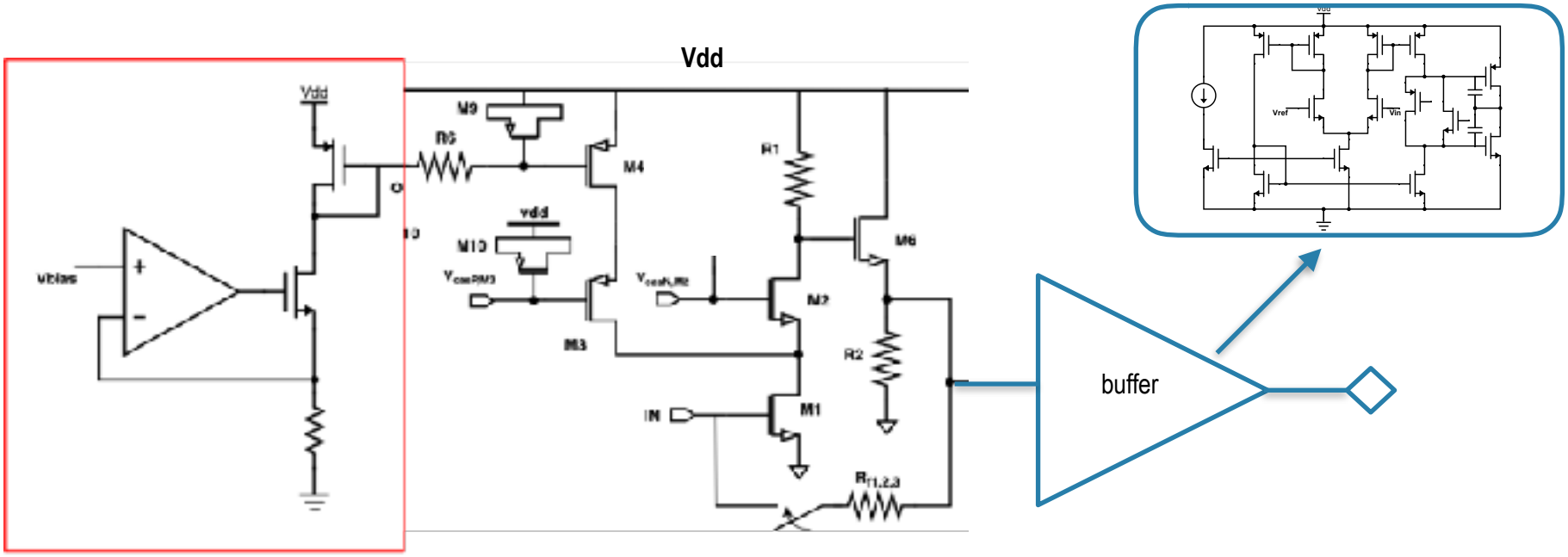




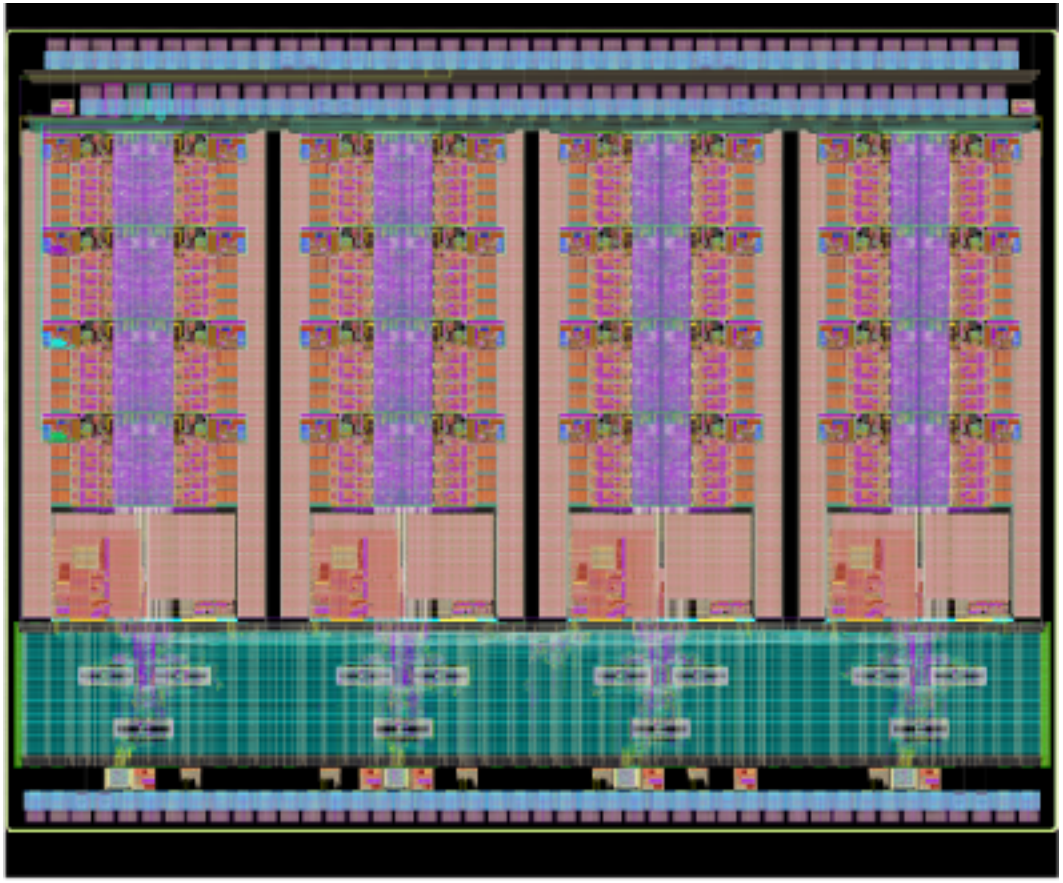
Experimental time resolution of UFSD + FAST2 system using the beta telescope br90 (Landau uncertainy).



Front-end for LGADs - 4



Including also TDC…



UMC 110 nm, now in production

Timing with CMOS sensors

- Attract FastPix
- ALICE ITS3 (C. Ferrero)
- LF 110 nm (ARCADIA project

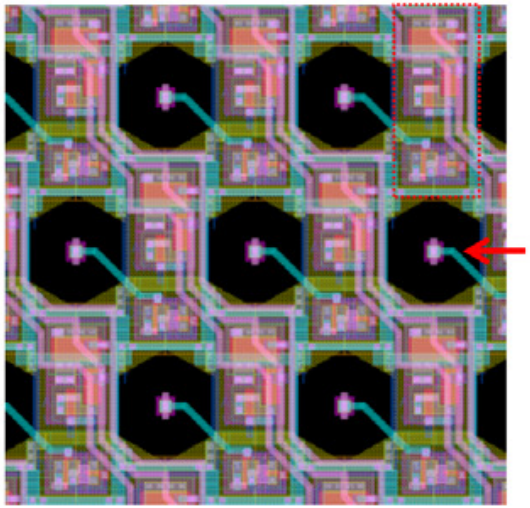
ATTRACT FastPix

Monolithic CMOS sensors for sub-nanosecond timing

Thanushan Kugathasan [a,*], Taeko Ando [b], Dominik Dannheim [a], Takeharu Goji Etoh [b], Magdalena Munker [a], Heinz Pernegger [a], Angelo Rivetti [c], Kazuhiro Shimonomura [b], Walter Snoeys [a]

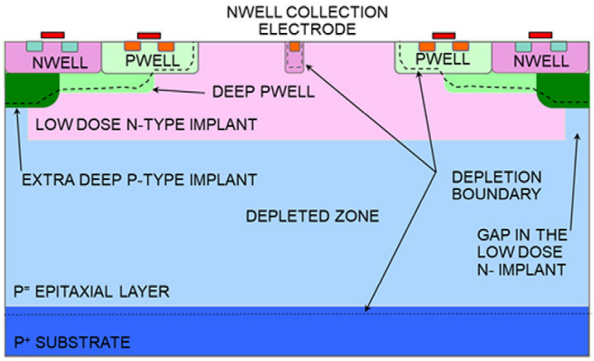
[a] *CERN, Geneva, Switzerland*
[b] *Ritsumeikan University, Kyoto, Japan*
[c] *INFN, Torino, Italy*

Pixel in the matrix



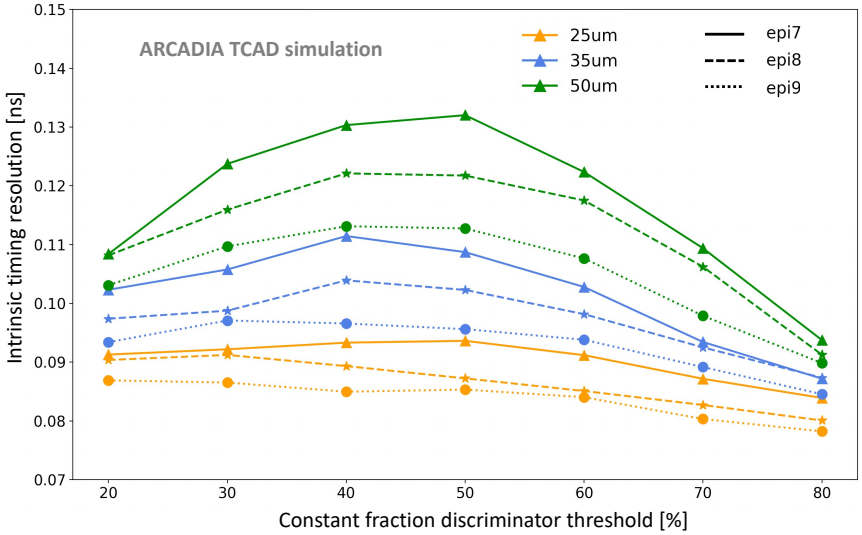
5 PMOS per pixel

n-well electrode

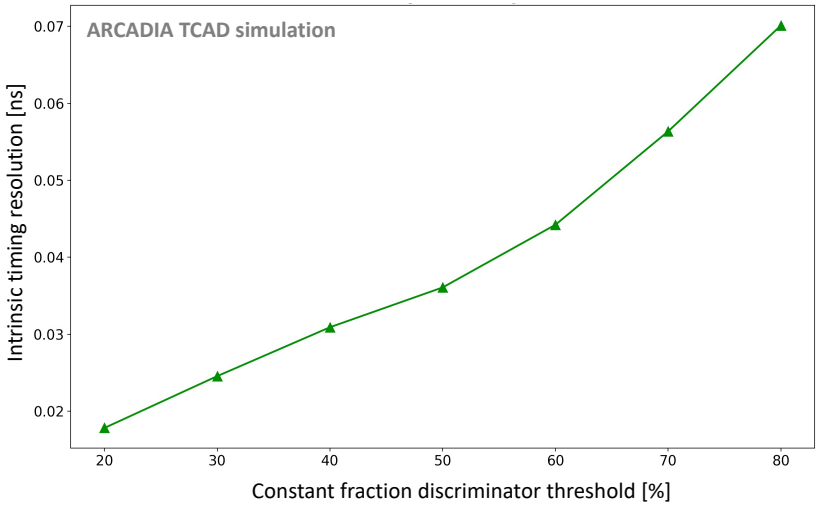


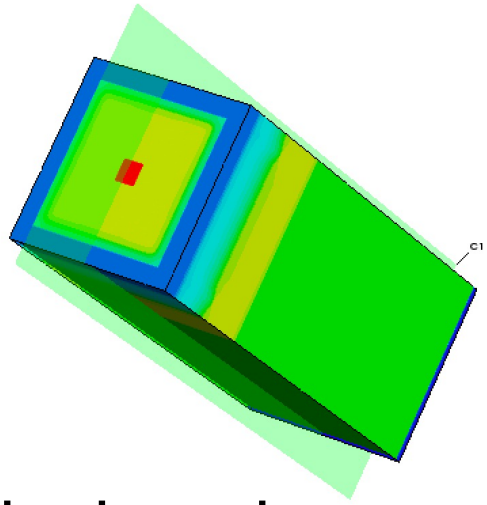
Small and large electrodes

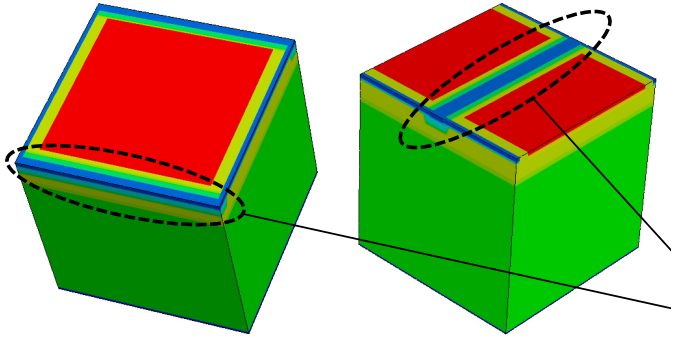
- **Studies done in the preparation of the ALIC3 LoI**



Large collection electrode



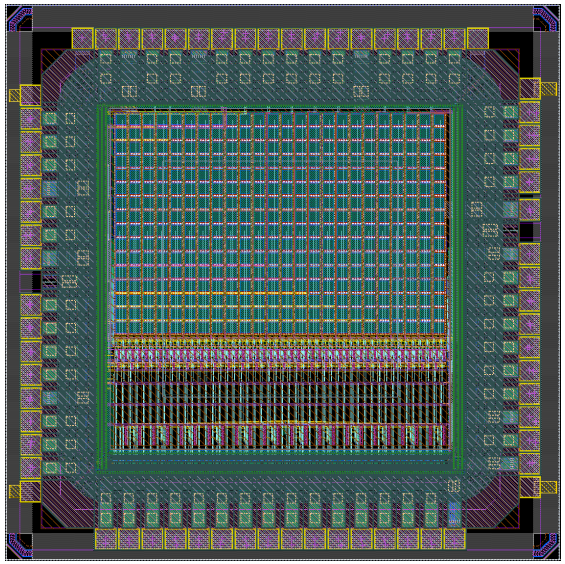




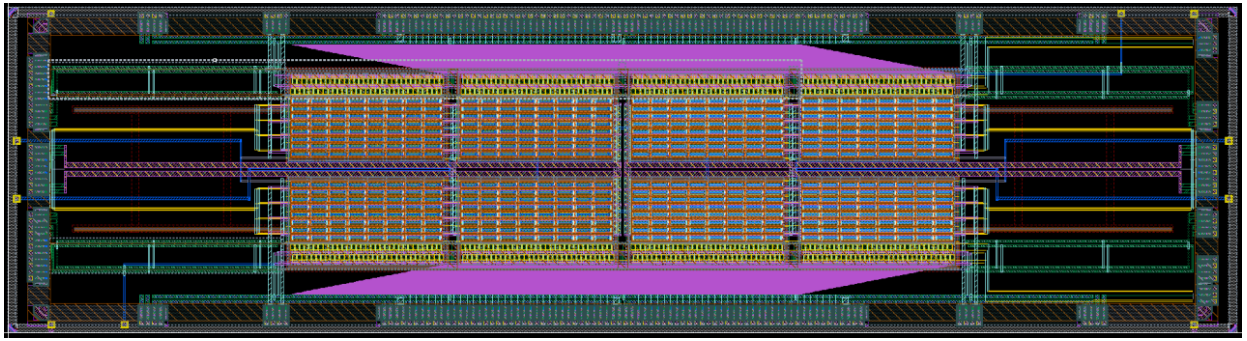
- **L. Pancheri and coworkers**

In LF 110 nm

- Without gain

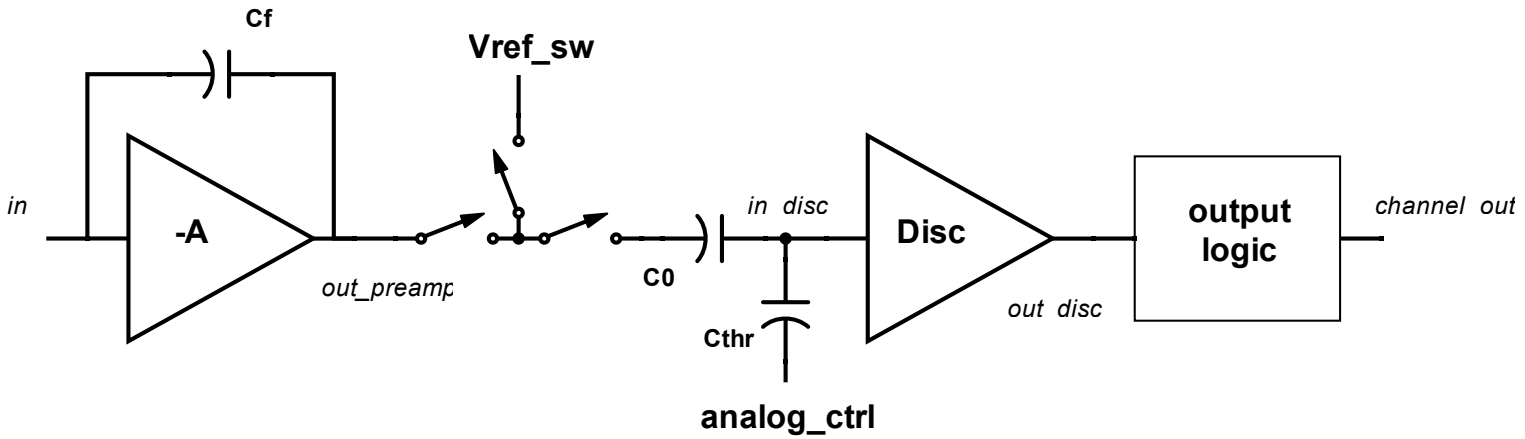


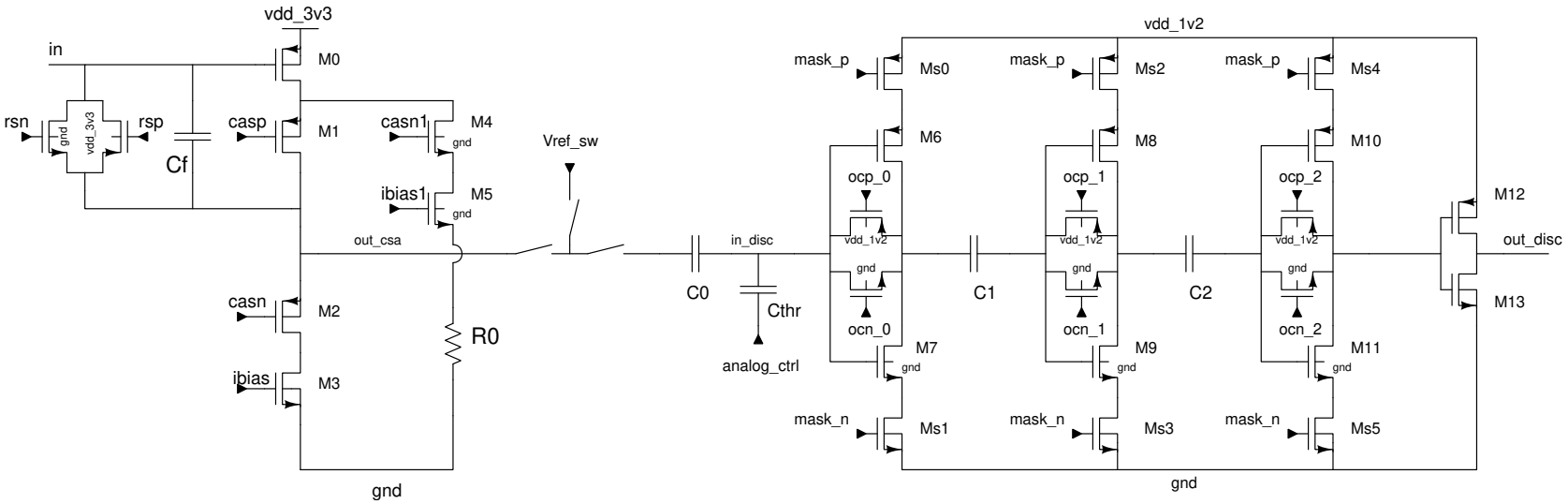
- With gain



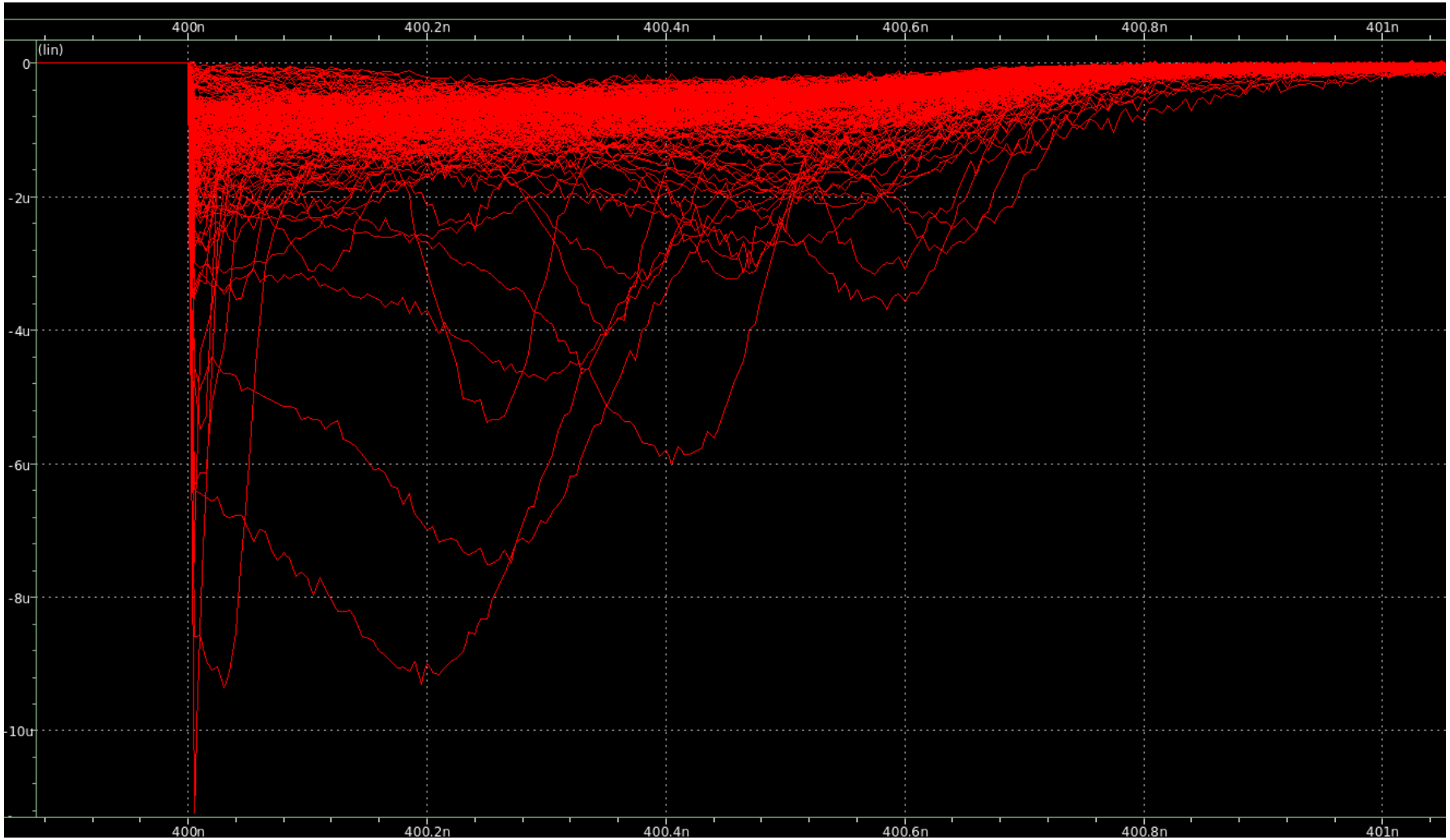
- Both in production, to be tested soon

Front-end for no-gain sensors

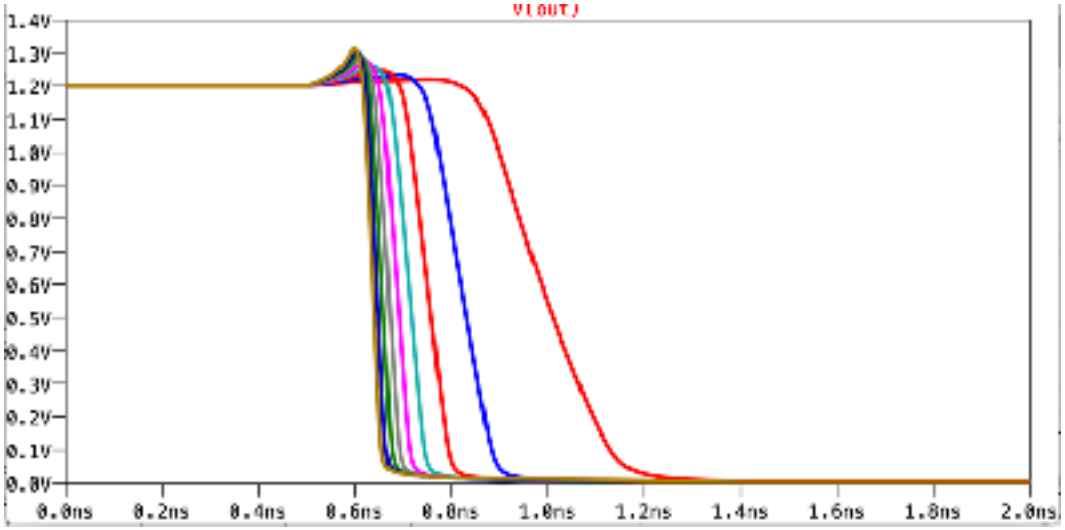


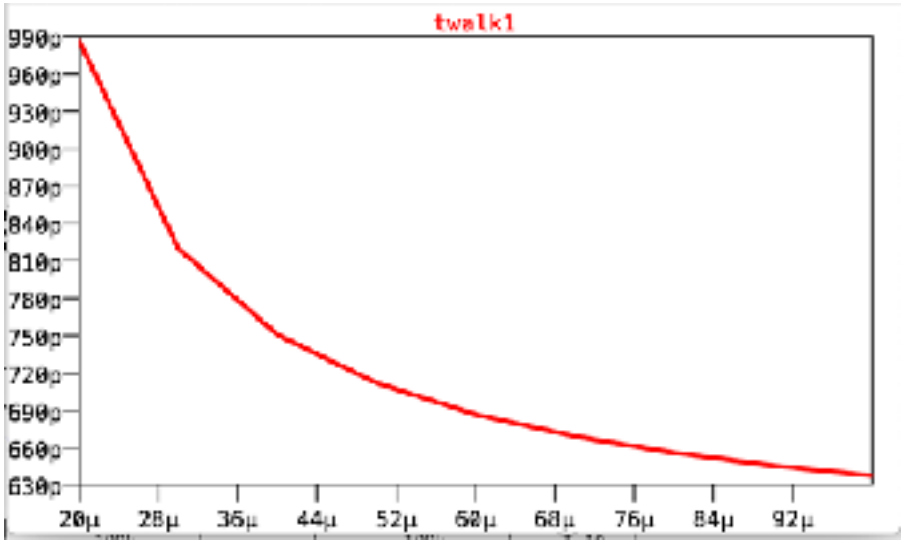


Signal samples

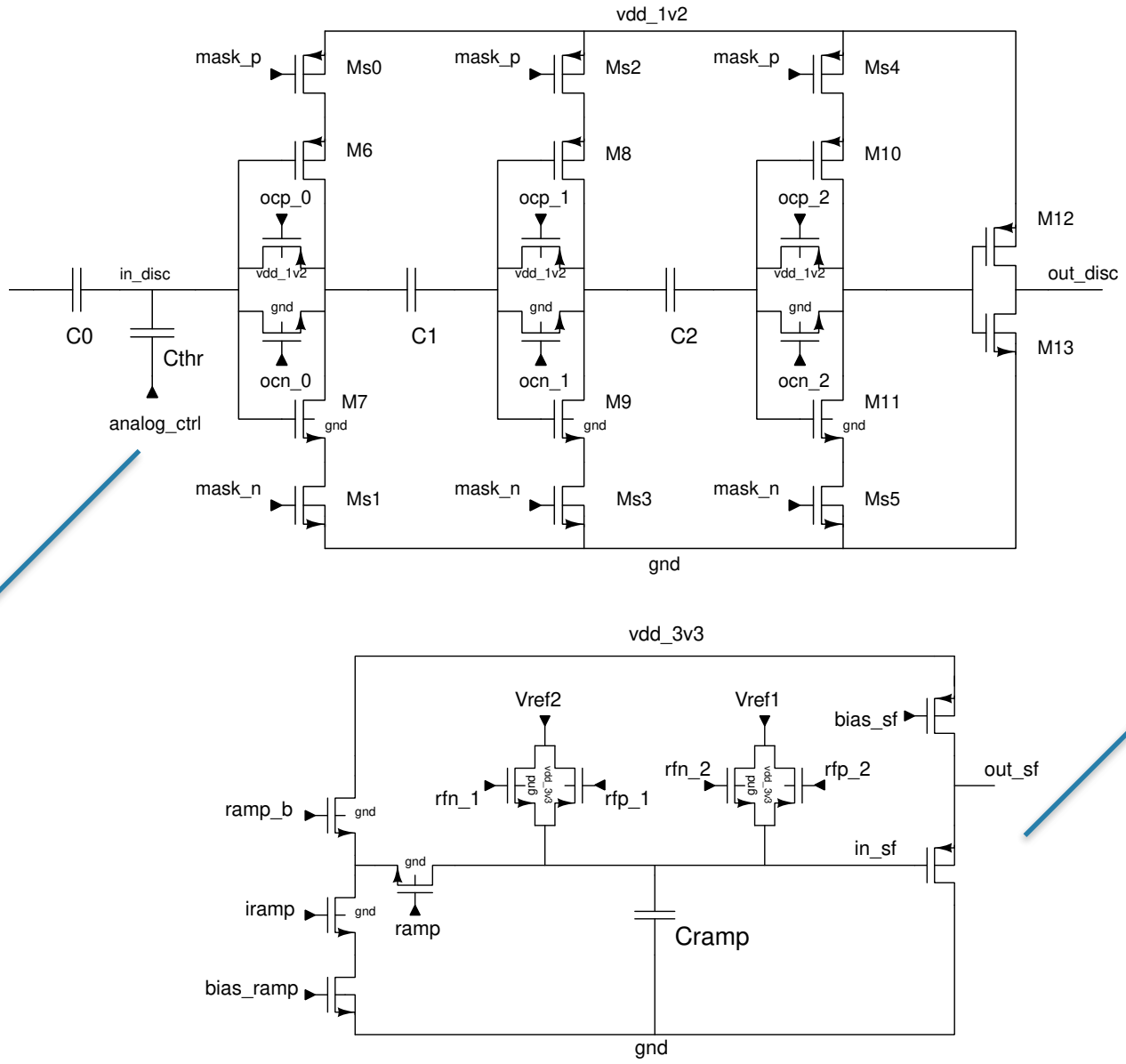


Even inverters have time walk

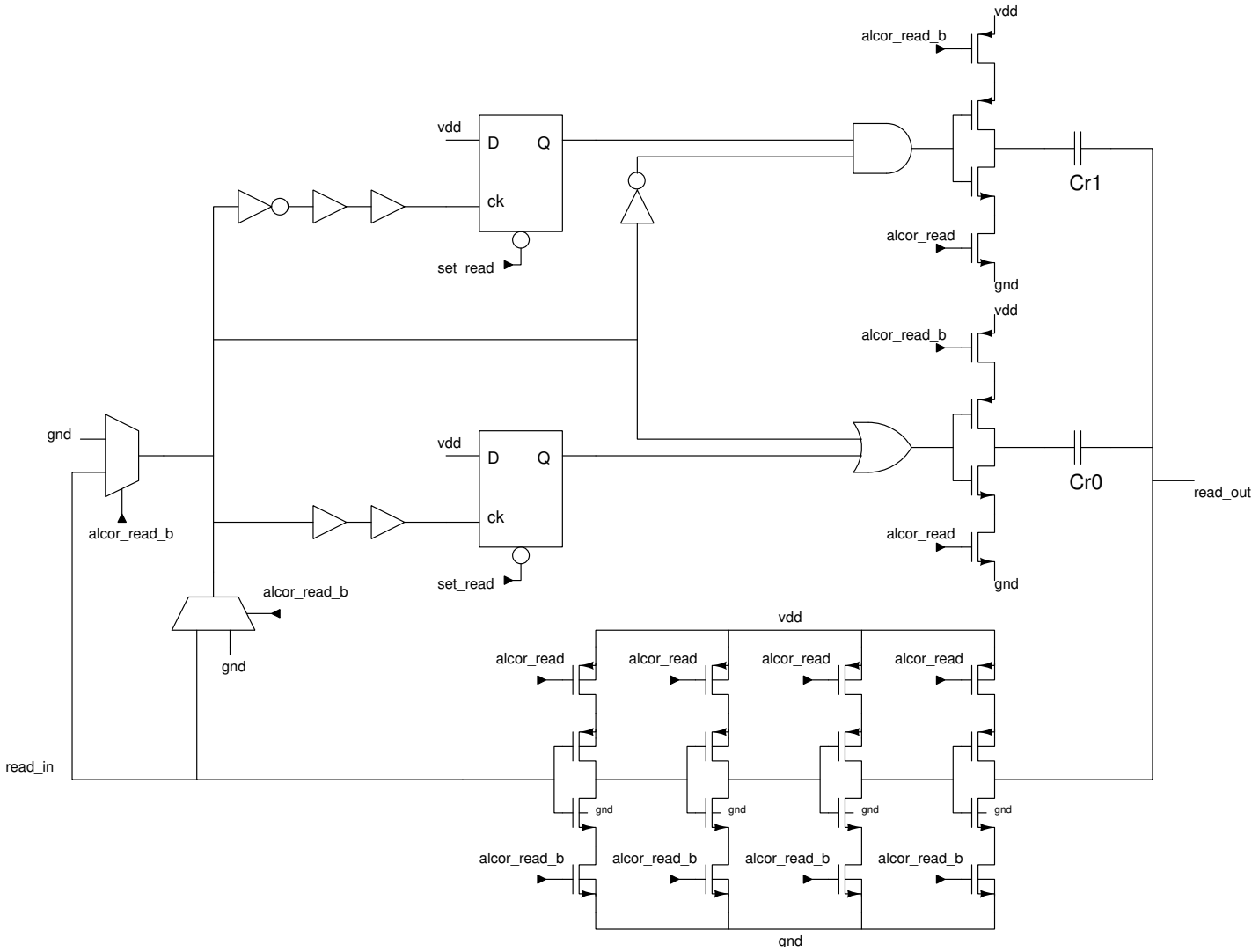




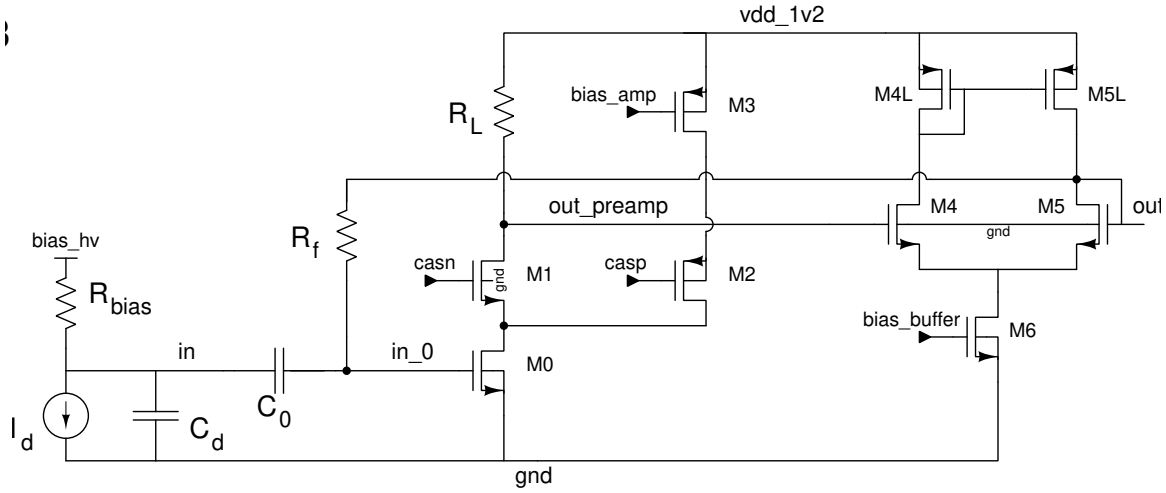
Time-walk correction

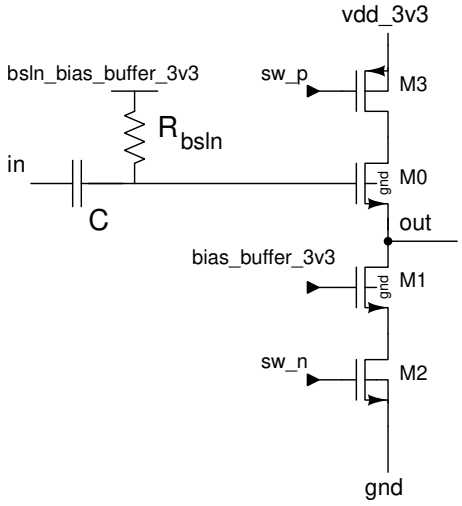


Output stage



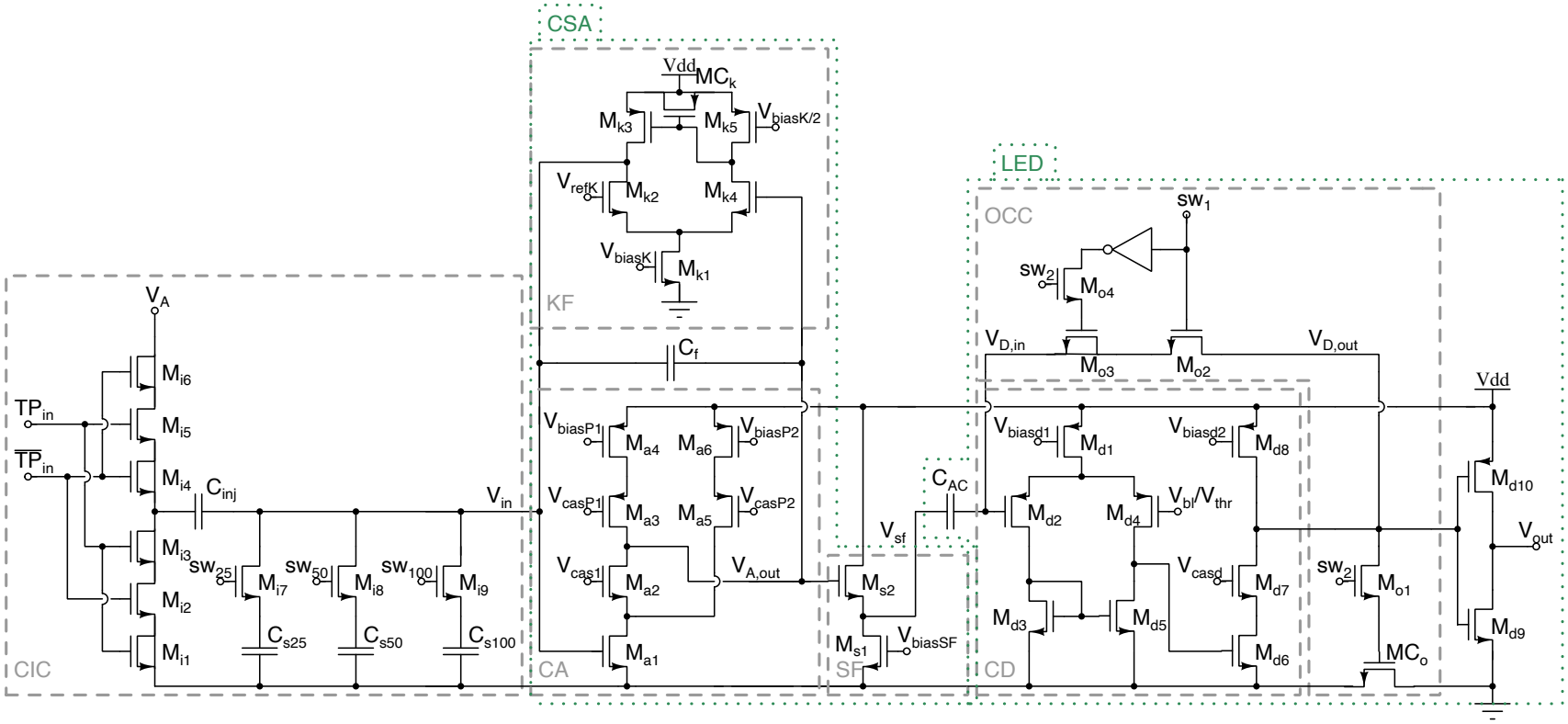
Front-end for sensors with gain





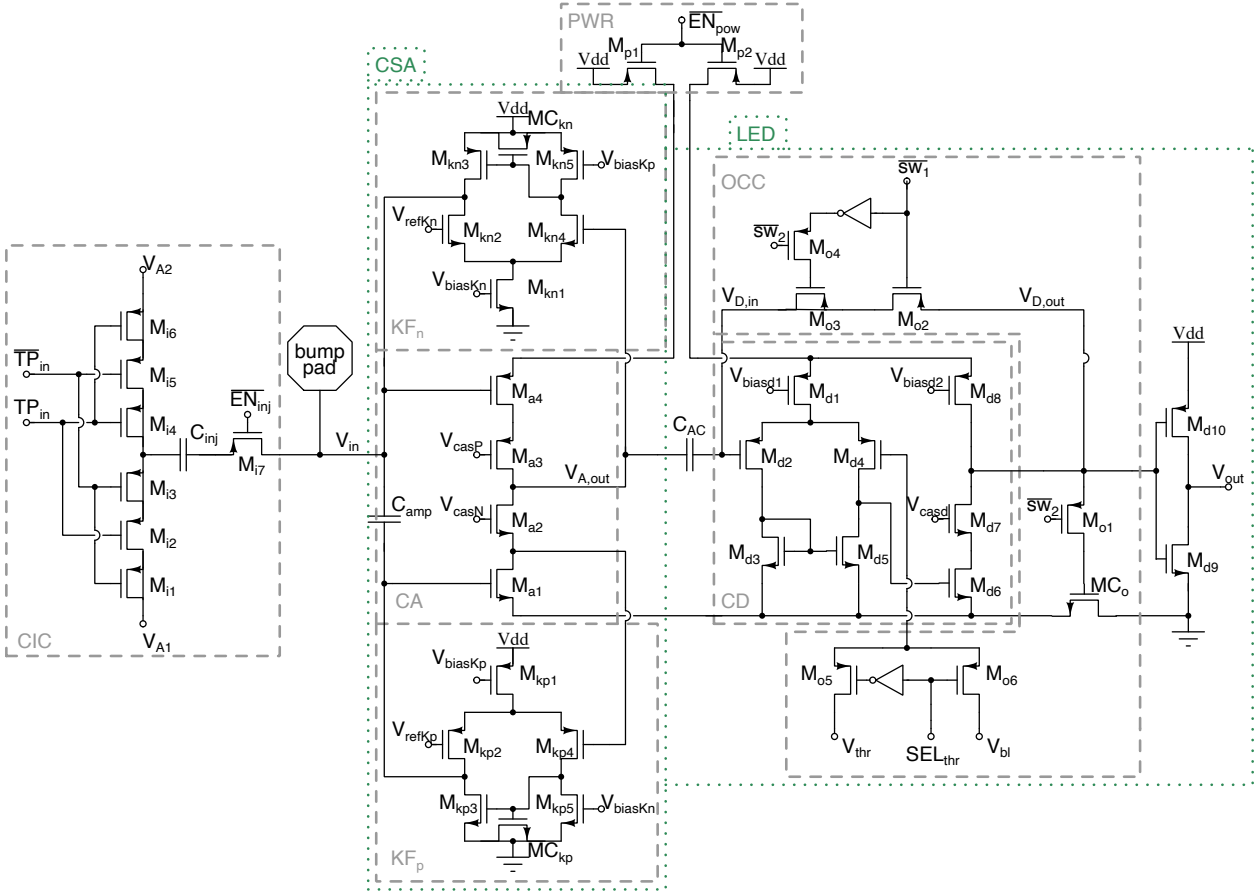
Back to hybrids

- **TimeSpot FE version 1 (L. Piccolo et al.)**



Back to hybrids

- **TimeSpot FE version 2 (L. Piccolo et al.)**

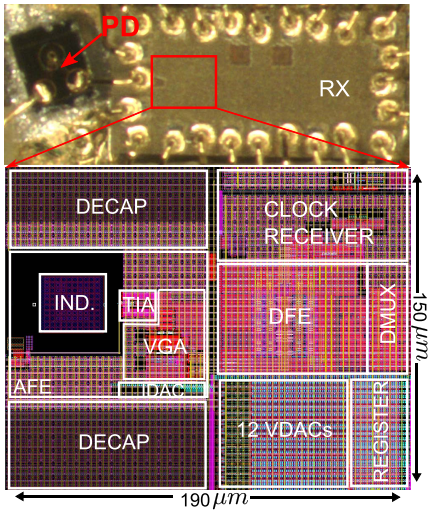


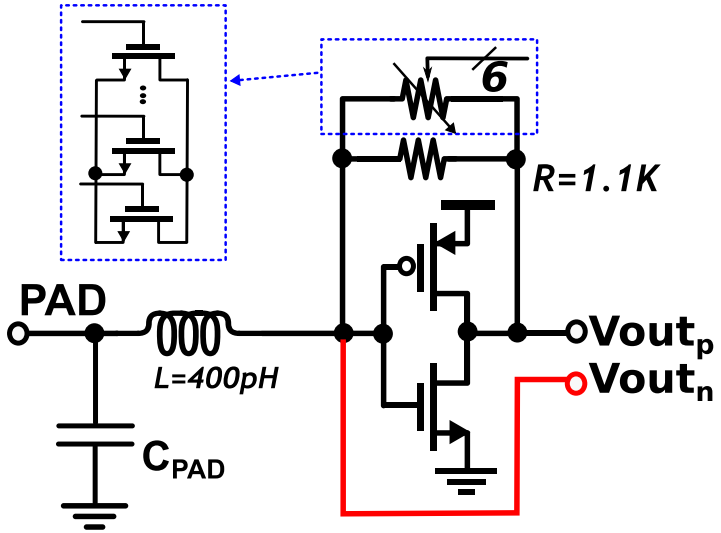
Can we exploit the signal rise time?

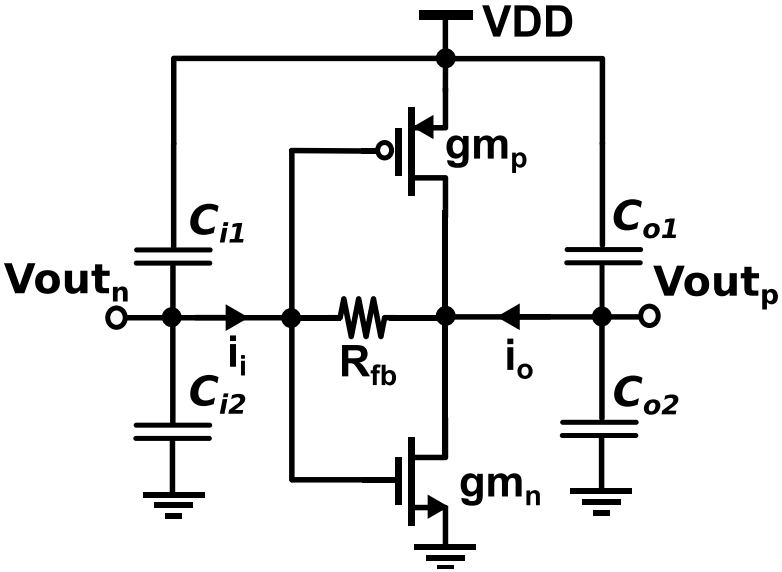
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 12, DECEMBER 2017

A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

Ilter Ozkaya, *Student Member, IEEE*, Alessandro Cevrero, *Member, IEEE*, Pier Andrea Francese, *Senior Member, IEEE*, Christian Menolfi, *Member, IEEE*, Thomas Morf, *Senior Member, IEEE*, Matthias Brändli, Daniel M. Kuchta, *Senior Member, IEEE*, Lukas Kull, *Senior Member, IEEE*, Christian W. Baks, Jonathan E. Proesel, *Senior Member, IEEE*, Marcel Kossel, *Senior Member, IEEE*, Danny Luu, *Student Member, IEEE*, Benjamin G. Lee, *Senior Member, IEEE*, Fuad E. Doany, Mounir Meghelli, *Member, IEEE*, Yusuf Leblebici, *Fellow, IEEE*, and Thomas Toifl, *Senior Member, IEEE*



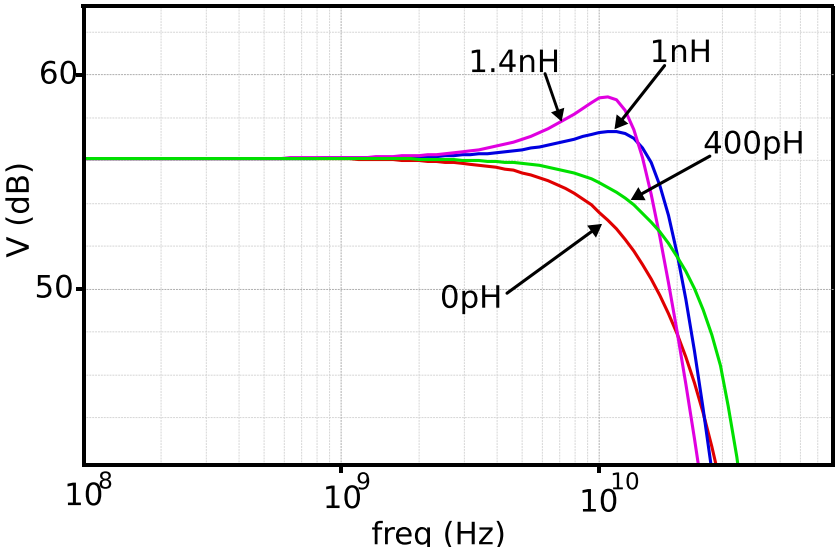


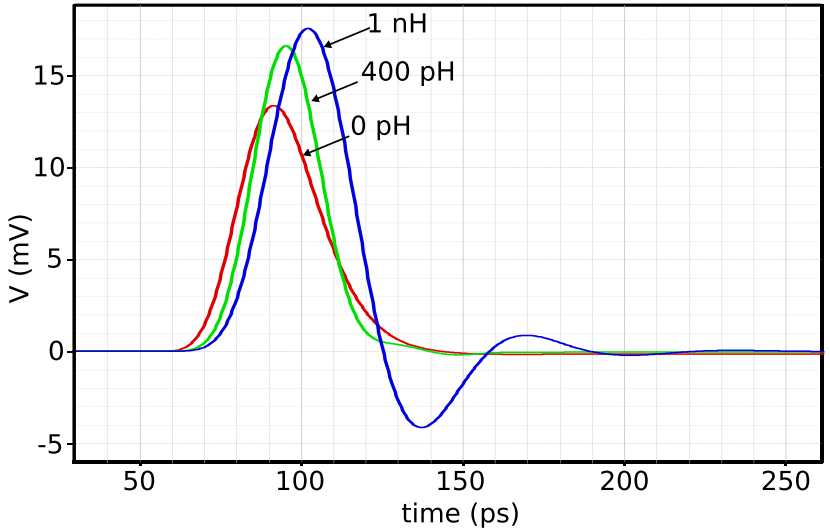


Front-end with 25 ps peaking time!?

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 12, DECEMBER 2017

A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

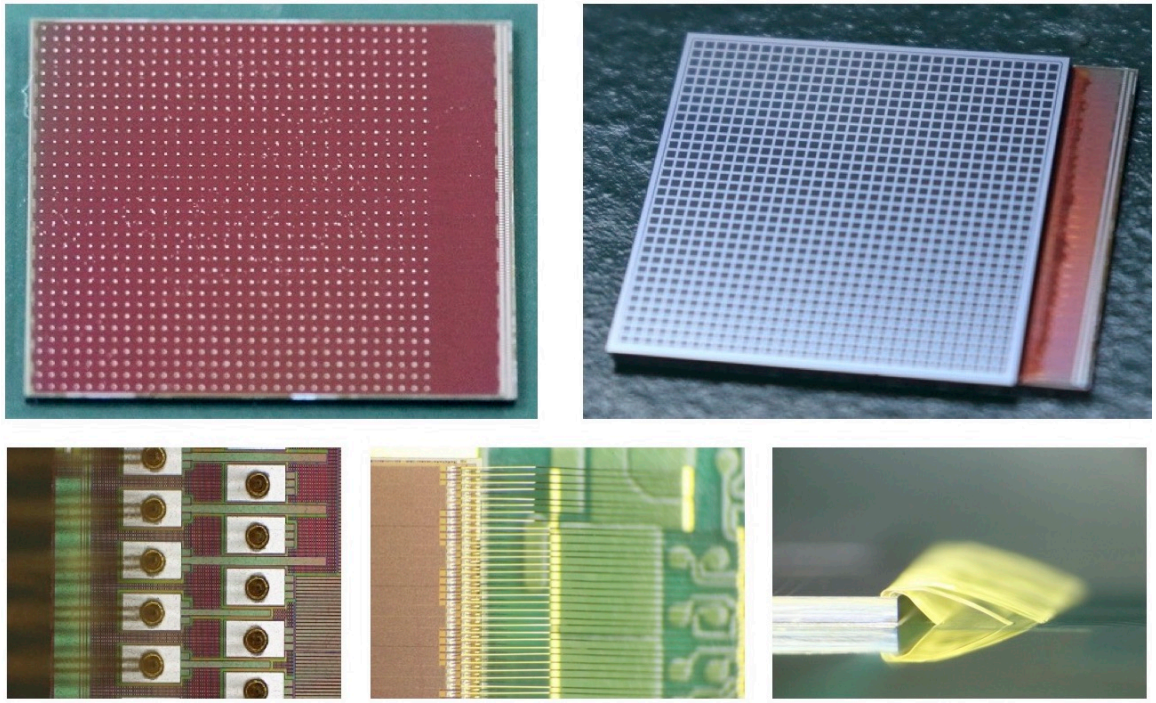




- **Power O(10 mW) for 100 fF input capacitance**
- **Power density: 25 W/cm^2**
- **Sensor performance are very important!**

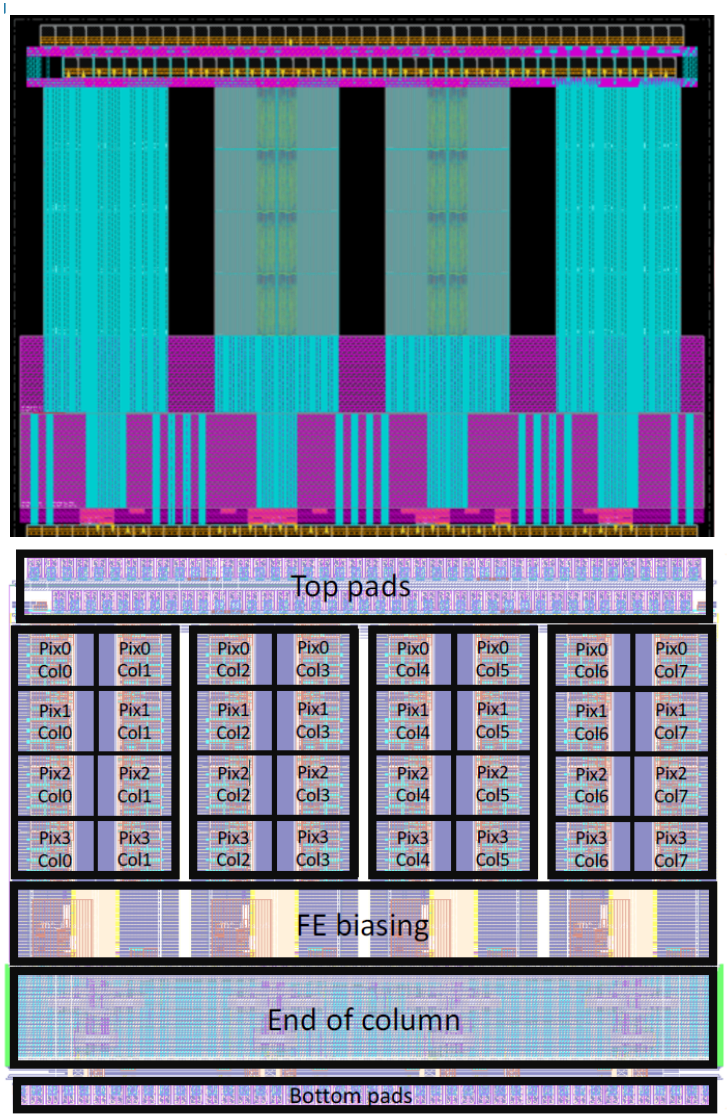
Thank you!

(Macro)-pixel ASIC



- Timing front-end ASIC: 1024 channels, 4096 TDC, 20 Gbit/s output bandwitdth
- Technology 110 nm CMOS
- Pixel size 400 μm$\times$400 μm
- TDC binning 20$\div$100 ps, DNL %
- Overall system jitter $\approx$ 30 ps r.m.s.

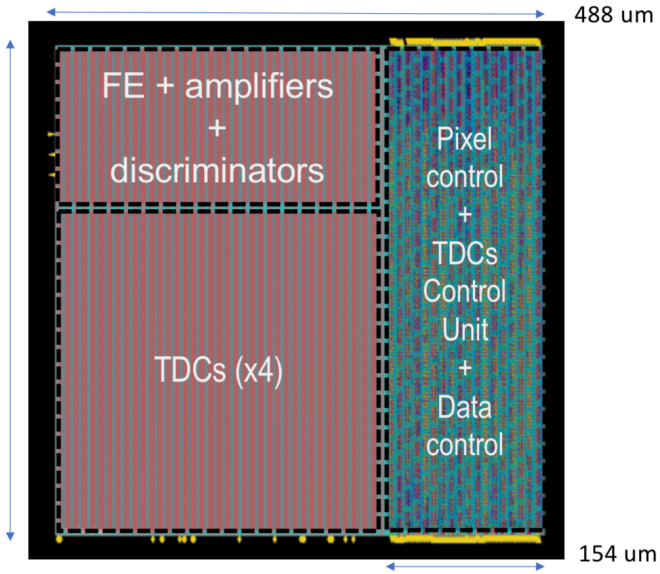
ALCOR chip for SiPM

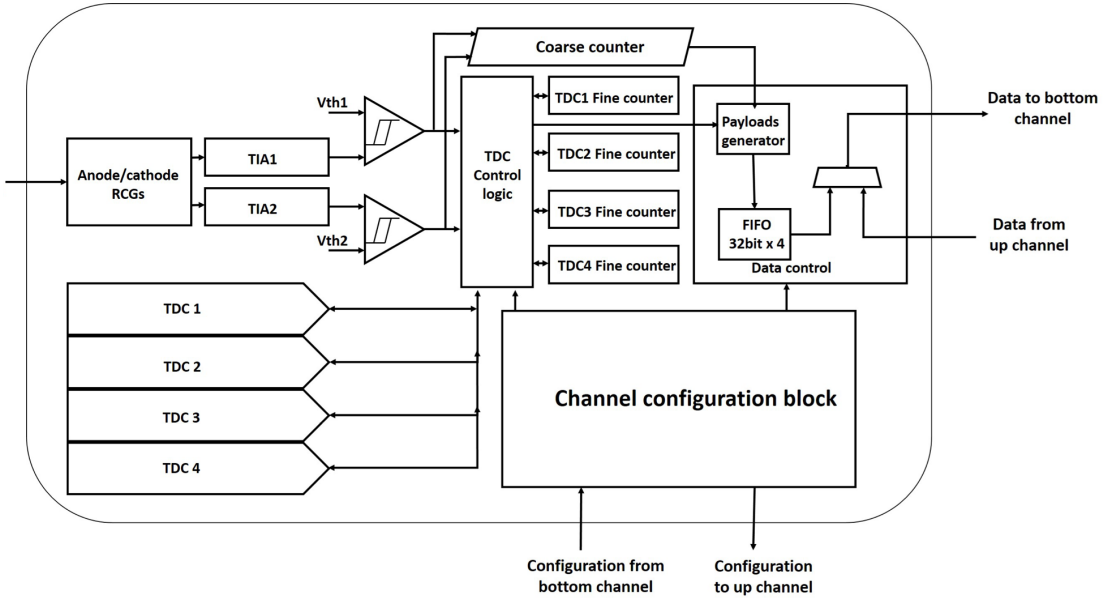


- towards a 3D a-SiPM "digital tile"
- Developed by INFN (CSN2) for the readout of SiPMs at 77K, in the framework of Darkside
- 32-pixel matrix mixed signal ASIC
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O
- Single-photon time tagging mode or time and charge measurement
- 4 LVDS TX data links, SPI configuration
- operation up to 320 MHz (TDC binning down to 50 ps)

F. Cossio, G. Dellacasa, M. Rolo

ALCOR chip for SiPM

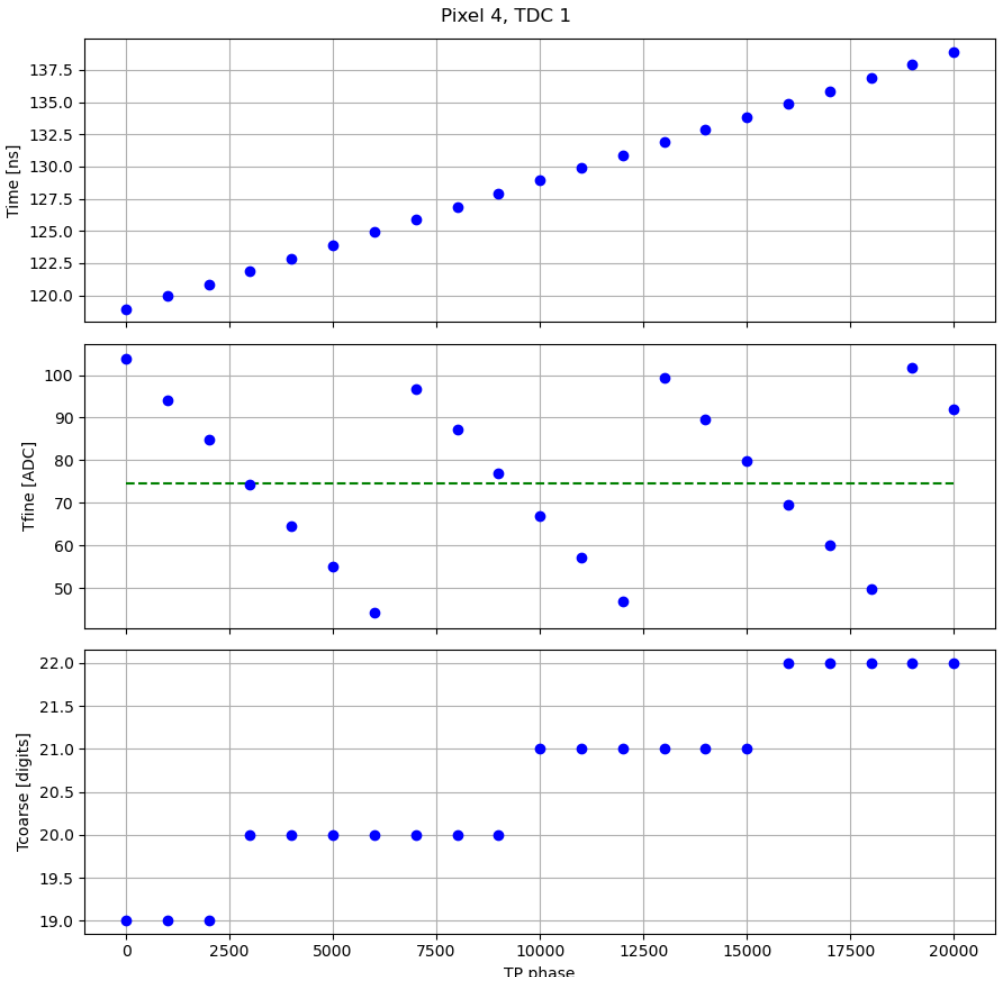


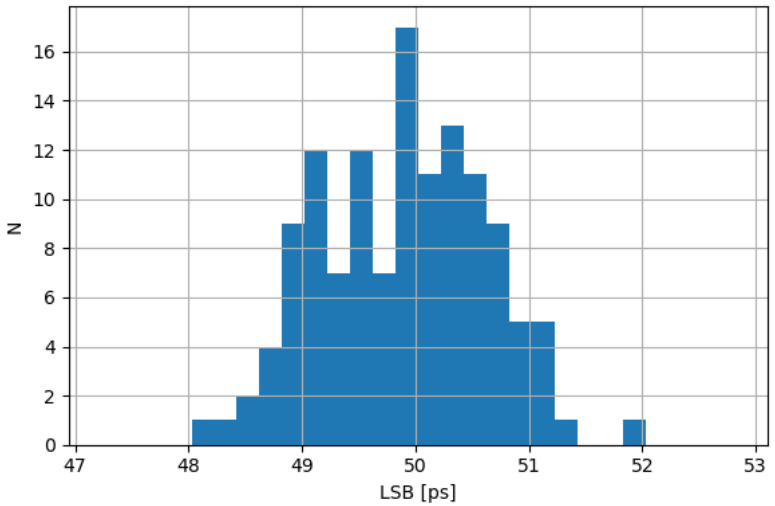


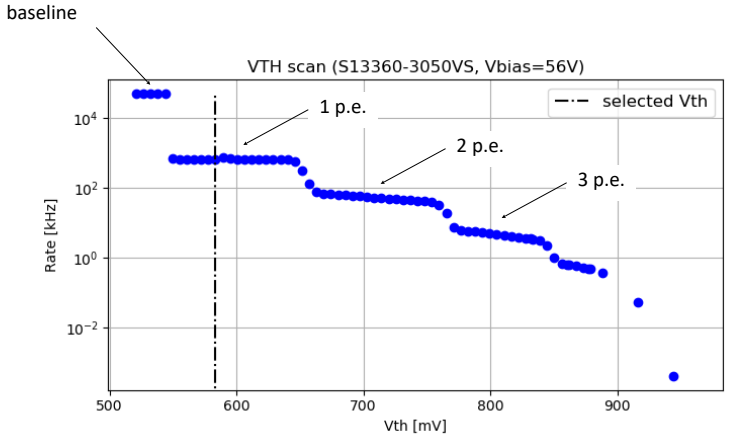
- dual-polarity RCG-based preamplifier: high bandwidth and low input-impedance (10-20 Ω)
- 2 independent post-amp branches and 4 gain settings
- Dual leading edge discriminators with independent (and per pixel) threshold settings (6-bit DAC)
- Pixel control logic handles quad-TDC operation, pixel configuration and data transmission

F. Cossio, G. Dellacasa, M. Rolo

Some ALCOR performance

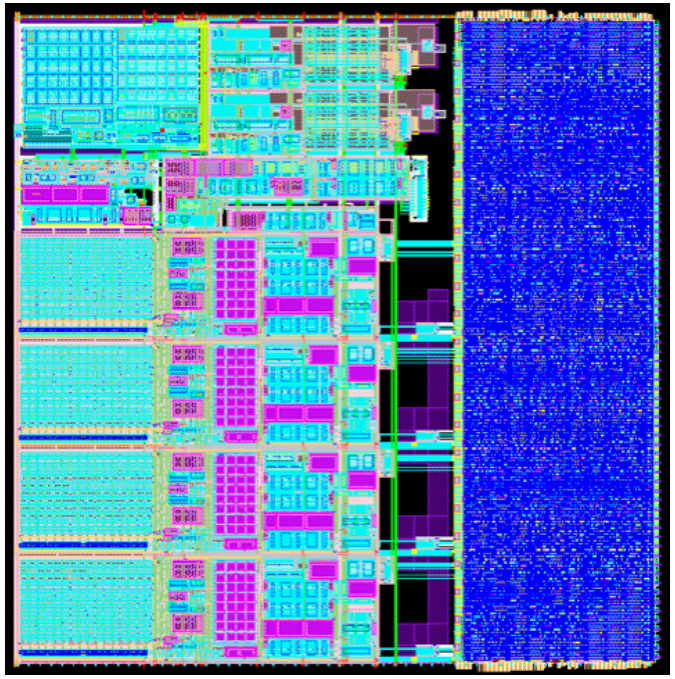




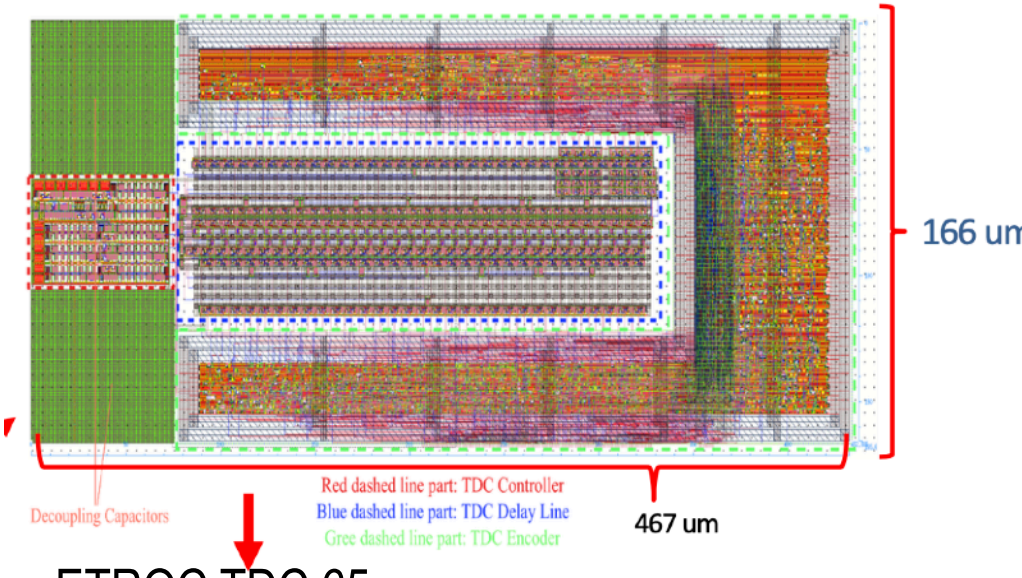


σ = 250 ps r.ms. with 3.5 nF sensors

A curiosity…



Full channel, 110 nm, 4 TDCs



ETROC TDC 65 nm