SiGe BiCMOS Technology

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IHP – Leibniz-Institut für innovative Mikroelektronik

Outline

- Motivation
- High-frequency performance of SiGe HBTs
- Next generation BiCMOS technology
- Integration of HBT circuits inside detector pixel
- Conclusions

Motivation

SiGe BiCMOS combines high-speed HBTs with computing power of digital CMOS

- HBTs extend RF performance beyond that of state-of-the-art CMOS

High-volume SiGe BiCMOS applications today:

- High-data-rate optical networks
  - Trans-impedance amplifiers, laser and modulator drivers, clock and data recovery
- Front-end modules for cell phones
  - Amount of SiGe in cell phones strongly increased over last decade
  - Higher integration capability of SiGe BiCMOS compared to competing III-V ICs
- Automotive radar at 77 GHz
  - SiGe dominates the market but CMOS is coming up

Ongoing Demand for Higher Frequencies

Higher frequencies of MMICs facilitate

- Higher communication bandwidth
- Higher special resolution of radar
- THz imaging and sensing in medicine, industry, and science

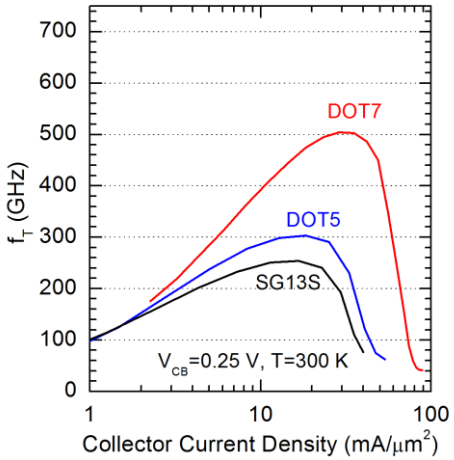
Cut-off frequencies (f_T, f_{max}) typically 3-10X larger than operating frequency

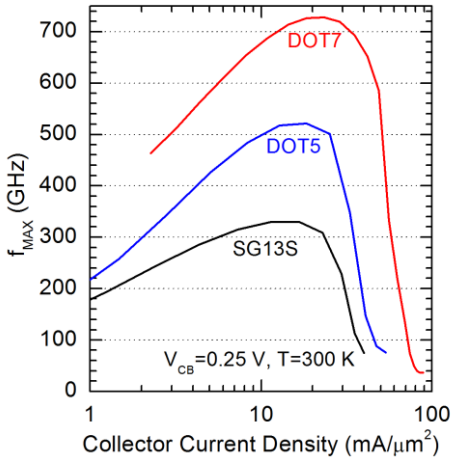
- Larger design margins, lower noise, higher gain, better linearity
- Lower power consumption ➔ low-cost packaging

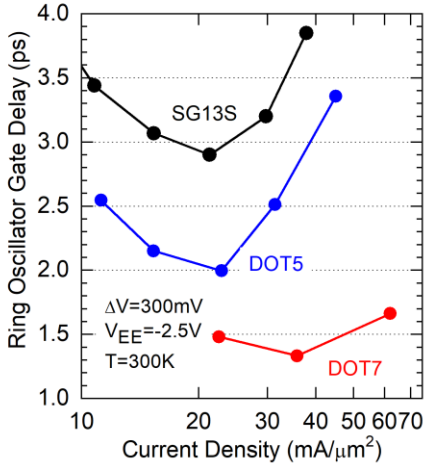
Key Parameters of BiCMOS Processes

Company	f_T	f_{MAX}	CMOS node	Name
Industrial Production				
Infineon	250 GHz	360 GHz	130 nm	B11HFC
ST Microelectronics	320 GHz	370 GHz	55 nm	B55
NXP	260 GHz	350 GHz	180 nm	xHBT2
Global Foundries	300 GHz	360 GHz	90 nm	9HP
TowerJazz/Intel	240 GHz	340 GHz	180 nm	SBC18H4
Low-Volume Fabrication				
IHP	350 GHz	450 GHz	130 nm	SG13G2
IHP (development)	470 GHz	650 GHz	130 nm	SG13G3

EU Projects addressed High-Performance SiGe HBTs







DOTFIVE (2008-2011)

- Demonstration of HBTs with 500 GHz f_{MAX}

DOTSEVEN (2012-2016)

- Demonstration of HBTs with 700 GHz f_{MAX}

TARANTO (2017-2021)

- Next generation BiCMOS platforms: ST (55nm), Infineon (90nm), IHP (130nm)

Scenario for Performance Enhancement

- Scaling of lateral and vertical device dimensions
- Device and technology concepts suitable for low parasitics
- Utilize materials with low specific resistances and capacitances

Vertical Profile Scaling for Higher f_T

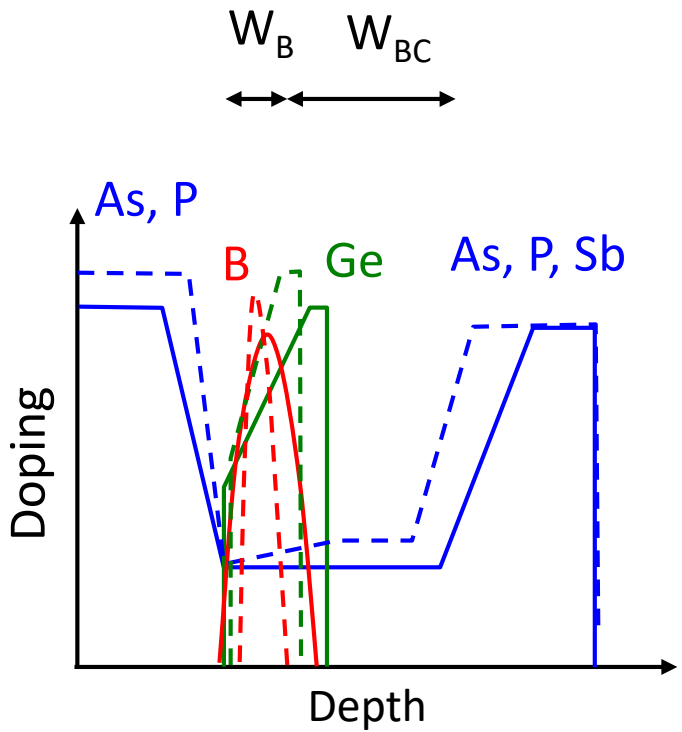
Reduce W_B ➔ low t_B
- As-grown W_B<5nm for R_{sBi}~2kΩ
- Minimize diffusion

Reduce W_{BC} ➔ low t_{BC}
- Lower BV_{CBo}
- Higher C_{BC}

Reduce W_{EB} ➔ low C_{diff}
- Lower BV_{EBo}
- Tunneling

Heavy collector doping ➔ low R_C

Mono-crystalline emitter ➔ low R_E



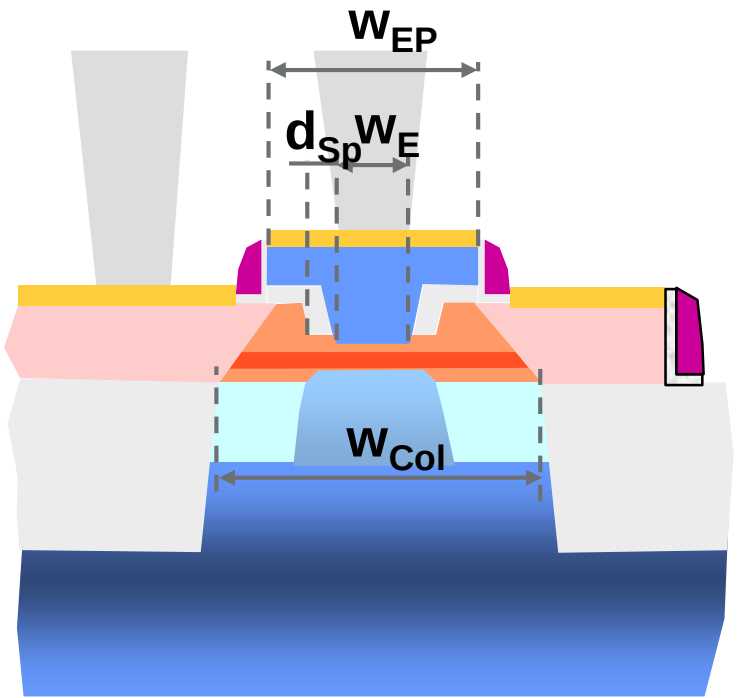
Lateral Scaling for Higher f_{MAX}

Smaller emitter-window w_E

- Lower R_{Bi}
- But higher R_E, R_C, and R_{Th}

Optimize critical region near emitter

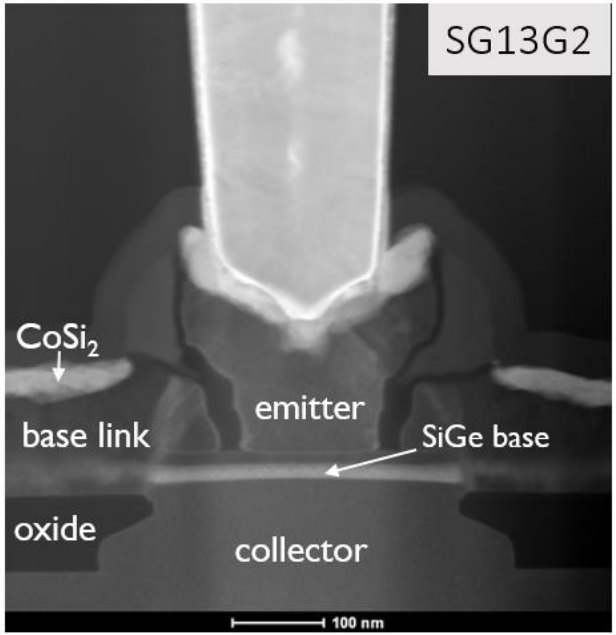
- Smaller emitter-poly w_{EP}
  - Lower R_{Bx}
- Smaller BE spacer d_{SP}
  - Lower R_{Bx}
  - But higher $C_{BE,x}$
- Smaller collector-window w_{Col}
  - Lower C_{BCx}
  - Effect on R_{Bx} depends on architecture

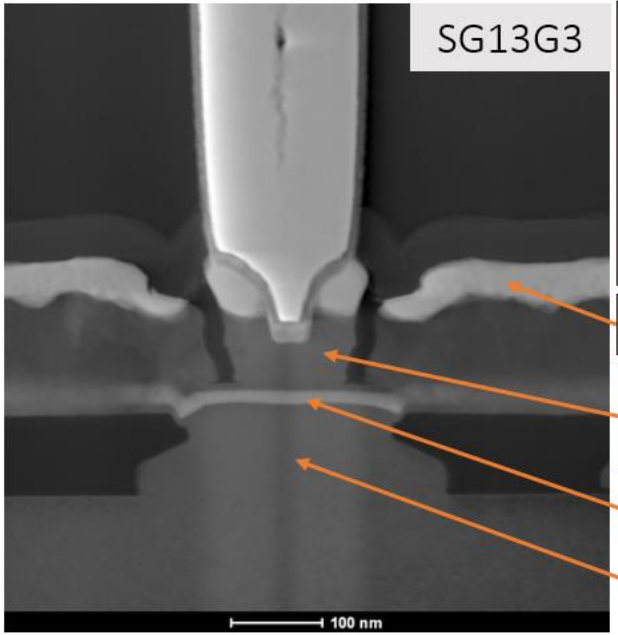


HBT Technology

Advances in HBT technology incorporated into new generations of IHPs 130nm BiCMOS

- DOTFIVE-HBT integrated in SG13G2
- DOTSEVEN-HBT integrated in currently developed SG13G3





Scaled lateral dimensions:
- Emitter-poly width
- Emitter window
- EB spacer width
- Collector window
- Salicide blocking spacer

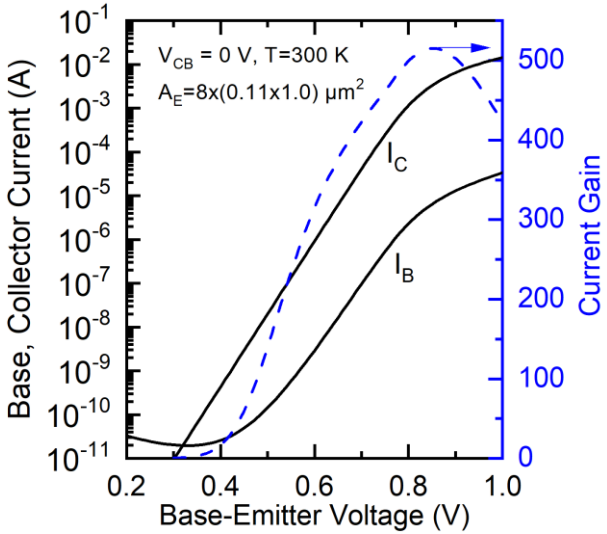
NiSi

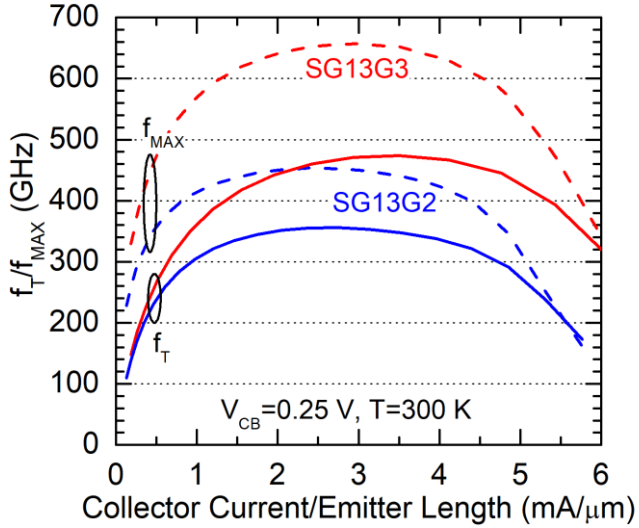
Enhanced doping in emitter and base link

New SiGe epi process

Enhanced SIC doping

HBT Characteristics

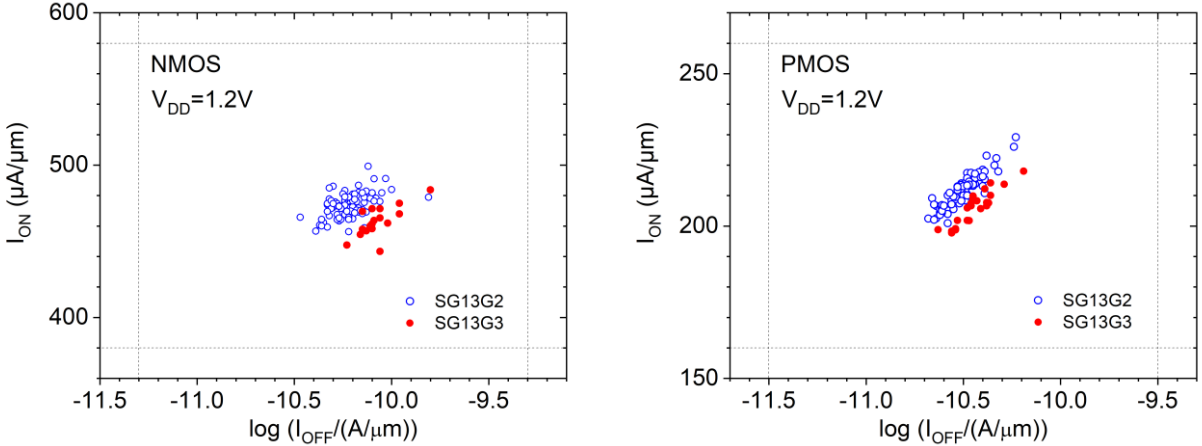


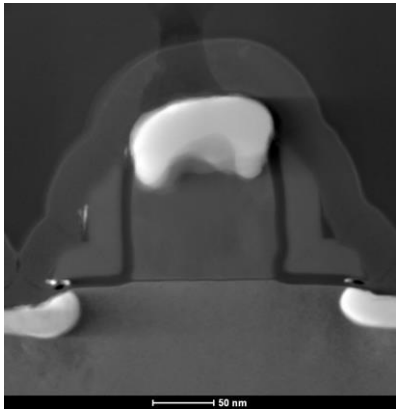


- HBTs with aggressively scaled doping profiles show ideal I_C and I_B over wide range of V_{BE}
- Non-ideal I_B at V_{BE} < 0.5 V indicate tunneling through narrow base-emitter junction
- Cutoff frequencies of SG13G3 far beyond predecessor process SG13G2

130-nm CMOS Process

- 1.2V core and 3.3V I/O devices with same specifications in SG13G2 and SG13G3
- Same portfolio of passive components in all three process generations
  - Poly-Si Resistors, MOS varactors, MIM capacitors
  - Thick top metal layers for inductors, transmission lines, and transformers



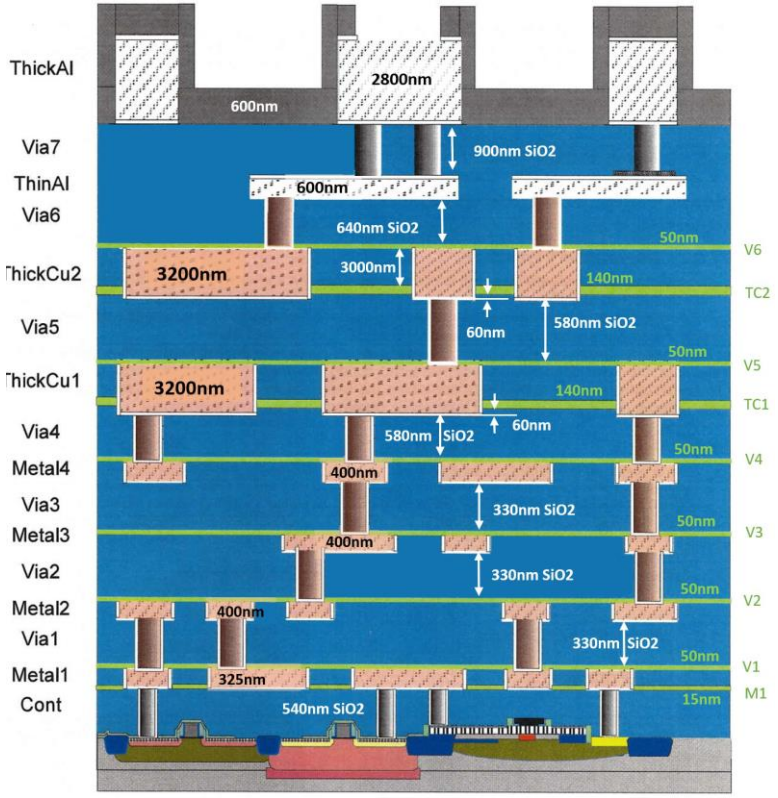


On-current vs. off-current of NMOS and PMOS transistors of technologies SG13G2 (blue) and SG13G3 (red). Dashed lines indicate spec limits.

BEOL

- SG13G3 will be offered with Cu-BEOL in MPW and prototyping service
  - Four thin and two thick Cu layers
  - Two Al top layers
  - Cu-BEOL fabricated at XFAB

- Additional process option with seven-layer Al-BEOL of IHP supports research activities
  - Flexible for integration of new component
  - Research in hetero-integration and post-processing in IHP pilot line

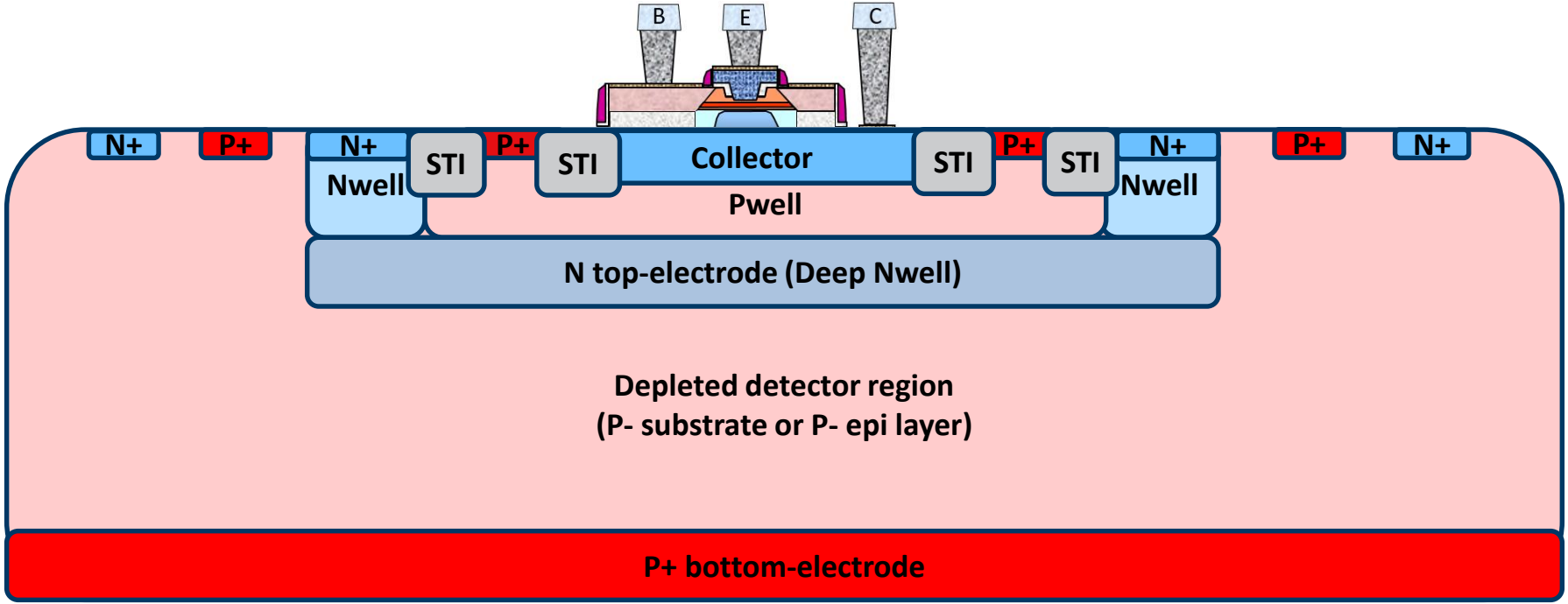


Circuits

- Performance of new HBT generation benchmarked in early-access fabrication runs of SG13G3 by IHP circuit design groups and external partners
  - 300 GHz low-noise amplifies, [Gadallah, MWW Comp. Lett. 2022]
  - 300 GHz power amplifiers, [Bücher, JSSC 2022]
  - Analog 2:1 Multiplexer with over 110 GHz Bandwidth [Tannert, BCICTS 2021]
    - >150 GBd PAM-4 electrical signal generated with this AMUX by time-interleaving two channels of an commercial arbitrary waveform generator (Schostak et al., EuMW 2022)
  - Distributed amplifier with average gain of 19 dB and over 170 GHz BW [Baeyens, EuMW 2022]

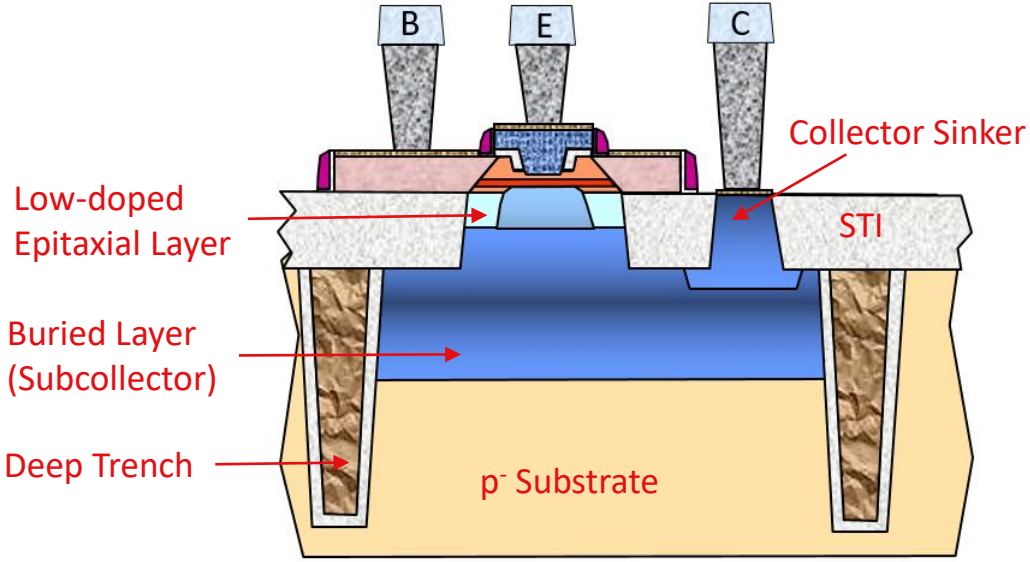
Integration of HBT Circuits inside Detector Pixel

- Transistor regions need to be isolated from top electrode of detector
  - Is it possible to fabricate isolated n-region below HBT collector?

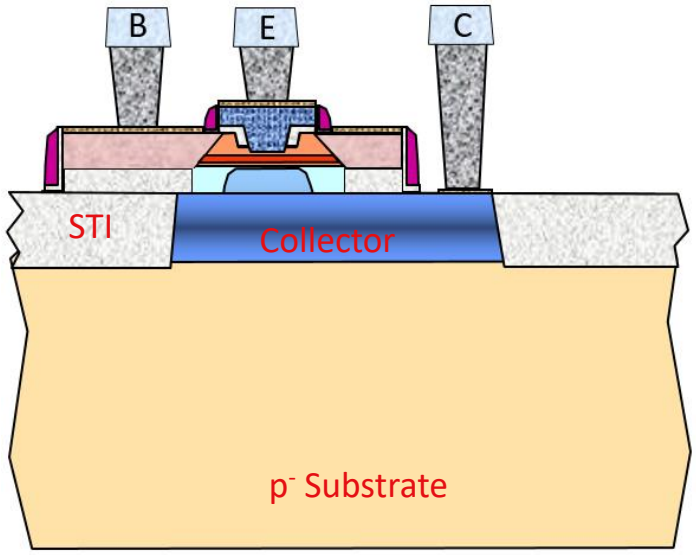


Collector Construction of High-Speed HBTs

Epitaxially-buried sub-collector with DT isolation
(applied is state-of-the-art industrial processes)



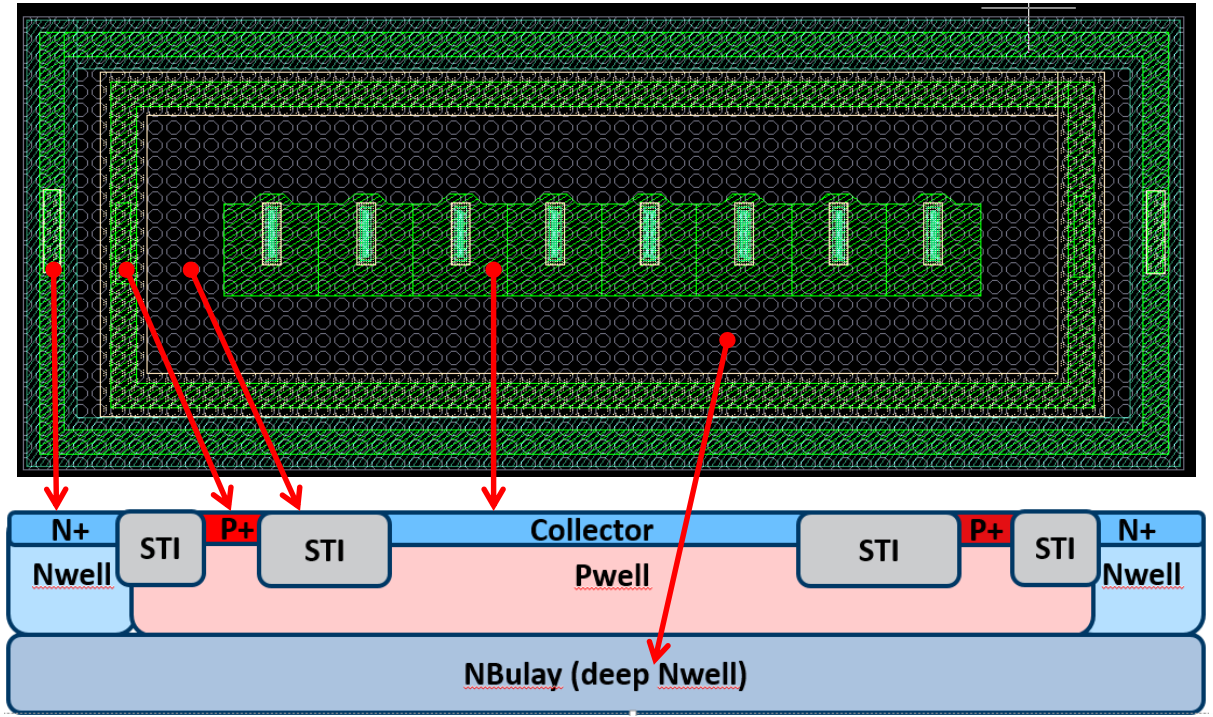
Implanted collector with ST isolation
(applied in IHP BiCMOS processes)



- Shallow collector construction of IHP BiCMOS facilitates fabrication of isolated n-region below collector using Pwell and Deep-Nwell of CMOS process

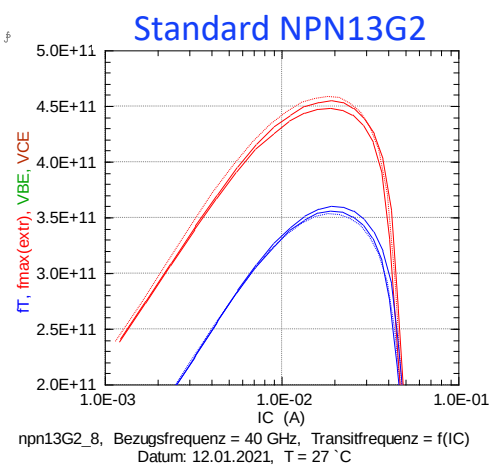
Isolation of HBT by Layout in Standard Process

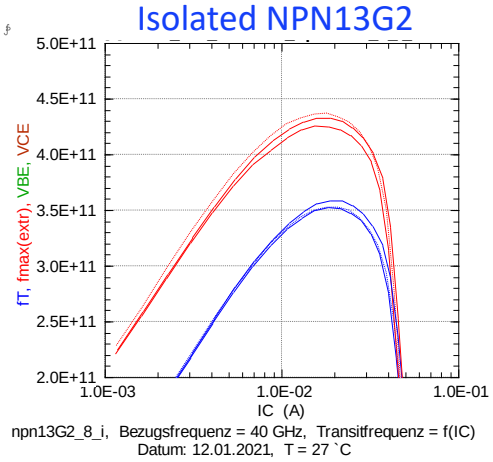
- Draw Nbulay layer over entire HBT
  - Applicable for NPN13P in SG13S and NPN13G2 in SG13G2
  - Pwell will be automatically generated during mask generation for HBTs inside Nbulay

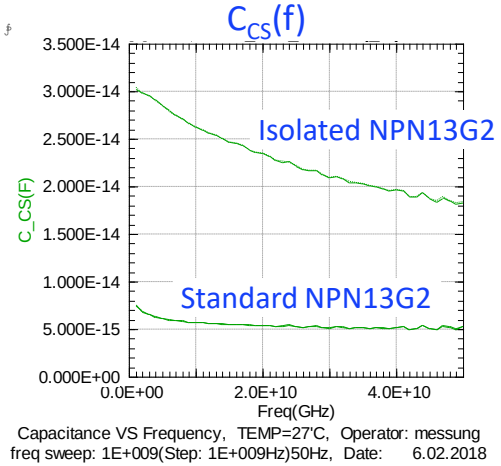


Electrical Characteristics

- DC characteristics of the isolated HBTs are identical to the reference HBTs w/o Nbulay
- Biasing of Pwell and Nbulay below collector should avoid parasitic bipolar effects
- The Isolated HBTs have enhanced collector-substrate capacitance (Ccs) due to Pwell
- The isolations leaves f_T unchanged, f_{MAX} is slightly reduced due to enhanced C_{CS}







Conclusions

- Continuing interest in SiGe BiCMOS technologies for frequencies and data-rates that are out of reach for state-of-the-art CMOS
- Significant potential for enhanced HBT performance demonstrated in research
- New generation of high-speed HBTs in SG13G3 offers unsurpassed cutoff frequencies f_T of 470 GHz, f_{MAX} of 650 GHz, and BV_{CES}= 3.7 V
  - Early access MPW starts in March 2023
- Moderate complexity of BiCMOS process favors integration of new functions

Thank you for your attention!

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