

The FastIC project: From the FastIC ASIC to FastIC+ and FastRICH

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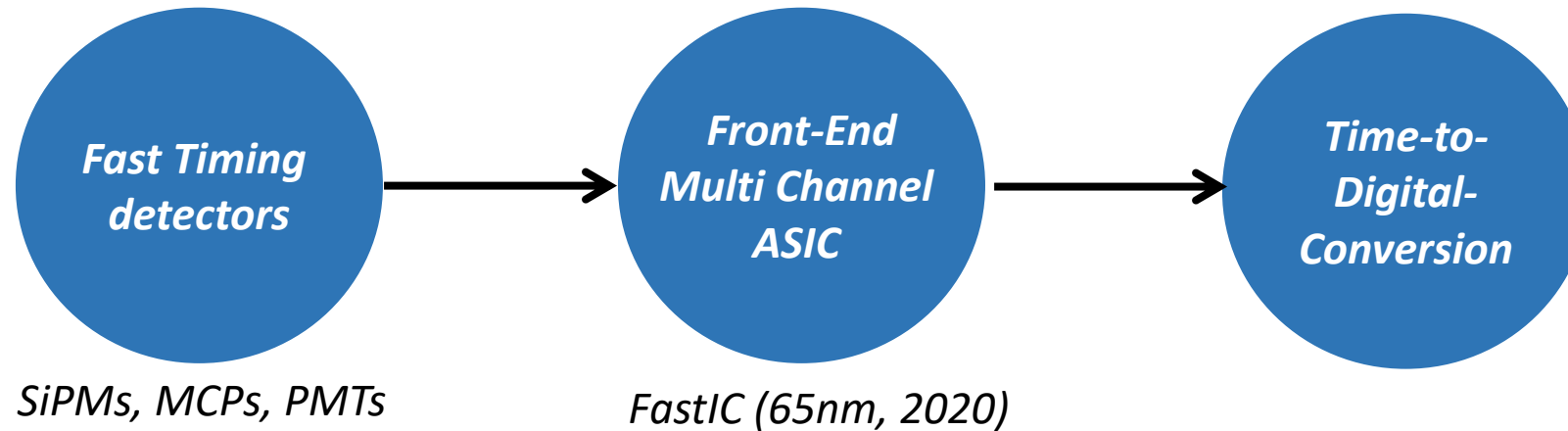
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Outline

- FastIC project context
- Architecture
- Readout
- Measurements (Linearity, Energy resolution, SPTR, CTR)
- Derivatives of FastIC (FastIC+, FastRICH)
- Summary

The FastIC project: context

The FastIC project: motivation



FastIC addresses limitations from NINO (2004, 0.25 μ m): mainly non-linearity of the energy measurement and power consumption

Highly configurable:

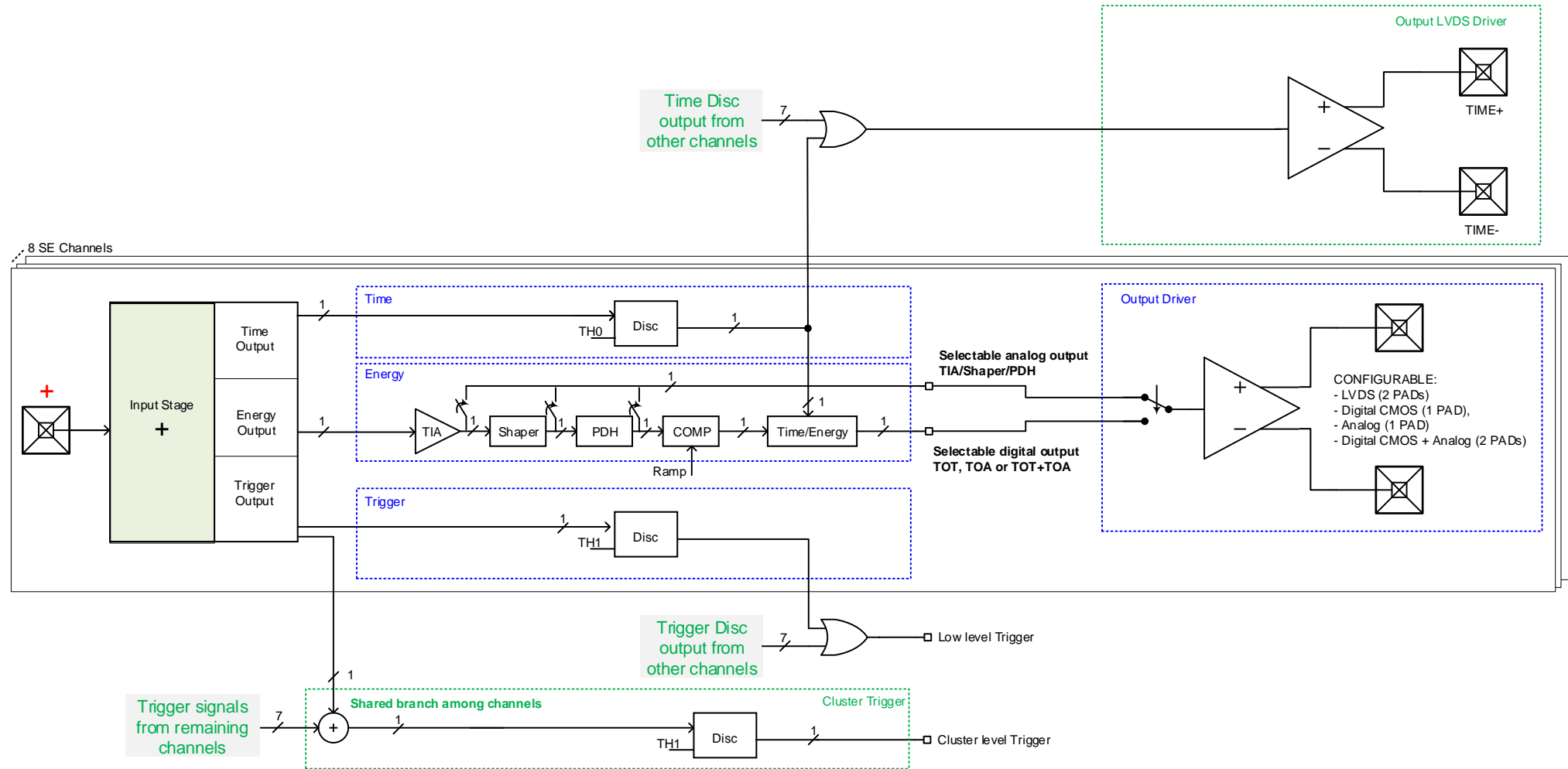
- Singled ended, differential and summation of 4 single-ended channels to explore benefits of segmentation of detector areas
- Positive and negative polarity
- Large range of input capacitances
- Large dynamic range (with positive and negative polarity readout)

\sim 30 ps r.m.s. Jitter (electronics) (Hamamatsu S13360-3050CS, 3600x50 μ m microcells, 4.5V_{OV}, wirebonded) + Linear energy measurement (\sim 2.5 % error) up to 20 mA peak (12mW single ended channel)

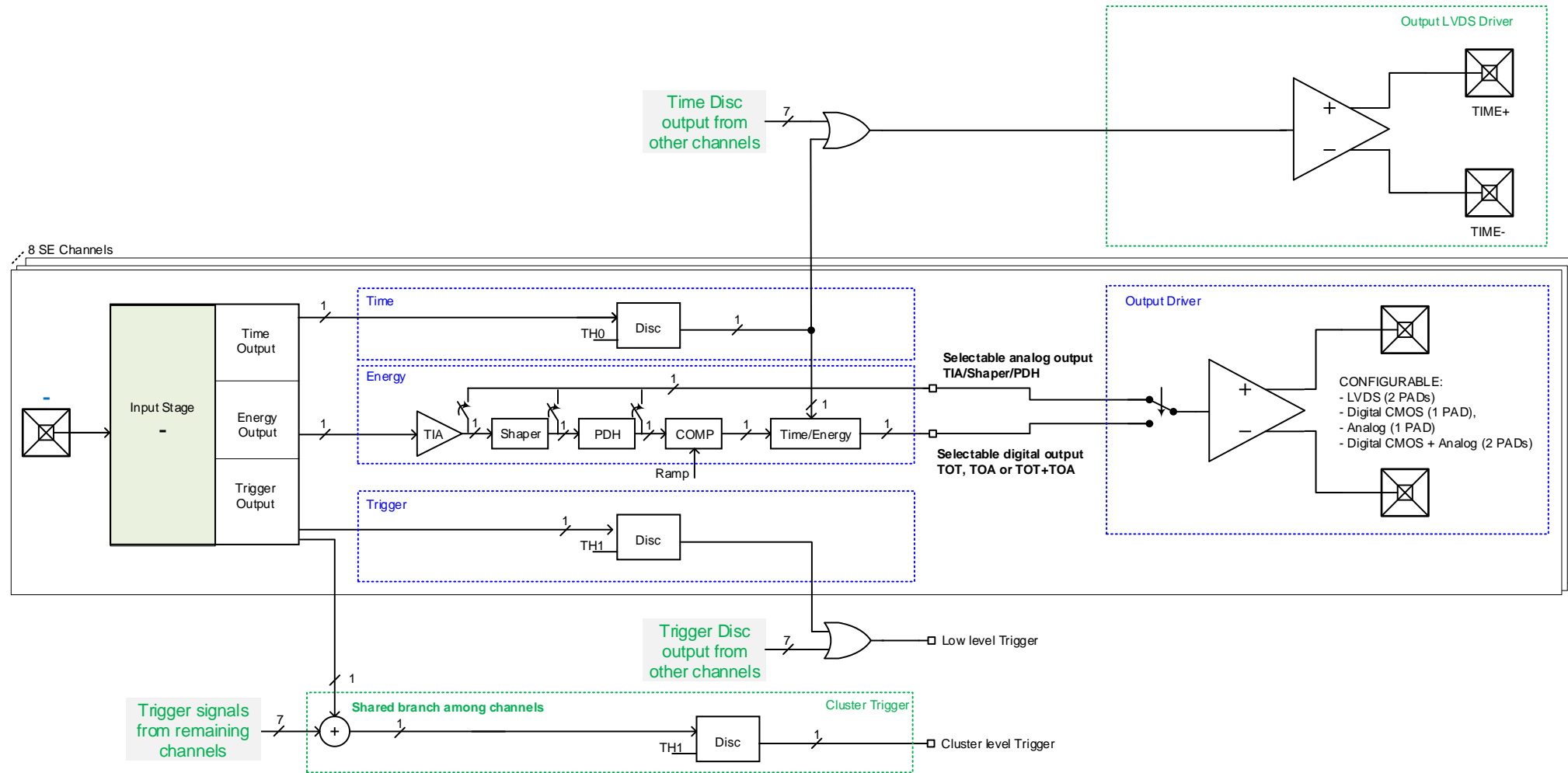
Collaboration between CERN (KT funded) and University of Barcelona (ICCUB)

The FastIC project: Architecture

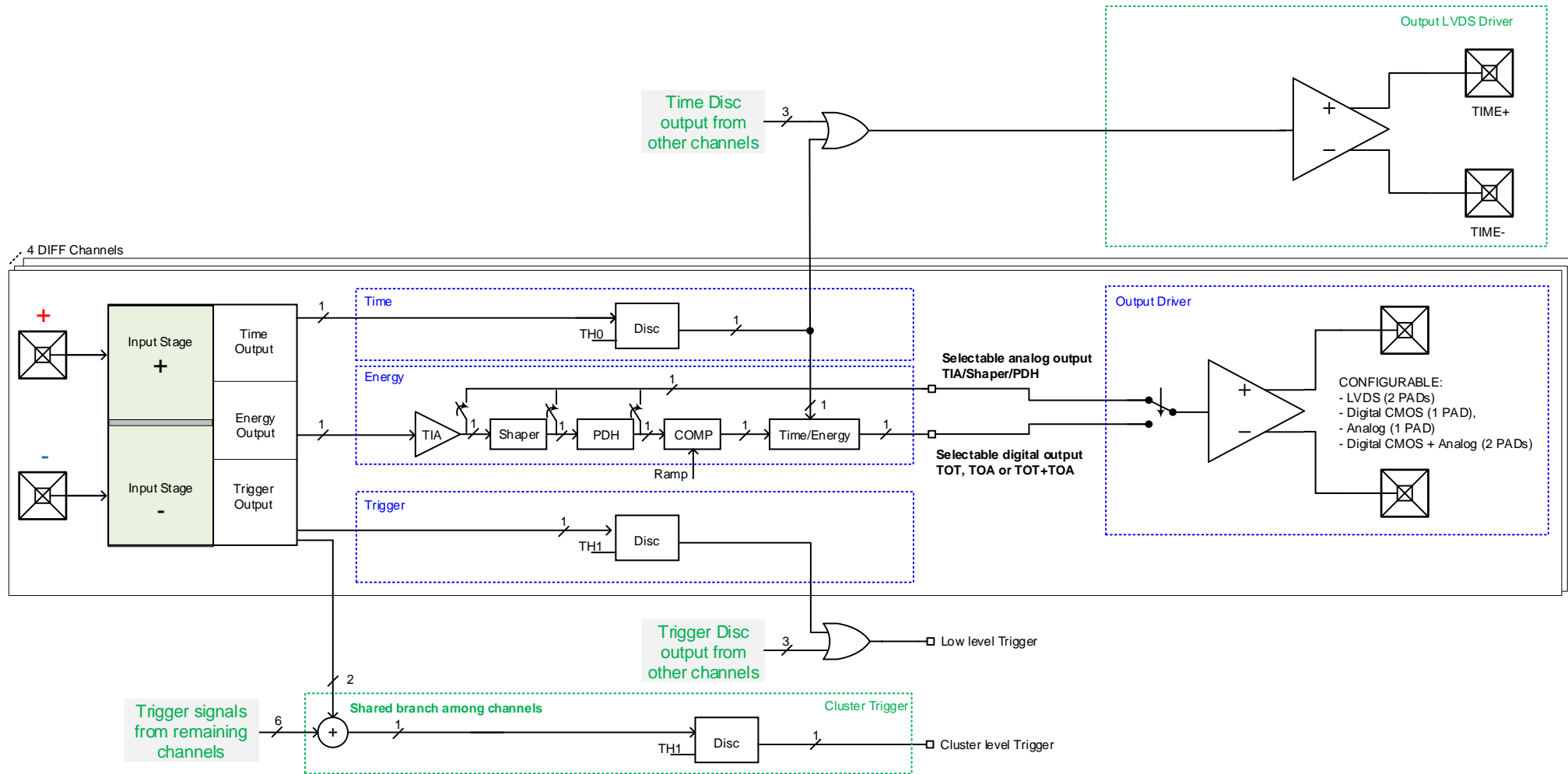
Single Ended (Positive Polarity) configuration



Single Ended (Negative Polarity) configuration

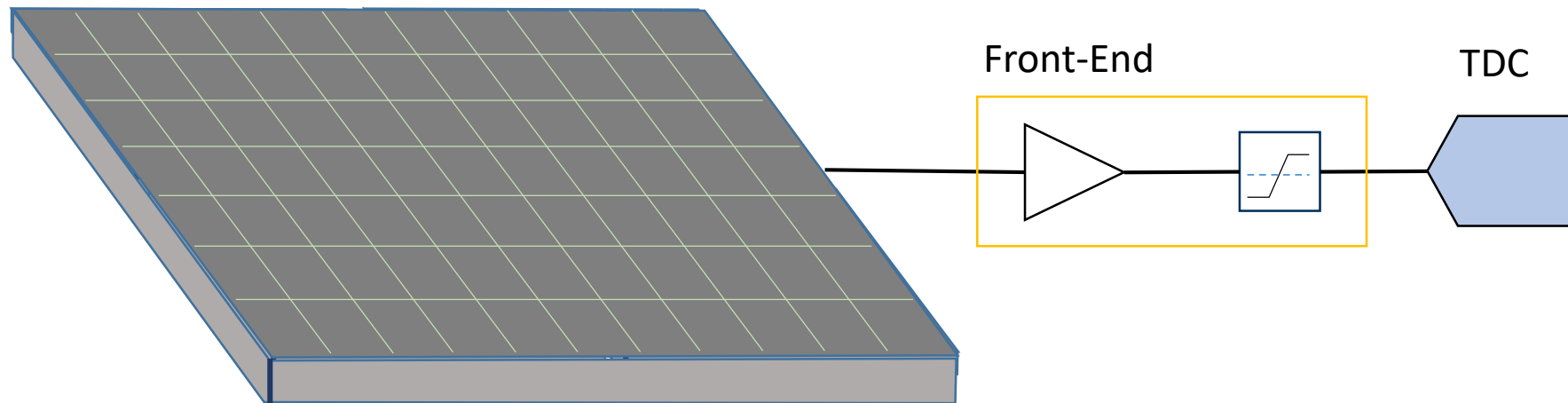


Differential configuration



Implementation: combination of signals

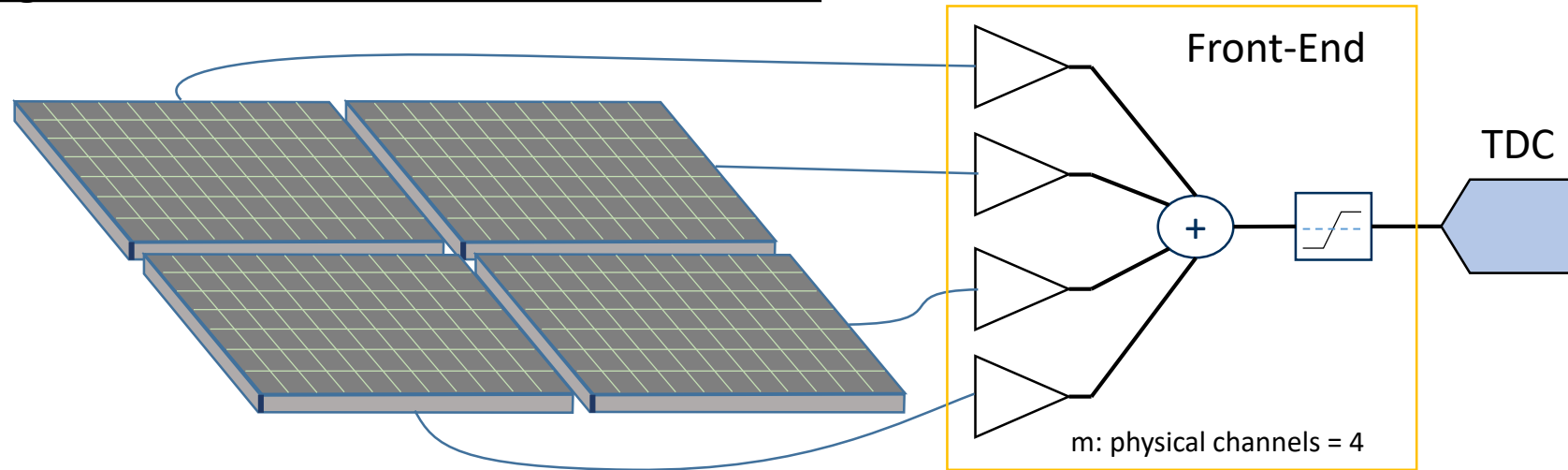
Large area SiPM → Large C_{det}



- Large area SiPMs can have an equivalent detector capacitance higher than 1 nF
- This high input capacitance degrades the slew-rate $SR \propto \frac{Q_{det}}{C_{det}}$

Strategy to cope with large detectors

Segment SiPMs to cover same area $\rightarrow C_{det}/4$



- Segmentation: Cover same area with m smaller sensors.

- Potential improvement of the slew-rate by a factor of m (i. e. $SR \propto m \frac{Q_{det}}{C_{det}}$)
- Series noise contribution is approximately constant w.r.t. segmentation

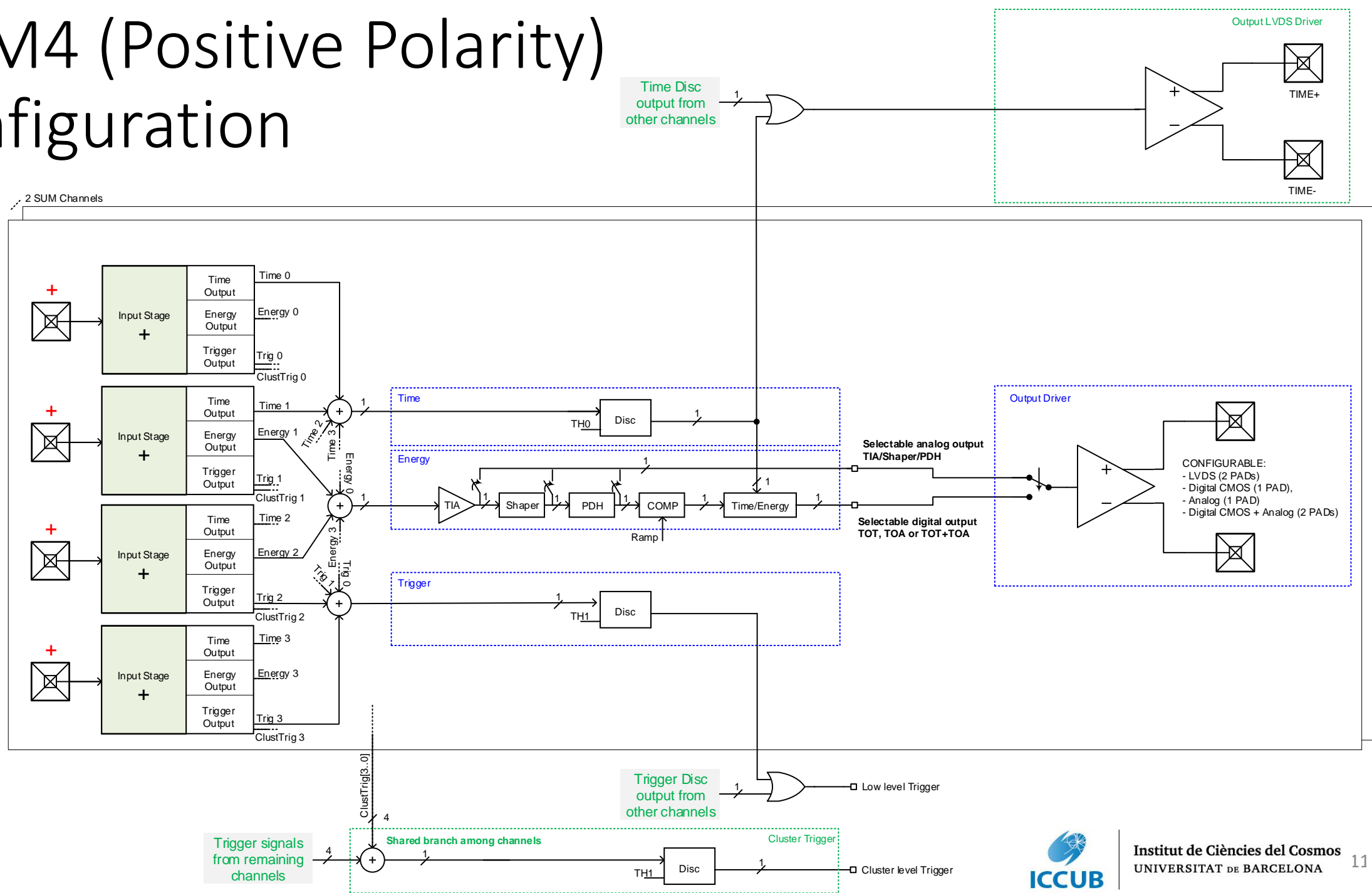
- (i.e. $\sigma_n \sim \sqrt{m} \cdot \sigma_{n,smallDet} \sim \sqrt{m} \cdot \frac{C_{largeDet}}{\sqrt{m}}$)

Sum of m uncorrelated contributions

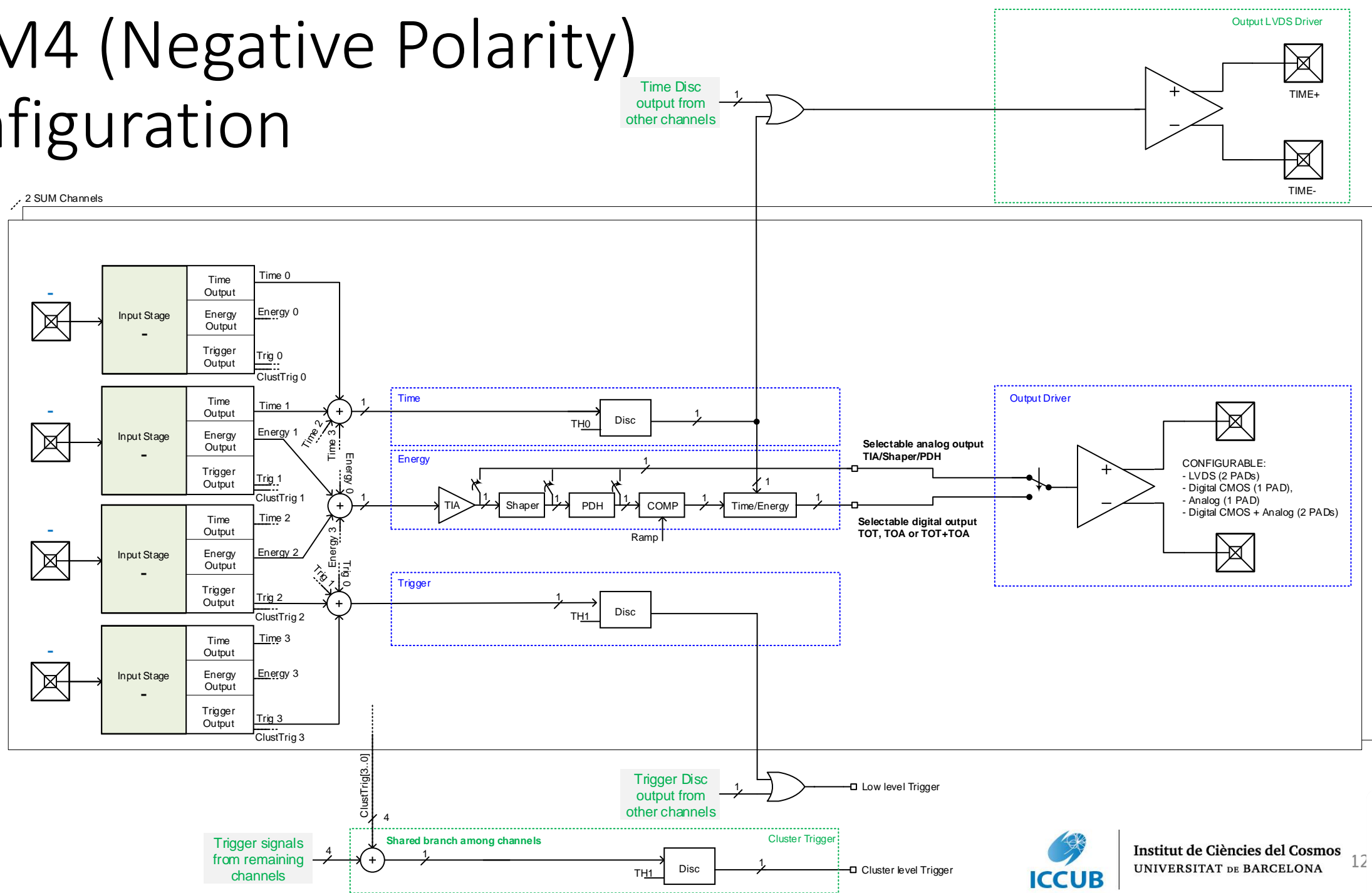
The series noise is proportional to the detector capacitance, which reduces a factor \sqrt{m}

Potential reduction of σ_t by a factor m

SUM4 (Positive Polarity) configuration



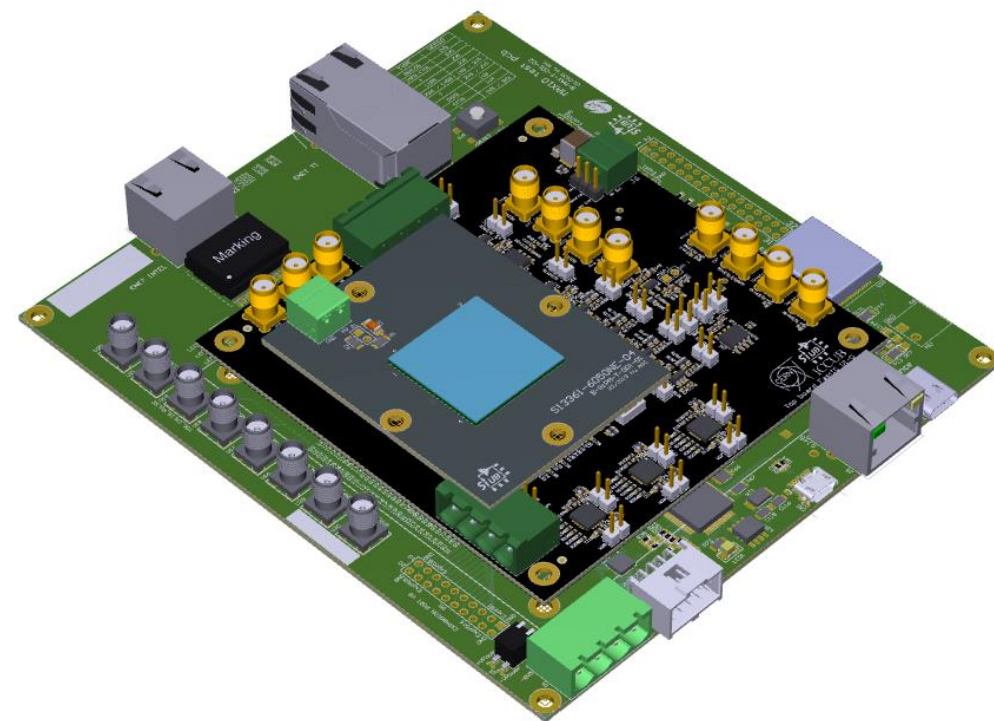
SUM4 (Negative Polarity) configuration



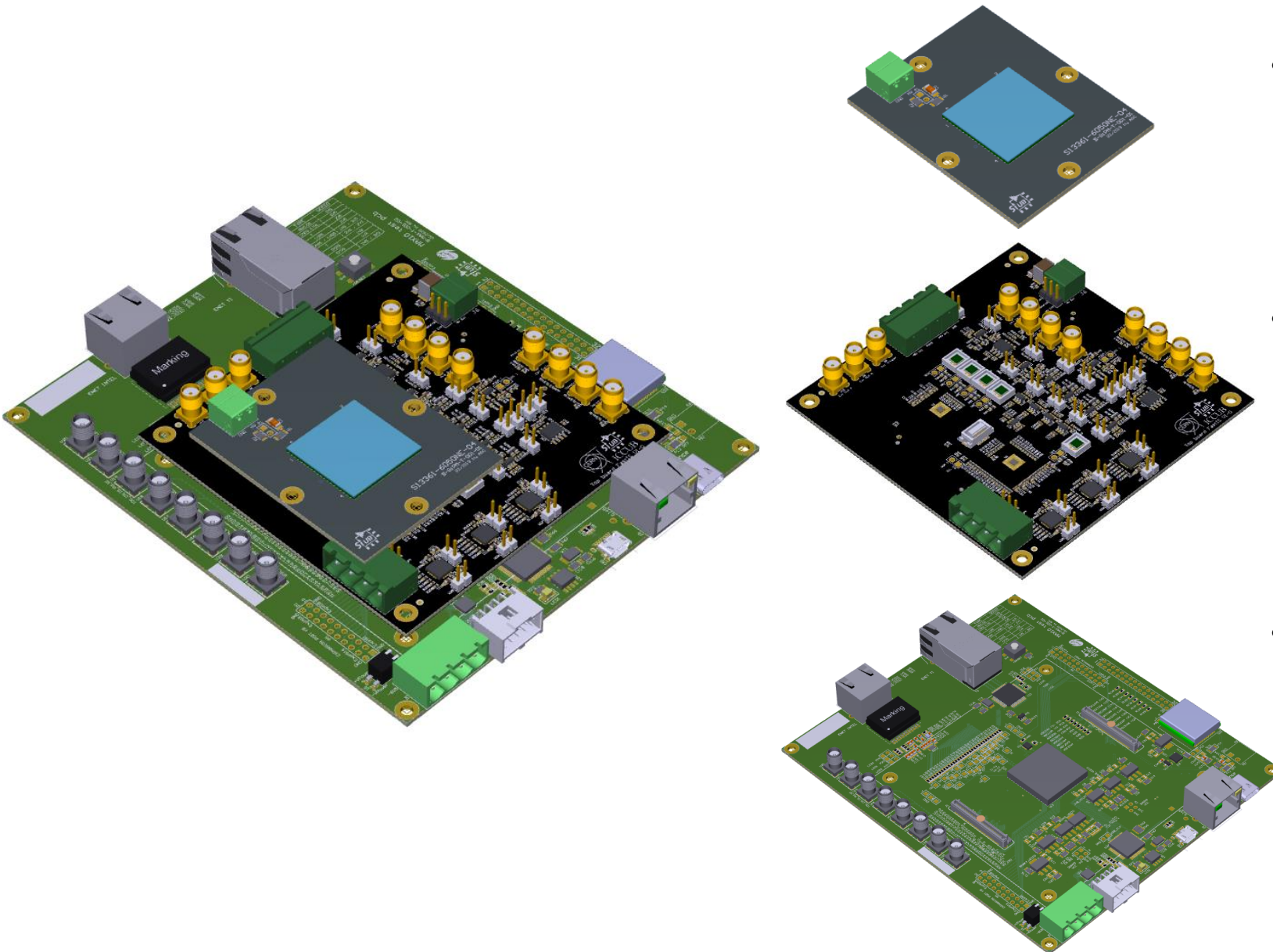
The FastIC project: readout system

Evaluation system

- Aims of the evaluation system:
 - Basic operational test & debug ASIC functionalities
 - Initial electrical characterization and linearity analysis.
 - Initial benchmark i.e. evaluate the FastIC chip by comparison
 - With respect previous designs (NINO, HRFlexTOT)
 - Using reference SiPM sensor:
 - Hamamatsu S13360-3050CS
 - FBK NUV-HD
 - Interface with other sensor based on adaptor board
 - Signal acquisition:
 - FPGA-based TDC (45ps time bin)
 - Differential sLVS link to external system



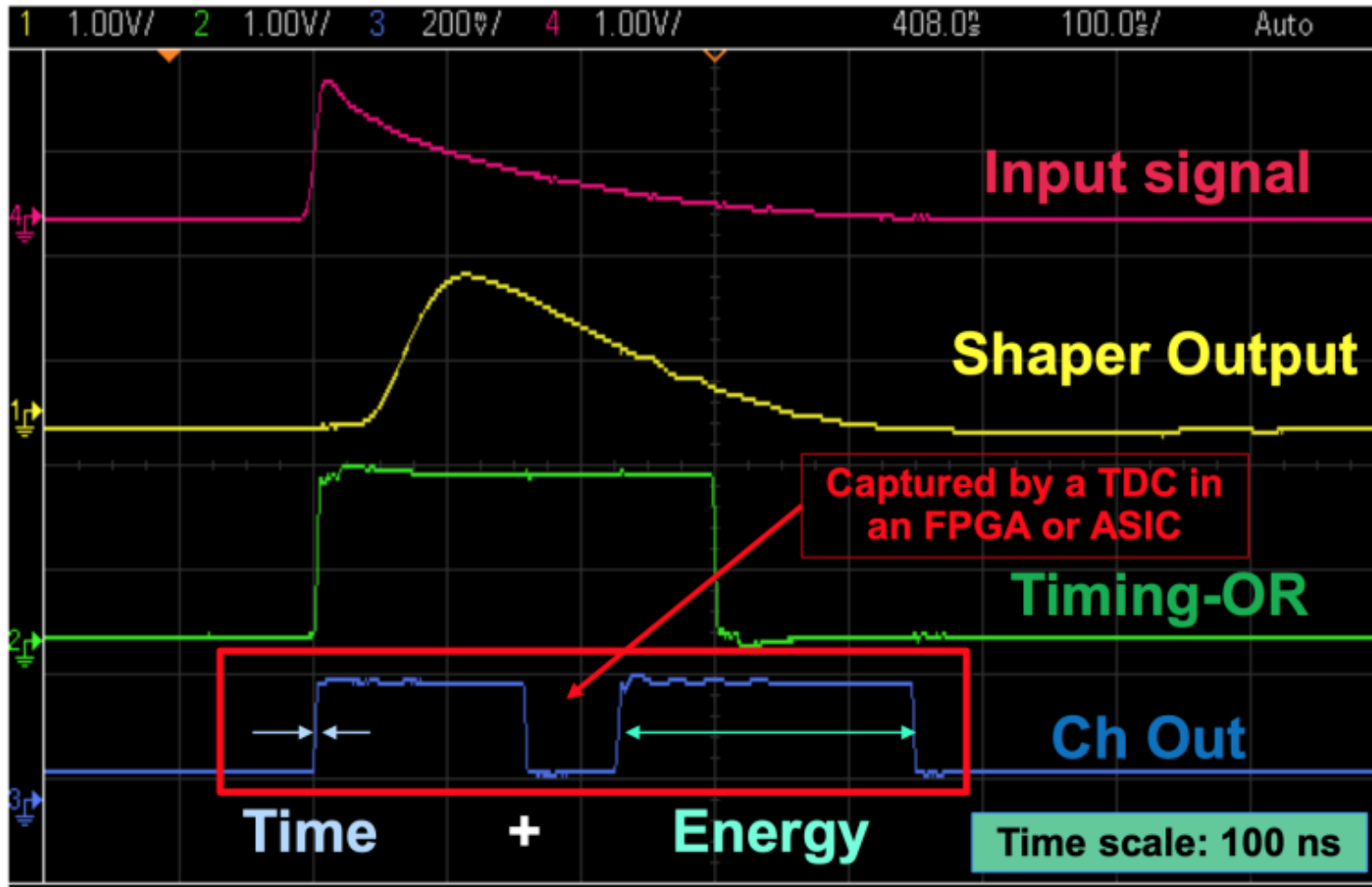
Evaluation system



- Custom sensor board
- FastIC generic board
 - 2 FastICs on QFN64 (16 channels)
 - Reference SiPM sensors included
 - The board can be used stand alone
- FPGA board
 - FPGA board for slow control, acquisition and additional biasing.
 - Multichannel TDC is implemented in the FPGA (45ps time bin)

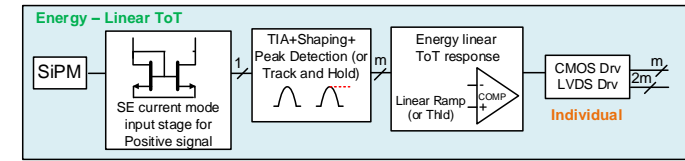
The FastIC project: measurements

Time waveforms

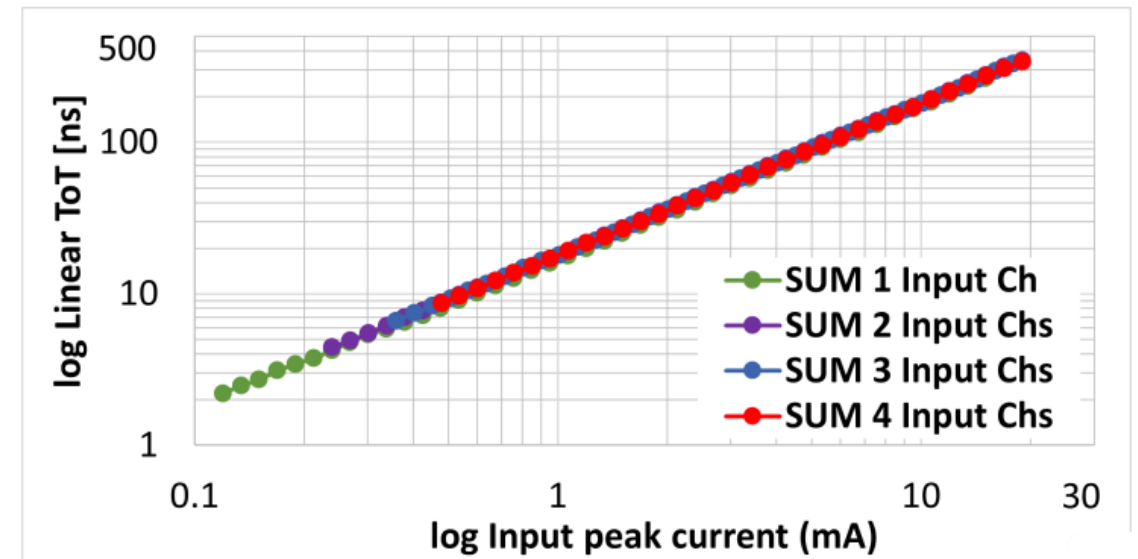
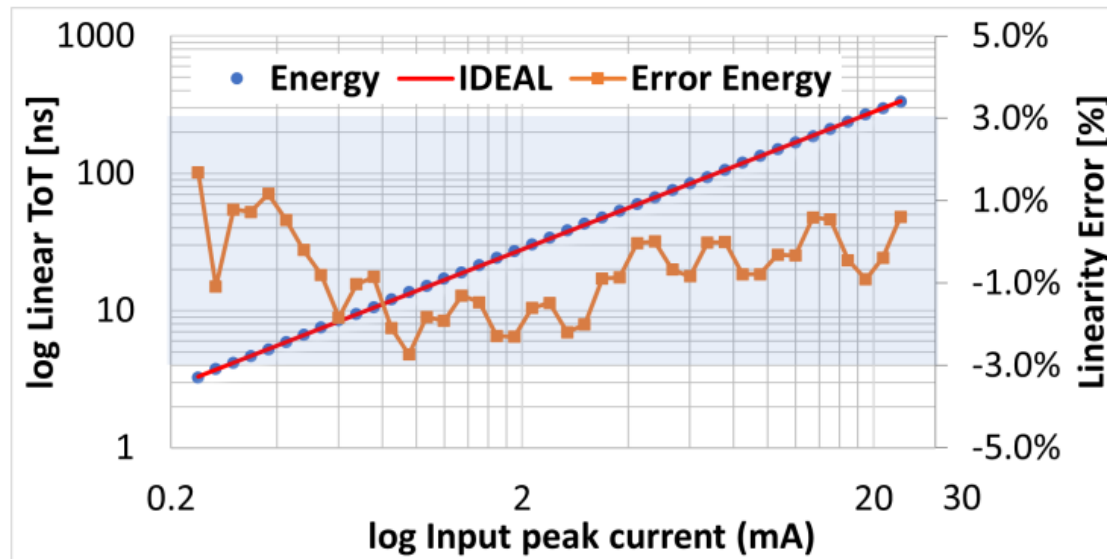


- FastIC provides a measurement of time and energy per channel in two consecutive pulses
- Time is encoded in the rising edge of the first pulse
- Energy is encoded on the width of the second pulse. The readout is based on HRFlexToT architecture*

Linearity of the energy measurement



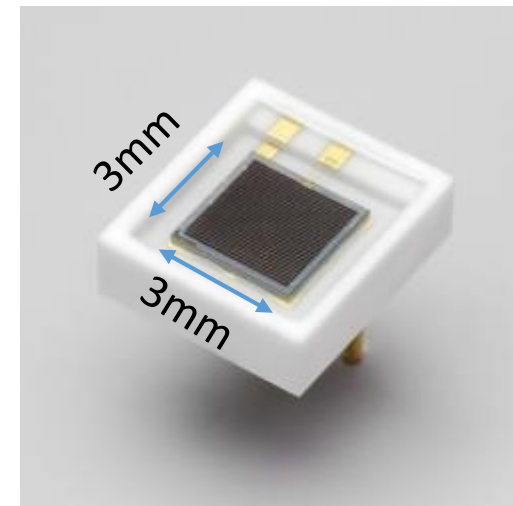
- An electrical SiPM-like signal is injected into the FastIC for energy evaluation using an AWG
- Linearity error is below 3% over the whole dynamic range
- Saturation is reached at 25 mA input current (positive polarity) and 20 mA (negative polarity)
- Summation in the energy is linear, independently of the channels added
- This makes FastIC very versatile and suitable for LYSO/LSO, BGO, Cherenkov, Monolithic, etc.



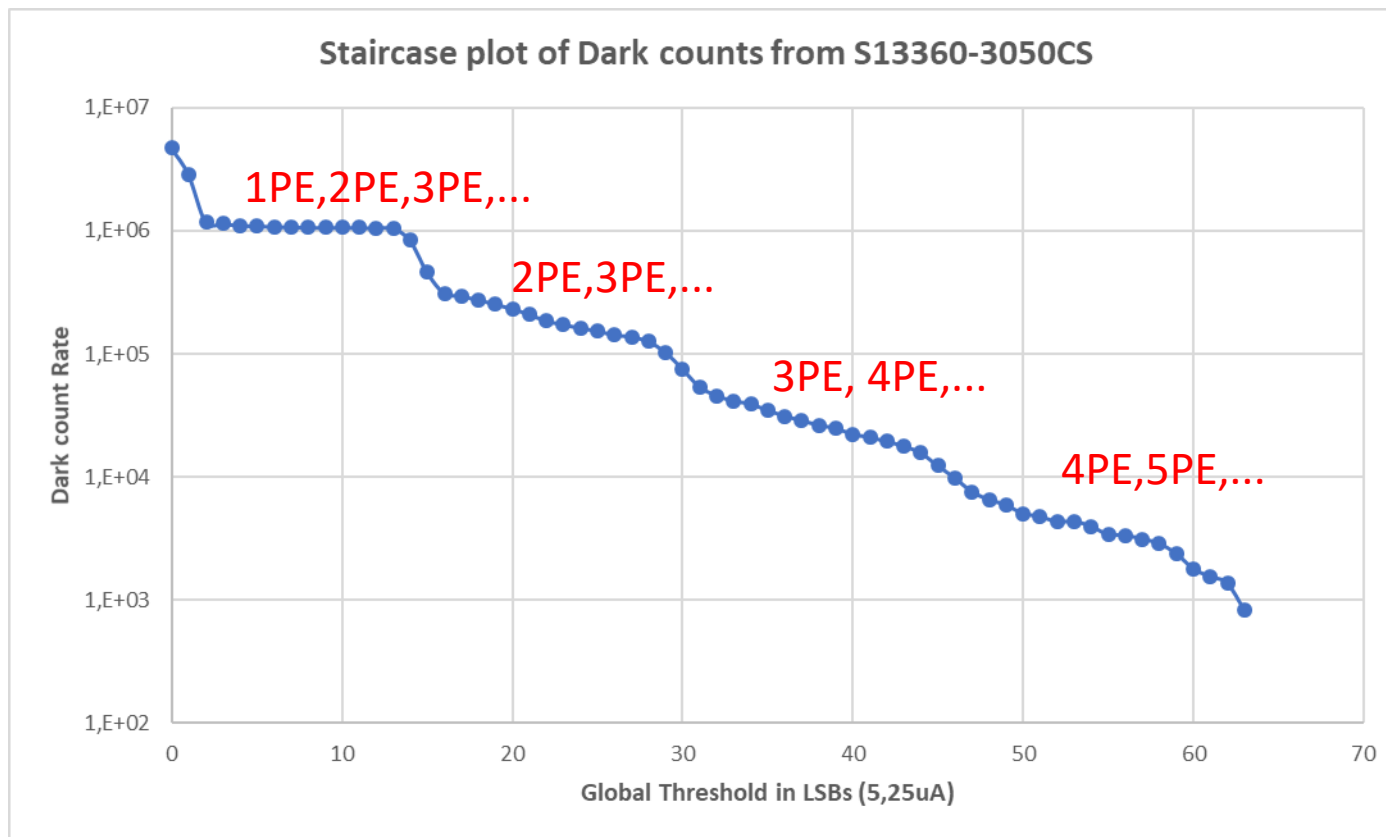
The FastIC project: measurements with sensors

SiPM measurements

- Positive Input stage
- SiPM S13360-3050CS operated at 60V of HV (Over-voltage $\sim 7.6V$)

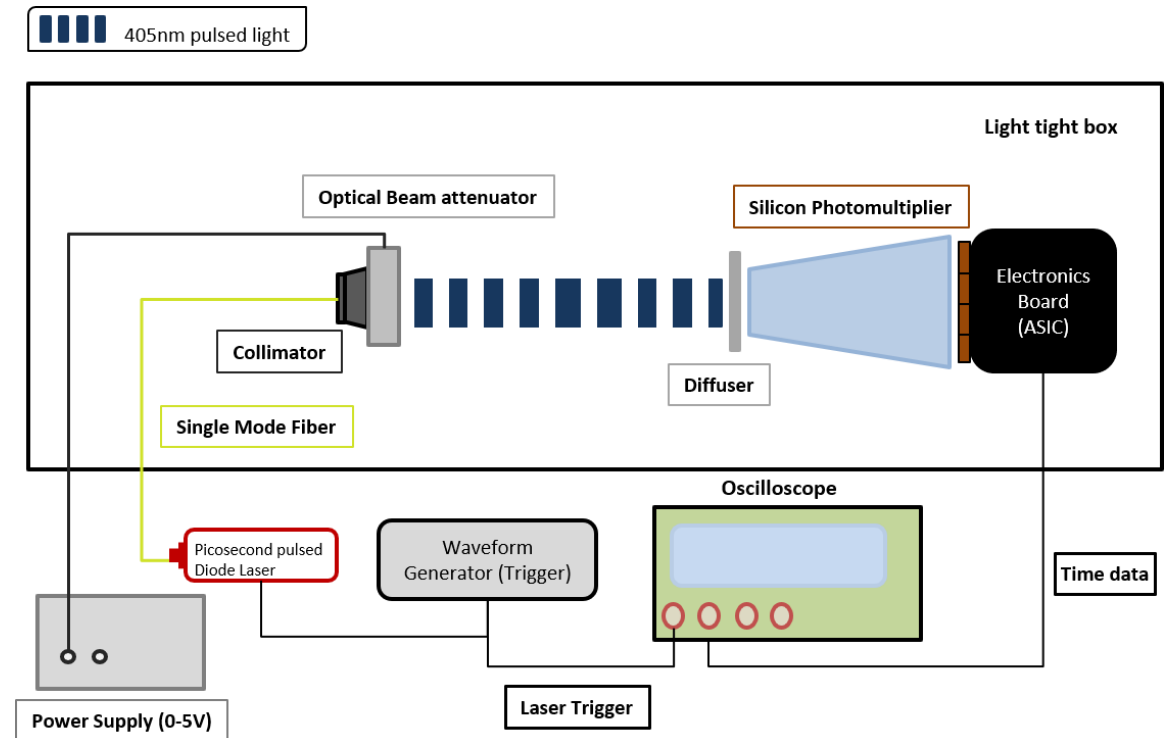
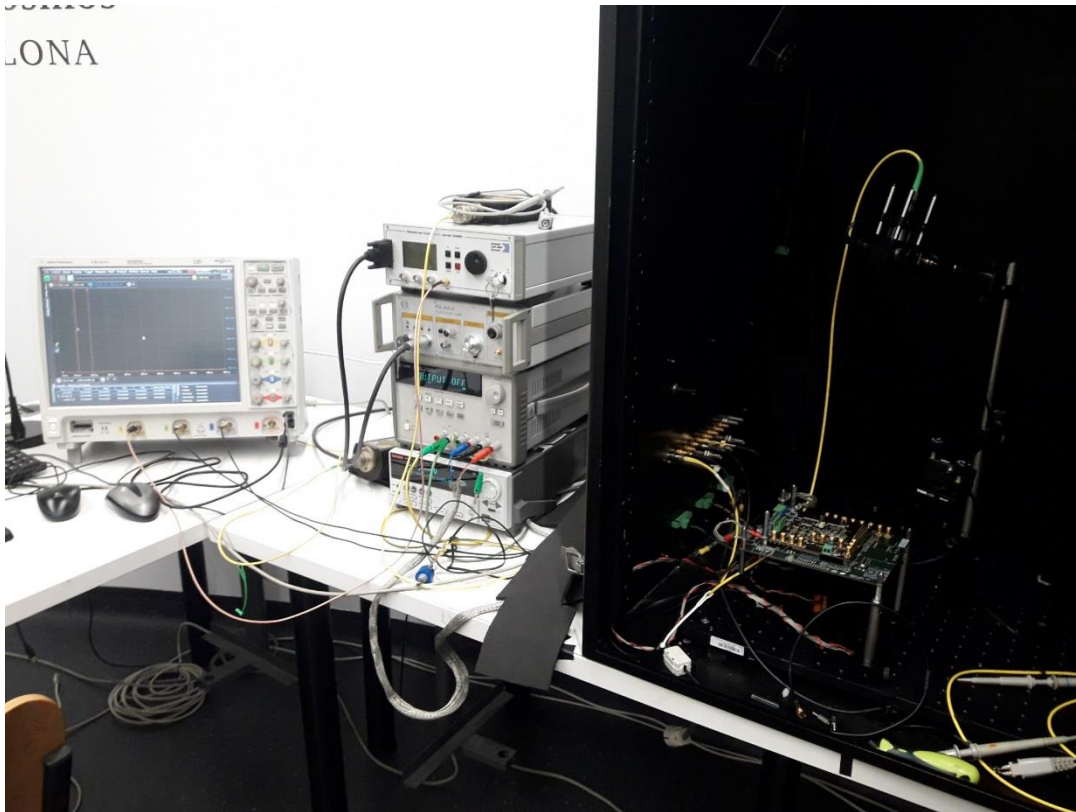


SiPM Hamamatsu
S13360-3050CS

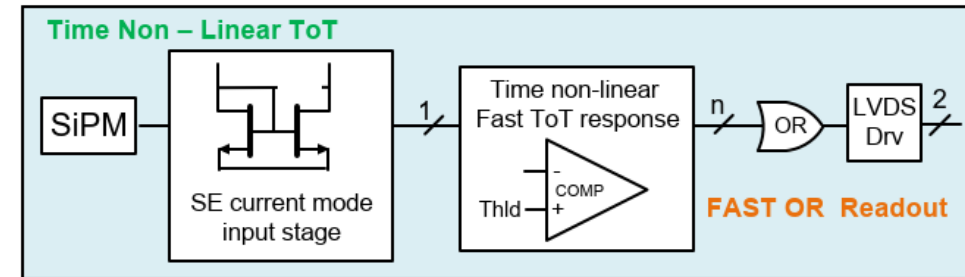
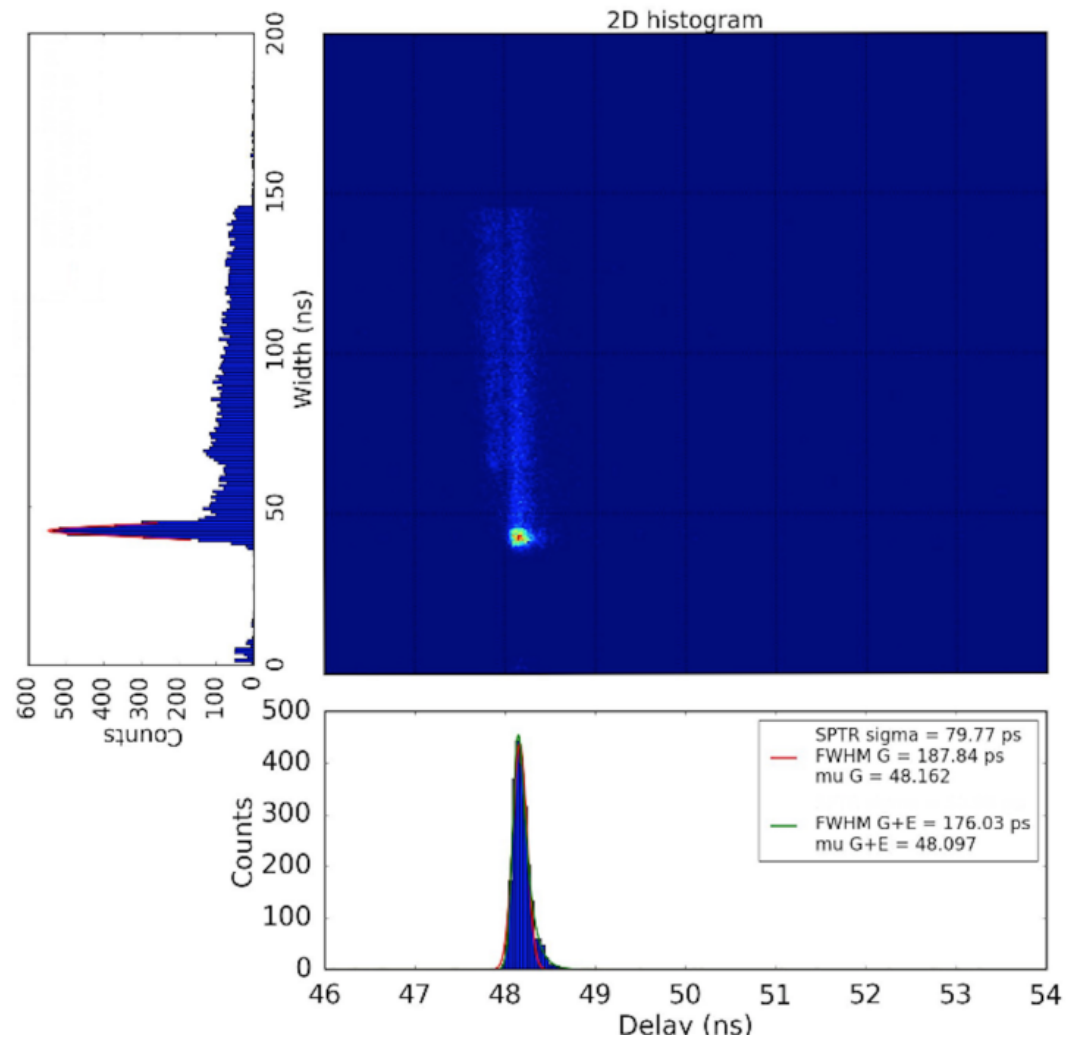


Setup for SPTR measurement

- Laser (405 nm) – 40 ps FWHM pulse width



SPTR measurement



Hamamatsu S13360-3050CS (3x3 mm² 50μm cell pitch, $V_{OV}=11V$)

SPTR= 176 ± 5 ps FWHM

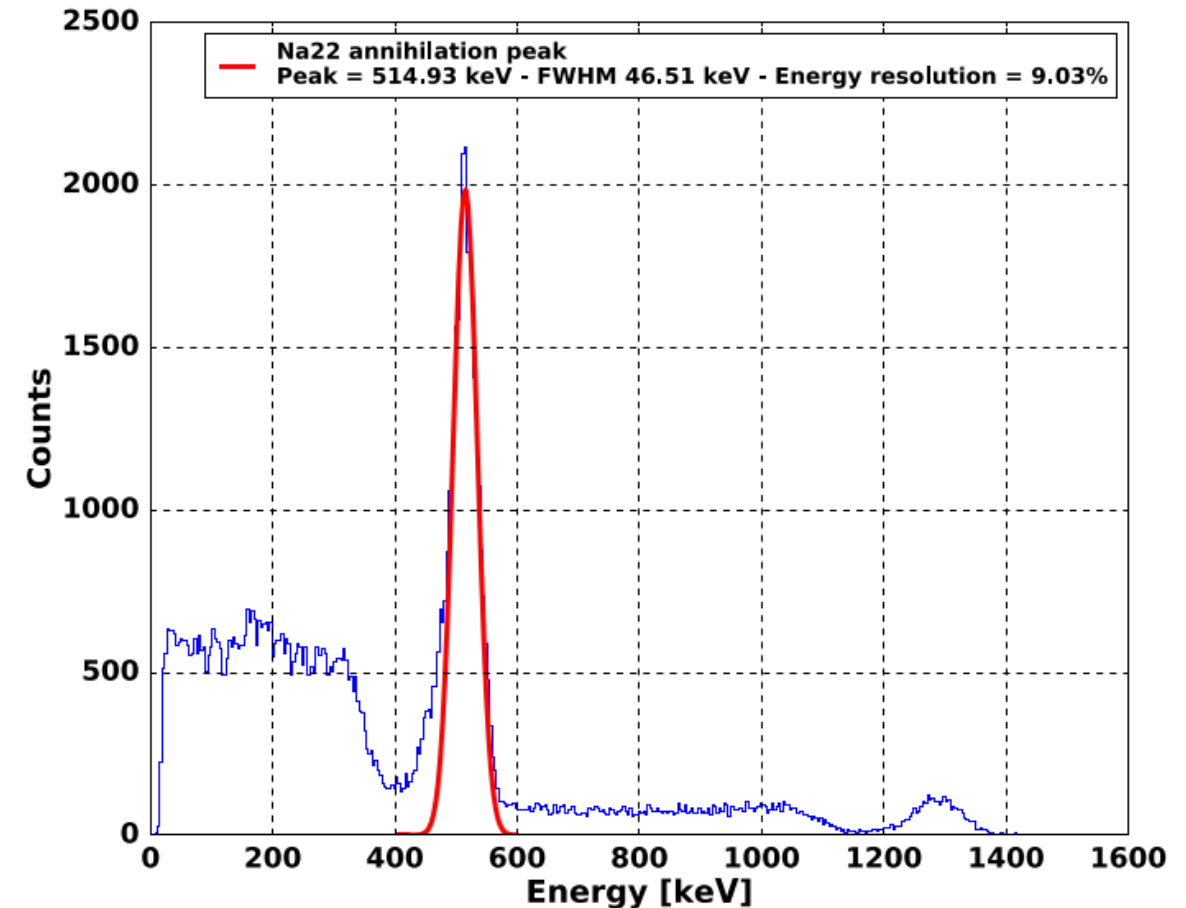
FBK NUV-HD Low Field V2 (3.12x3.2 mm² 40μm cell pitch, $V_{OV}=10.5V$)

SPTR= 151 ± 5 ps FWHM

Energy resolution measurement

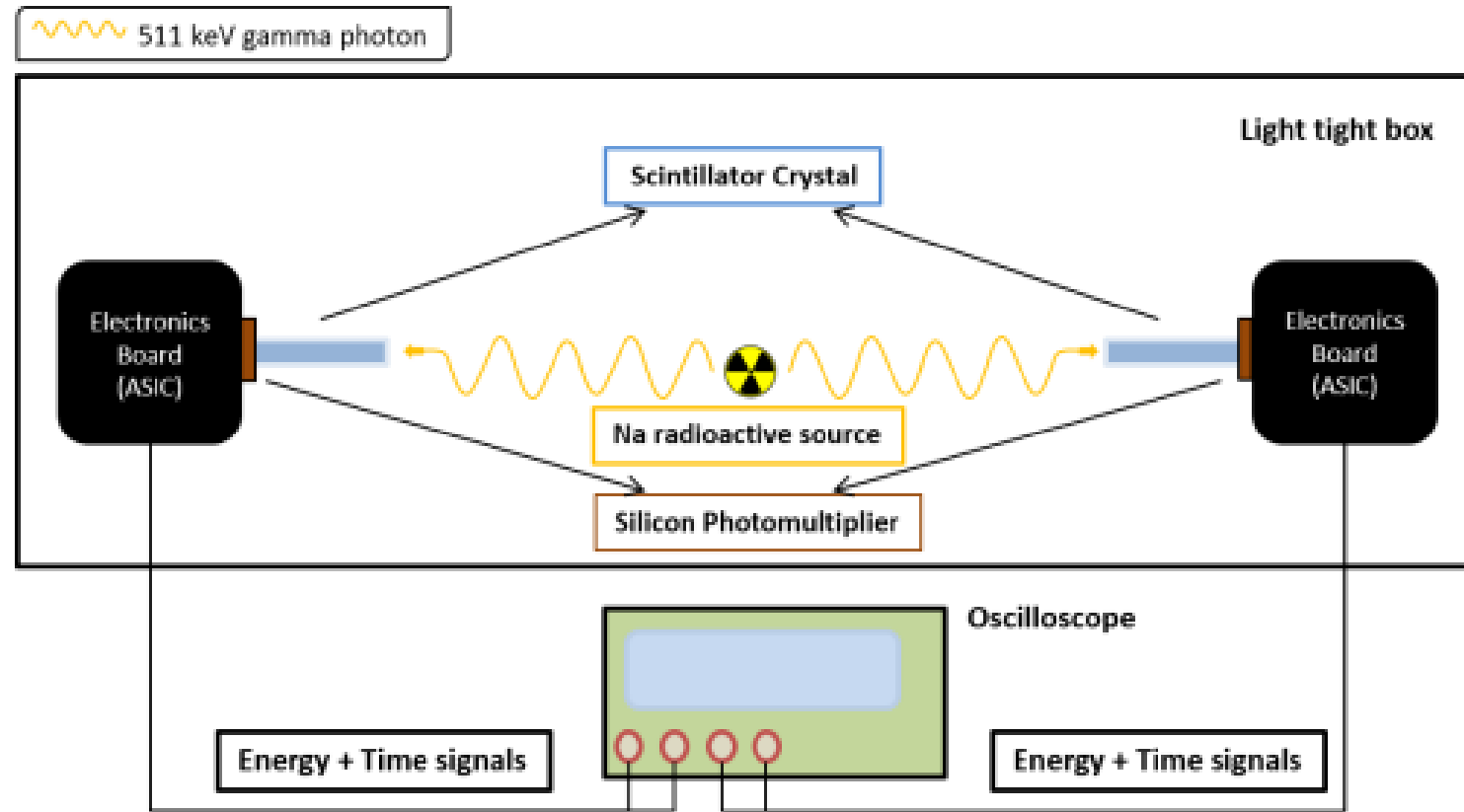
- The Energy Resolution was measured with a ^{22}Na source
- The TDC implemented in the FPGA was used to digitize the data
- Crystal: LYSO:Ce:0.2%Ca $3.13 \times 3.13 \times 20 \text{mm}^3$
- SiPM: Hamamatsu S13360-3050CS ($3 \times 3 \text{ mm}^2$ $50 \mu\text{m}$ cell pitch, $V_{OV}=3\text{V}$)
- Compton edges and gamma peaks are used to calibrate the nonlinearities of the SiPM*
- Energy resolution expressed in FWHM/μ [%].

Energy resolution of 511 keV ^{22}Na ~9%



S. Gómez

Coincidence Time Resolution

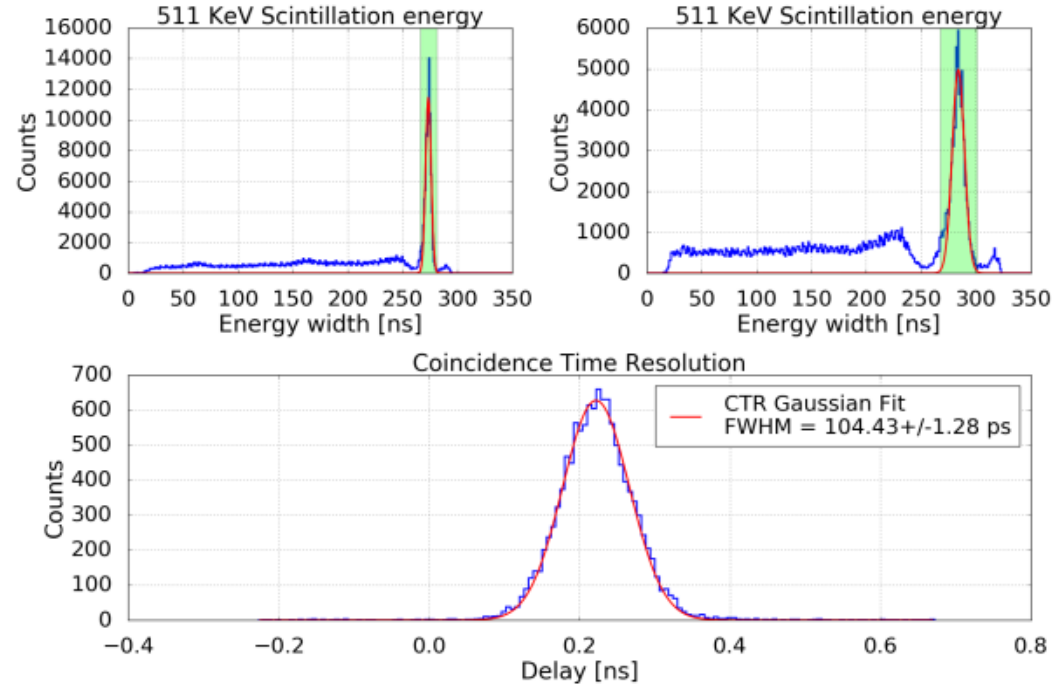
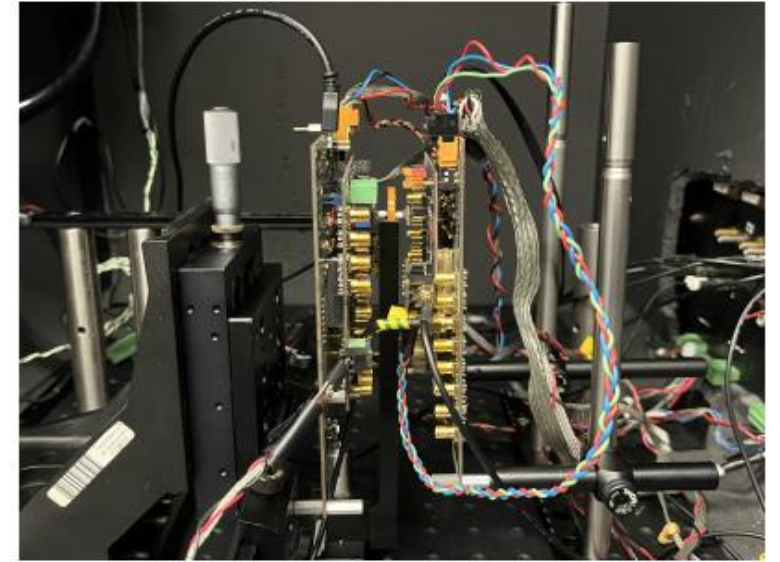


Coincidence Time Resolution

Crystal: LSO:Ce:0.2%Ca 2x2x5 mm², LY=39.2 ph/keV, $\tau_d \sim 32$ ns

SiPM: Hamamatsu S13360-3050CS (3x3 mm² 50 μ m cell pitch, $V_{OV}=8$ V)

CTR= 104 \pm 3 ps FWHM

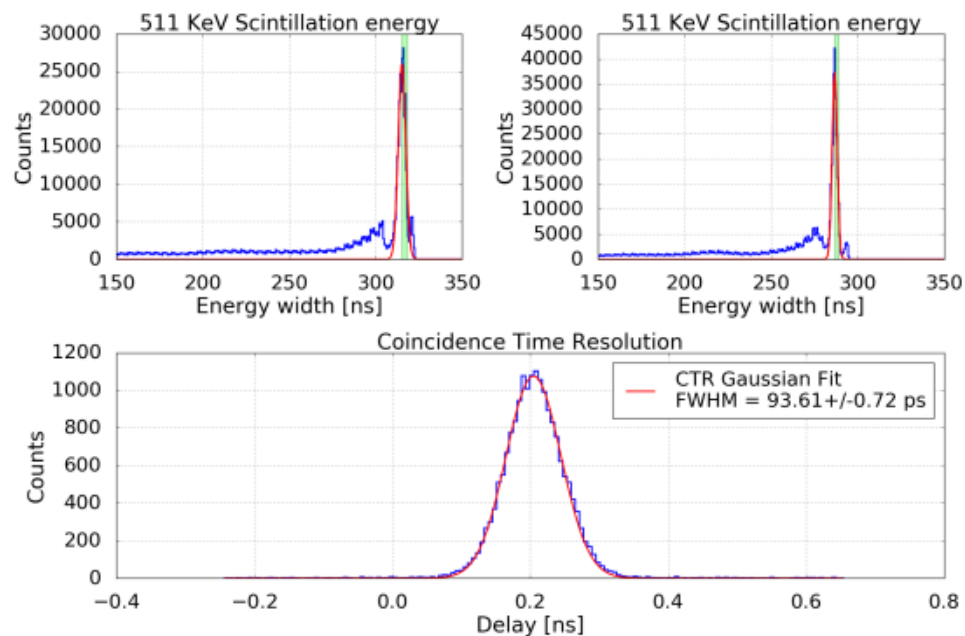


Coincidence Time Resolution

Crystal: LSO:Ce:0.2%Ca 2x2x3 mm², LY=39.2 ph/keV,
 $\tau_d \approx 32$ ns

SiPM: Hamamatsu S13360-3050CS (3x3 mm² 50 μ m
cell pitch, $V_{OV}=8$ V)

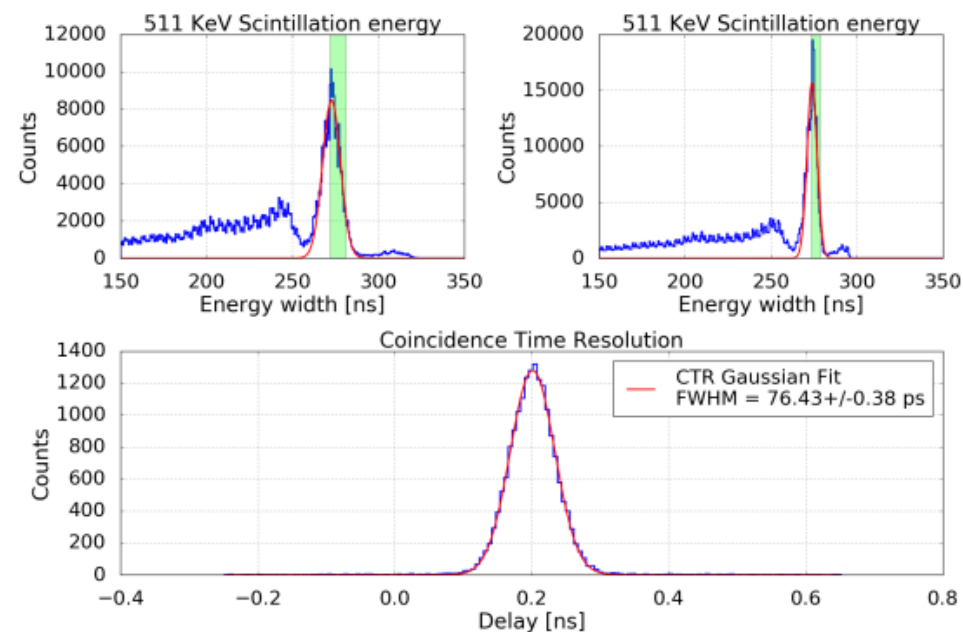
CTR = 93 \pm 3 ps FWHM



Crystal: LSO:Ce:0.2%Ca 2x2x3 mm², LY=39.2 ph/keV,
 $\tau_d \approx 32$ ns

SiPM: NUV-HD LF V2 (3.12x32 mm², 40 μ m cell
pitch, $V_{OV}=6.1$ V)

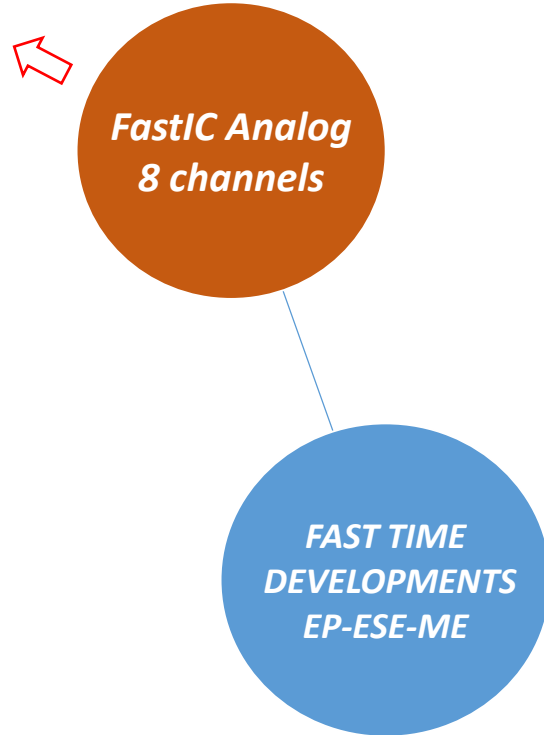
CTR = 76 \pm 2 ps FWHM



Design completed (CERN-UB)

FastIC Analog:

- Analog chip
- Generic
- Wide range C_{DET}
- Large dynamic range
- Signal summing
- Used with external TDC
- Not radiation hard



Design completed (CERN-UB)

FastIC Analog:

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Design ongoing (CERN-UB)

FastIC+:

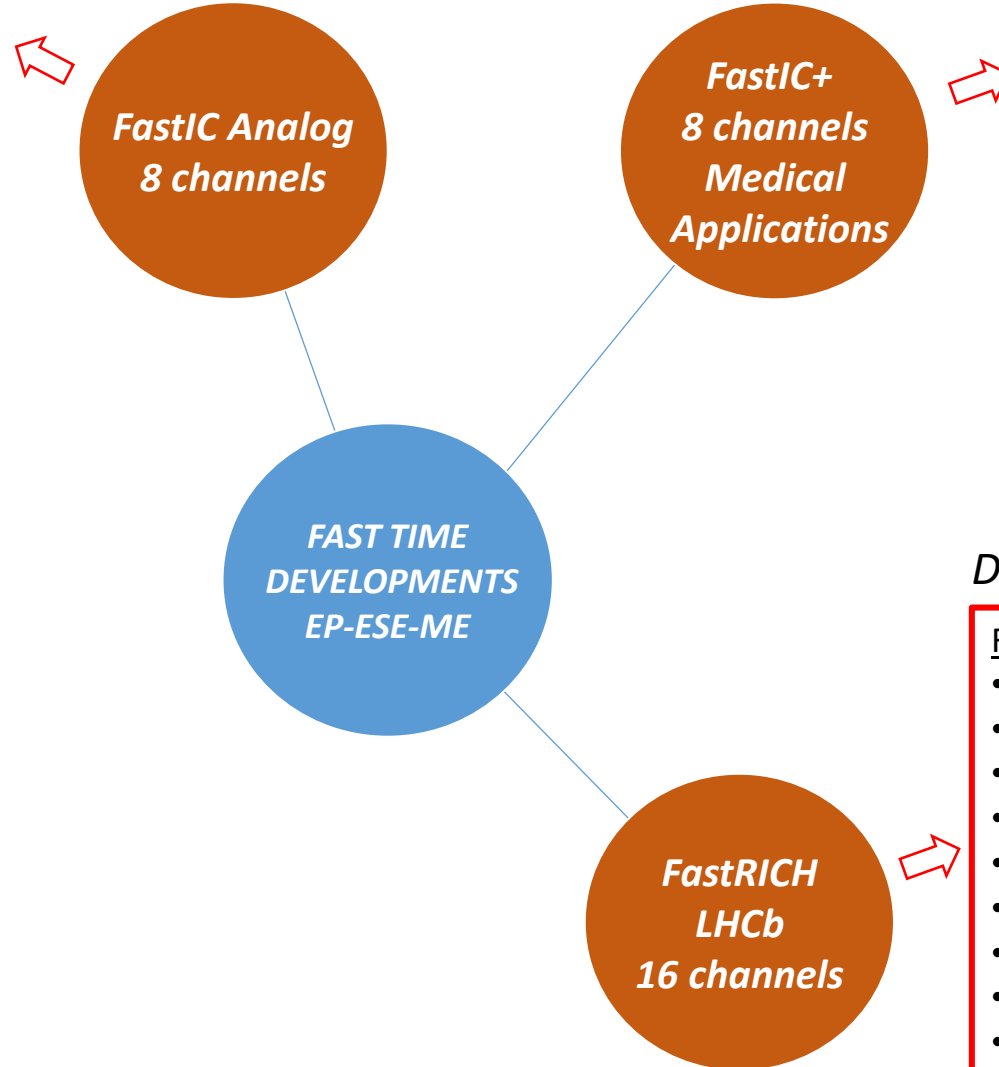
- Analog and Digital chip
- Generic
- Wide range C_{DET}
- Large dynamic range
- Signal summing
- Used with internal ~ 25 ps bin TDC
- Not radiation hard



Design completed (CERN-UB)

FastIC Analog:

- Analog chip
- Generic
- Wide range C_{DET}
- Large dynamic range
- Signal summing
- Used with external TDC
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Design ongoing (CERN-UB)

FastIC+:

- Analog and Digital chip
- Generic
- Wide range C_{DET}
- Large dynamic range
- Signal summing
- Used with internal ~ 25 ps bin TDC
- Not radiation hard

Design ongoing (CERN-UB)

FastRICH:

- Analog And Digital chip
- Application specific
- Smaller range C_{DET} (PMTs/Small SiPMs)
- Small dynamic range (single photon operation)
- No signal summing
- Internal TDC (~ 25 ps bin TDC)
- ~ 2 ns Gate (duration/phase programmable)
- CFD
- Radiation hard

Towards FastRICH

- FastRICH is based on the experience from the CERN-UB team on the design of FastIC for the readout of fast detectors
- The design involves major changes in the analog part, the implementation of a TDC and a full digital readout
- The chip provides a radiation hard (TID and SEE), low power and compact system for the LHCb RICH detector for interfacing with the detector on one side and on the other with IpGBT/optical links
- The chip aims at reducing the amount of data generated
 - With Zero Suppressed Readout
 - A programmable ~ 2 ns Shutter signal
 - A Constant Fraction Discriminator (CFD)
- And also a configurable number of output links (1/2/4) to adapt to the occupancy of the different regions of the experiment

Design completed (CERN-UB)

FastIC Analog:

- Analog chip
- Generic
- Wide range C_{DET}
- Large dynamic range
- Signal summing
- Used with external TDC
- Not radiation hard



*FastIC Analog
8 channels*

Design ongoing (CERN-UB)

FastIC+:

- Analog and Digital chip
- Generic
- Wide range C_{DET}
- Large dynamic range
- Signal summing
- Used with internal ~ 25 ps bin TDC
- Not radiation hard



*FastIC+
8 channels
Medical
Applications*

**FAST TIME
DEVELOPMENTS
EP-ESE-ME**

Design ongoing (CERN-UB)

FastRICH:

- Analog And Digital chip
- Application specific
- Smaller range C_{DET} (PMTs/Small SiPMs)
- Small dynamic range (single photon operation)
- No signal summing
- Internal TDC (~ 25 ps bin TDC)
- ~ 2 ns Gate (duration/phase programmable)
- CFD
- Radiation hard



*FastRICH
LHCb
16 channels*



*Future
developments*

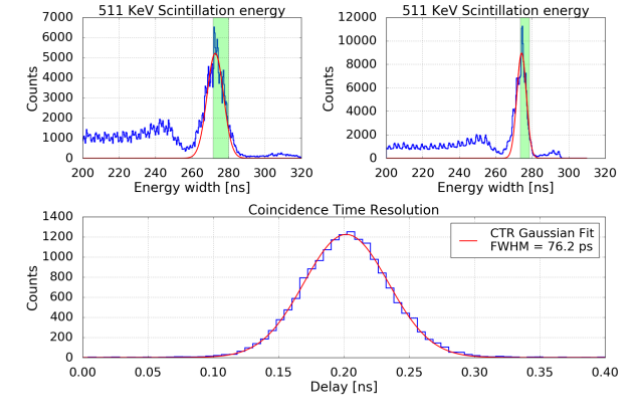
Future Roadmap

- Emphasis on module
- Analog and Digital chip
- **Pixelized, Sensor co-design, hybrid integration**
- More channels
- Smaller range C_{DET}
- Large dynamic range
- No signal summing
- Used with internal TDC

Summary of results with FastIC

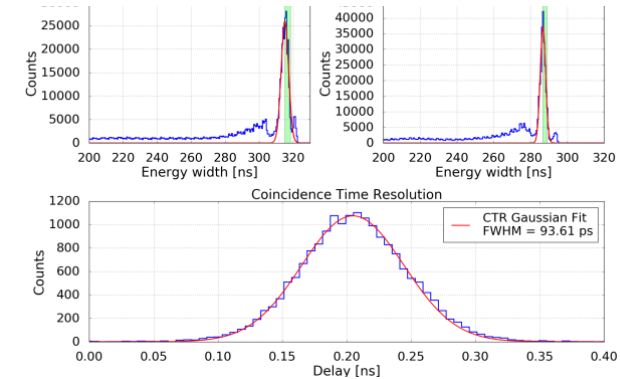
- Single Photon Time Resolution (SPTR) measurements
 - Blue light laser (PiL040X, 405nm, jitter <3ps, pulse width <45ps)
 - Agilent MSO 9404A, 4GHz, 20GS/s
 - 18°C Temperature
 - 176 ±3ps FWHM (HPK SiPM S13360-3050CS, 3x3mm² V_{OV}=10.6V)
 - 151 ±3ps FWHM (FBK HD-NUV Low Field SiPM, 40µm cell, 3.12x3.12mm² V_{OV}=10.6V)
 - Fits with the initial spec ~30ps_{rms} contribution from electronics with large SiPM
- Coincidence Time Resolution (CTR) measurements
 - LSO:Ce:0.2%Ca 2x2x3mm³
 - 93 ±3ps FWHM (HPK SiPM S13360-3050CS, 3x3mm² V_{OV}=8V)
 - 76 ±2ps FWHM (FBK HD-NUV Low Field SiPM, 40µm cell, 3.12x3.12mm² V_{OV}=6.1V)
- Linearity error <3% up to 25mA (+ polarity stage) or up to 20mA (- stage)
- 9% energy resolution for 511keV (LYSO:Ce:0.2%Ca 3.13x3.13x20mm³)
- R5900 Hamamatsu PMT, 800V.
 - Jitter of ~340 ps FWHM, which corresponds to the intrinsic PMT time uncertainty when detecting tens of photons.
- Two spin-off projects: FastIC+ and FastRICH

CTR measurement with 2 × 2 × 3 mm³ LSO:Ce0.2%Ca crystals coupled to FBK (a) and HPK (b) devices in coincidence (20 K events used).



(a) FBK HD-NUV Low Field SiPM at 7 V of over-voltage.

FBK HD-NUV Low Field SiPM at 6.1 V of over-voltage.



HPK S13360-3050PE SiPM at 8 V of over-voltage.

