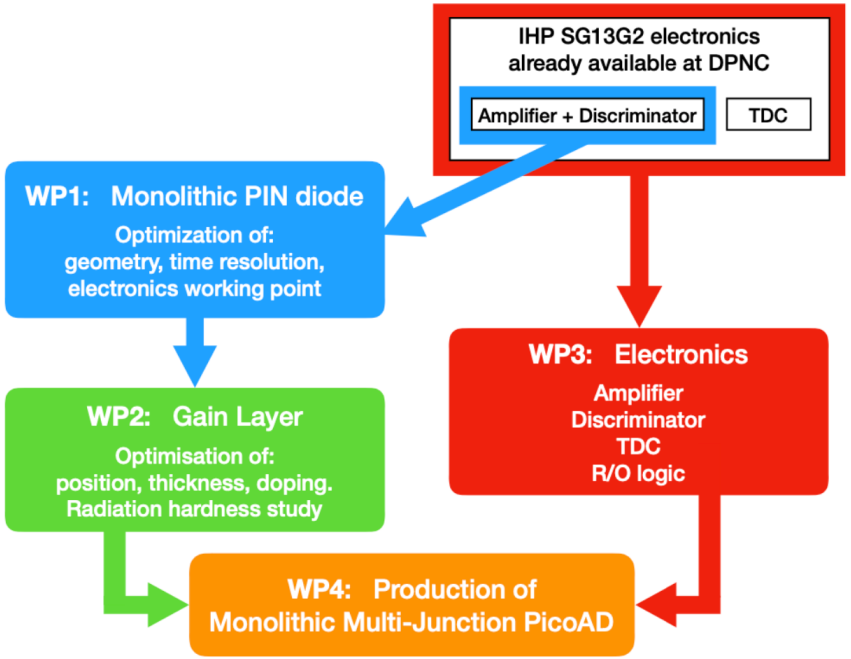
MONOLITH ERC project

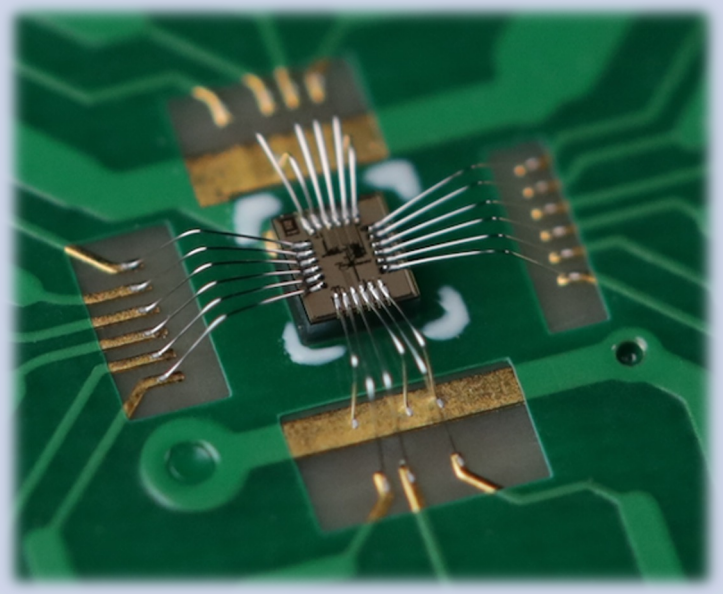


H2020 ERC Advanced grant 884447,
July 2020 - June 2025

Low Power and scalability
Small Area for integration
Time resolution of ≈1ps

UNIVERSITÉ DE GENÈVE
FACULTY OF SCIENCE
Department of Nuclear and Particle Physics

Monolith TDC



130nm CMOS – (SiGe IHP Bi-CMOS, no BJT used)

Method described in patent:
EP 3 591 477 A1
Sampling of a free running oscillator combined with frequency measurement for the relative time of arrival measurement

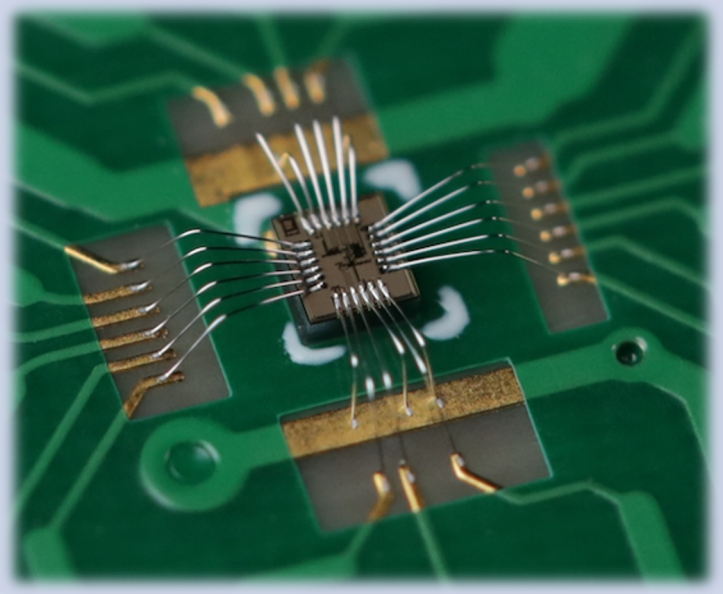
Target time resolution 1ps

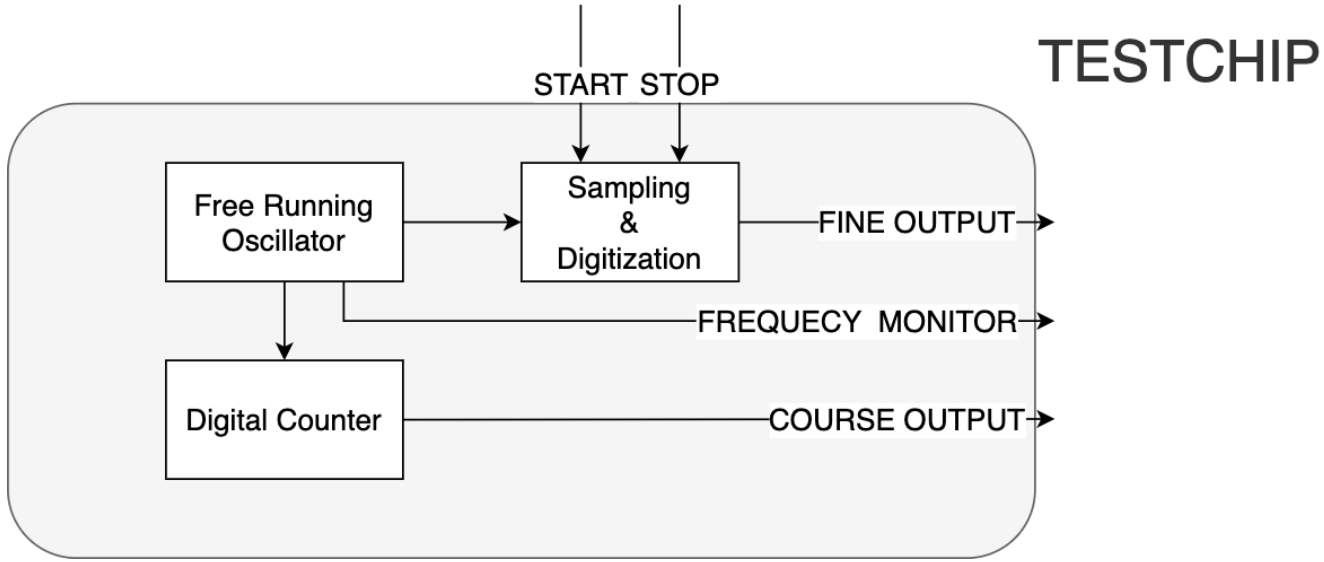
Proof of concept prototype: September 2020

3 new versions available since July 2022
- New power supply layout
- 2 versions of free running oscillator
- Triple well implementation

Embedded in MONOLITH 2021 prototype

TDC TESTCHIP





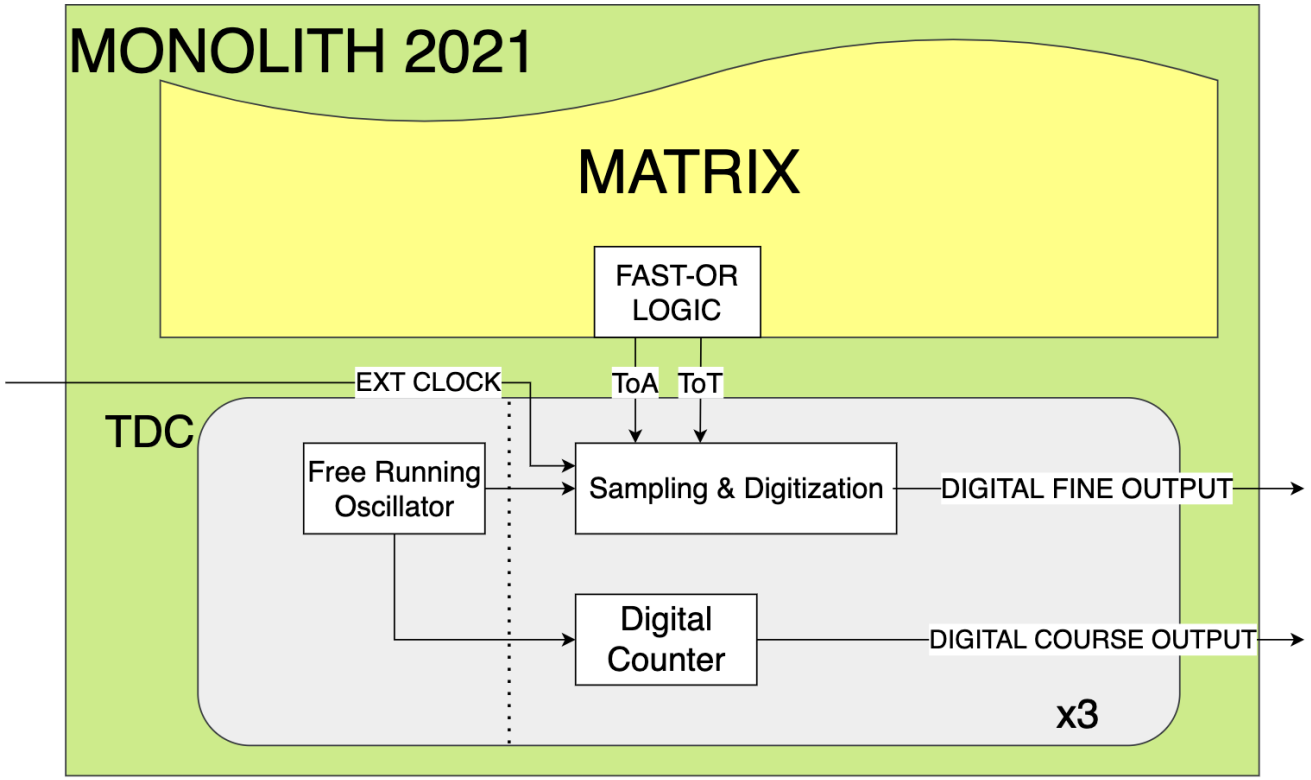
Proof of concept test chip:

Test chip AREA 1mm x 1mm

Oscillator AREA 900µm^2

Power Consumption Oscillator ≈3.8mW

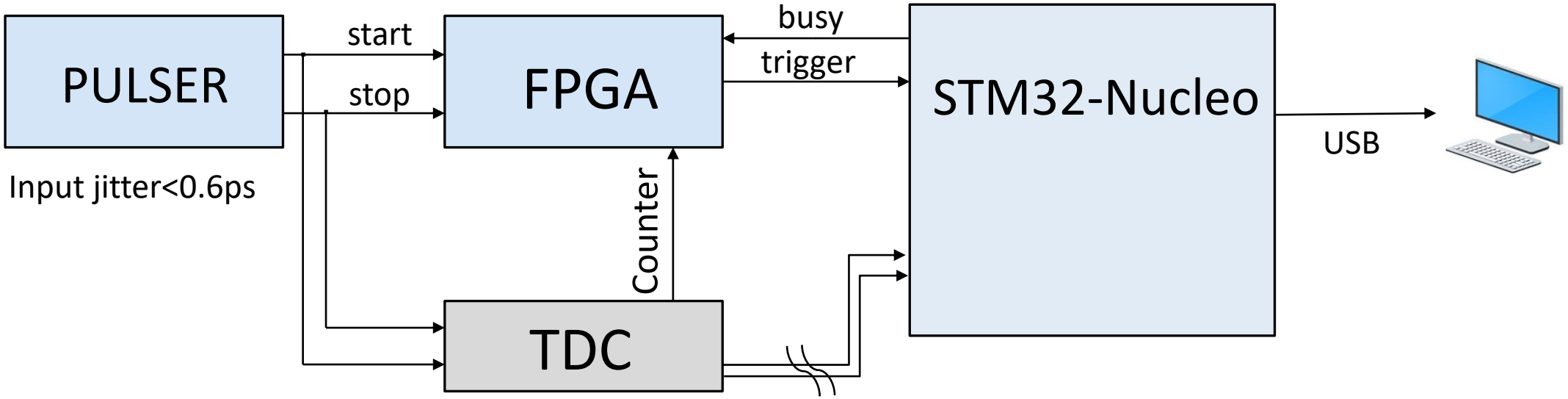
TDC in MONOLITH 2021



Embedded in triple well

A bug on the FAST-OR has been fixed in the last MONOLITH, test on TDC will start soon

Test chip measurement setup

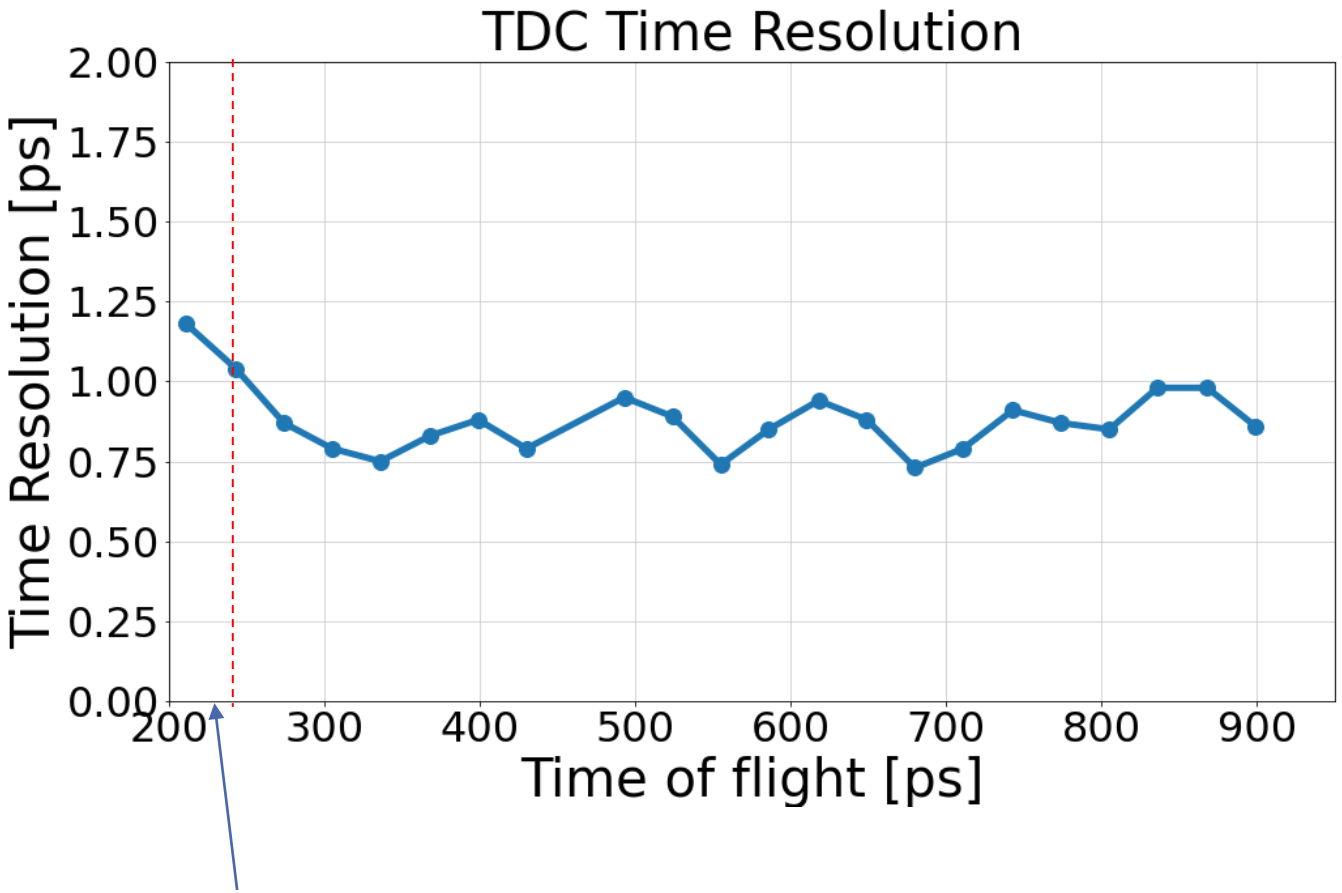


Software calibration:

The oscillation period of ≈460ps is divided into N bins via software.

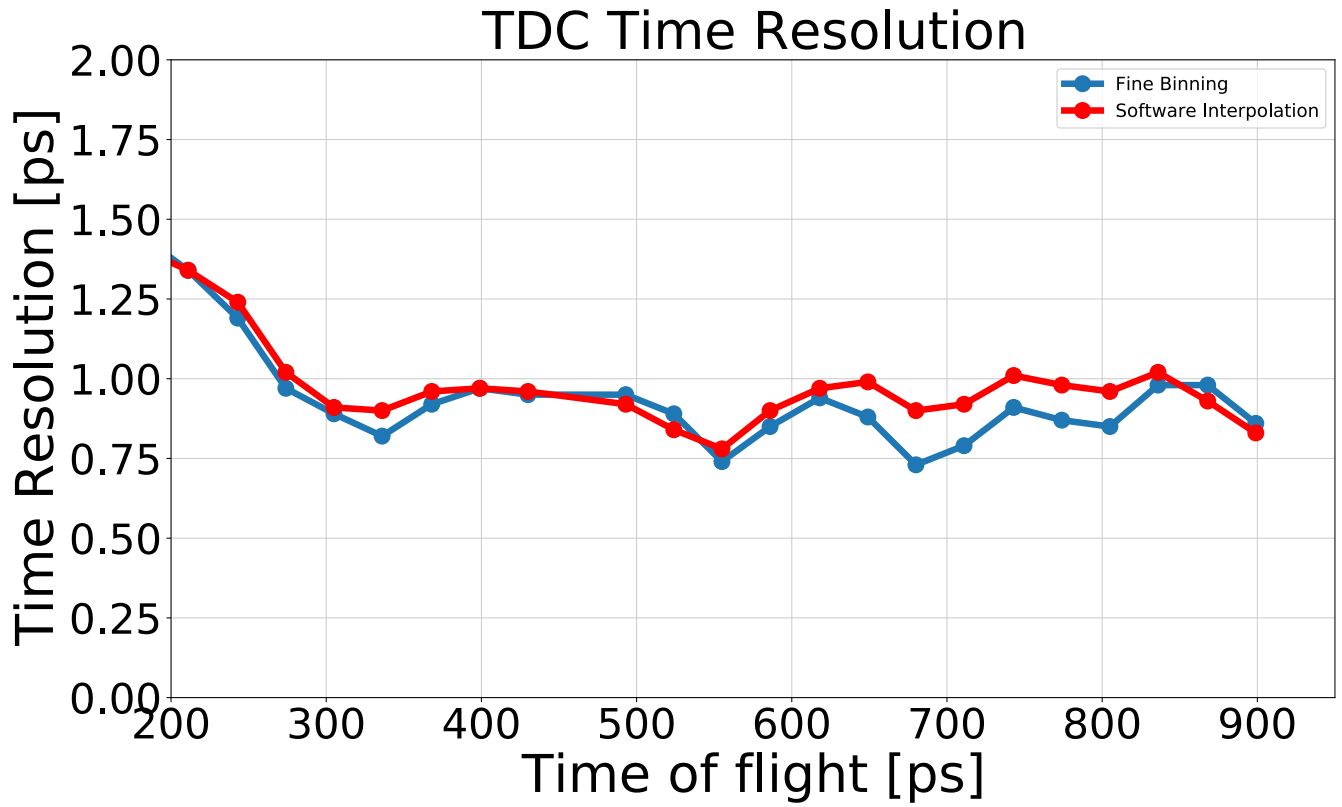
Best performance with 512 bins (≈0.9ps bin width)

TEST CHIP Timing performance



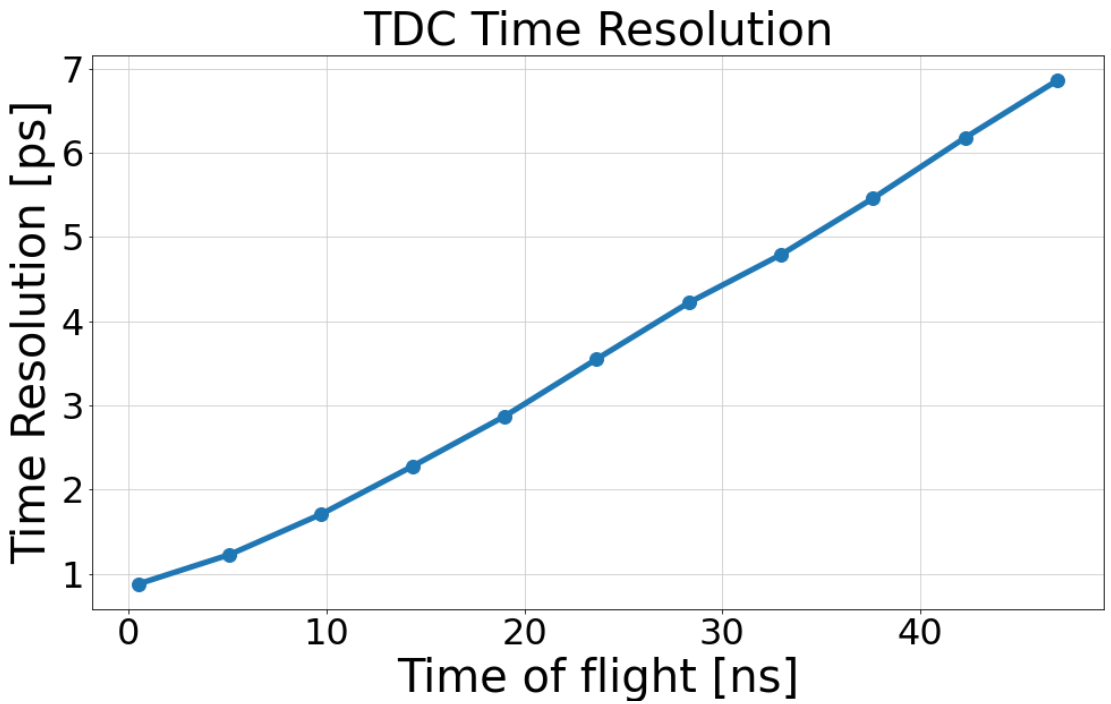
Short TOF affected by Start over Stop influence.

TEST CHIP Timing performance



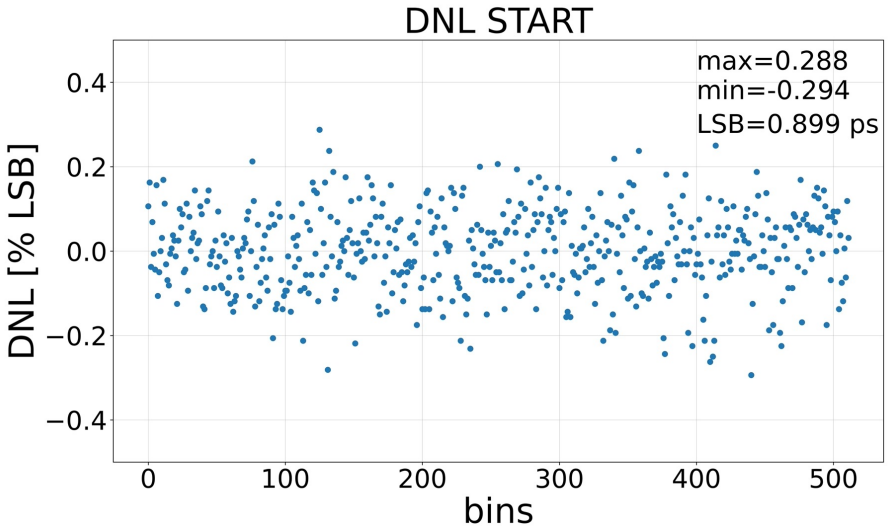
The same performance can be obtained by reducing the number of bins used for slicing the oscillation period and interpolating

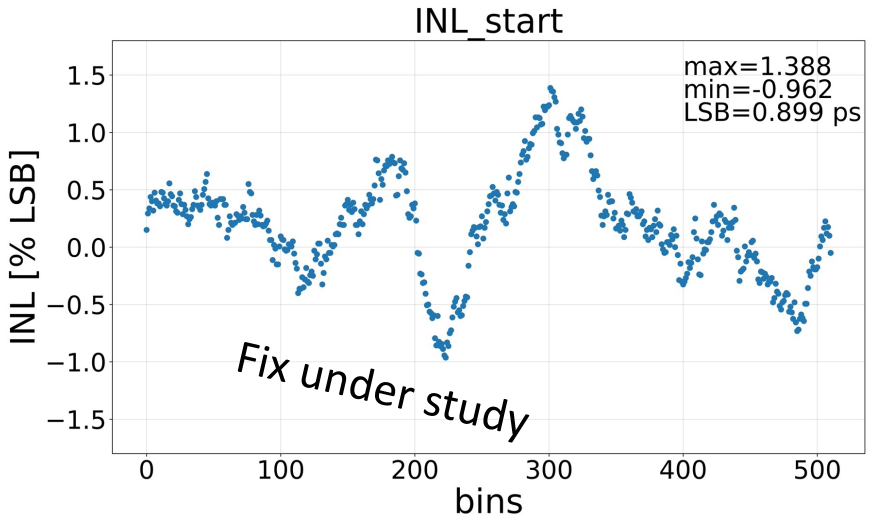
Dynamic range



Jitter increase linearly with the number of periods of the free running oscillator.
It can be improved with a better measurement of the frequency.
Current dynamic range ≈300ns

TEST CHIP Timing performance

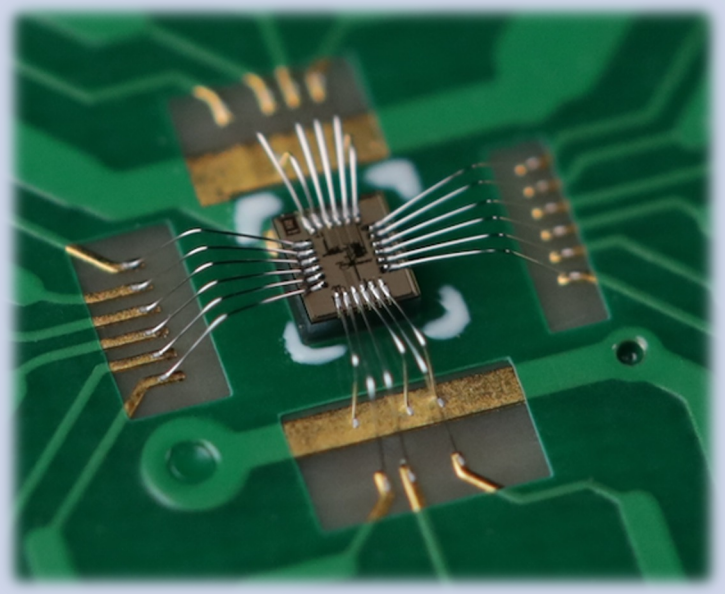




Next steps

Characterization

- Complete test on the available prototype
- Climate chamber measurement
- Start testing TDC embedded in MONOLITH 2021



Planned chip submissions

Dedicated test chips for optimization of TDC building blocks

Multichannel TDC

- 16 Channels with ADC

Design and test team

Roberto Cardella
Design

Fulvio Martinelli
Design

Antonio Picardi
Design and test

Luca Iodice
Test

Prof. Cardarelli, Prof. Iacobucci