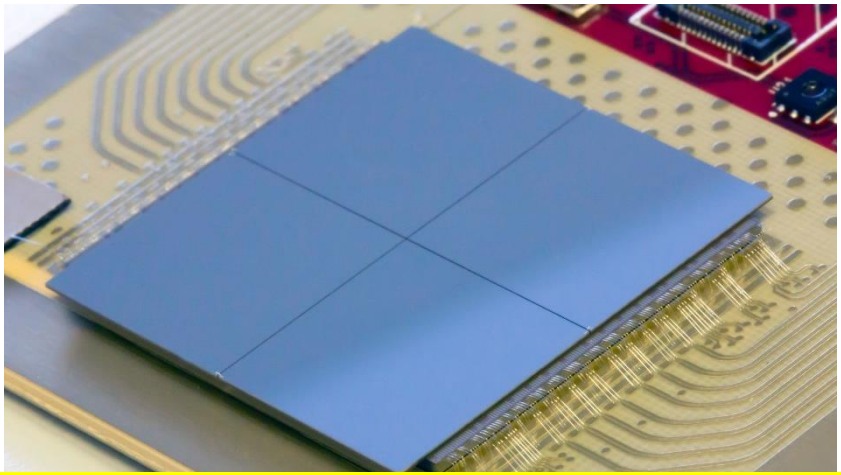
The PicoPix Project

Xavier Llopart

5th September 2022

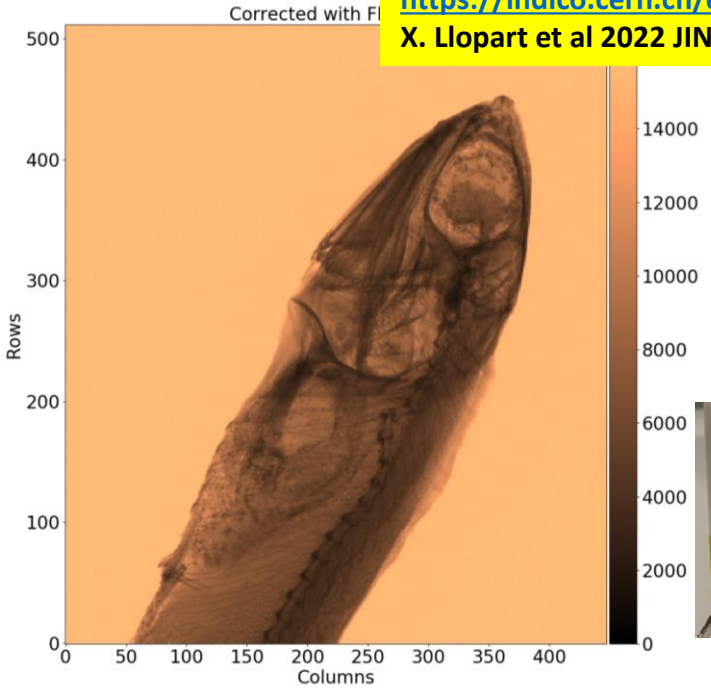
Timepix4 (2019)

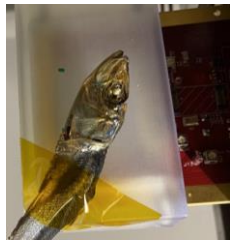
Technology			65nm – 10 metal
Pixel Size			55 x 55 µm
Pixel arrangement			4-side buttable 512 x 448
Sensitive area			6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA
		Event Packet	64-bit
		Max rate	**3.58x10^6 hits/mm^2/s**
		Max Pix rate	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	CRW: PC (8 or 16-bit)
		Frame	Not-zero-suppressed
		Max count rate	~5 x 10^9 hits/mm^2/s
TOT energy resolution			**< 1Kev**
Time resolution			**195ps bin → ~60ps$_{rms}$**
Readout bandwidth			16x @10.24 Gbps
Minimum threshold			<500 e^-



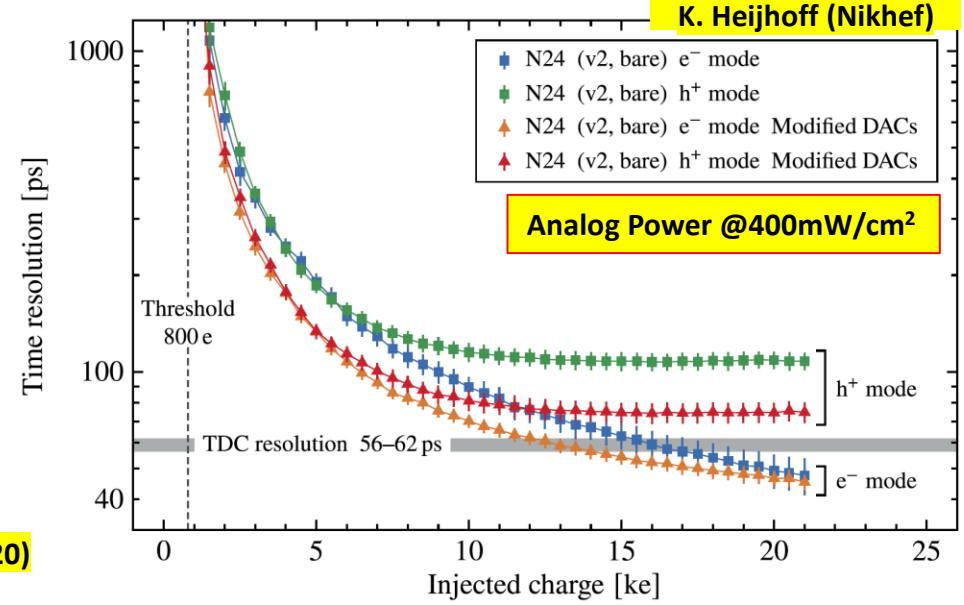
Timepix4v0 with 4x300 µm (256x256) edgeless Si sensor (August 2020)

https://indico.cern.ch/event/1121147
X. Llopart et al 2022 JINST 17 C01044





K. Heijhoff (Nikhef)



Initial LHCb requirements for Velopix2

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

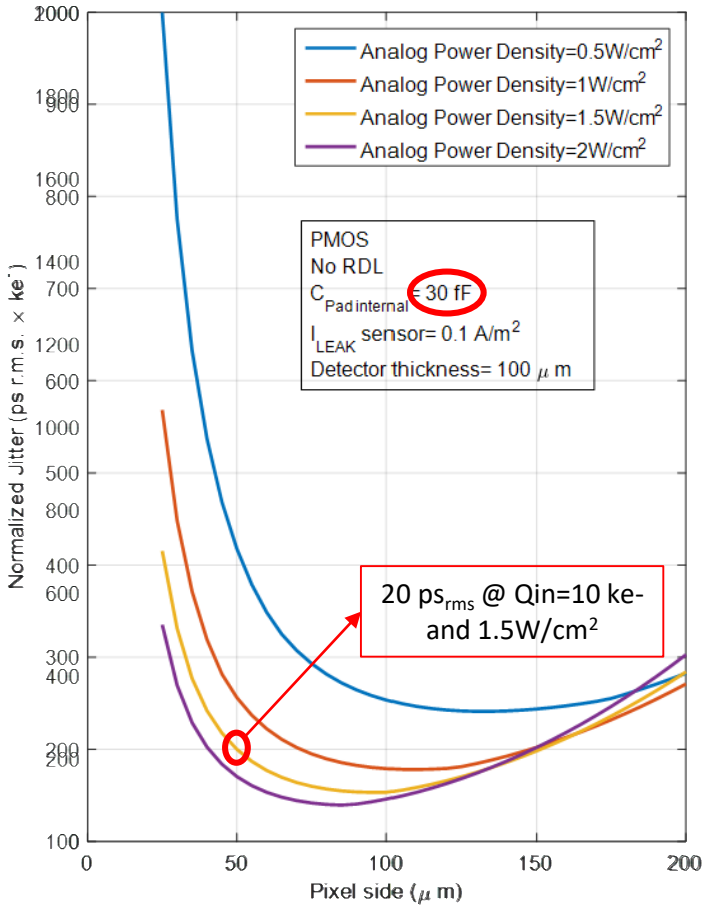
Priority

Challenging!

doable

Beyond Timepix4 → sub-25ps time resolution?

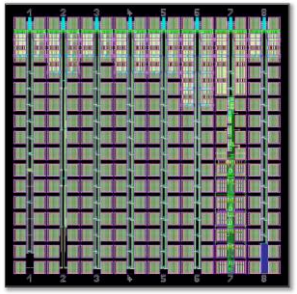
- Sensor: thin planar, LGAD, 3-D, …
  - Radiation hardness, input capacitance, …
- Front-end: There is a limit on time resolution that are achievable for small pixels with limited power
- TDC: Distribution of reference clock with <20ps skew for large pixel arrays:
  - N. Egidos et al., "20-ps Resolution Clock Distribution Network for a Fast-Timing Single-Photon Detector," in IEEE Transactions on Nuclear Science, vol. 68, no. 4, pp. 434-446, April 2021, doi: 10.1109/TNS.2021.3057581.
- High-speed serial links > 20-40 Gbps



R.Ballabriga, Fundamental limits to noise and time resolution in highly segmented hybrid pixel detectors: lessons learnt on the Timepix4 design [publication in preparation]

28nm TSMC HPC+ CMOS technology

- Overview:
  - Front-End Features:
    - 0.9V core transistors (thin oxide) and 1.8 I/O transistors (thick oxide)
    - Triple well, Deep N-Well (to isolate P-Wells)
    - Multiple Vt transistors (but only five different flavors in the same design: ulvt, lvt, reg, uhvt)
    - Only vertical poly (PO) is allowed → No ELTs
  - Many Std cell libraries (>2000) available with all flavors:
    - Row height, VTs, process, temperature and supply…
  - Back-End Features:
    - 9 copper layers plus last metal layer in AlCu pad



TID28

- Radiation hardness:
  - First indications shows that this tech is suitable for rad-hard designs
    - But no ELTs are possible
  - Tested up to 1 Grad with 30-50% Isat ON max degradation in core transistors

    Better than TSMC 65nm

Velopix2 demo chip → PicoPix

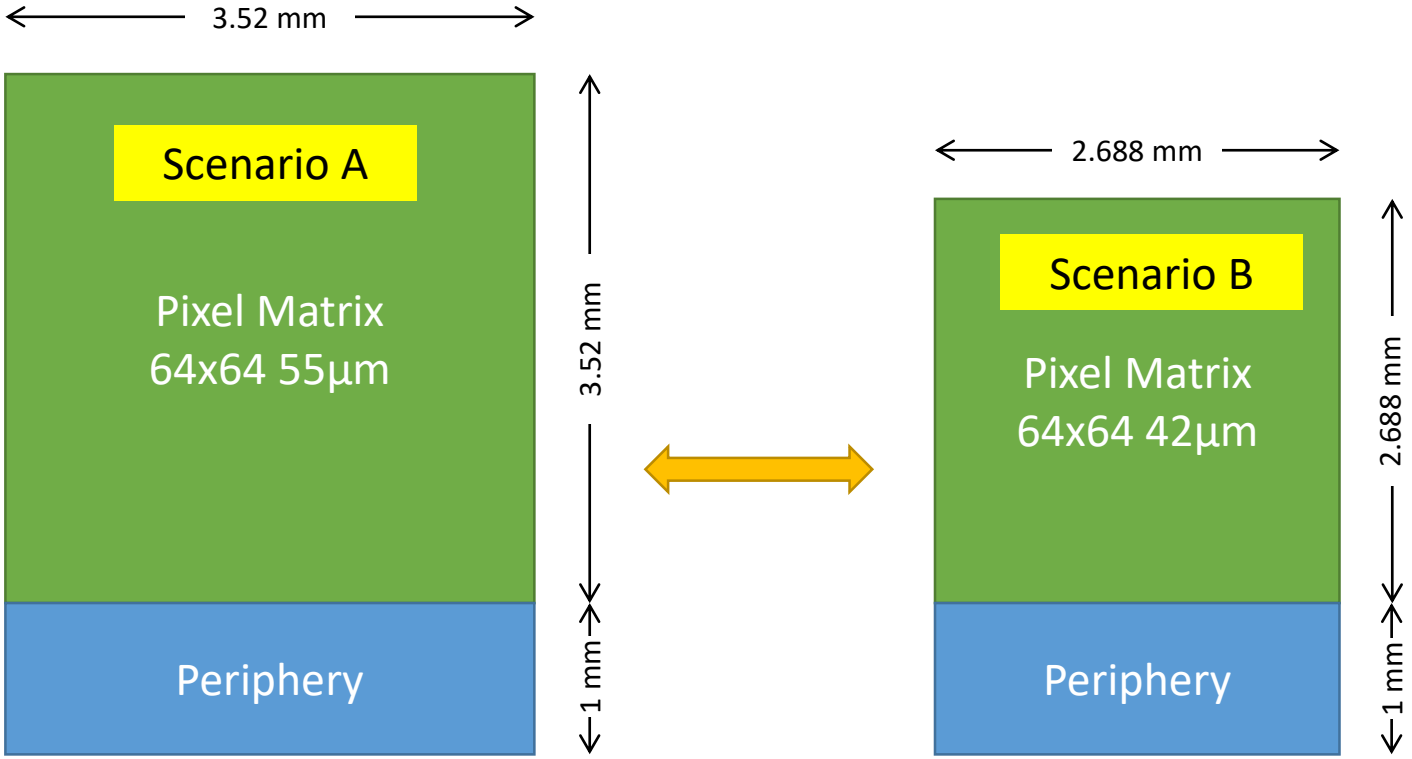
- Designed as a “real” small scale prototype of the large Velopix2:
  - Analog FE
  - Local VCO
  - Pixel data clustering
  - Pixel readout
  - SEE robust architecture
  - Clock distribution using dDLL approach (as in Timepix4)
  - High-speed links
  - On-chip Bandgap and biasing DACs
  - UVM Functional verification

- Chip should be ready to be bump bonded to different sensor types:
  - ACF Anisotropic Conductive Film

- Slow Control protocol can be simplified → reused from Medipix4/Timepix4?

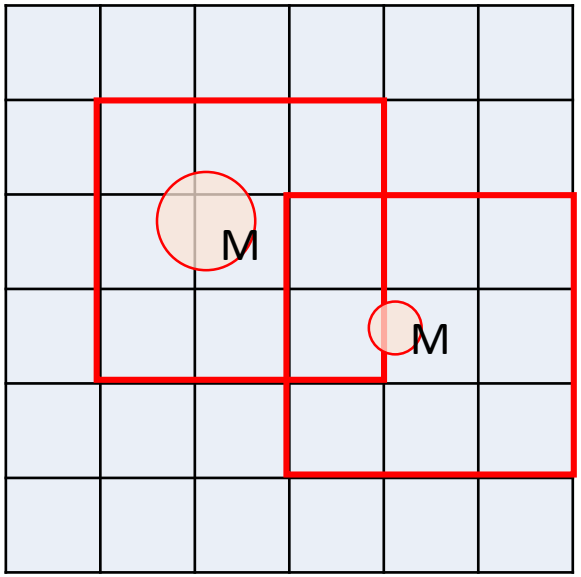
- Why?
  - CMOS 28nm technology is most certainly the choice for this project given the time scale and experience
  - Avoid to get false expectations on final design
  - If this design is successful the large scale chip should be simple and minimizes risk (time and money)

PicoPix ASIC



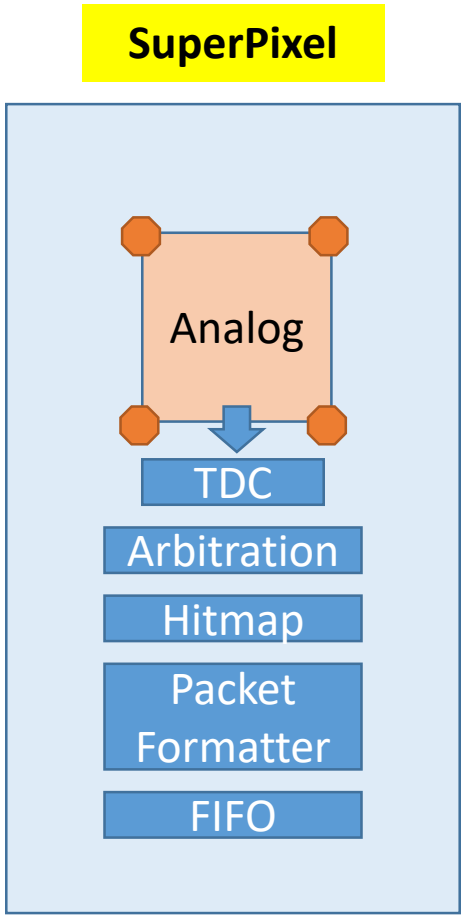
- Design time comparable to a full-scale design if targeting a “real” Velopix2 prototype
  - Might be spaced limited in the periphery…
- Bump-bonding with diced ASICs

On pixel event processing → Data reduction



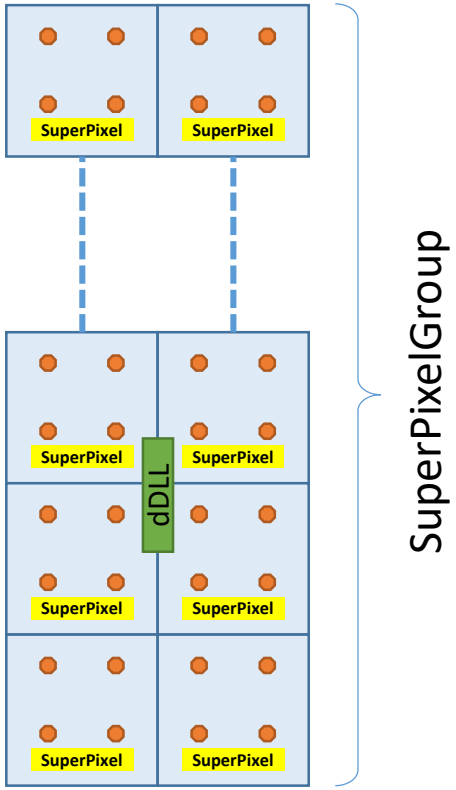
- Most events are clusters of 1-4 pixels
  - Readout only the largest event in a cluster → Best time (TOA) and energy (TOT) resolution
- Cluster events in X and Y in a single data output packets:
  - 1 data packet per cluster
  - Master (M) pixel found using arbitration circuitry as in Medipix4
  - TOA and TOT only on Master (M) pixel
  - Hitmap of pixels around Master (M)
- Advanced on-pixel data filtering possible:
  - Accept events only in certain TOT range
  - Accept events only in certain TOA range
  - Accept events only for certain hitmap range

PixeMatrix organization: PicoPix SuperPixel



- 1 Analog island:
  - 4 FE + 4 Disc
- 1 TDC:
  - Discriminator inputs are OR-ed → Only 1 TDC measurement per SuperPixel
  - In Timepix4 each pixel has an independent measurement → "Simpler" block for PicoPix
- Arbitration:
  - Finds the pixel with larger charge → Winner
  - From Medipix4
  - Works in 2D
- Hitmap:
  - Finds pixel with a HIT around the Winner
  - Works in 2D
- Packet Formatter:
  - Might add local filtering: TOT, size of hitmap,…
- FIFO:
  - Stores data temporarily

PixeMatrix organization: SuperPixelGroup and Full Columns

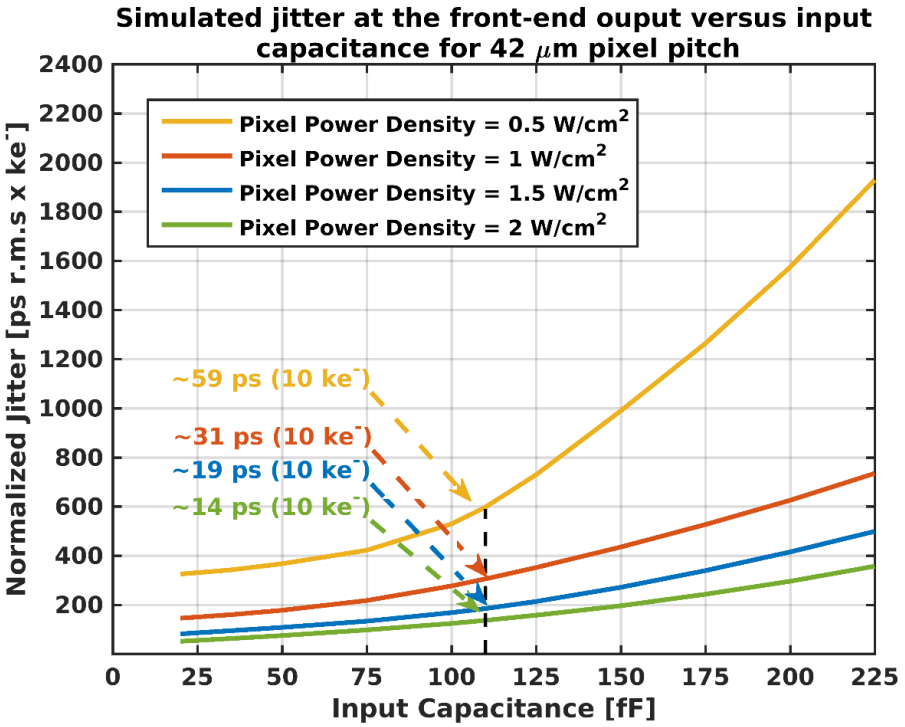


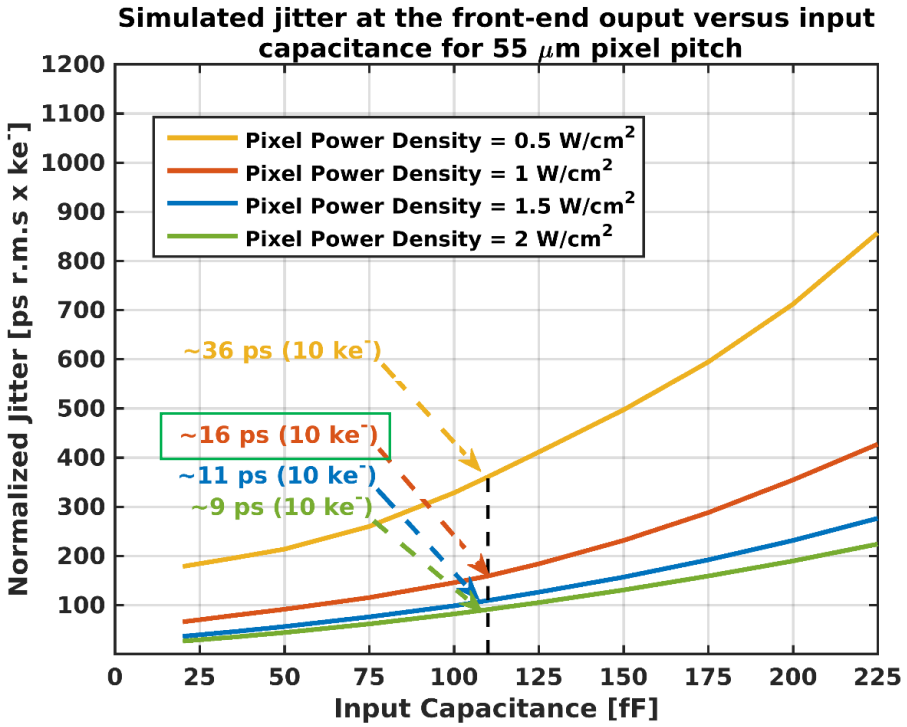
- Contains 2xN SuperPixels:
  - N is a parameter in the RTL code
  - N=4 → 32 pixels
  - N=8 → 64 pixels
- 1 dDLL station node
- Pixel readout architecture
- Pixel and SuperPixel configuration
- Should be the macro block for array formation

- M SuperPixelGroups from a full pixel column:
  - M is a parameter in the RTL code
  - M=16, N=4 → 512 pixels

Simulated jitter at FE output versus input capacitance

V. Sriskaran





- *Pixel pitch = 42 μm*
- $I_{LEAK/pixel} = 300\ pA$
- $I_{KRUM} = 60\ nA$

Simulation using schematic view!!

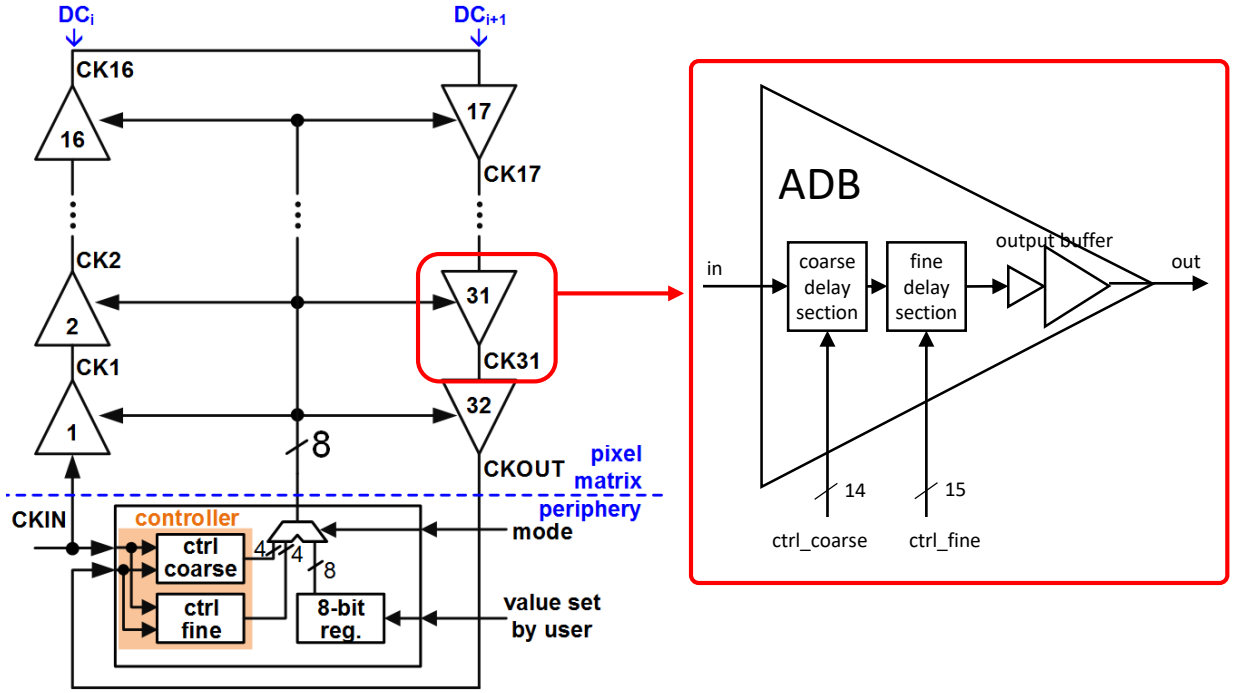
- *Pixel pitch = 55 μm*
- $I_{LEAK/pixel} = 300\ pA$
- $I_{KRUM} = 60\ nA$

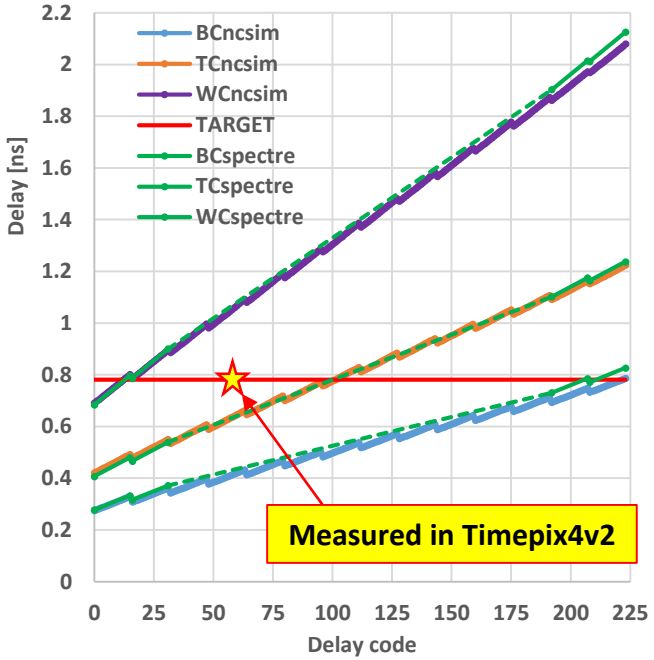
NB: 110 fF is the total pixel capacitance obtained with 3D-trench sensor.
DOI: 10.1088/1748-0221/15/09/P09029

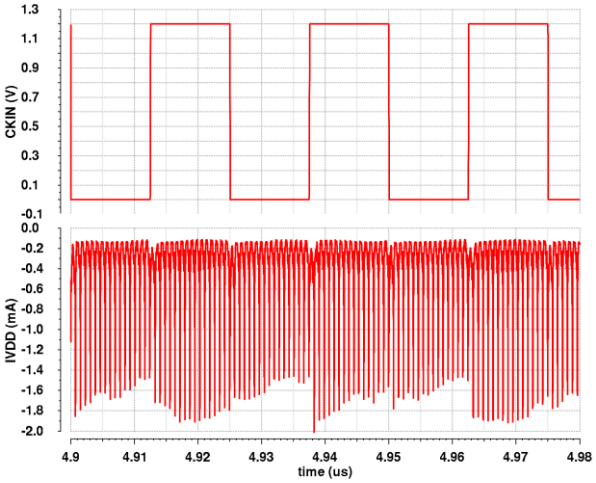
Full digital double column DLL

[448 dDLL: 224 Top Matrix and 224 Bottom Matrix]

iWoRID 2018
X. Llopart et al 2019 JINST 14 C01024

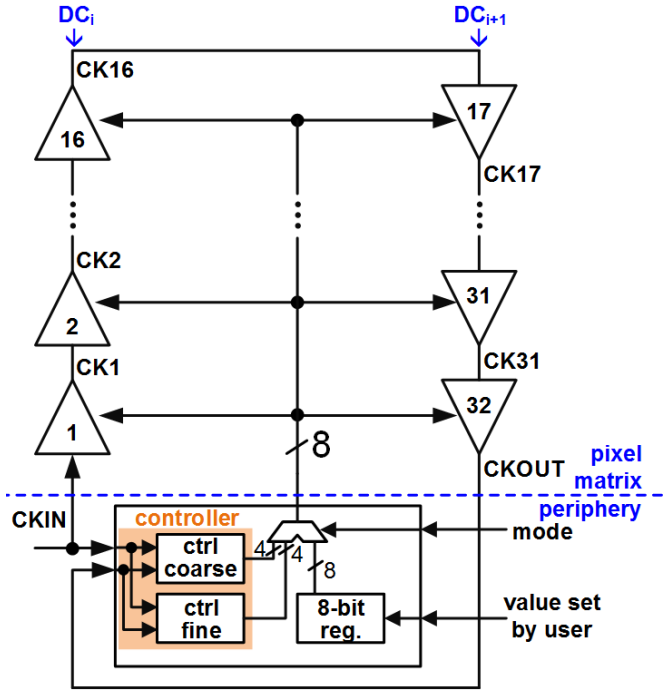




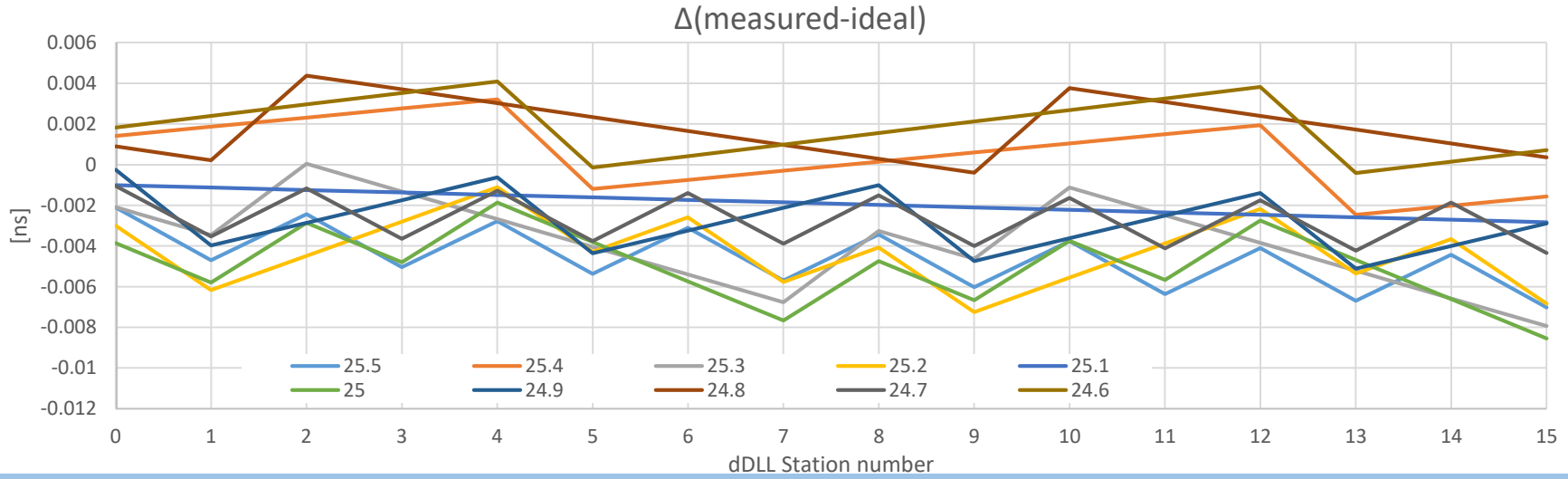


- Timepix4 ~23 mW/cm^2 @40MHz clock with <**100ps skew**
- Timepix3 ~100mW/cm^2 @40MHz clock with **~1.2ns skew**
- Dynamic digital power consumption is distributed across the clock period

Full digital double column DLL for 4DPix



- Initial studies of a dDLL with individual DLL station phase configuration:
  - Using Timepix4 dDLL digital control delay blocks (LSB= ~4-5 ps)
- Serial protocol to communicate with the dDLL column stations:
  - Broadcast command to speed-up DLL lock (as in Timepix4)
  - Non-Broadcast command for fine tuning
  - Bypass dDLL stations
  - Delay equalization for top-down delay mismatch

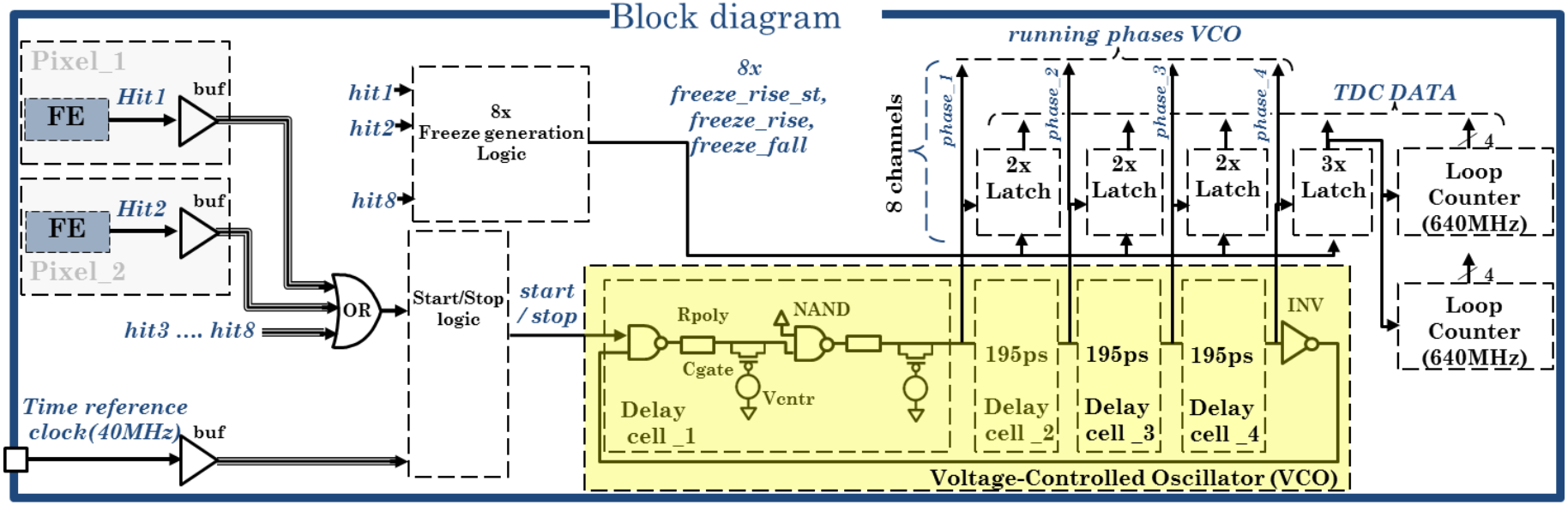


On-Pixel TDC

- Can we extend the Timepix4 VCO (195ps bin)?
  - VCO @1.28GHz with 10 phases 78.125ps bins → **22.5 ps_{rms}**
  - Only latch STOP phase for master pixel
- Or maybe a free-running VCO + on pixel calibration?
  - VCO @[1.5-2.5GHz] with 10 phases 40 to 66 ps bins → **11.5 to 19.2 ps_{rms}**
  - Requires event-by-event calibration

VCO Oscillation pattern

stage	Phase[4]	Phase[3]	Phase[2]	Phase[1]	Phase[0]
0	1	1	1	1	1
1	1	1	1	1	0
2	1	1	1	0	0
3	1	1	0	0	0
4	1	0	0	0	0
5	0	0	0	0	0
6	0	0	0	0	1
7	0	0	0	1	1
8	0	0	1	1	1
9	0	1	1	1	1



Free running On-pixel VCO?

- Explored the idea of the on-pixel **free-running VCO**:
  - With 3-4 bits oscillation control
  - Using 7T cells with extracted parasitic
- **Advantages**:
  - No control voltage distributed along the column
  - Top down mismatch due to radiation can be minimized
  - Faster oscillation times and lower dynamic power → better time resolution
- **Disadvantages**:
  - Requires VCO calibration measurement → data bandwitdth!

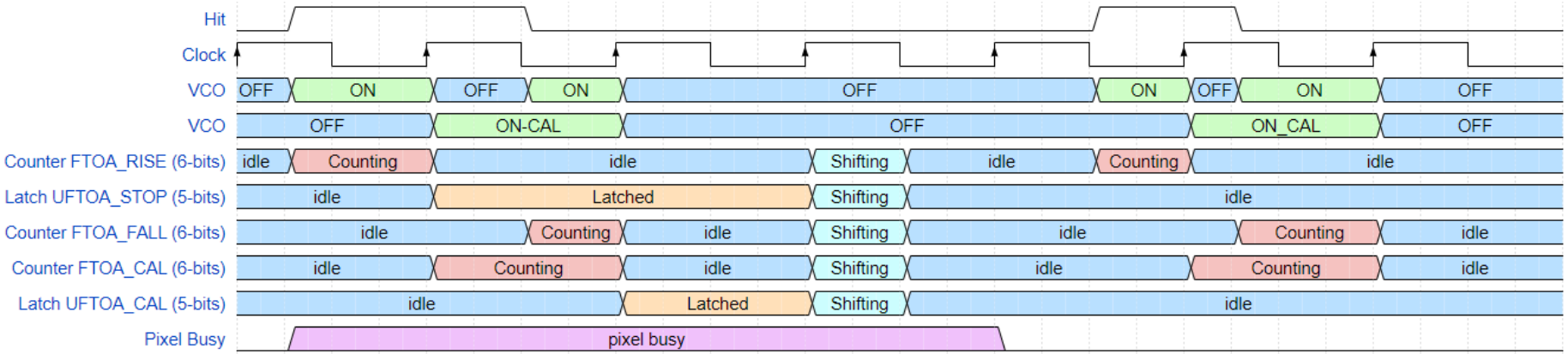
	freq	Phases	LSB	Area	power
Timepix4	640 MHz	8	195ps	~350µm^2	~500µW
Free-running VCO in 28nm	1.5-2.5 GHz	10	66-40ps	~70µm^2	~150µW

Parameter				Slow	Fast	Typical
VDD				810m	990m	900m
tcbn28hpcplusb...				rc_cworst	rc_cbest	rc_typical
tcbn28hpcplusb...				rc_cworst	rc_cbest	rc_typical
temperature				80	-40	25
toplevel.scs				ass_ps	aff_pf	att_pt

Output	Pass/Fail	Min	Max	Slow	Fast	Typical
thr		405m	495m	405m	495m	450m
freqVCO_2		1.449G	3.325G	1.449G	3.325G	2.287G
uftoa_bin		30.07p	69.02p	69.02p	30.07p	43.72p
Start_bin		10.5p	24.47p	24.47p	10.5p	15.6p
uftoa0		30.62p	69.88p	69.88p	30.62p	44.16p
uftoa1		29.53p	68.17p	68.17p	29.53p	43.3p
uftoa2		30.63p	69.89p	69.89p	30.63p	44.16p
uftoa3		29.52p	68.17p	68.17p	29.52p	43.3p
uftoa4		30.62p	69.87p	69.87p	30.62p	44.16p
uftoa5		29.52p	68.17p	68.17p	29.52p	43.29p
uftoa6		30.63p	69.89p	69.89p	30.63p	44.16p
uftoa7		29.52p	68.17p	68.17p	29.52p	43.3p
uftoa8		30.63p	69.88p	69.88p	30.63p	44.15p
uftoa9		29.51p	68.1p	68.1p	29.51p	43.27p
uftoaT		300.7p	690.2p	690.2p	300.7p	437.2p
freqVCO	fail	1.449G	3.325G	1.449G	3.325G	2.287G
uftoaI		30.07p	69.02p	69.02p	30.07p	43.72p
start_off	fail	-65.09 %	-64.32 %	-64.54 %	-65.09 %	-64.32 %
uftoa0_off	pass	997.3 m%	1.826 %	1.246 %	1.826 %	997.3 m%
uftoa1_off	pass	-1.816 %	-978.3 m%	-1.234 %	-1.816 %	-978.3 m%
uftoa2_off	pass	992.5 m%	1.852 %	1.267 %	1.852 %	992.5 m%
uftoa3_off	pass	-1.84 %	-978.2 m%	-1.235 %	-1.84 %	-978.2 m%
uftoa4_off	pass	986.5 m%	1.827 %	1.238 %	1.827 %	986.5 m%
uftoa5_off	pass	-1.83 %	-986.5 m%	-1.234 %	-1.83 %	-986.5 m%
uftoa6_off	pass	1.004 %	1.841 %	1.261 %	1.841 %	1.004 %
uftoa7_off	pass	-1.826 %	-970.1 m%	-1.234 %	-1.826 %	-970.1 m%
uftoa8_off	pass	981.2 m%	1.85 %	1.252 %	1.85 %	981.2 m%
uftoa9_off	pass	-1.885 %	-1.049 %	-1.325 %	-1.885 %	-1.049 %
Power		75.49 uW	260.7 uW	75.49 uW	260.7 uW	147.8 uW

Event-by-event VCO calibration

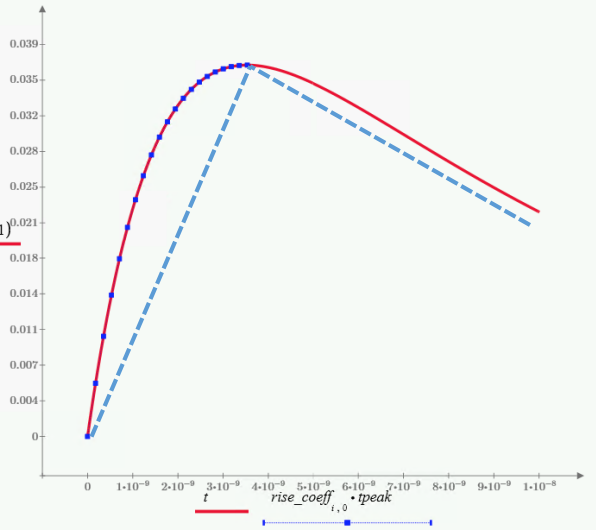
- Ref clock @40MHz:
  - FTOA 6-bits → Max VCO freq before overflow 2.52 GHz
  - Calibration could be done after event (ON-CAL):
    - To measure the VCO frequency: FTOA_CAL(6) + UFTOA_STOP(5) + UFTOA_CAL(5) = 16-bits
  - Pixel (cluster) busy for 3-4 clock cycles → 100ns @40MHz



Digital simulation environment

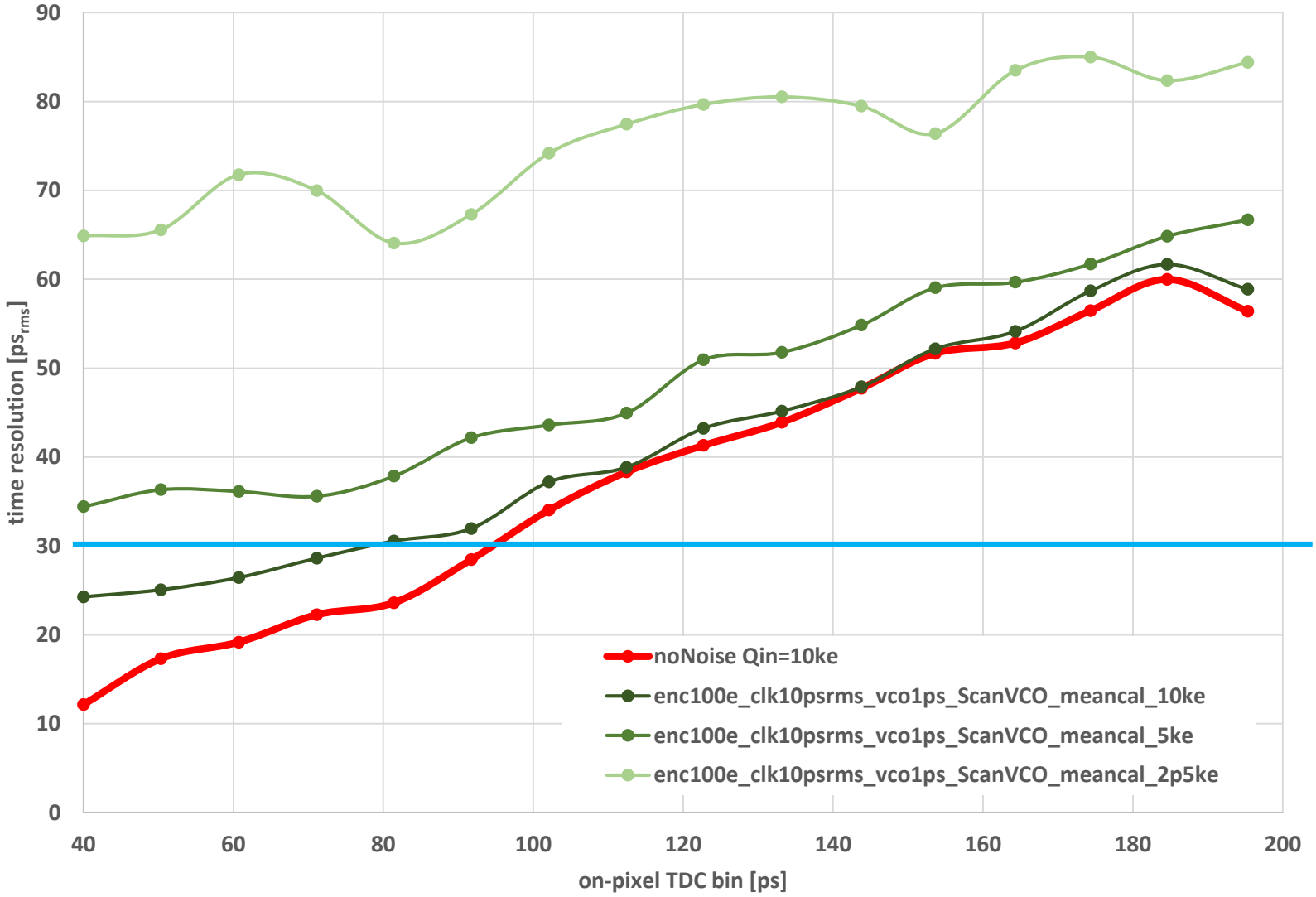
- Full Column → M=16 SuperPixelGroups and N=4 SuperPixels
  - 128 TDCs
  - Full dDLL + EOC controller
- Noise sources modelled:
  - ClkDLL jitter as random gaussian
  - VCO jitter as random gaussian
  - FE ENC as random Gaussian
- Modified FE pixel model represent more realistically the rise-time slope → critical to extract correct timing
  - Model includes analog pile-up
  - Fall time is a constant slope

$$\frac{Vfe\left(t, 1000, 3.1\cdot 10^{6}, 3\cdot 10^{-15}, 5\cdot 10^{-15}, 100\cdot 10^{-15}, 160\cdot 10^{-6}\right)\ (1)}{rise\_coeff_{i,1}\cdot gain\ \ (1)}$$



$$rise\_coeff = \begin{bmatrix} 0 & 0 \\ 5\cdot 10^{-11} & 0.14308 \\ 1\cdot 10^{-10} & 0.26932 \\ 1.5\cdot 10^{-10} & 0.38046 \\ 2\cdot 10^{-10} & 0.47802 \\ 2.5\cdot 10^{-10} & 0.56339 \\ 3\cdot 10^{-10} & 0.63784 \\ 3.5\cdot 10^{-10} & 0.70248 \\ 4\cdot 10^{-10} & 0.75833 \\ 4.5\cdot 10^{-10} & 0.80631 \\ 5\cdot 10^{-10} & 0.84723 \\ 5.5\cdot 10^{-10} & 0.88184 \\ 6\cdot 10^{-10} & 0.9108 \\ 6.5\cdot 10^{-10} & 0.93472 \\ 7\cdot 10^{-10} & 0.95413 \\ 7.5\cdot 10^{-10} & 0.96952 \\ 8\cdot 10^{-10} & 0.98133 \\ 8.5\cdot 10^{-10} & 0.98994 \\ 9\cdot 10^{-10} & 0.99572 \\ 9.5\cdot 10^{-10} & 0.99898 \\ 1\cdot 10^{-9} & 1 \end{bmatrix}$$

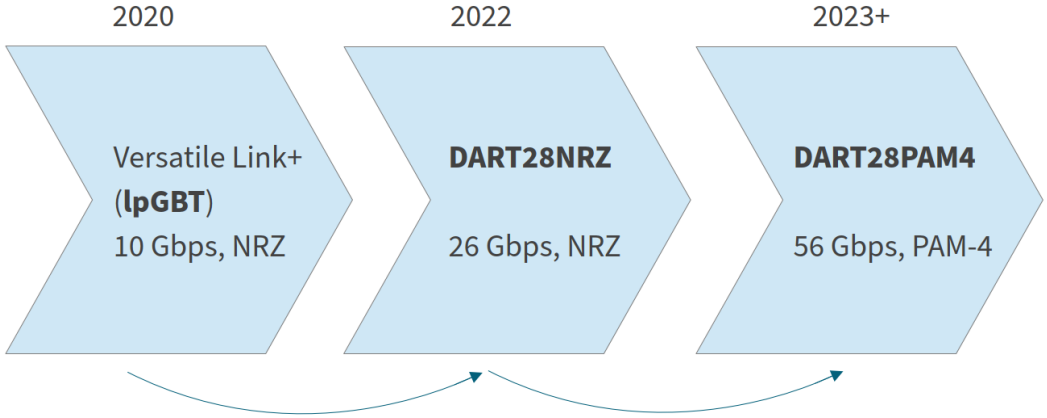
Preliminary simulations of the full column [THR at 1Ke-]



High Speed Links in 28nm

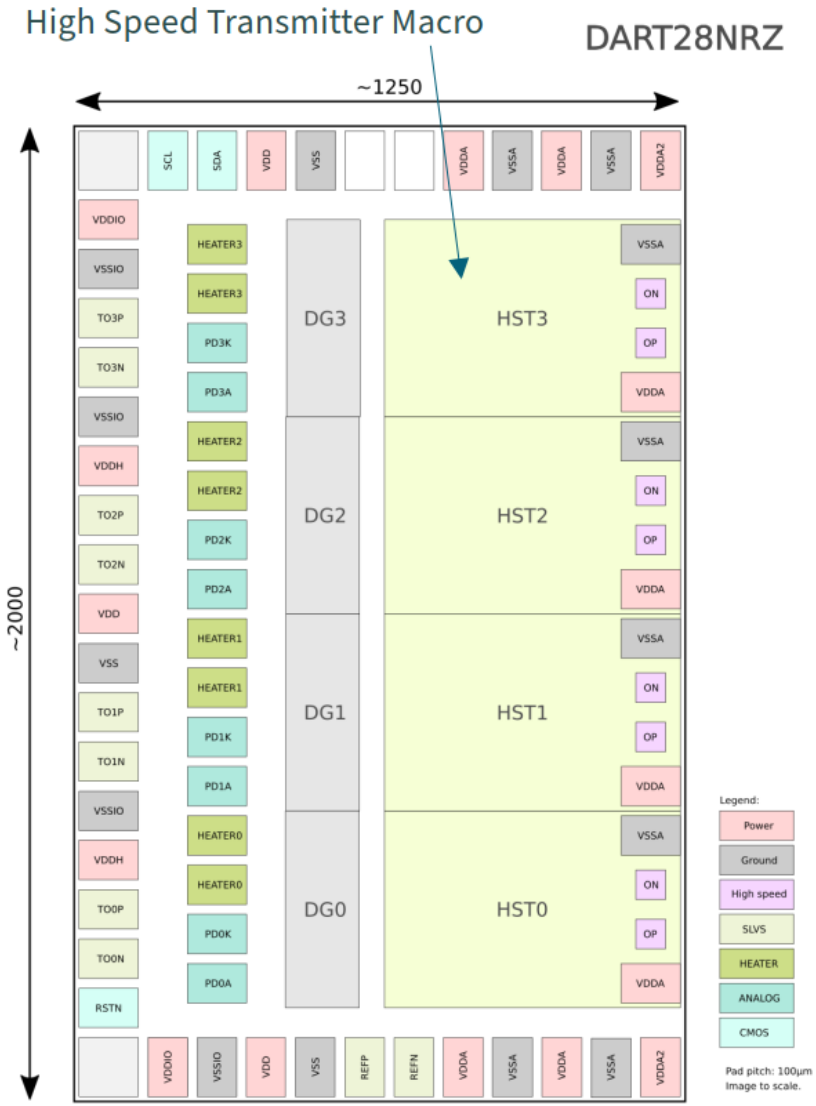
S.Bieregel (CERN-ESE-ME)
https://indico.cern.ch/event/1138500/

- WP6 ASIC Roadmap



- 28 nm technology adoption
- 2.5x increase of data rate
- IP block form factor
- SiPh co-integration (wire-bond)

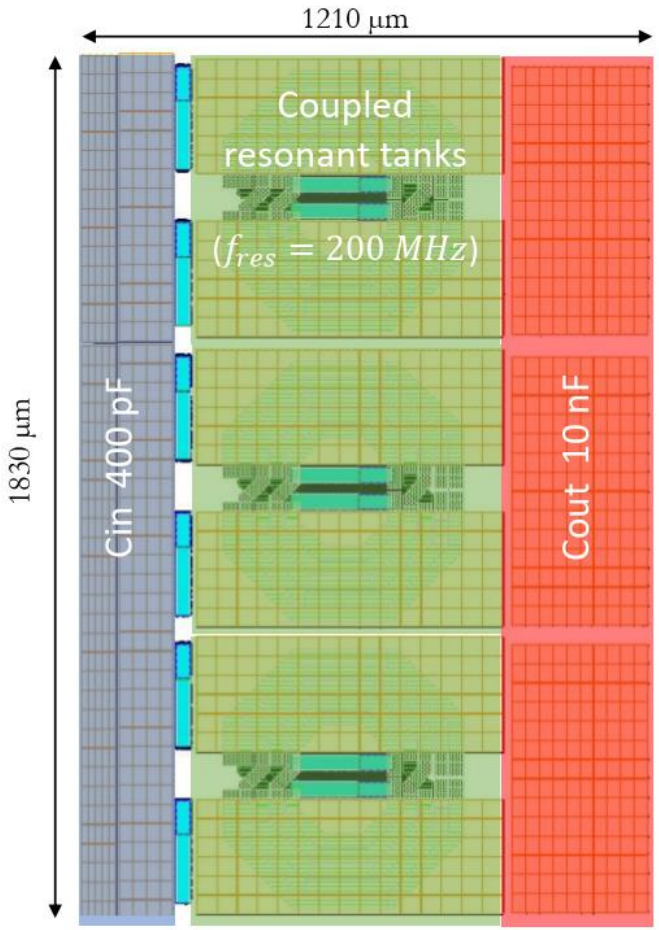
- PAM-4 signaling
- = 2x increase of data rate
- IEEE 802.3cd compatibility
- SiPh co-integration (flip-chip)



On chip DC-DC Converter?

G. Ripamonti (CERN-ESE-ME)
https://indico.cern.ch/event/1138502/

- A proposal for a 5V, 250mA fully-integrated DC-DC converter in 28nm CMOS: 5V to 0.9V converter
- Great simplification of the module
- Target TID 1Grad
- Expected output ripple <3mV
- Output current limits the power consumption but can be done if internal power is split by blocks of columns



Summary and Project Status

- PicoPix is intended to be a “realistic” demonstrator chip for a future upgrade of the LHCb Velo project (LS4)
  - Main requirement is to target a time resolution < **$30ps_{rms}$**
  - Other very challenging requirements (pixel size, radiation hardness, power, bandwidth,…)

- Status → “exploration phase” of the specs limitations for a large 30psrms target ASIC:
  - Front-end limits and optimization
  - On-pixel TDC
  - dDLL reference clock distribution
  - On-pixel clock-cleaning PLL (Nikhef)
  - 1st full column RTL exists

- Project organization:
  - Monthly design meetings have been organized
  - Design team: CERN and Nikhef

- Expected submission ~2023-2024