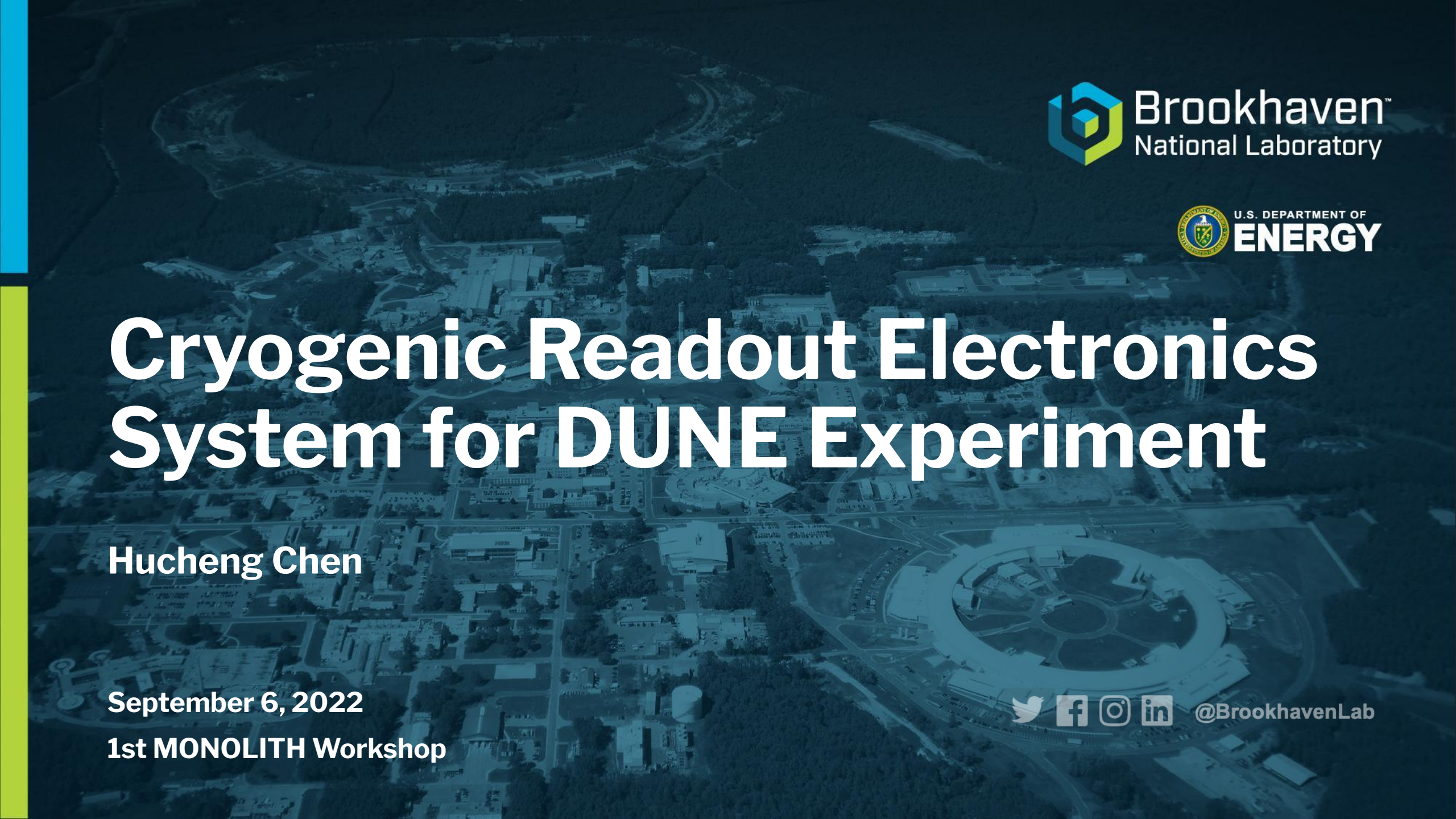


Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

Cryogenic Readout Electronics System for DUNE Experiment

Hucheng Chen

September 6, 2022

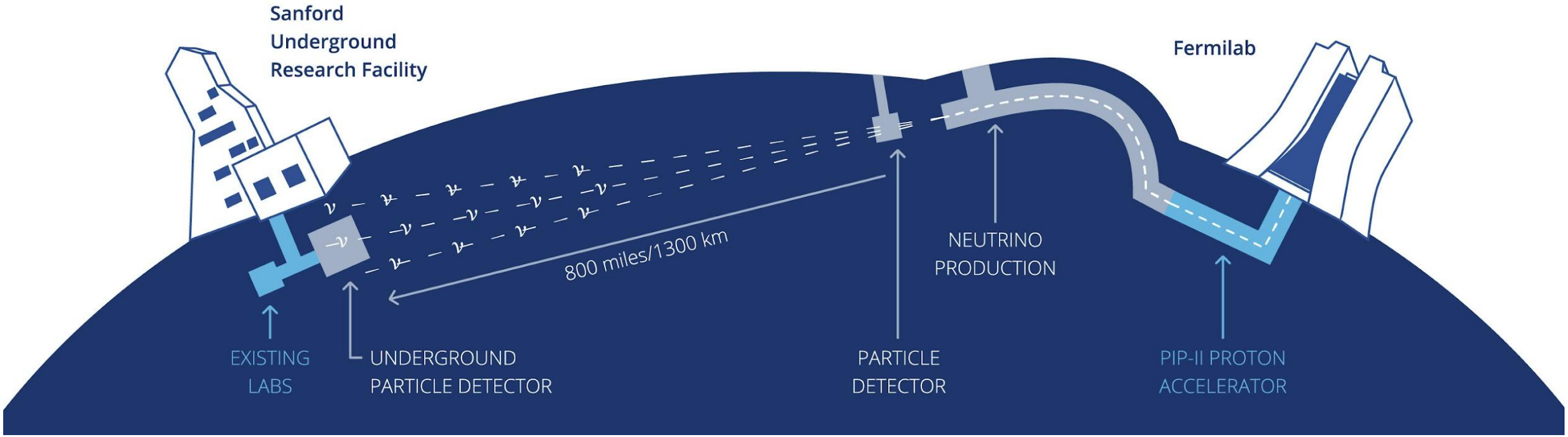
1st MONOLITH Workshop

@BrookhavenLab

Outline

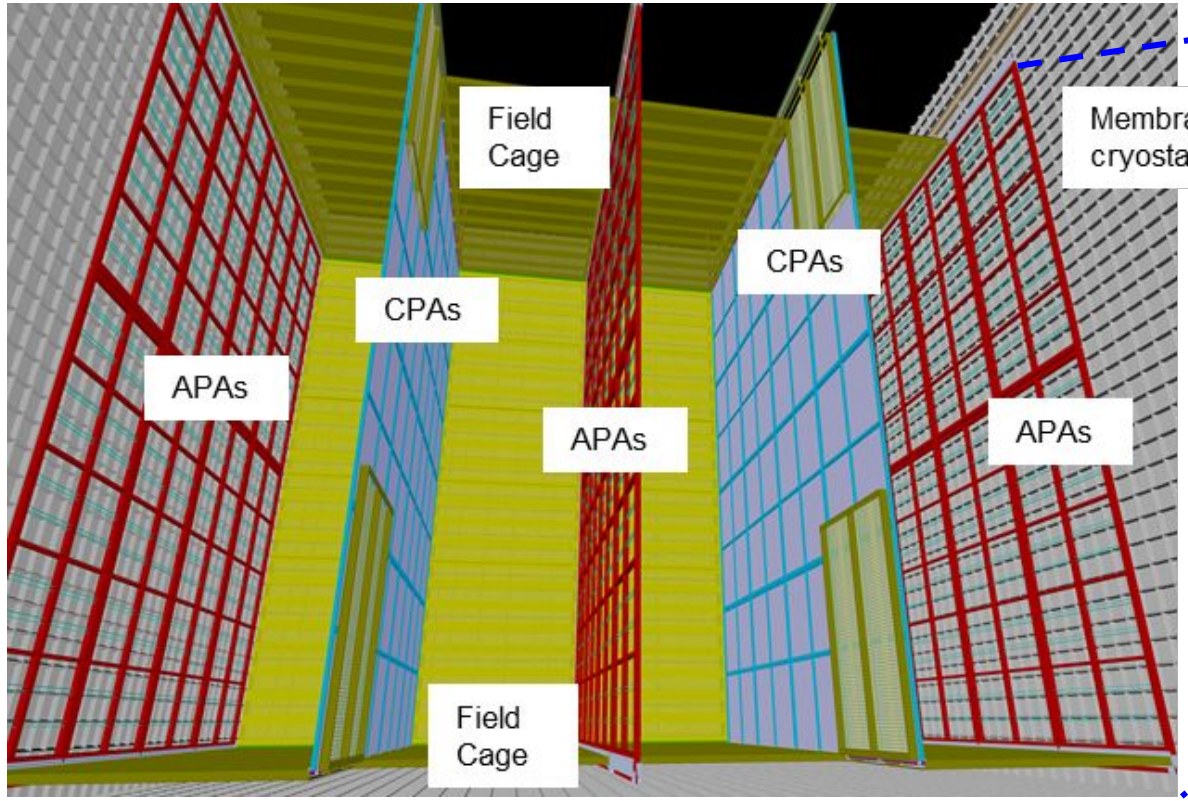
- **Deep Underground Neutrino Experiment**
  - LBNF/DUNE
  - DUNE Far Detectors: FD1-HD and FD2-VD
- **Cold Electronics for LArTPC**
  - Advantages of cold electronics for LArTPC
  - CMOS cold electronics R&D
  - Integral system design concept
- **ProtoDUNE-I Readout Electronics**
  - System design
  - Detector performance
- **CRP Coldbox Test**
  - Detector performance
- **ProtoDUNE-II Readout Electronics**
  - New ASICs
  - System design
  - Electronics performance
- **Outlook**

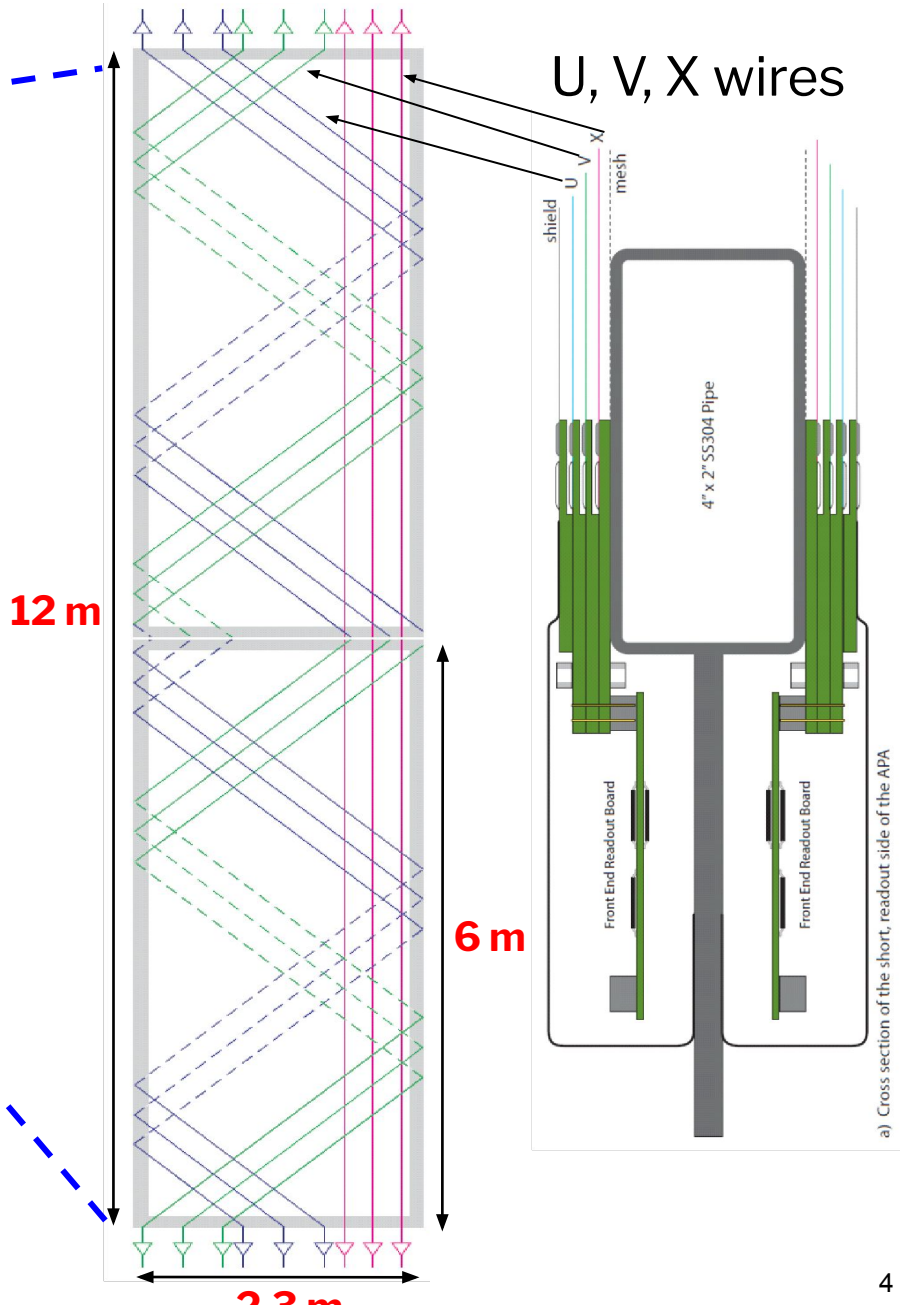
Long Baseline Neutrino Program: LBNF/DUNE



- **Neutrino beam from FNAL to Homestake: 1,300 km long baseline**
  - Muon neutrinos/anti-neutrinos from high-power proton beam: ~1.2 MW (→ ~2.4 MW)
  - Two parallel caverns each have two 10 kt detector pits with a laydown space in between
- **DUNE primary science program**
  - ***Neutrino Oscillation Physics***: Discover CP Violation in the leptonic sector; Mass Hierarchy; Precision Oscillation Physics
  - ***Nucleon Decay***: e.g. targeting SUSY-favored modes, $p \rightarrow K^{+}\nu$
  - ***Supernova burst physics & astrophysics***: Galactic core collapse supernova, sensitivity to ν_e

DUNE Far Detector: FD1-HD

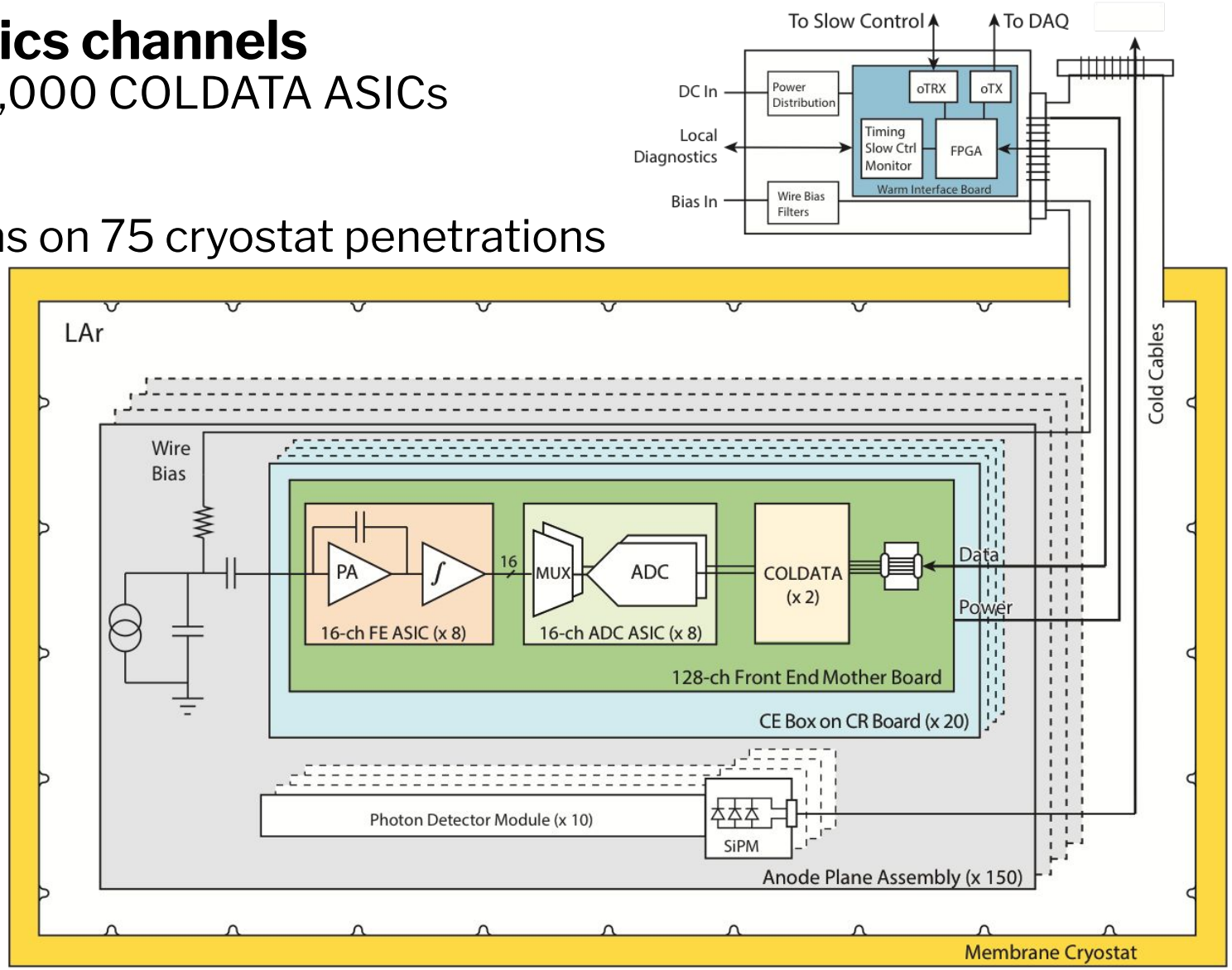




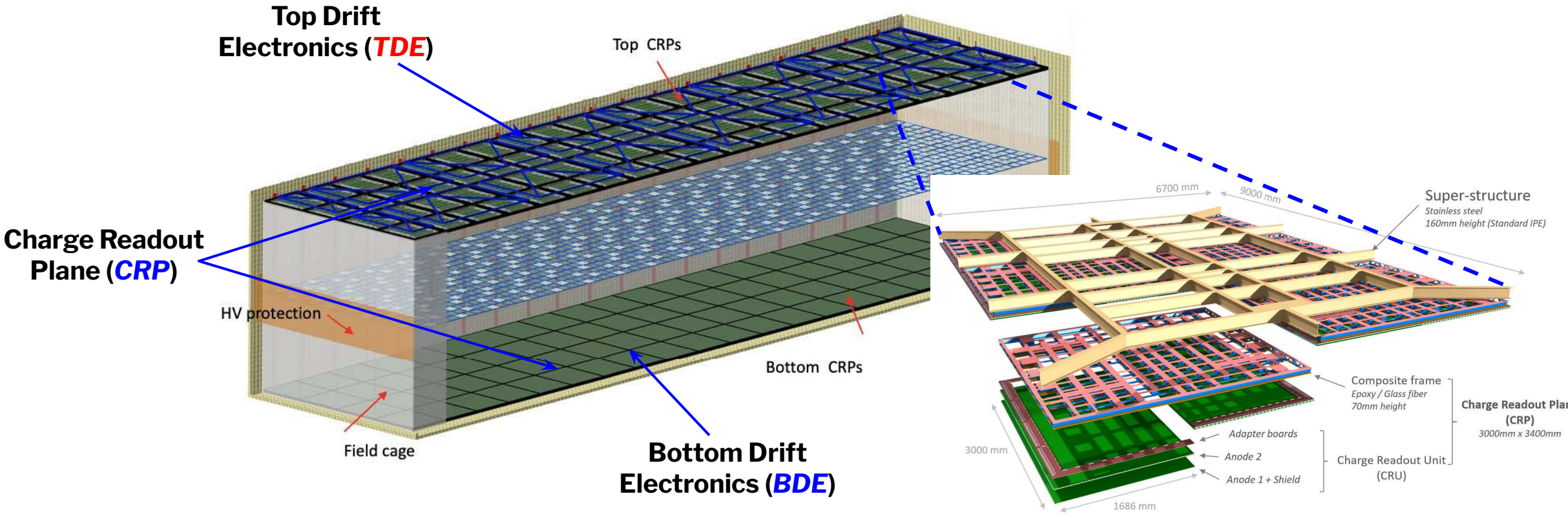
- **DUNE first 10 kt Far Detector: FD1-HD**
  - Consisting of 150 APAs plus 300 CPAs → 4 x 3.5 m ***horizontal drift*** regions
  - Active volume: ~12 m x 14 m x 58 m
  - Total ***384,000*** TPC channels read out by ***cold electronics***

FD1-HD APA TPC Electronics System

- **Total 384,000 cold electronics channels**
  - 24,000 FE/24,000 ColdADC/6,000 COLDATA ASICs
  - 3,000 FEMB assemblies
  - 150 sets of cold cable bundles
  - 150 sets of signal feed-throughs on 75 cryostat penetrations
  - 150 WIECs
    - 750 WIBs
    - 150 PTCs
    - 150 PTBs



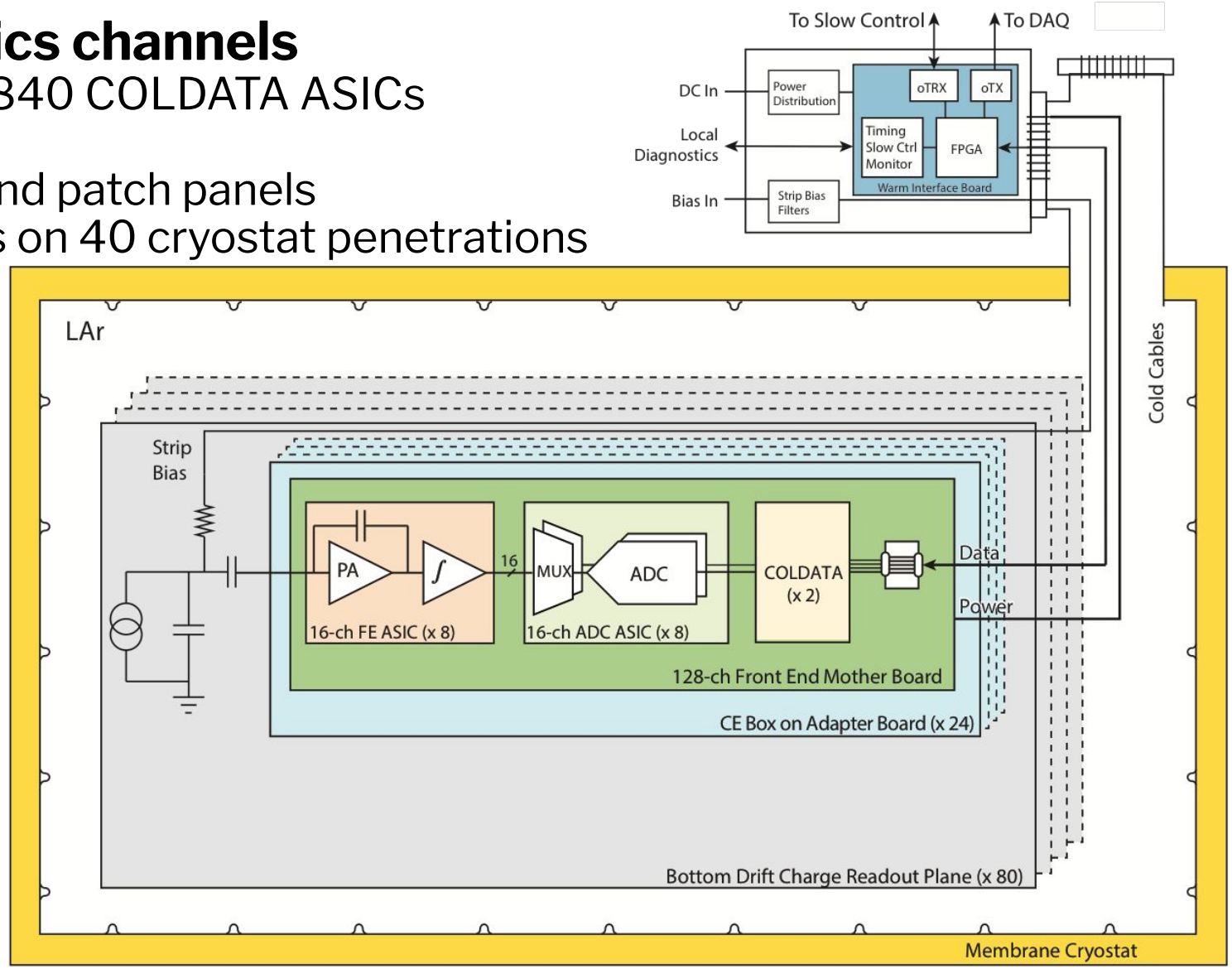
DUNE Far Detector: FD2-VD



- **DUNE second 10 kt Far Detector: FD2-VD**
  - Consisting of 160 CRPs plus 80 cathode modules → 2 x 6 m ***vertical drift*** regions
  - Active volume: ~12 m x 14 m x 60 m
  - Total ***491,520*** TPC channels: TDE + BDE
- **BDE for the 80 CRPs on the bottom drift volume are the same as FD1-HD**
  - Total ***245,760*** TPC channels read out by ***cold electronics***

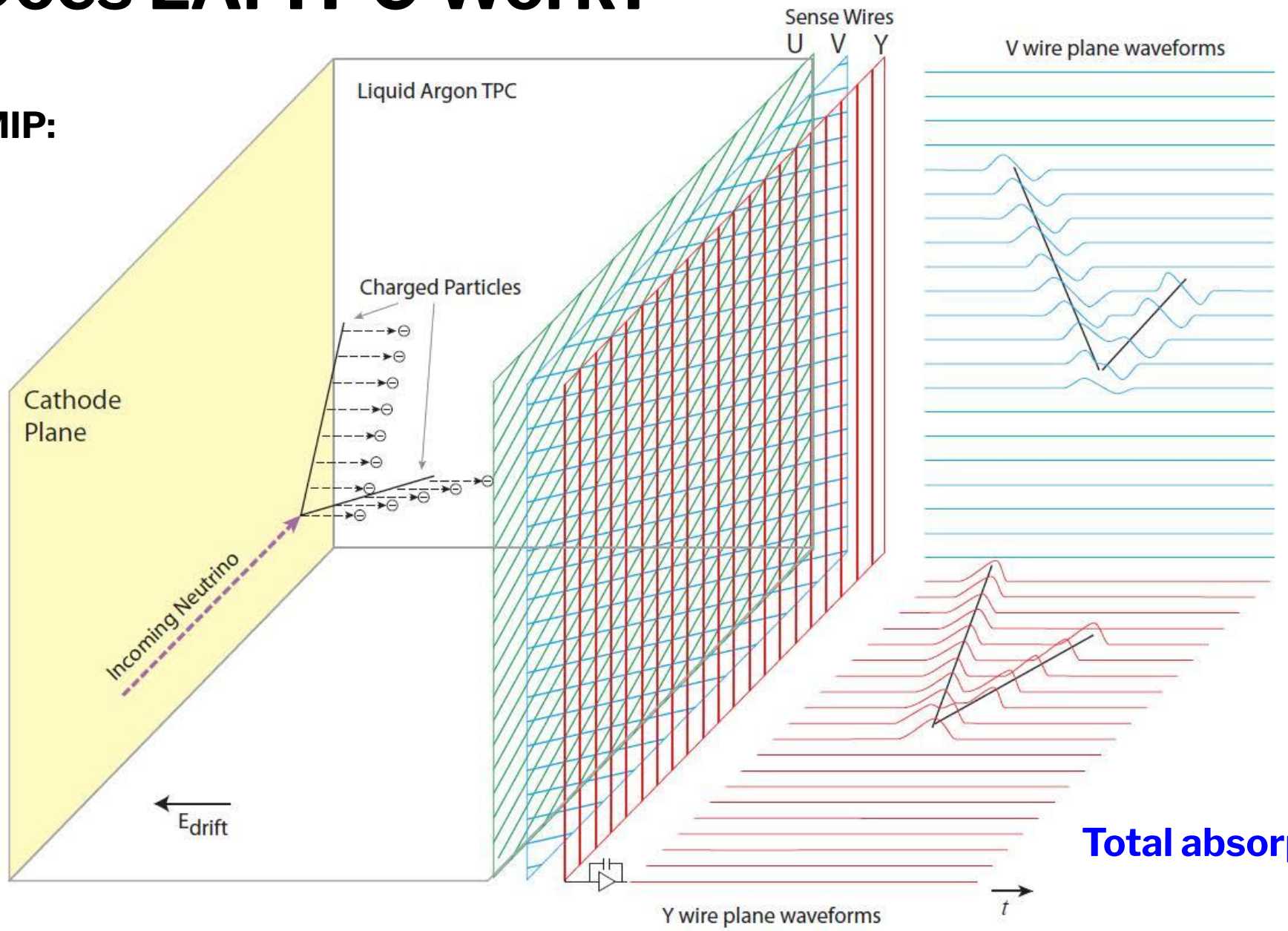
FD2-VD CRP Bottom Drift Electronics System

- **Total 245,760 cold electronics channels**
  - 15,360 FE/15,360 ColdADC/3,840 COLDATA ASICs
  - 1,920 FEMB assemblies
  - 80 sets of cold cable bundles and patch panels
  - 80 sets of signal feed-throughs on 40 cryostat penetrations
  - 80 WIECs
    - 480 WIBs
    - 80 PTCs
    - 80 PTBs



How Does LArTPC Work?

dE/dx of 1 MIP:
2.1 MeV/cm



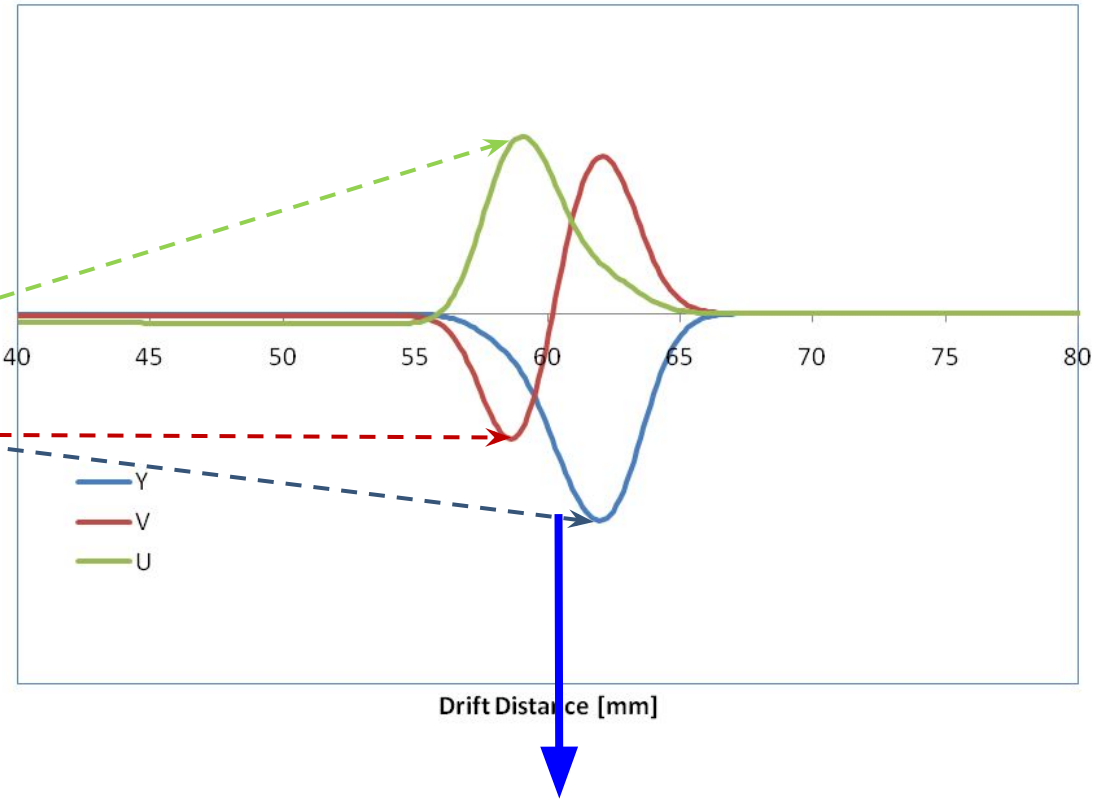
Detecting Signals Induced by Drifting Electrons

Total absorption calorimetry

Signals in LArTPC

- **Charge signal**
  - A 3 mm MIP track should create 210 keV/mm x 3 mm / 23.6 eV/e = 4.3 fC
  - After a 1/3 initial recombination loss: ~2.8 fC
  - Assume the drift path to equal the charge life time, reducing the signal to 1/e ≈ 0.368
  - The expected signal for 3mm wire spacing is then ≈ 1 fC = 6250 e^-, … and for 5mm, ≈ 10^4 e^-, for **the "collection signal"**
  - The induction signals are smaller
  - The ***time scale*** of TPC signals is determined by the **wire plane spacing** and **electron drift velocity** (~1.5 mm/μs at 500 V/cm)
- **There is no electron amplification inside LAr → noise sensitive!**

Induced Current Waveforms on 3 Sense Wire Planes

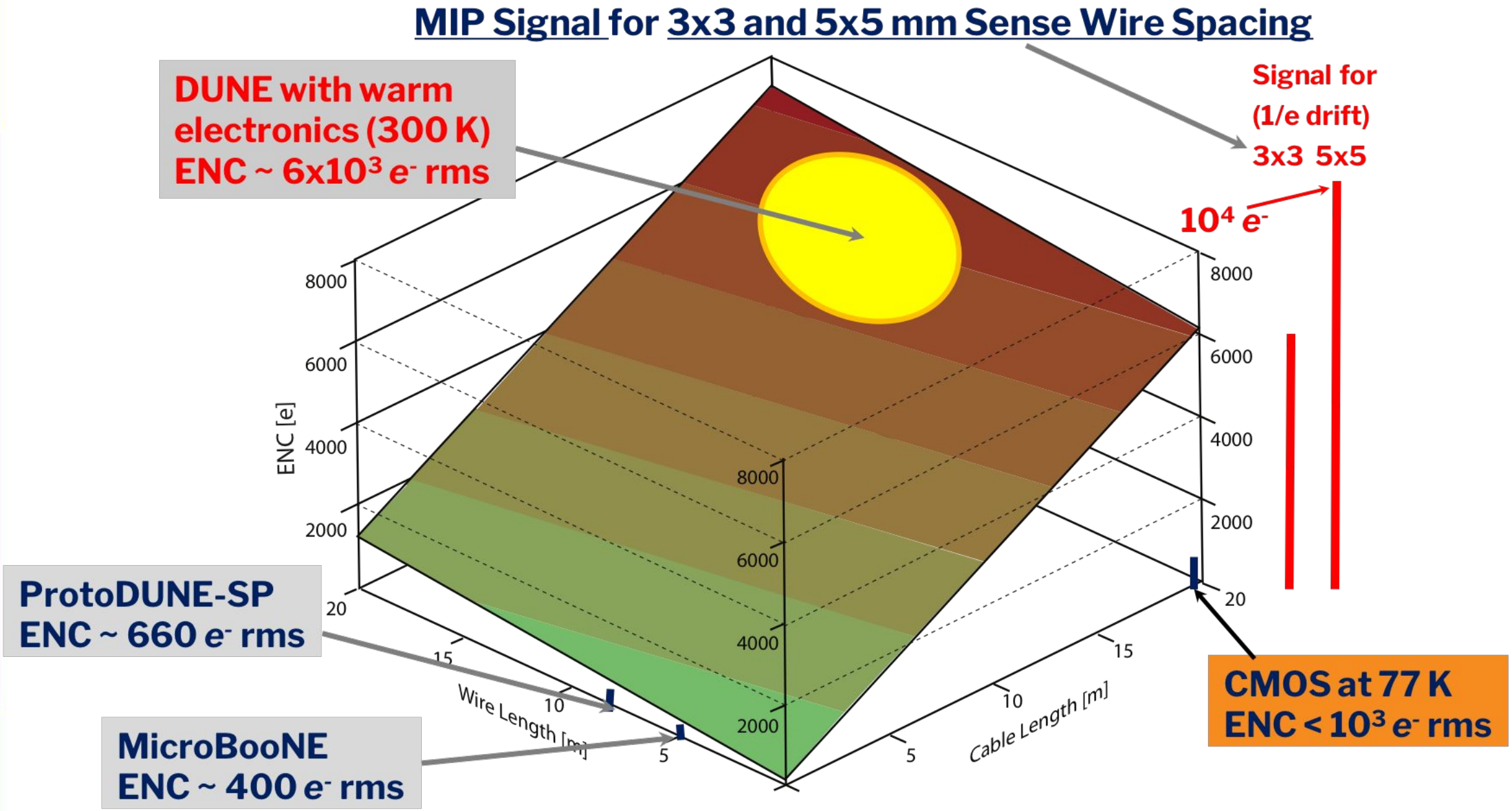


Sampling rate ≤ 2 Ms/s

Motivation of Cold Electronics

- **Readout electronics developed for low temperatures (77K-300K) is an enabling technology for noble liquid and mixed phase detectors for neutrino and dark matter research**
  - Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics
    - The amplifier input noise, $e^2 \propto C_d^2/g_m$, linearly increases with detector and cable capacitance, C_d, and decreases with input stage transconductance, g_m
  - Signal multiplexing results in large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/cryostat penetrations
- **R&D of CMOS cold electronics started at BNL in 2008**
  - The cold electronics development for LArTPC was launched, before the final decision for LArTPC (and not for Water Cherenkov) for LBNF/DUNE had been made in January 2012
  - MicroBooNE started with plans for JFETs and, the FE ASIC caught up with MicroBooNE delays → ***MicroBooNE became the first experiment instrumented with cold CMOS ASICs, total 8,256 channels***
  - MicroBooNE released ***flagship neutrino results*** show no hint of a sterile neutrino in fall 2021
    - "Search for an Excess of Electron Neutrino Interactions in MicroBooNE Using Multiple Final State Topologies", arXiv:2110.14054
    - "Search for Neutrino-Induced Neutral Current Δ Radiative Decay in MicroBooNE and a First Test of the MiniBooNE Low Energy Excess Under a Single-Photon Hypothesis", arXiv:2110.00409

Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length for CMOS at 300 K and 89 K



1st International Workshop towards the Giant Liquid Argon Charge Imaging Experiment (GLA2010)

Cold electronics for "Giant" Liquid Argon Time Projection Chambers

Veljko Radeka[1*], Hucheng Chen[1], Grzegorz Deptuch[2], Gianluigi De Geronimo[1], Francesco Lanni[1], Shaorui Li[1], Neena Nambiar[1], Sergio Rescia[1], Craig Thorn[1], Ray Yarema[2] , Bo Yu[1]

[1] Brookhaven National Laboratory, Upton, NY 11973-5000, USA

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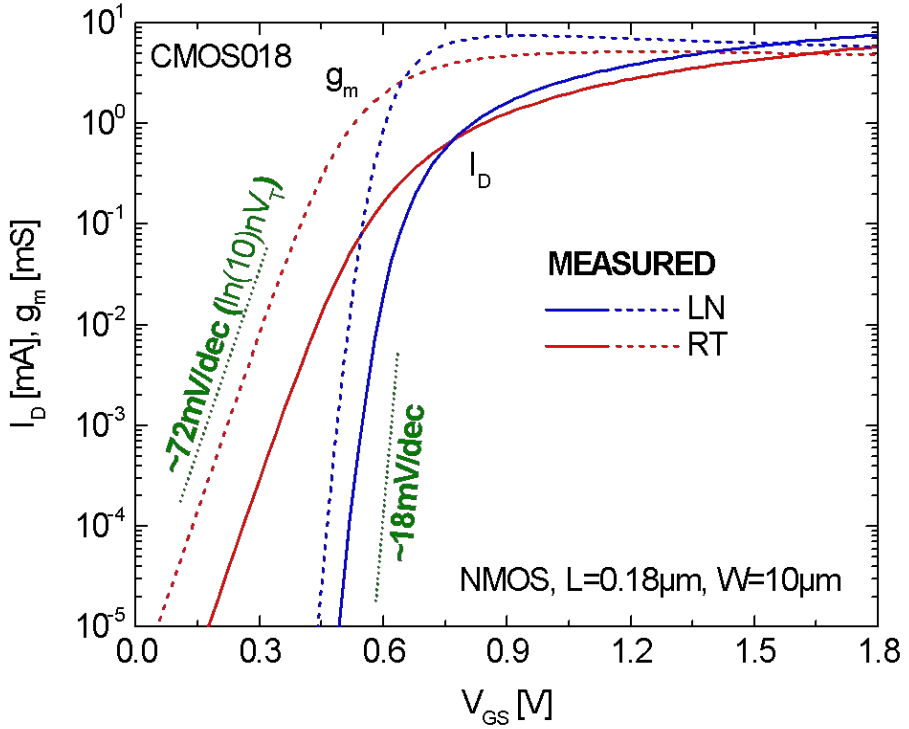
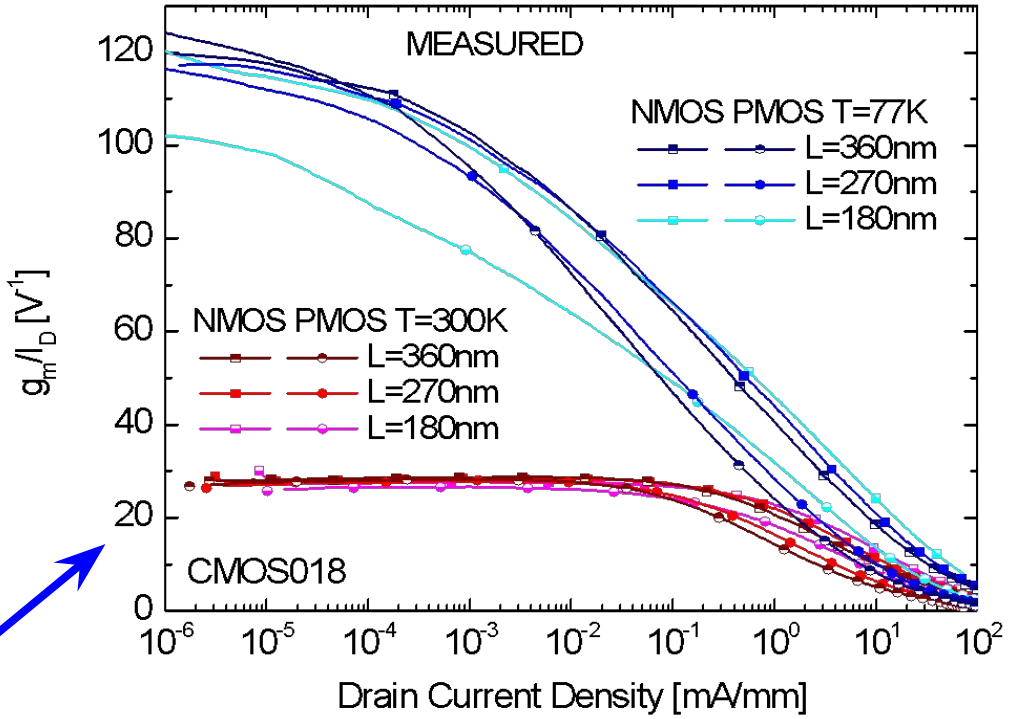
Abstract. The choice between cold and warm electronics (inside or outside the cryostat) in very large LAr TPCs (>5-10 ktons) is not an electronics issue, but it is rather a major cryostat design issue. This is because the location of the signal processing electronics has a direct and far reaching effect on the cryostat design, an indirect effect on the TPC electrode design (sense wire spacing, wire length and drift distance), and a significant effect on the TPC performance. All these factors weigh so overwhelmingly in favor of the cold electronics that it remains an optimal solution for very large TPCs. In this paper signal and noise considerations are summarized, the concept of the readout chain is described, and the guidelines for design of CMOS circuits for operation in liquid argon (at ~89 K) are discussed.

CMOS Transistors *Become Better* in LAr/LN2



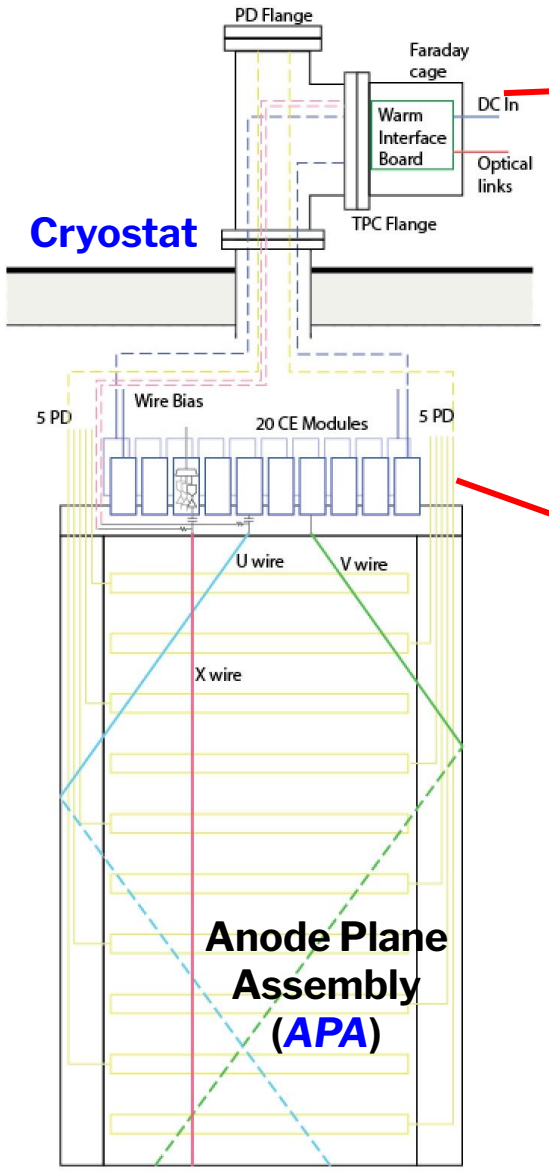


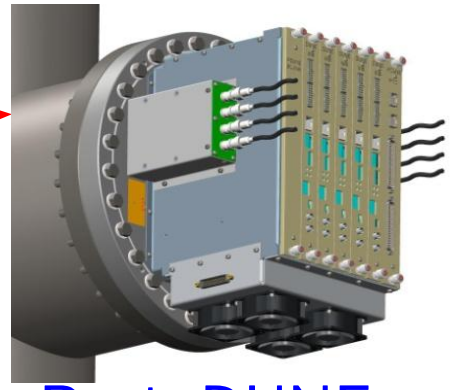
Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

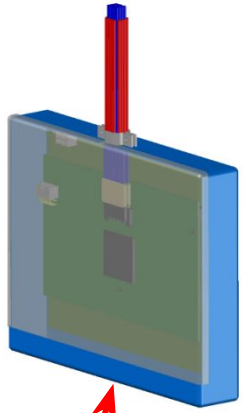
At 77-89K, charge carrier **mobility** in silicon increases, **thermal fluctuations** decrease with **kT/e**, resulting in a **higher gain**, **higher g_m /I_D**, **higher speed** and **lower noise**

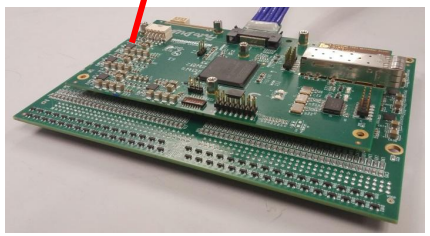
Integral System Design Concept





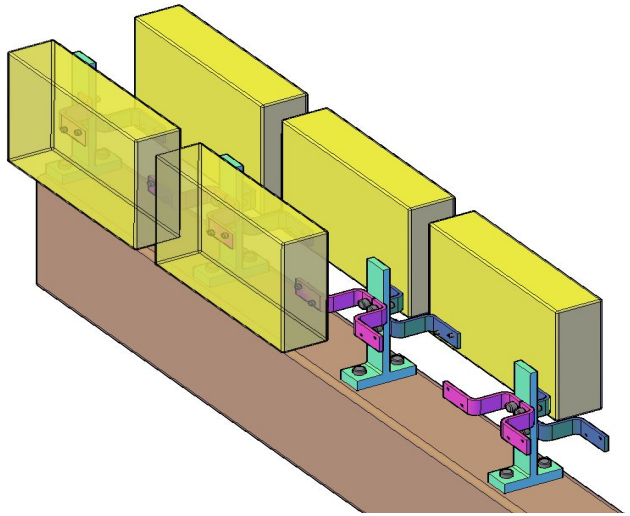
ProtoDUNE



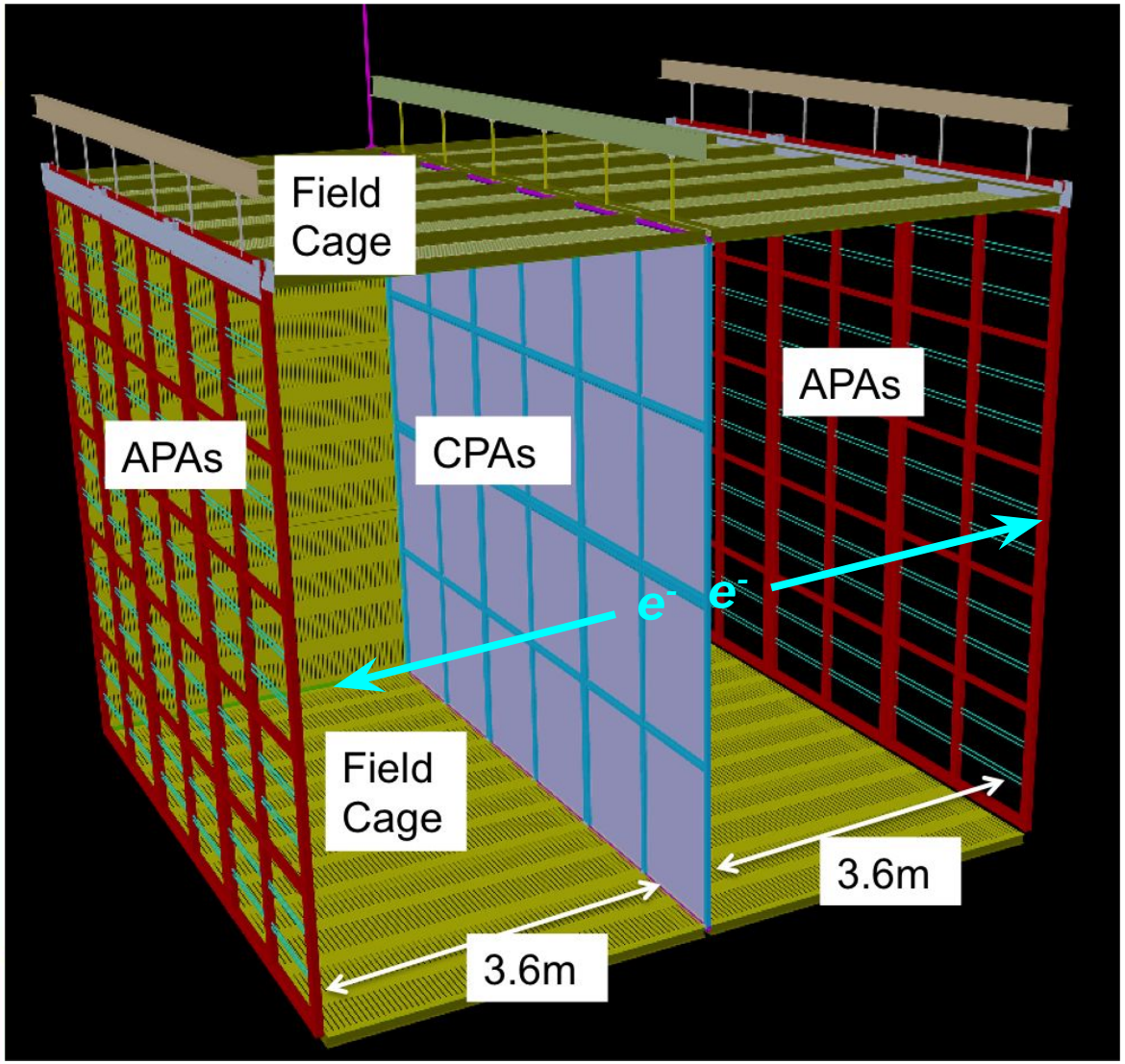


A necessary (but not sufficient!) condition to achieve a good system performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostics** and strict isolation and **grounding rules** will have to be followed

Cold electronics (CE) module and its attachment to the APA frame

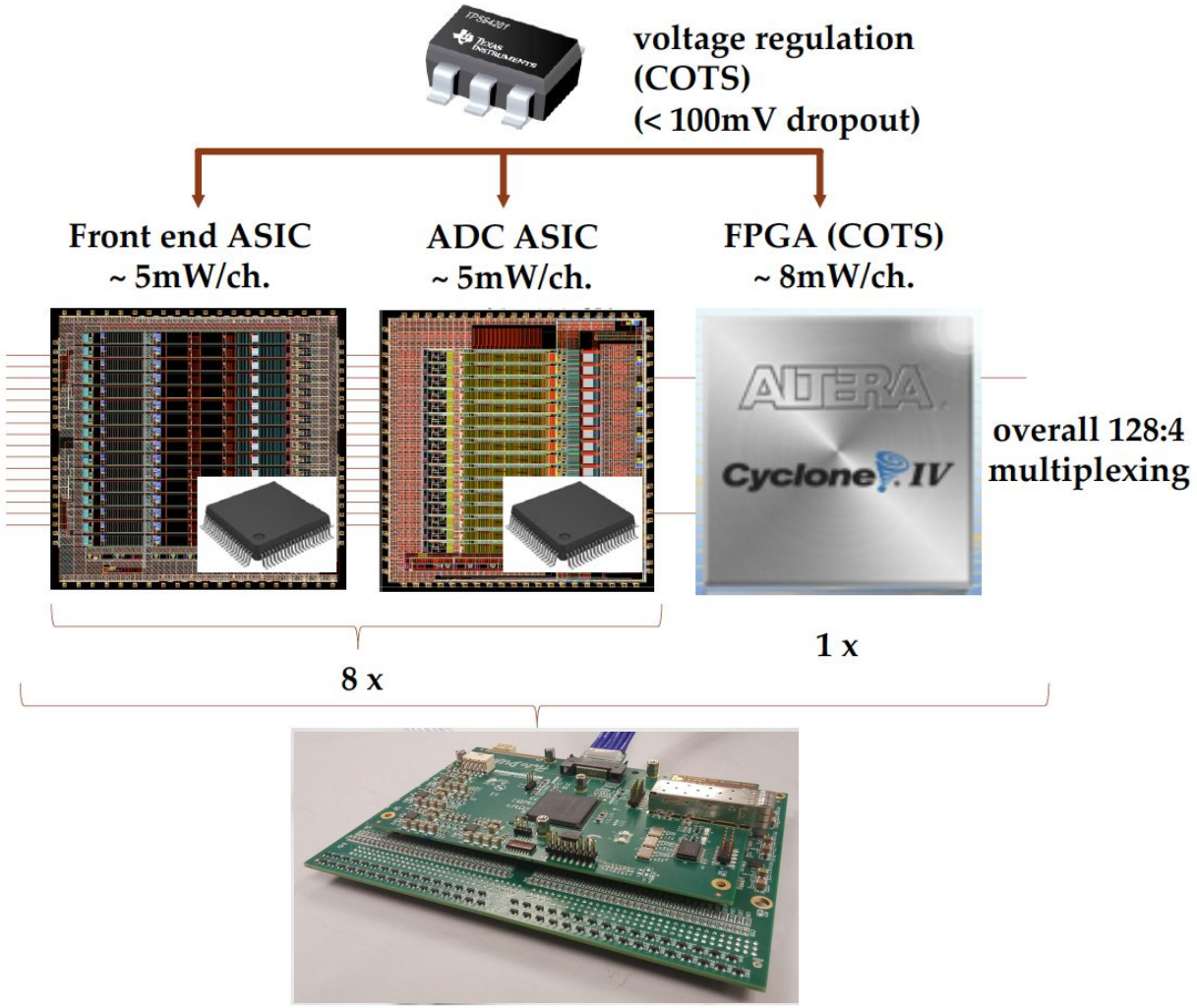


ProtoDUNE-I: First Stage of ProtoDUNE Experiment



- **Verifying LArTPC technologies for DUNE – a key test platform for DUNE FD**
  - Components
  - Construction methods
  - Installation procedures
  - Commissioning
  - Detector response to particles
- **ProtoDUNE-SP: Single-phase LArTPC prototype**
  - Sit in H4 beam line in EHN1 @ CERN
  - Consisting of 6 full-size APAs plus CPAs → 2 x **3.6 m** drift regions
  - Total ***15,360*** TPC channels
  - Use photon detectors of different fabrication methods
- ***Successful operation*** **with beam data taking in 2018**
  - Operation completed in 2020

From R&D at BNL to Full Cold Readout Chain

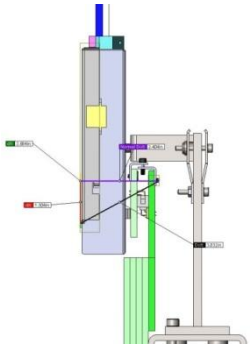
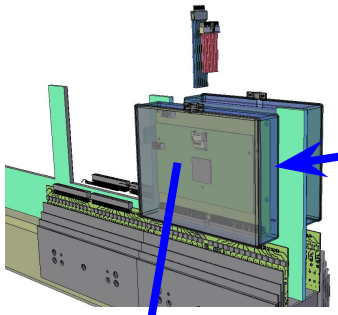


- **Front-End ASIC**
  - 16 channels, programmable
  - Adjustable gain & filter time constant
  - Built-in pulse generator with 6-bit DAC
- **ADC ASIC**
  - 16 channels, programmable
  - 12-bit ADC at 2 MS/s sampling rate
  - Multiplexer 8:1 or 16:1
  - Serializer 12:1
- **Cold FPGA**
  - Format digitized signal and drive data out of cryostat through serial links

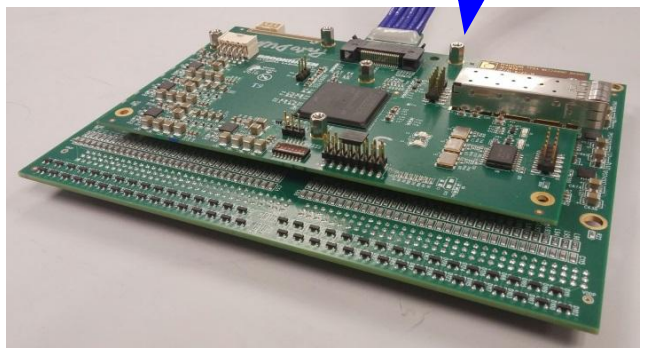
- **Full cold readout chain with FE ASIC, ADC ASIC and cold FPGA has been used to instrument the ProtoDUNE-SP LArTPC**

ProtoDUNE-SP Front End Electronics


7m Cold Cables

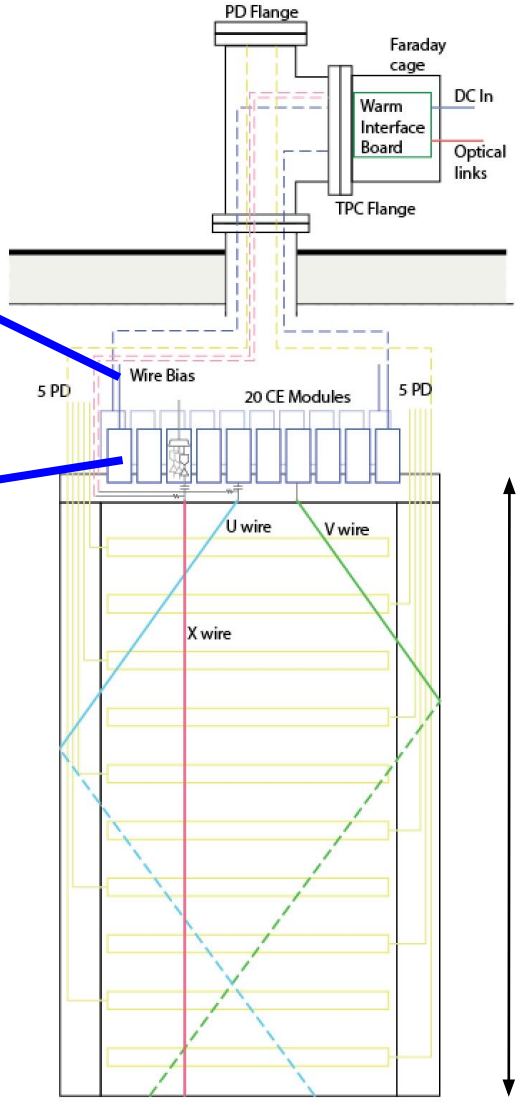



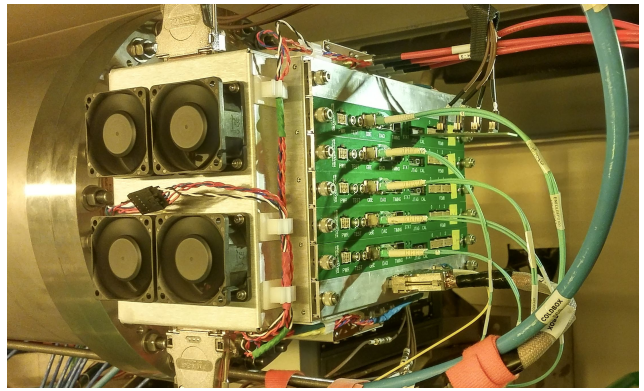
20 CE boxes on APA



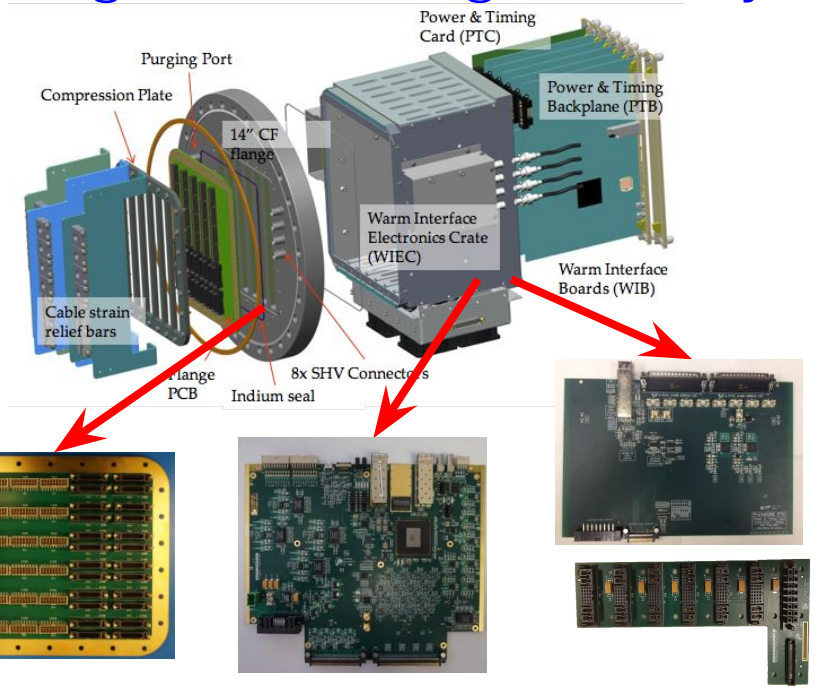
FEMB (inside CE box)

Cold Side





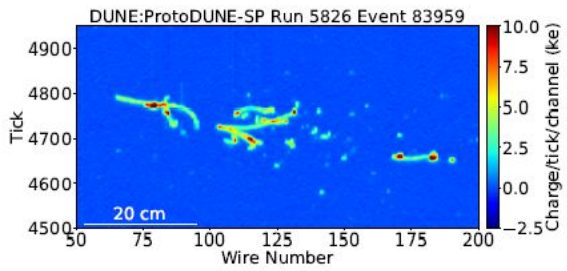
Signal Feed-through Assembly



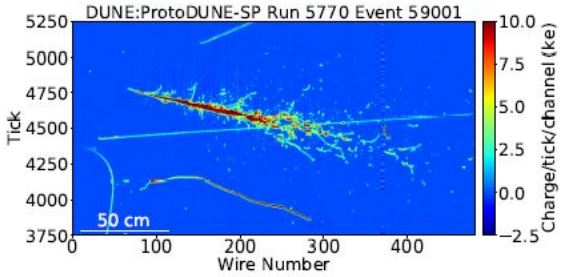
Warm Side

ProtoDUNE-SP LArTPC Performance

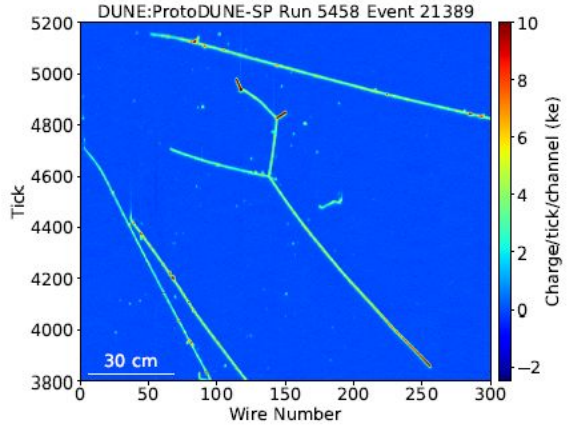
- **ArXiv:2007.06722 published on JINST**



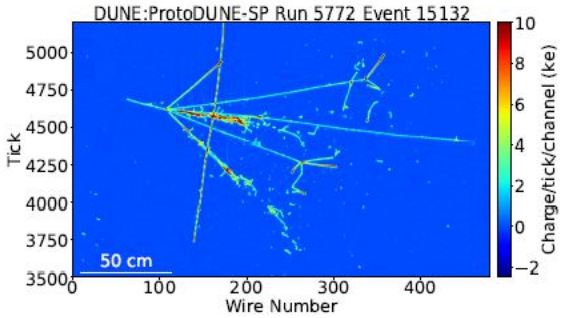
(a) A 0.5 GeV/c electron candidate.



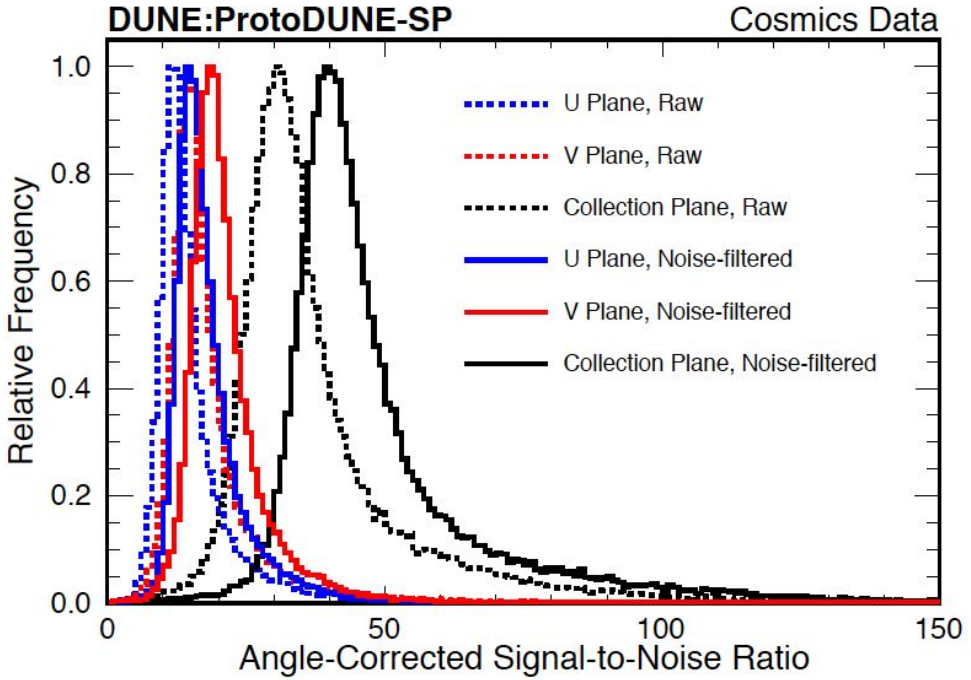
(b) A 6 GeV/c electron candidate.



(c) A 1 GeV/c pion candidate.



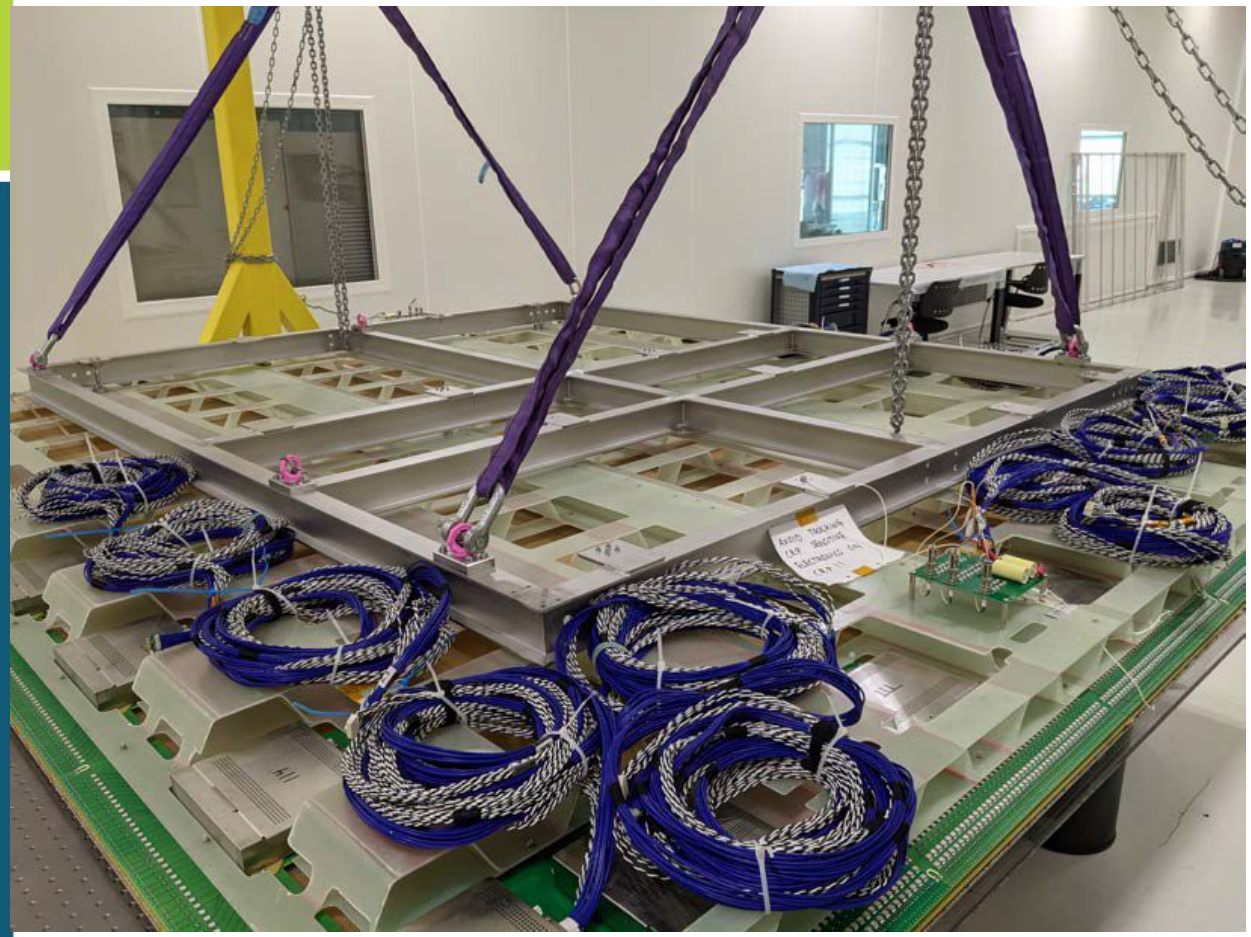
(d) A 6 GeV/c pion candidate.



- **S/N distributions after the noise mitigation**
  - **40.3** for the collection plane
  - **15.1** and **18.6** for the U plane and the V plane, respectively
  - TDR requirement is **9.0**

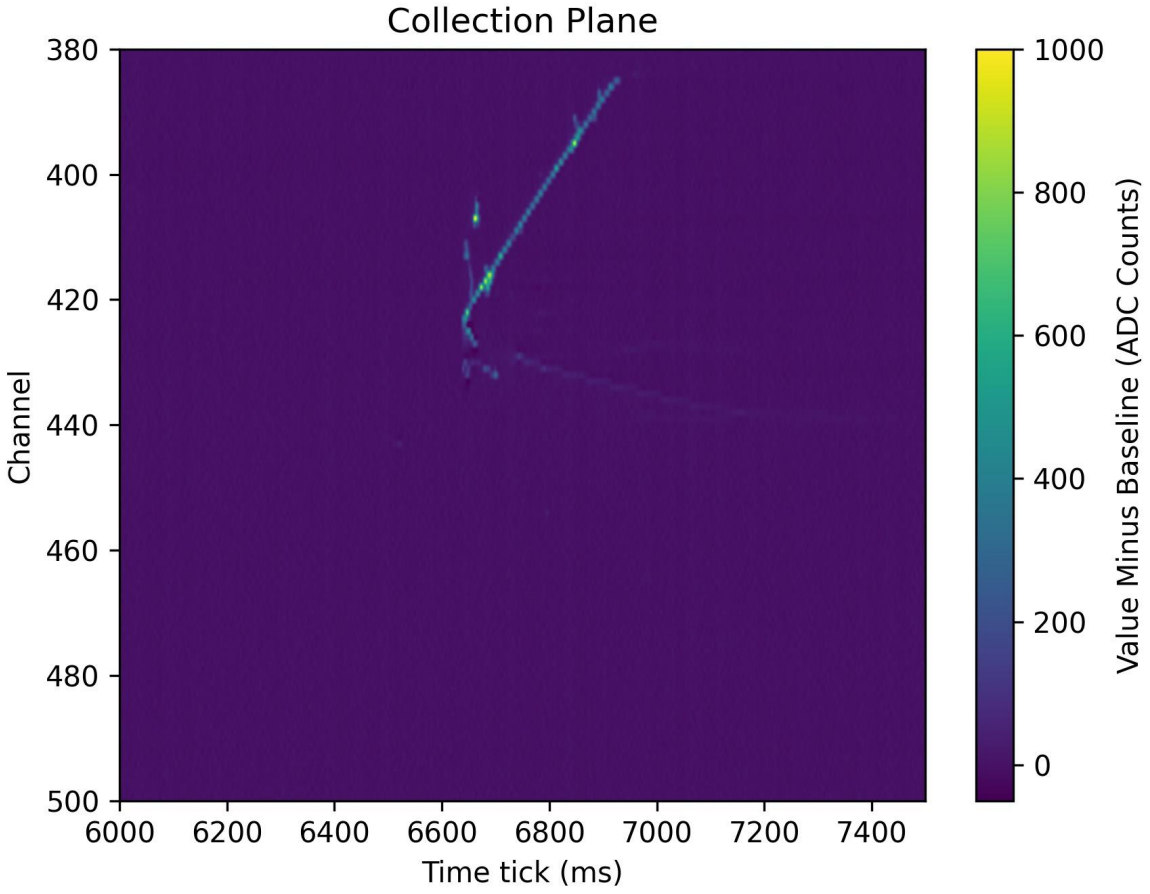
- ***Successful ProtoDUNE-SP experience*** **and ProtoDUNE-II assure DUNE FD1-HD**

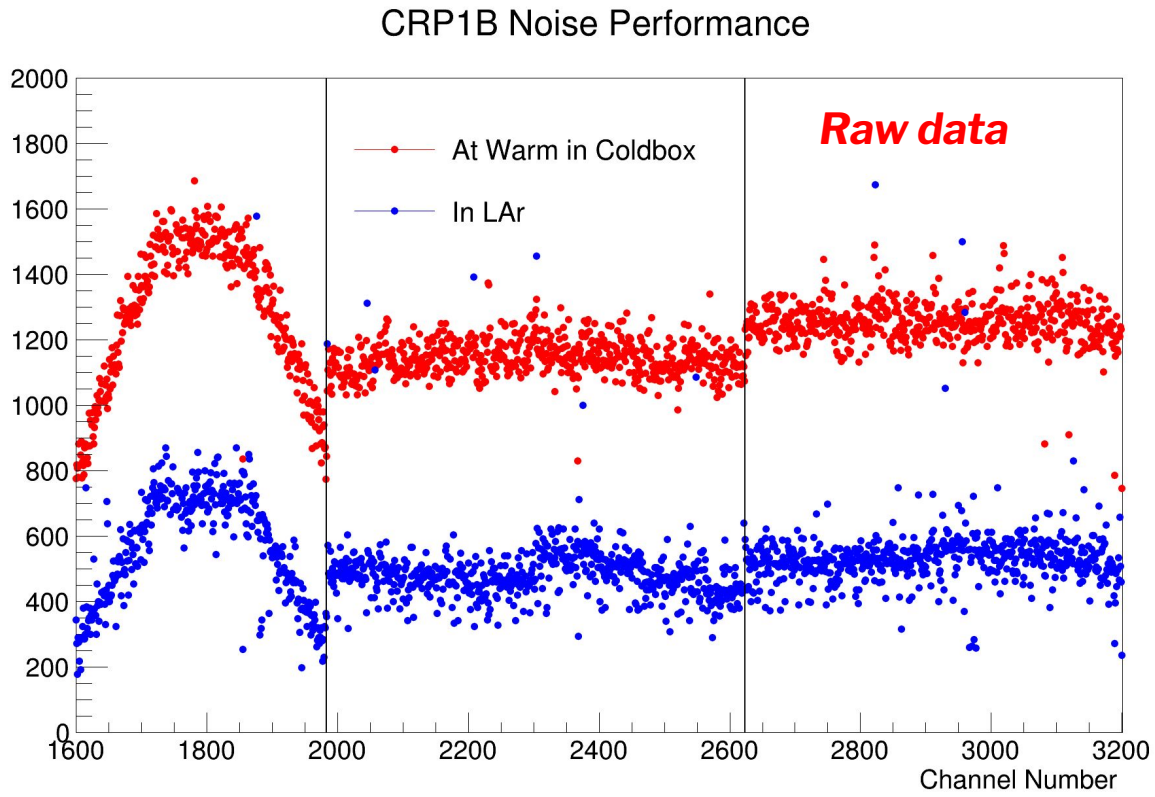
CRP Coldbox Test



- Half CRP1 instrumented with ProtoDUNE-SP cold electronics system in B185 at CERN
- CRP1 mounted under the lid being lowered into the coldbox in EHN1 at CERN

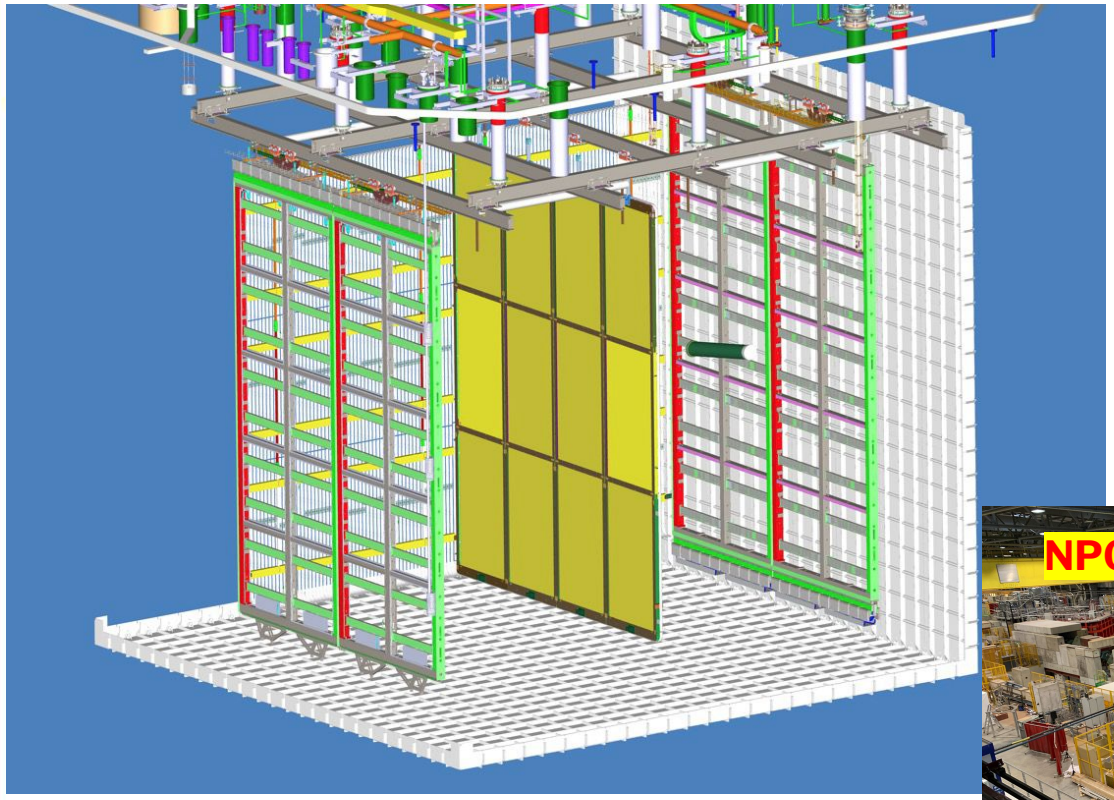
CRP1 LArTPC Performance

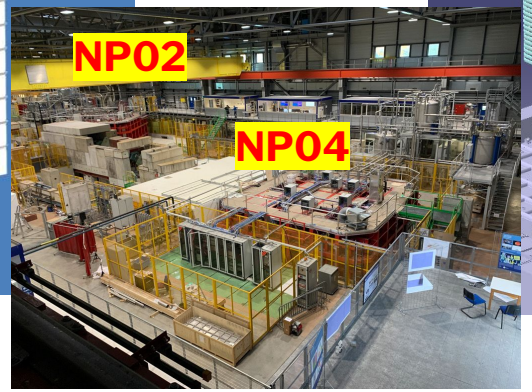


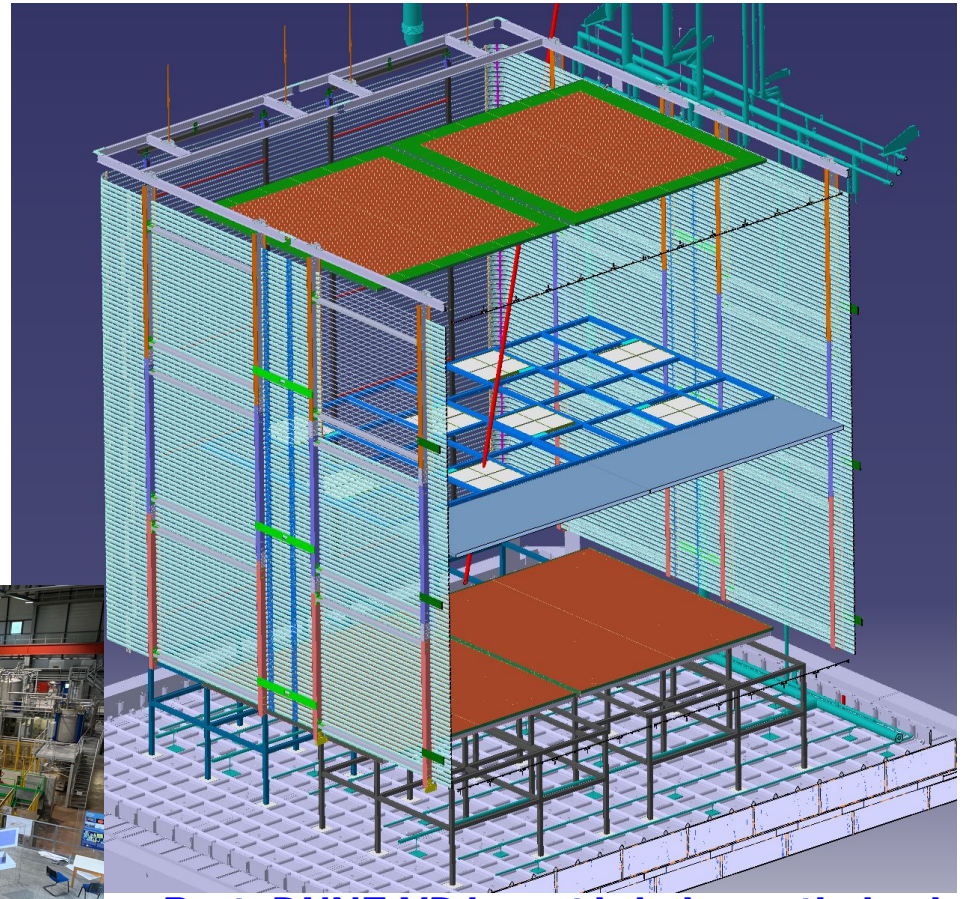


- **ENC of BDE in CRP1 coldbox test is *excellent and consistent* with ProtoDUNE-SP**
- ***Successful CRP1 operation in 2021/2022* and ProtoDUNE-II assure DUNE FD2-VD**

ProtoDUNE-II: Module 0 as Final Validation of FD1-HD and FD2-VD



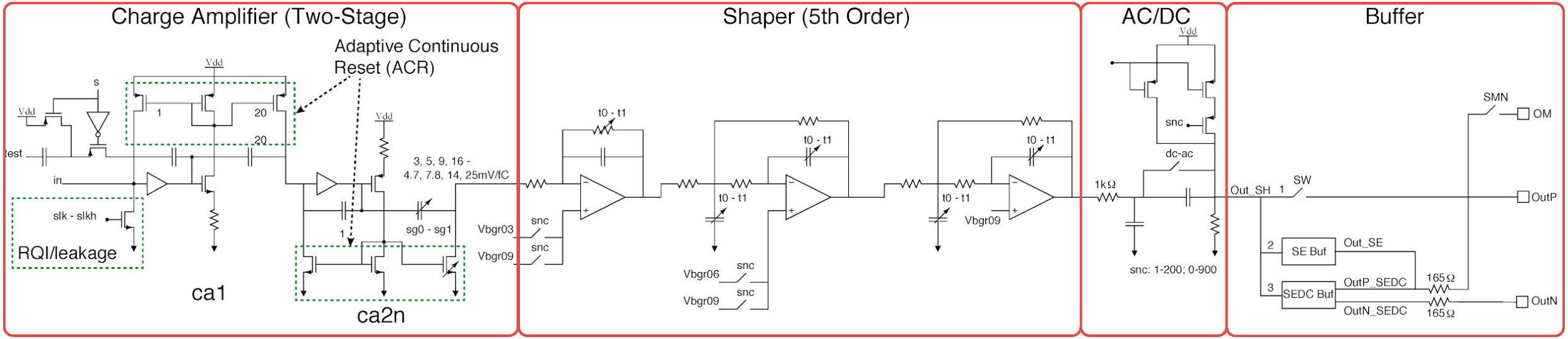


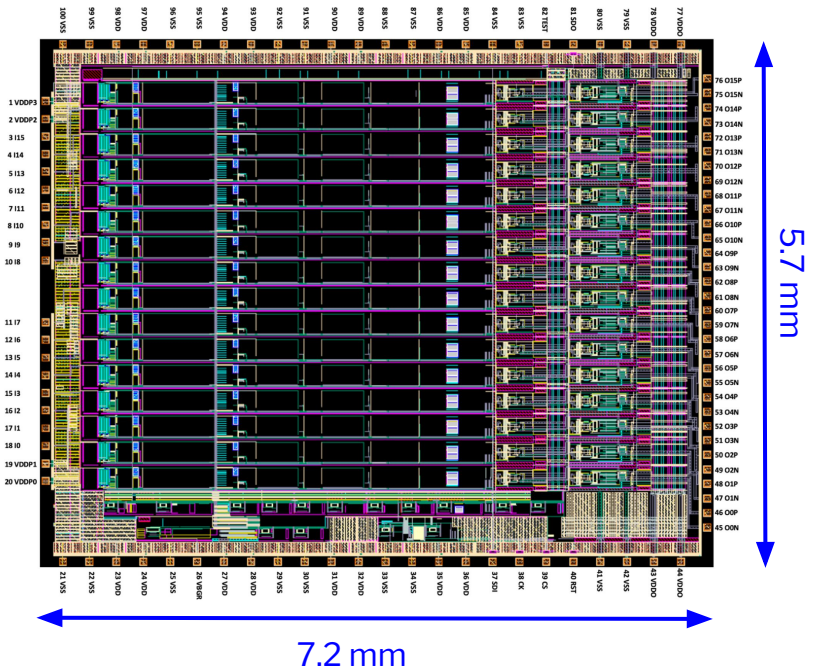


ProtoDUNE-VD layout is being optimized

- **ProtoDUNE-HD has 4 APAs in NP04 cryostat**
  - 2 APAs will have the ***cold electronics*** at the top
  - 2 APAs will have the ***cold electronics*** at the bottom
  - Total ***10,240*** TPC channels
- **ProtoDUNE-VD has 4 CRPs in NP02 cryostat**
  - 2 CRPs will have TDE at the top
  - 2 CRPs will have the ***cold electronics*** (BDE) at the bottom
  - Total 12,288 TPC channels, ***6,144 cold electronics*** channels

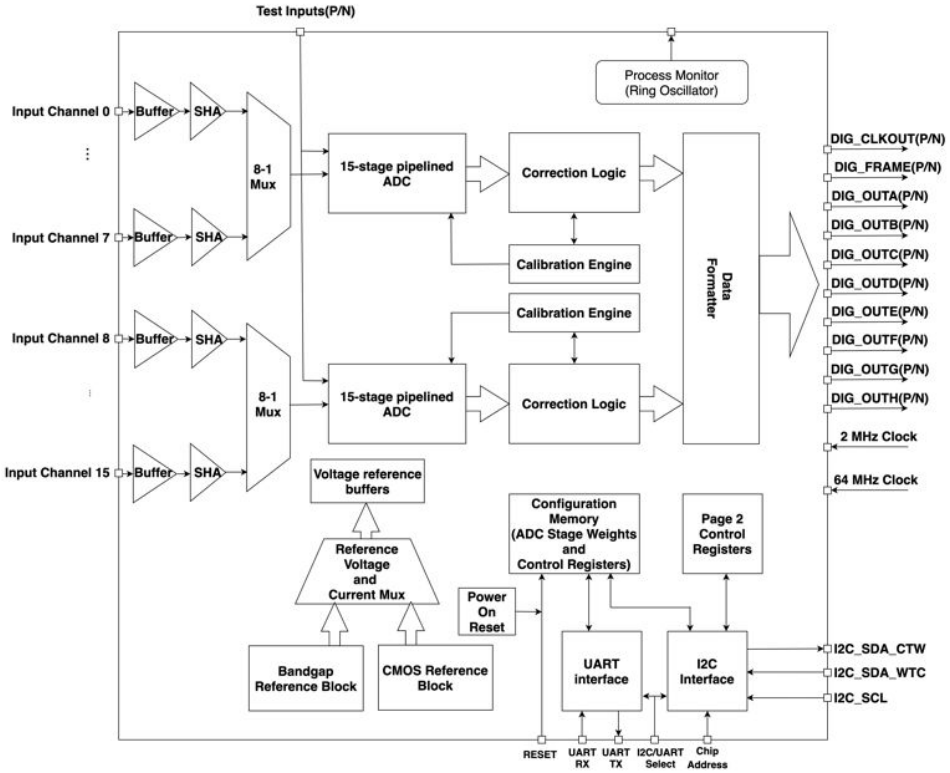
LArASIC – Front-End ASIC

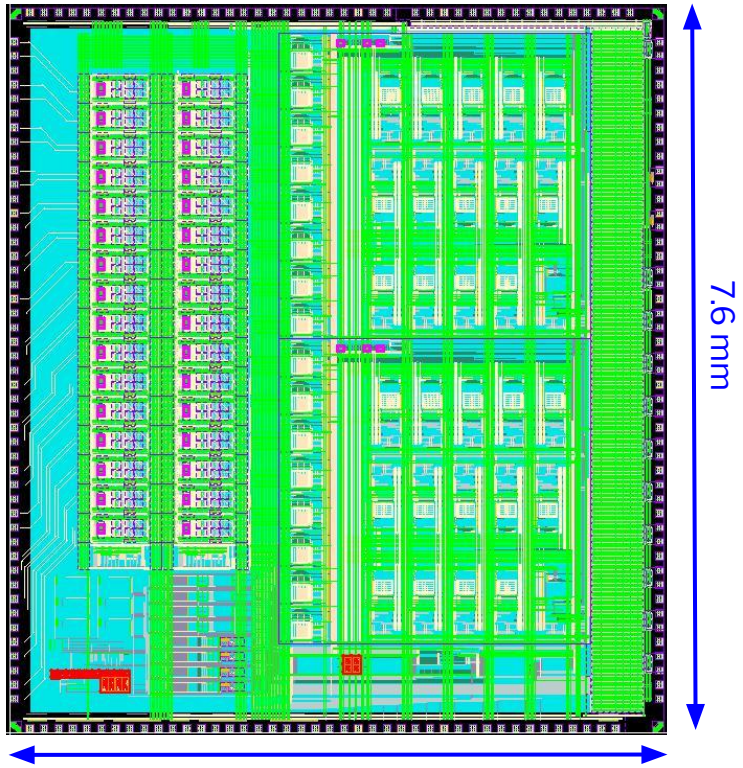




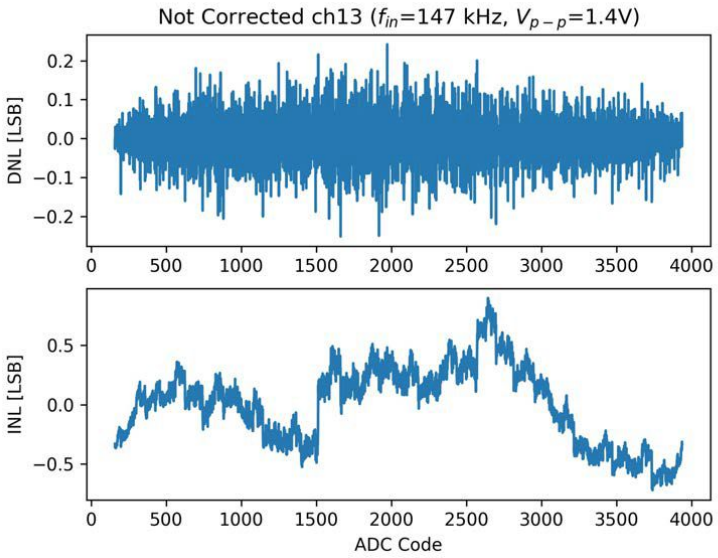
- **New Features**
  - Single-ended (SE) buffer or single-ended-to-differential conversion (SEDC) buffer
  - Integrated 6-bit DAC with 2-bit programmable gain for improved calibration pulse generator
  - SPI interface for 144 configuration register bits
  - Enhanced ESD protection without compromise noise performance
  - Leverages the existing cold models

ColdADC – ADC ASIC

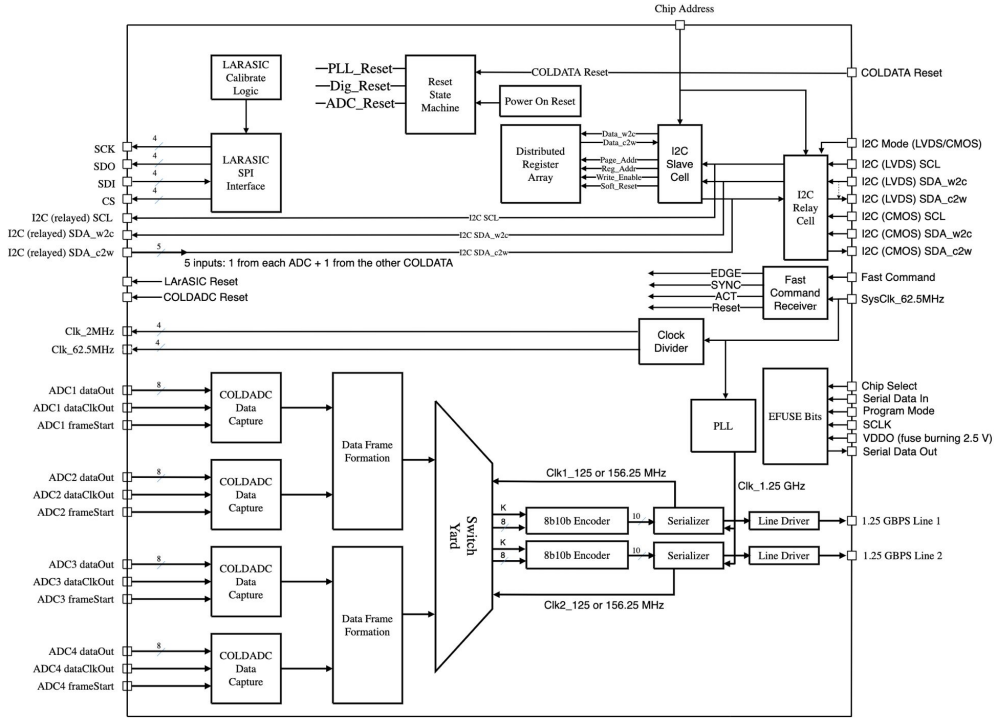


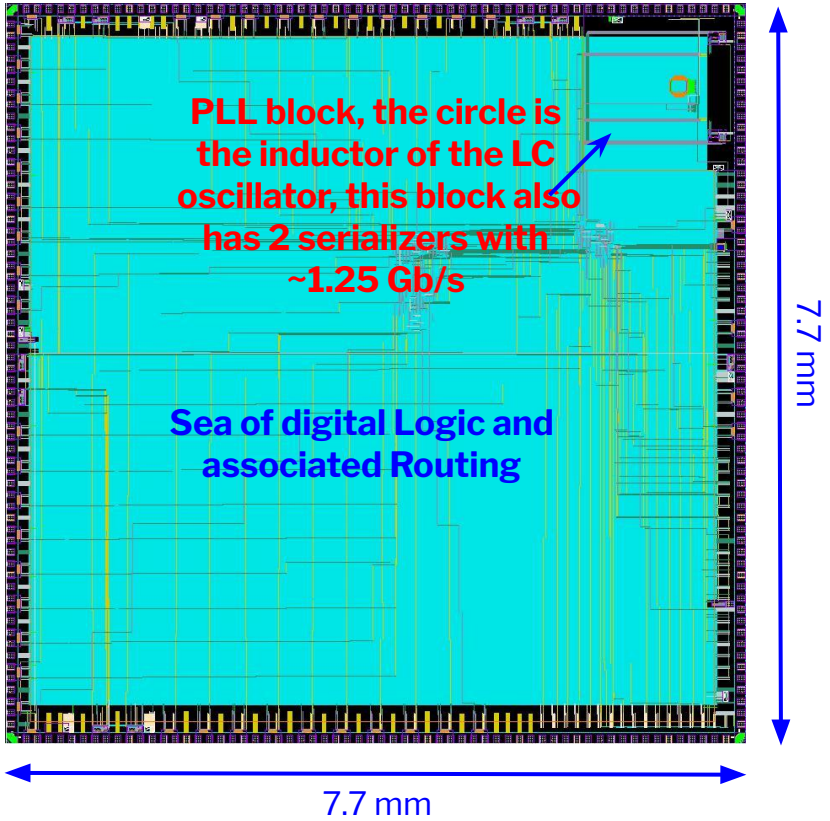


- **Key Features**
  - 16-channel, 12-bit 2 MS/s digitizer ASIC for 77-89 K
  - Two 15-stage pipelined ADCs
  - Designed by joint team from LBNL, FNAL and BNL
  - Low-noise and long lifetime operation in LAr
  - 65 nm CMOS process, 9 metal stack
  - Digital self-calibration for interstage gains

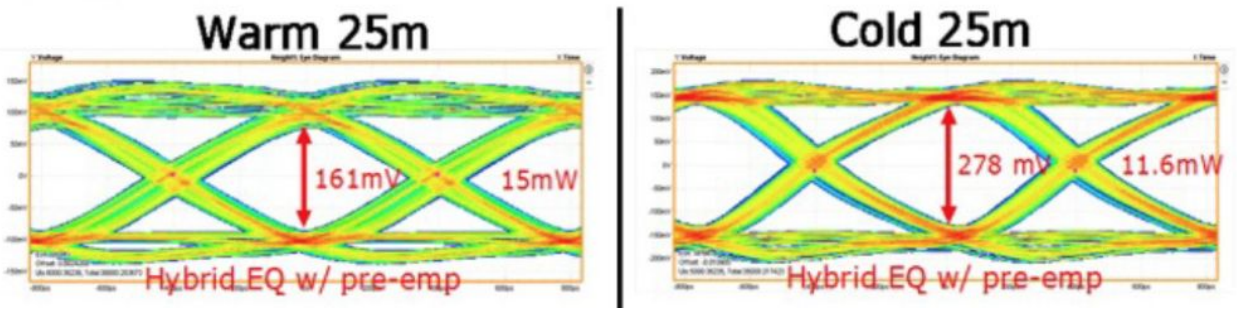


COLDATA – Serializer ASIC





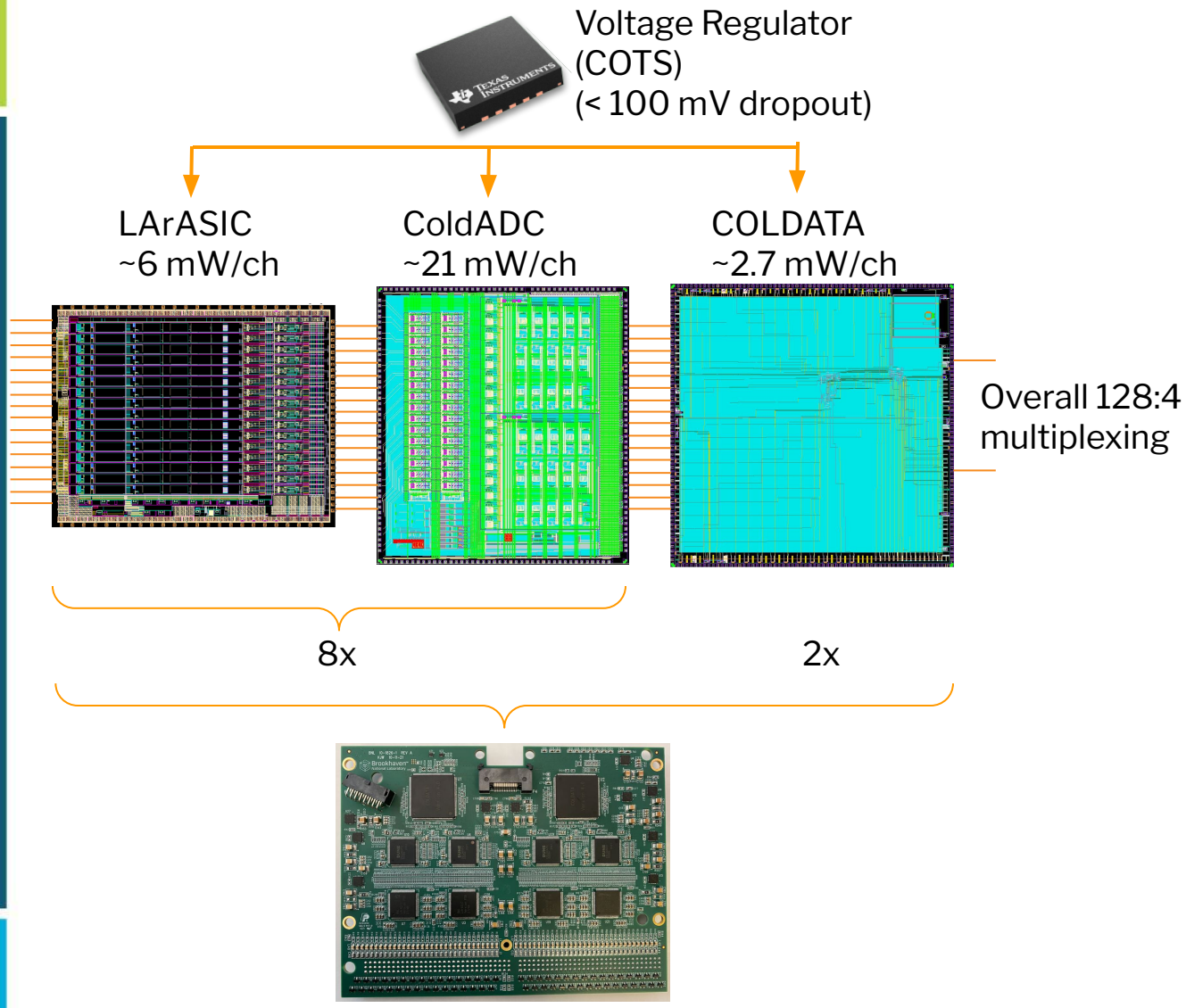
BER < 10^{-15}



Line driver eye diagram measurement results

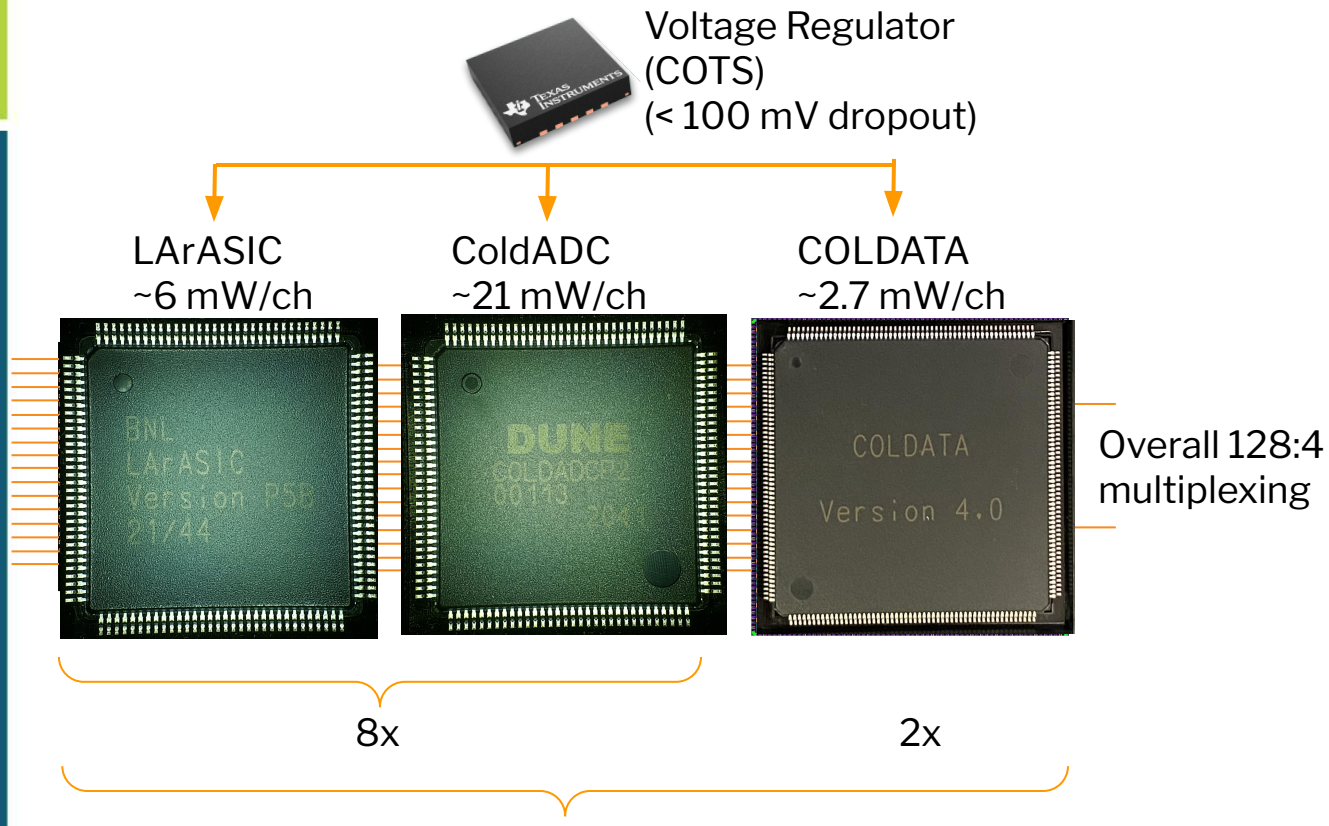
- **Key Features**
  - Designed by FNAL, BNL and SMU
  - Design for cryogenic, long lifetime operation
  - Control 4 ColdADCs and 4 LArASICs
  - Accept data from 4 ColdADCs
  - Format ADC data (truncate to 12 or 14 bits) & pack into an array of 8-bit words
  - Combine packaged arrays from pairs of ADCs into 2 output data frames
  - Encode the output data using 8b/10b
  - Drive the output data to a WIB at 1.25 Gb/s
  - Digital-on-Top design methodology
  - 65 nm CMOS process, 9 metal stack
  - Leverages the existing cold models

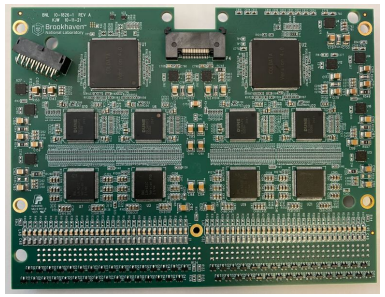
Cold Readout Chain for ProtoDUNE-II and DUNE FD



- **P5B LArASIC**
  - 16 channels, programmable
  - SE or SEDC buffer
  - Enhanced ESD protection
- **P2 ColdADC**
  - 16 channels, programmable
  - 12-bit ADC at 2 MS/s sampling rate
  - Two 15-stage pipelined ADCs
- **P4 COLDATA**
  - Control 4 ColdADCs and 4 LArASICs
  - Receive and format data from 4 ColdADCs
  - Drive data via 2 links to a WIB at 1.25 Gb/s

Cold Readout Chain for ProtoDUNE-II and DUNE FD





- **P5B LArASIC**
  - 16 channels, programmable
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- **P2 ColdADC**
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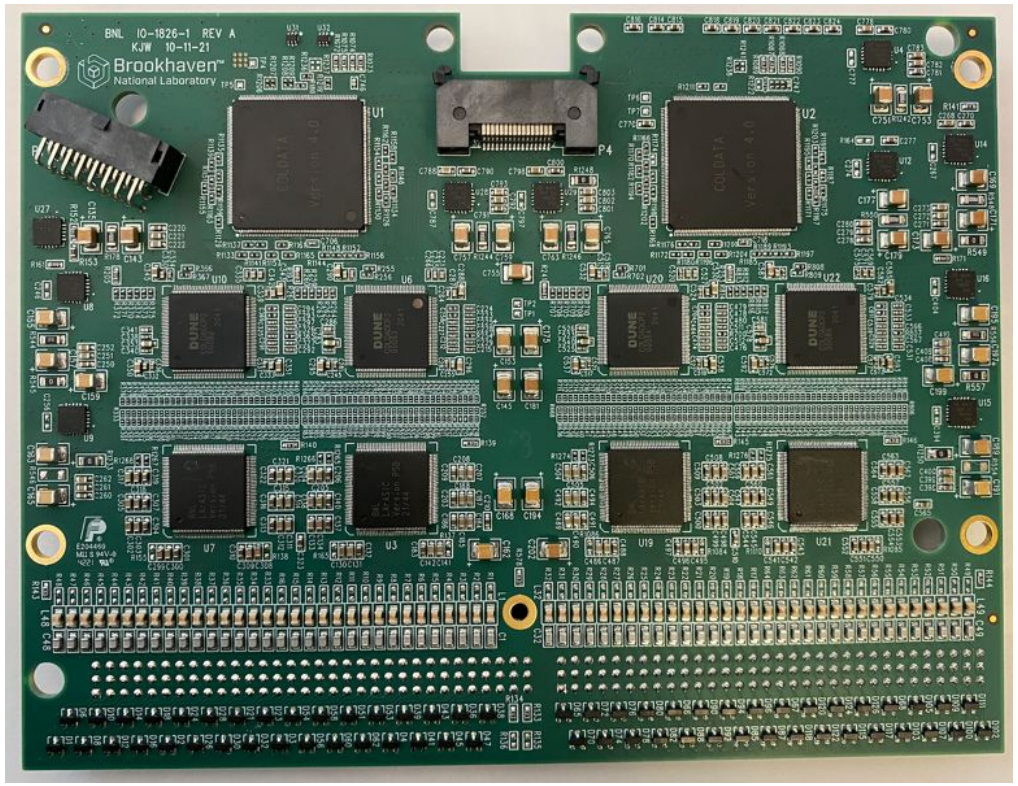
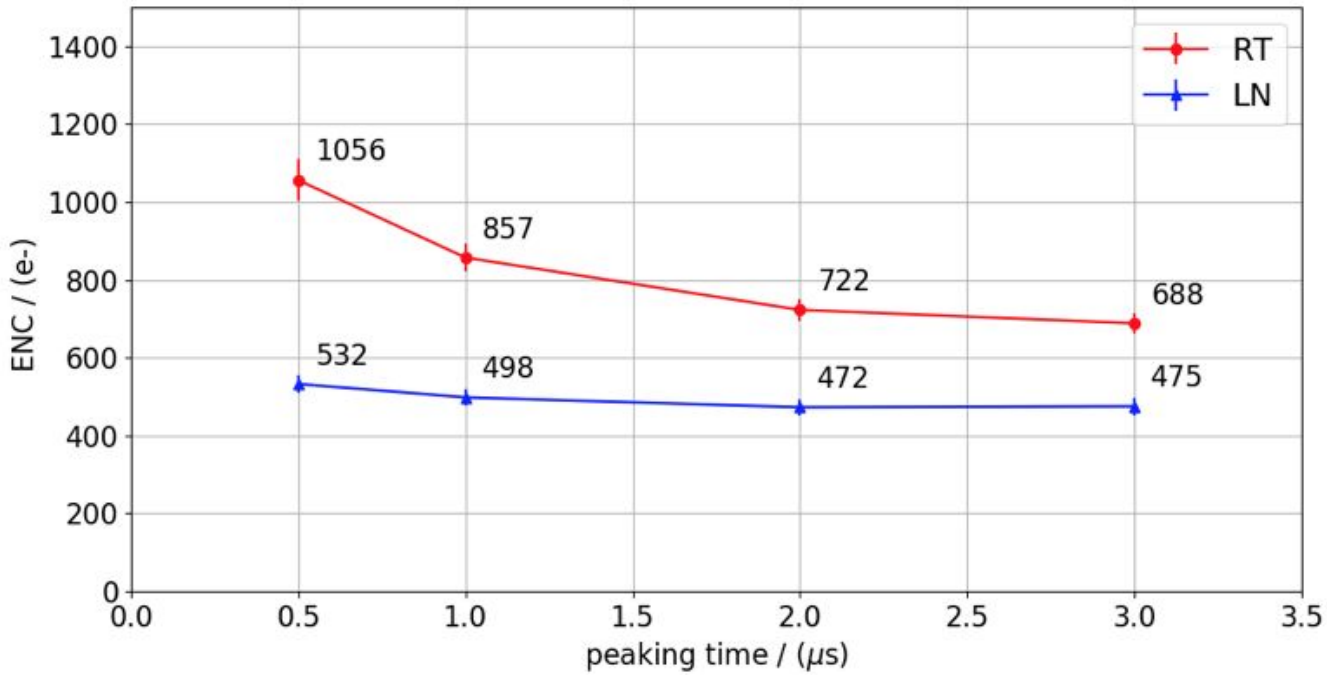
  - 12-bit ADC at 2 MS/s sampling rate
  - Two 15-stage pipelined ADCs
- **P4 COLDATA**
  - Control 4 ColdADCs and 4 LArASICs
  - Receive and format data from 4 ColdADCs
  - Drive data via 2 links to a WIB at 1.25 Gb/s

- **Full cold readout chain with P5B LArASIC, P2 ColdADC and P4 COLDATA will be used to instrument the ProtoDUNE-II LArTPC**

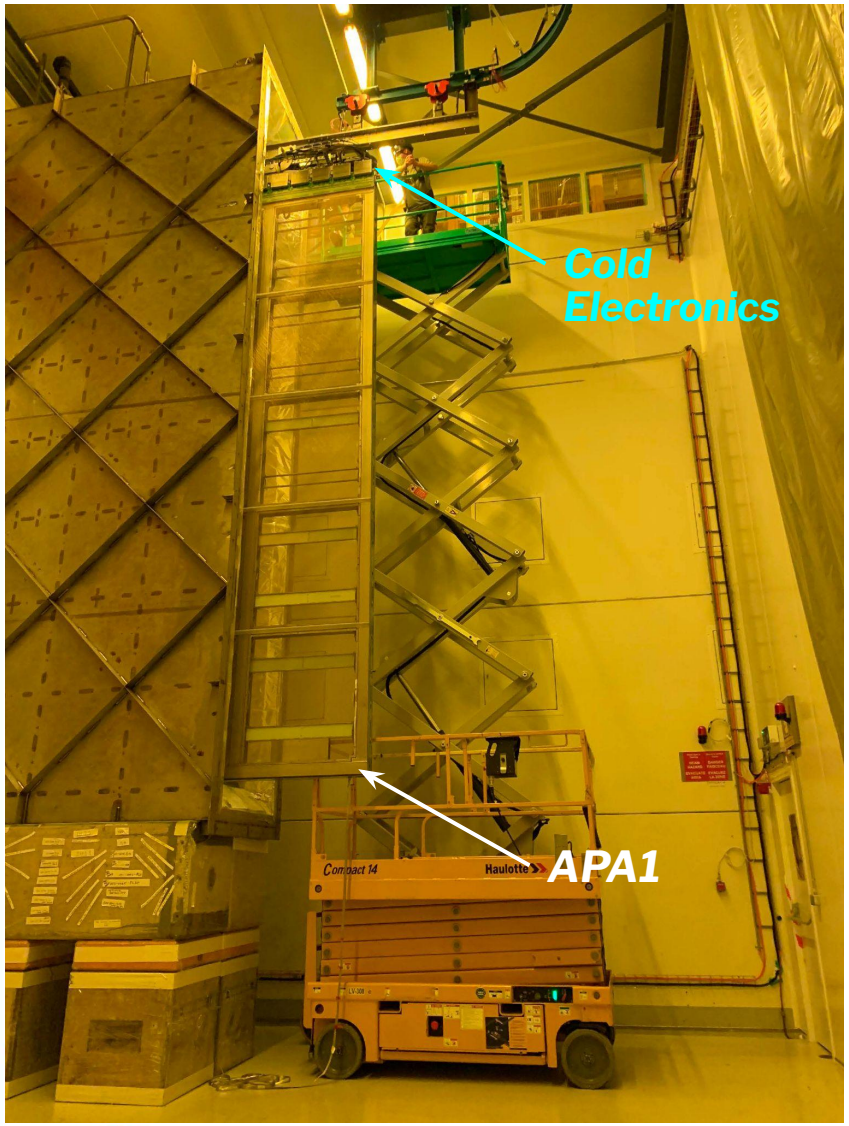
Monolithic FEMB



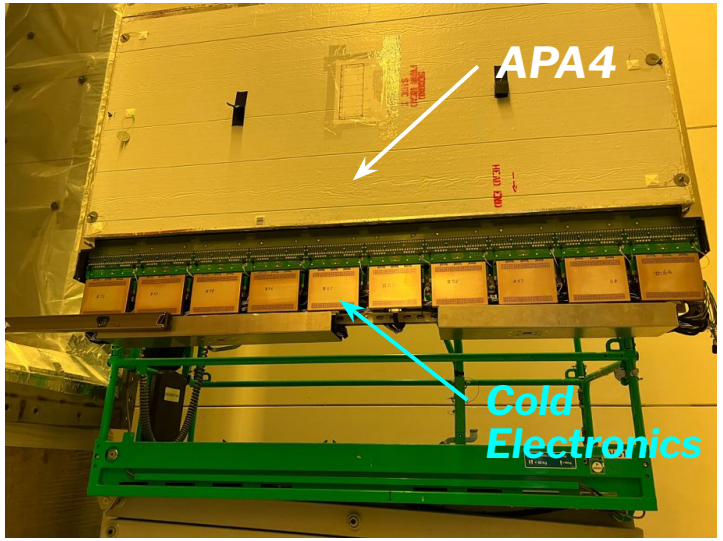


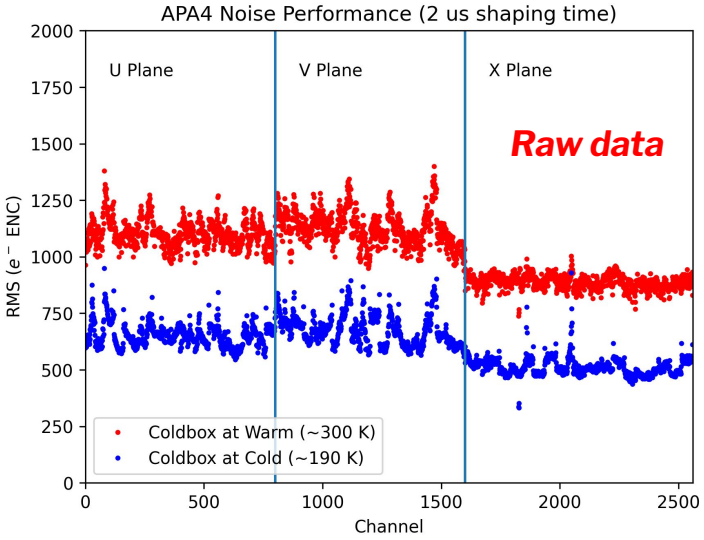
- **Monolithic FEMB with final design of three ASICs**
  - P5B LArASIC, P2 ColdADC and P4 COLDATA
- **The noise measurement of monolithic FEMB with 150 pF C_d shows good ENC performance**
  - ~500 e^- at 1 us peaking time and 14 mV/fC gain

Outlook



- **ProtoDUNE-HD cold readout electronics production is ongoing**
  - Plan to finish the detector installation and commissioning by fall **2022**
  - Start beam data taking before the end of year LHC technical stop
- **ProtoDUNE-VD will go through a series of coldbox tests at CERN EHN1 in 2022**
  - Plan to finish the detector installation, commissioning and start data taking in **2023**
- ***ProtoDUNE-II* as *Module 0* will serve as *important milestones* before the final *production* of the cold readout electronics system gets started as part of the construction of *FD1-HD* and *FD2-VD* modules**

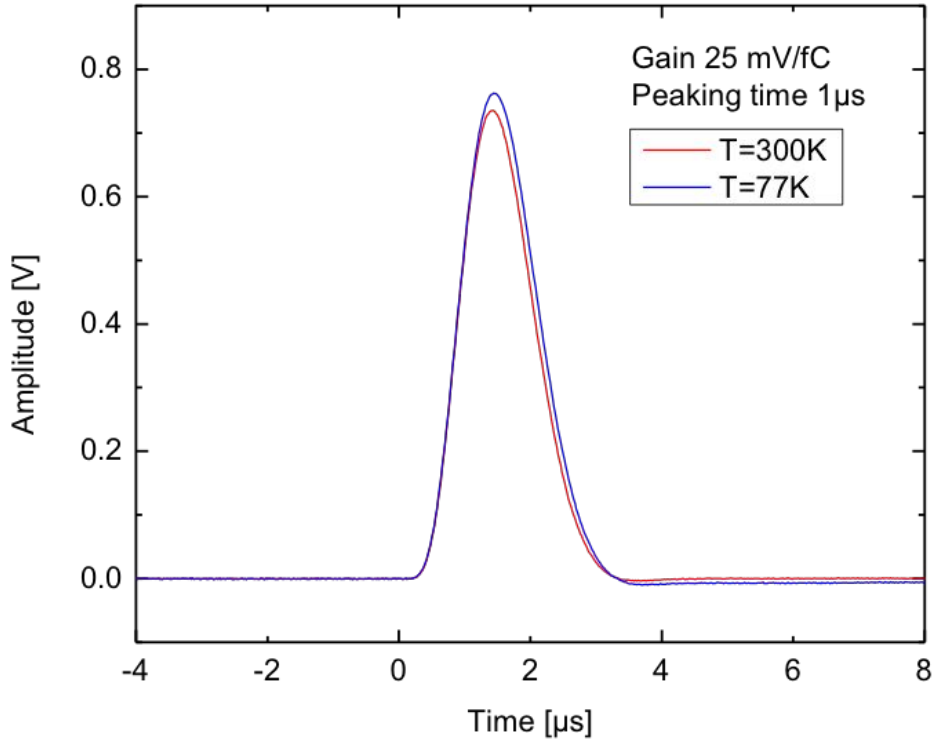




Brookhaven National Laboratory

Backup Slides

FE ASIC - Programmability



Bandgap Reference

$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{ at } \ 300\ ^{\circ}K \\ 1.164\ V \ \text{ at } \ 77\ ^{\circ}K \end{cases}$$

variation ≈ 1.8 %

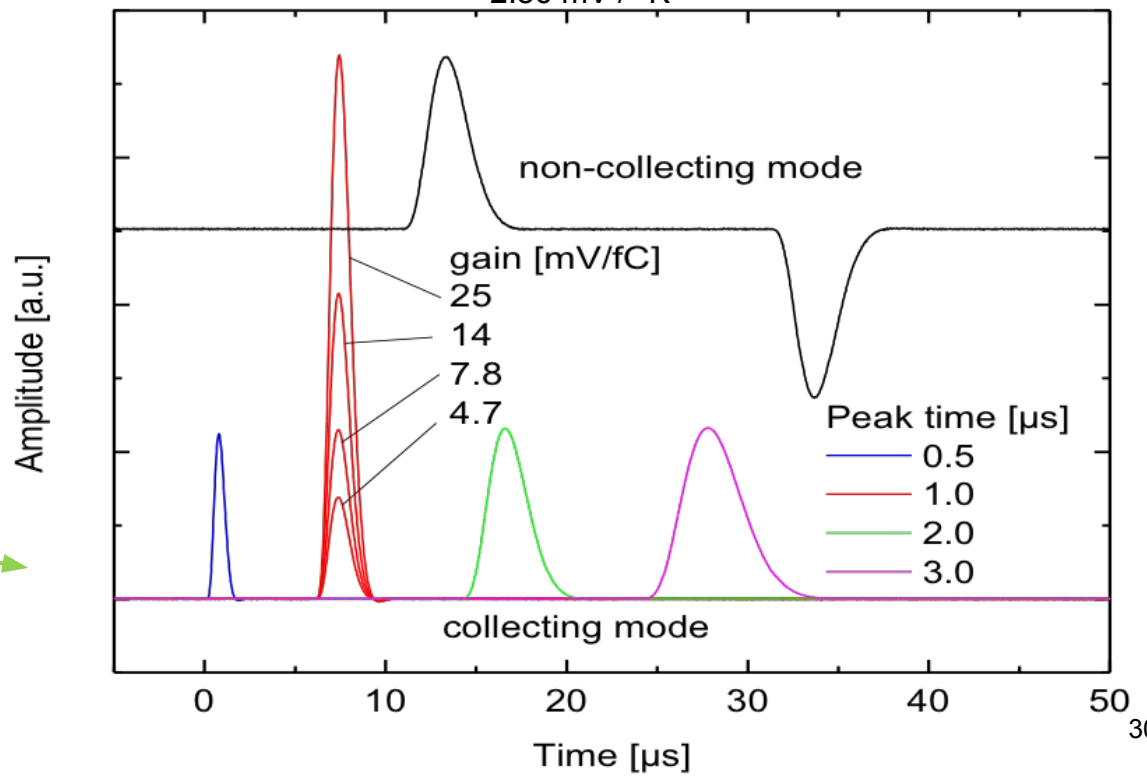
Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{ at } \ 300\ ^{\circ}K \\ 259.3\ mV \ \text{ at } \ 77\ ^{\circ}K \end{cases}$$

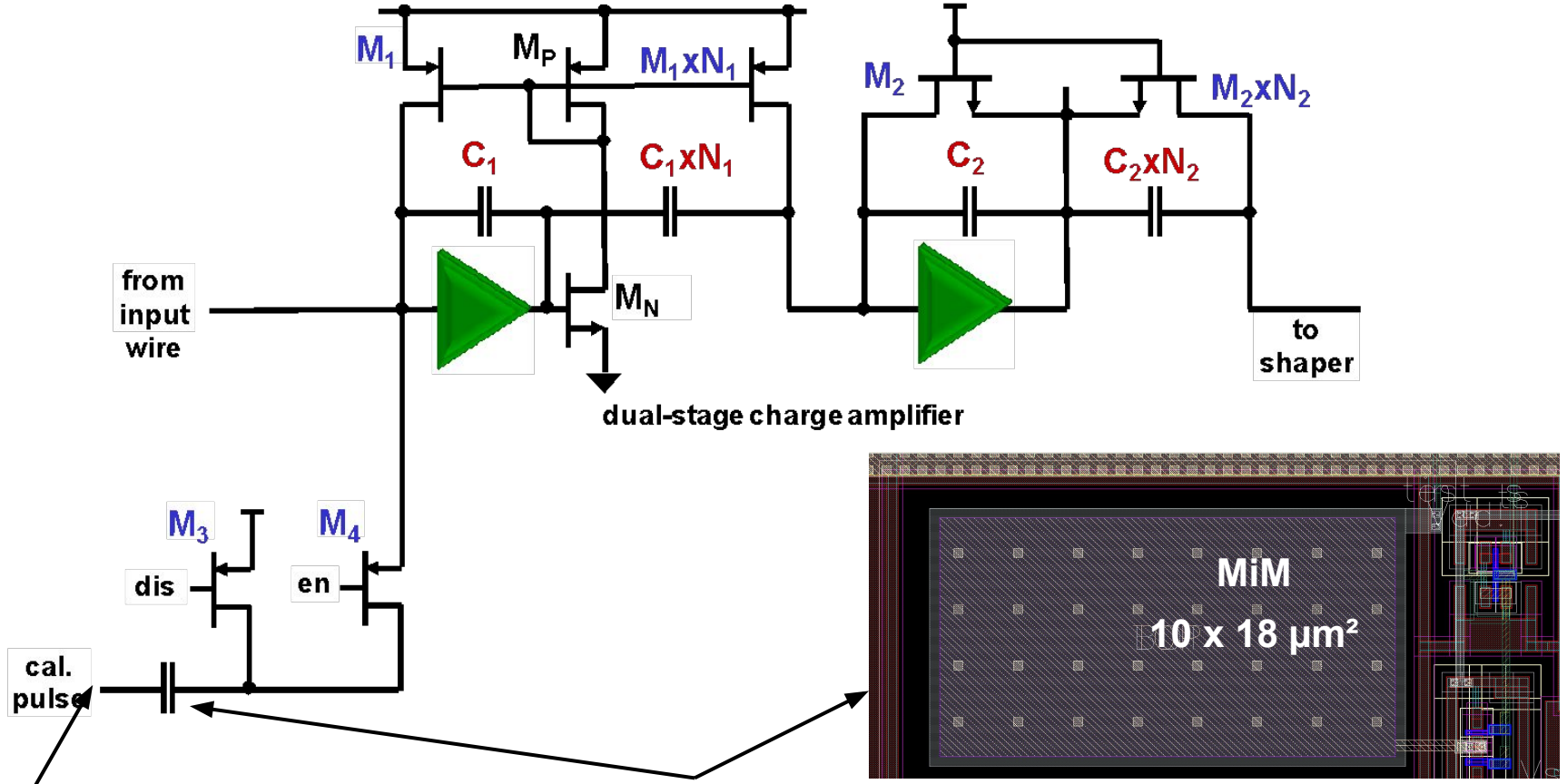
~ 2.86 mV / °K

Adjustable gain, peaking time and baseline

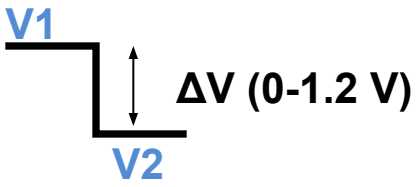
maximum charge 55, 100, 180, 300 fC



FE ASIC - Calibration Circuit



Internal or external pulse generator



injection capacitor (per-channel enable)

- nominal value: 198 fF
- same-run non-uniformity 0.25% rms
- run-to-run non-uniformity 2.5% rms
- measured: 184 fF at 300 K
  183 fF at 77 K (0.5 %)

$$\Delta Q = C_{inj} \cdot \Delta V$$

↓

0-230 fC

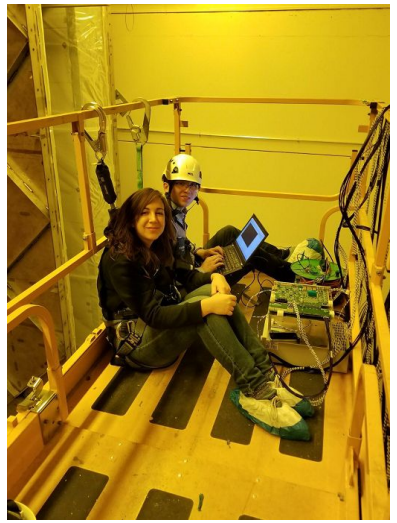
CMOS Lifetime Study – Principle Findings

- **In parallel, studies of CMOS lifetime and reliability at 77 K have been conducted**
  - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
- **A study of hot-electron effects on the device lifetime has been performed for the TSMC NMOS 180 nm technology node at 300 K and 77 K**
  - Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (V_{ds}), and a separate measurement of the substrate current (I_{sub}) as a function of $1/V_{ds}$
  - The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current , $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of V_{ds} *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and DUNE falls naturally into this domain, where hot-electron effects are negligible*
- ***Lifetime of digital circuits (ac operation) is extended by the inverse duty factor*** $4/(f_{clock} t_{rise})$ ***compared to dc operation***
  - This factor is large (> 100) for deep submicron technology and clock frequency needed for TPC

Cold Electronics Installation on APA

CE box checkout (in barrack)

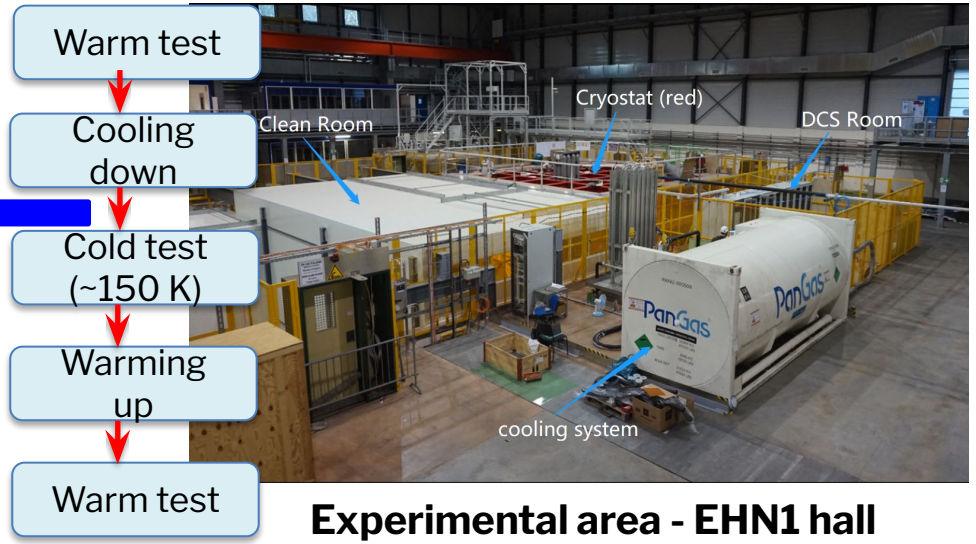
Install CE boxes on the top of APA



CE box checkout (on APA)

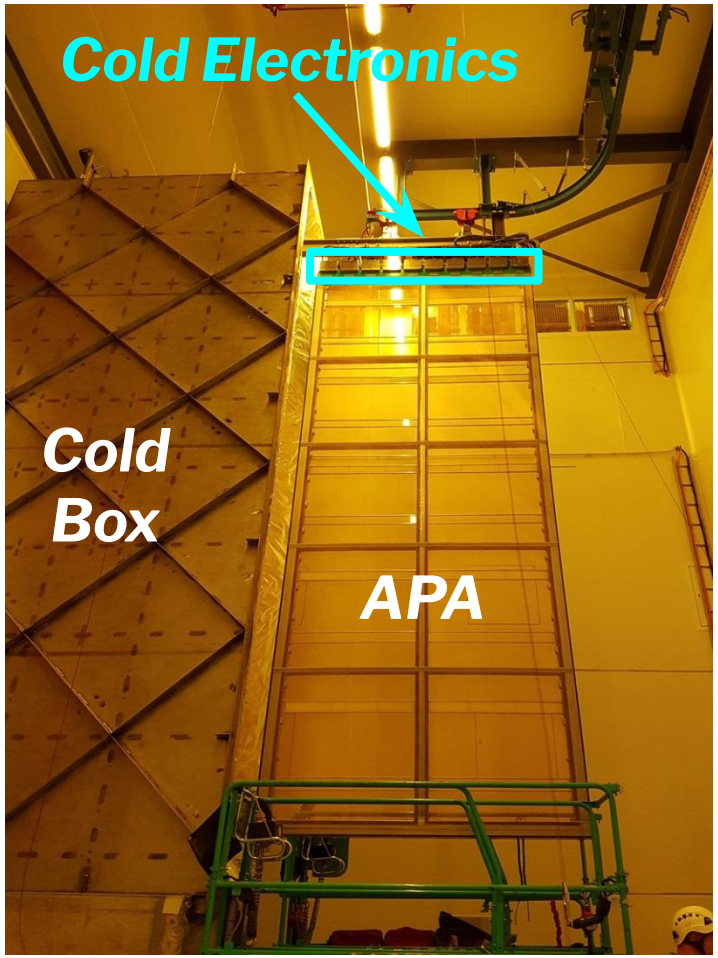
Move APA into the cold box

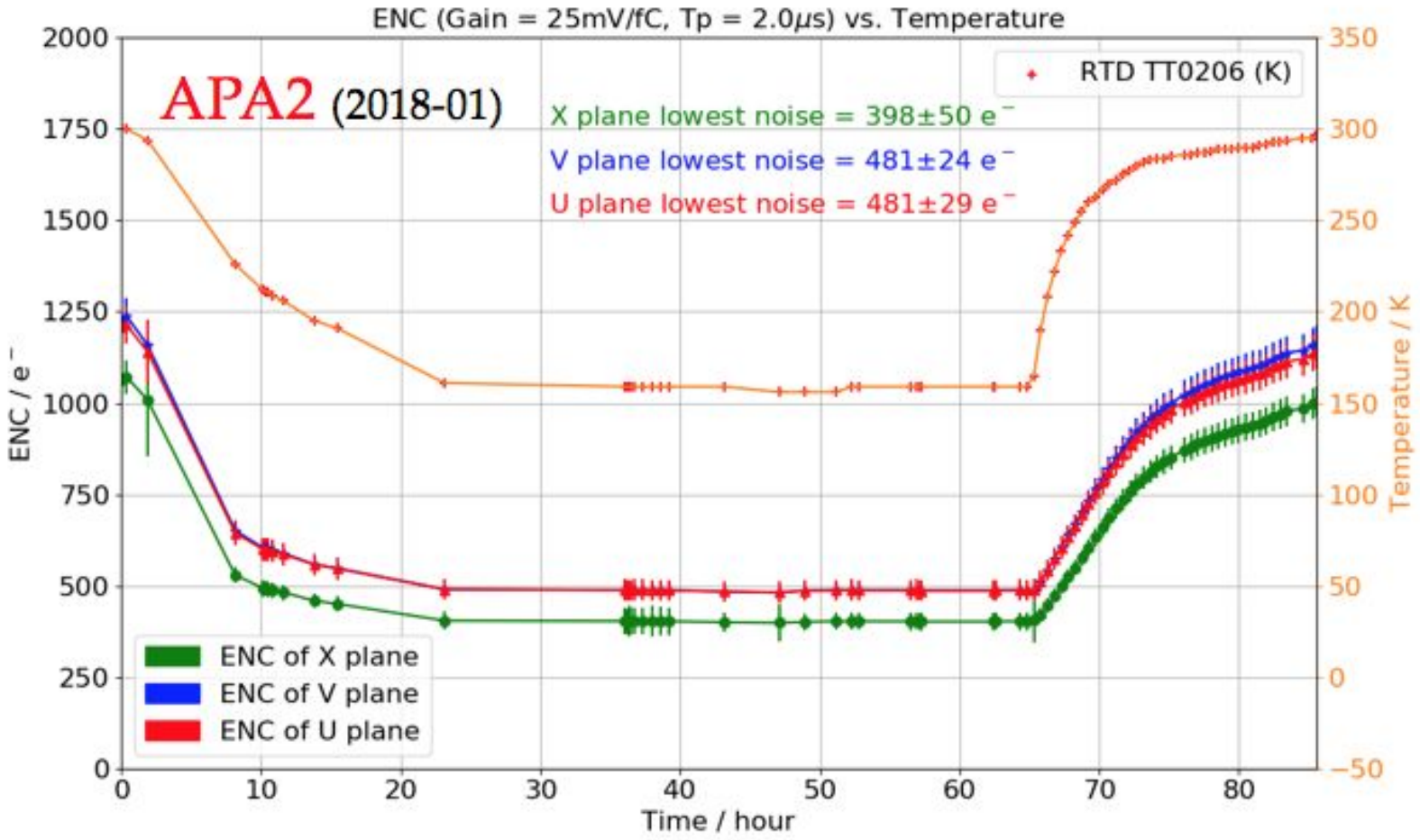
Move APA into Cryostat



Experimental area - EHN1 hall

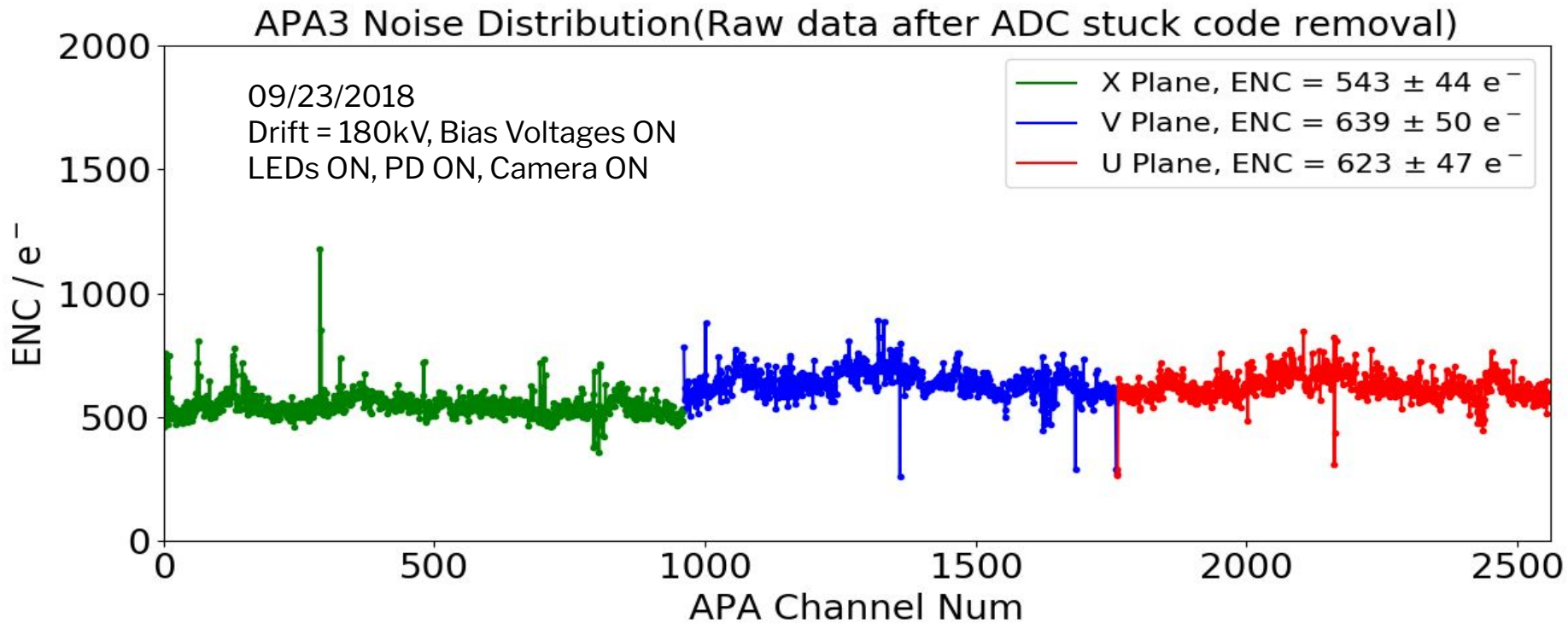
ProtoDUNE-SP Front End Electronics System Integration





- ***Excellent noise performance (< 500 e⁻) obtained in cold box test at CERN***
- ***All front-end electronics have been delivered, installed and tested on 6 APAs at CERN by summer 2018***

ProtoDUNE-SP ENC Performance



- **With drift 180 kV and nominal bias voltages**
  - **99.74% (15,320 of 15,360)** of TPC channels are active regardless of noise performance
  - Only 4 inactive FE channels, others can be attributed to TPC etc.
- **Noise performance with drift and bias on**
  - ENC of collection (X) plane (5,473 of 5,760 channels): **565 ± 60 e⁻**
  - ENC of induction (V) plane (4,347 of 4,800 channels): **662 ± 56 e⁻**
  - ENC of induction (U) plane (4,439 of 4,800 channels): **651 ± 54 e⁻**