EPFL AQUA Lab cryogenic projects

Edoardo Charbon

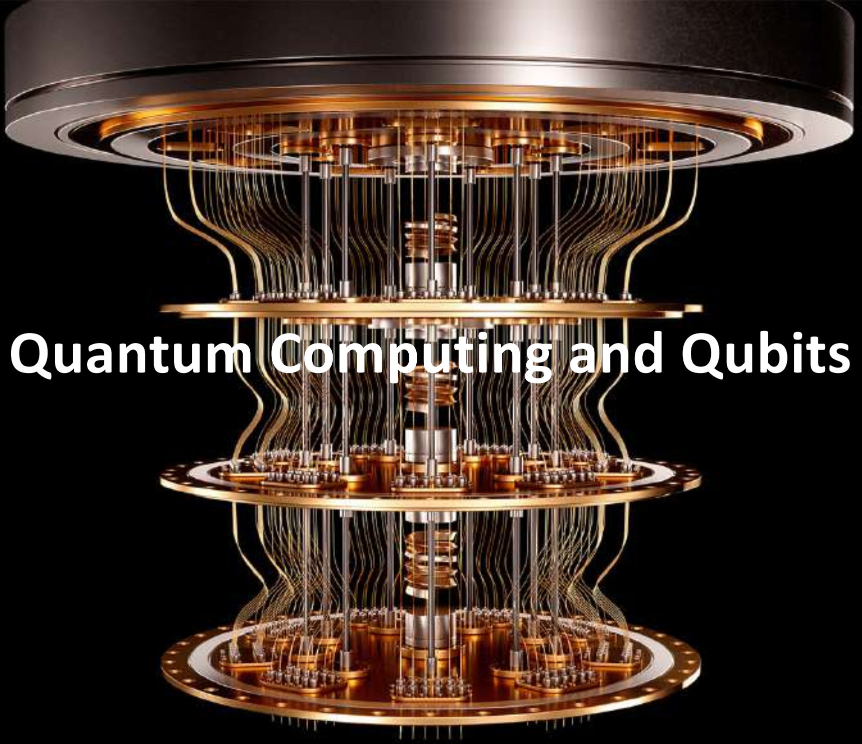
EPFL

MONOLITH, September 6th, 2022

Acknowledgements

Swiss National Science Foundation
STW-NWO
European Commission
aqualab
http://aqua.epfl.ch

Quantum Computing and Qubits



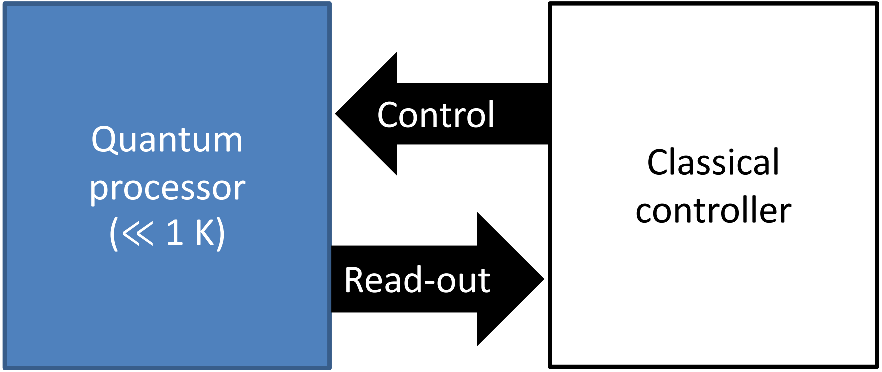
Quantum Computing

- Spearheaded by many, *in primis* Richard Feynman
- Proposal to use of **entanglement** and **superposition** for computation
- Fundamentals and theory developed in the 1980-2000

There is plenty of space at the bottom

- Richard Feynman

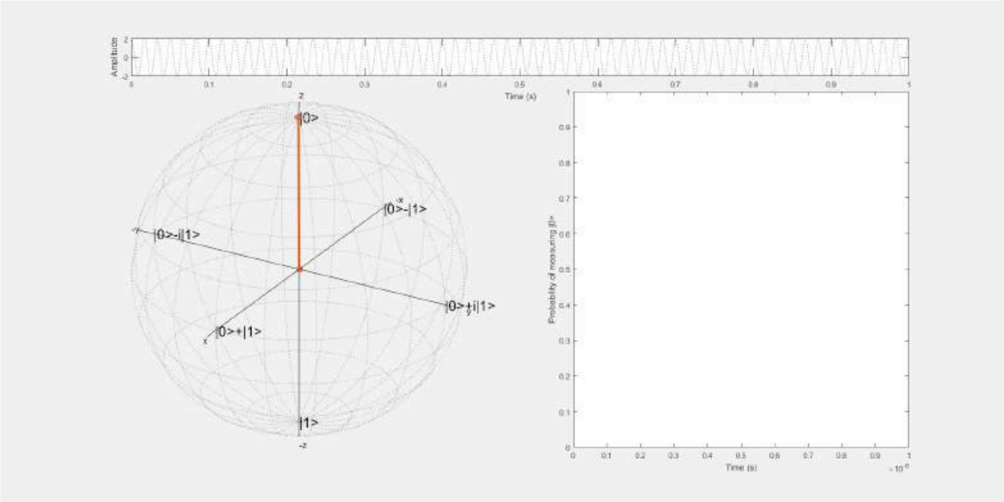
Interfacing Qubits with the Classical World



- Carrier frequency: 2 – 20 GHz
- Pulses: 10 – 100 ns
- Readout techniques for spin qubits: **ESR, EDSR**

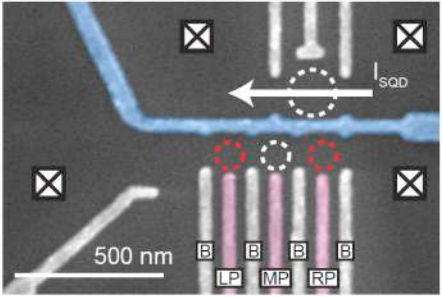
ESR: Electron spin resonance – EDSR: Electric dipole spin resonance

Example: Qubit Transition from $|0\rangle$ to $|1\rangle$

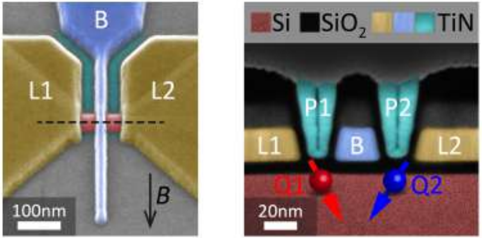


© Jeroen van Dijk

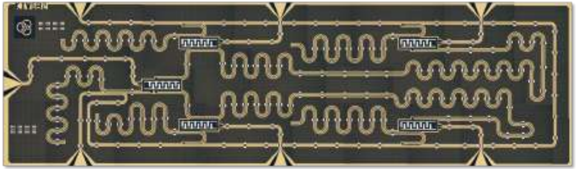
Solid-State Qubits: Spin and Superconductive

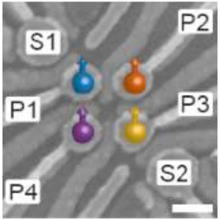


Semiconductor quantum dots (Vandersypen group)



Hole-spin qubits (Kuhlmann group)

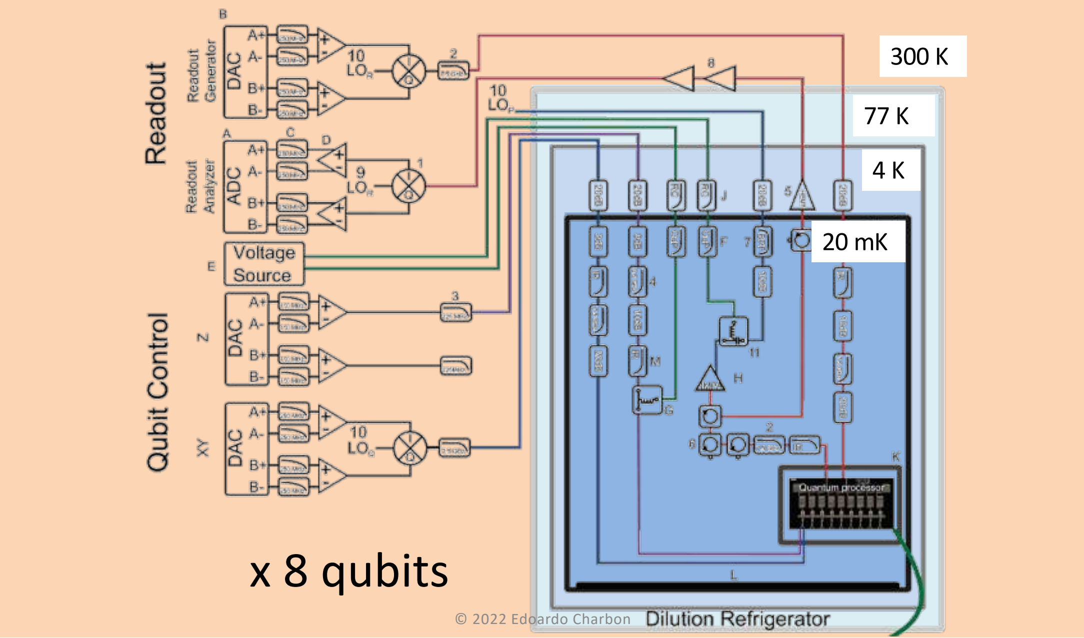

Superconducting circuits (DiCarlo group)



Ge qubits (Velthorst/Scappucci groups)

The Role of Cryogenic Electronics

A Real-life Quantum Computer



x 8 qubits

Today's Solution

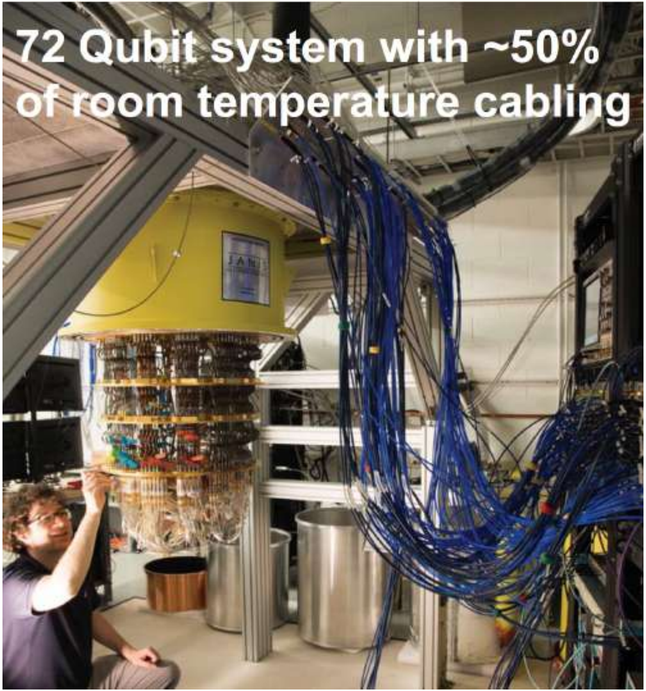
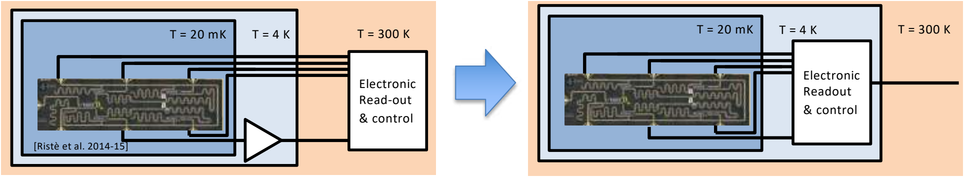


Image: Google Bristlecone. Taken from: J.C. Bardin et al., *"An Introduction to Quantum Computing for RFIC Engineers"* , RFIC Symposium 2019

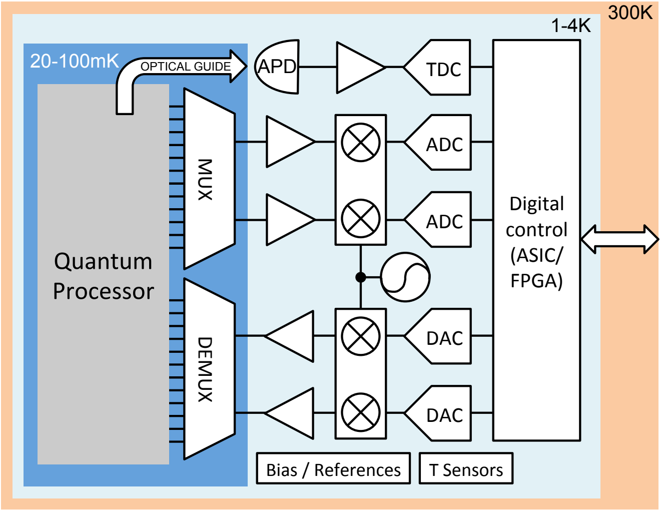
Proposed Solution

- **Proposed solution**
  - Electronics at 4 K
  - Only connections to 4 K to 20 mK are needed



- **Ultimate solution**
  - Qubits at 4 K
  - Monolithic integration

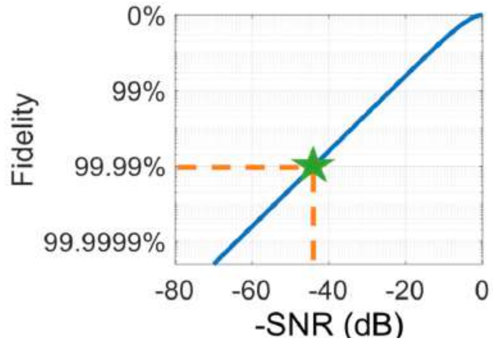
Electronic Readout & Control



E. Charbon *et al.*, *IEDM* 2016

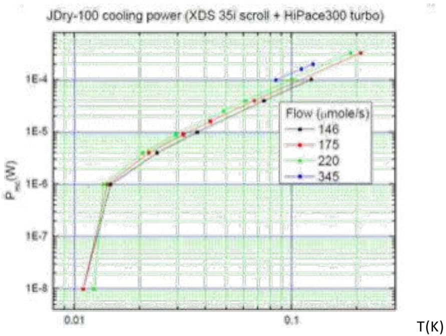
From Qubit Fidelity to Electrical Specs

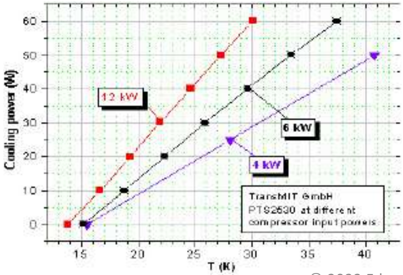
- State-of-the-art spin qubits: fidelity < 99.9%
- Target: 99.99% (four 9's)
  - This translates to a SNR > 44 dB for a bandwidth of 25 MHz



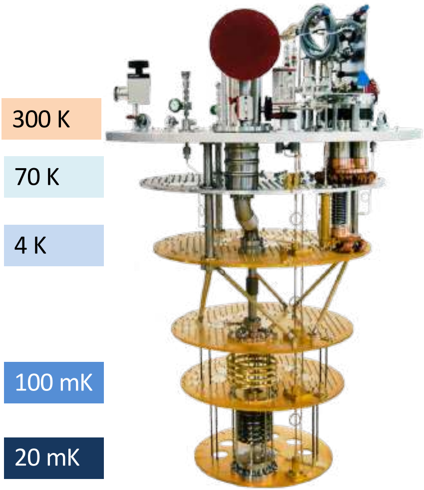
J. v.Dijk et al., *PRA* 2019

Cooling Power Issue





Dilution refrigerator



Courtesy: Oxford instruments

Scalability Issue

- Noise budget…………………………………………..< 0.1nV/√Hz
- Power budget (for scalability)………………… << 2mW/qubit
- Physical dimensions (for scalability)……… 30nm
- Bandwidth (for multiplexing)………………… 1-12GHz
- Kick-back avoidance

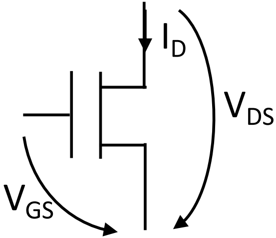
Designing for Cryogenic Operation

The Right Technology

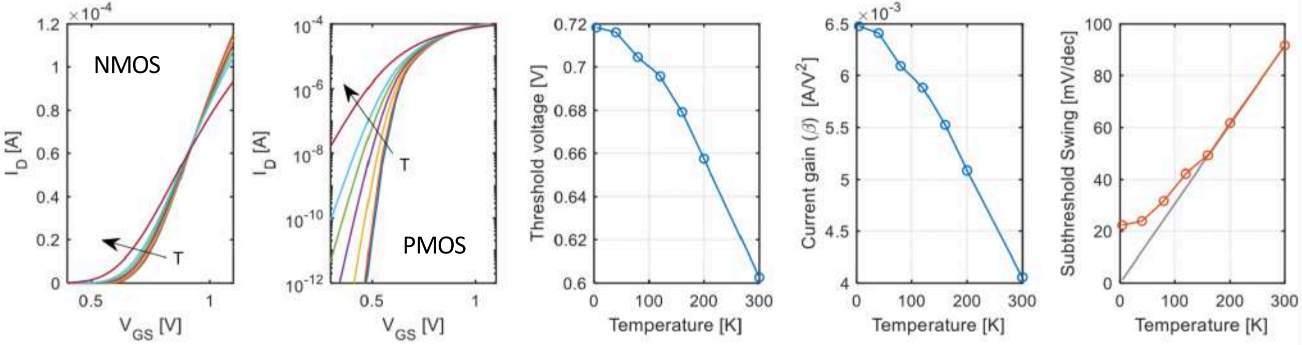
Device	Lowest useable temperature	Limit
Si BJT	100 K	Low gain
Ge BJT	20 K	Carrier freeze-out
SiGe HBT	4 K (or lower)	
Si JFET	40 K	Carrier freeze-out
III-V MESFET	4K (or lower)	Lower freeze-out?
CMOS (>160nm)	4 K	Non-idealities
CMOS (<40nm)	40 mK	Power dissipation

Most used

Extensive Modeling Campaign



- Mismatch increases
- Leakage drastically reduces
- Substrate become floating

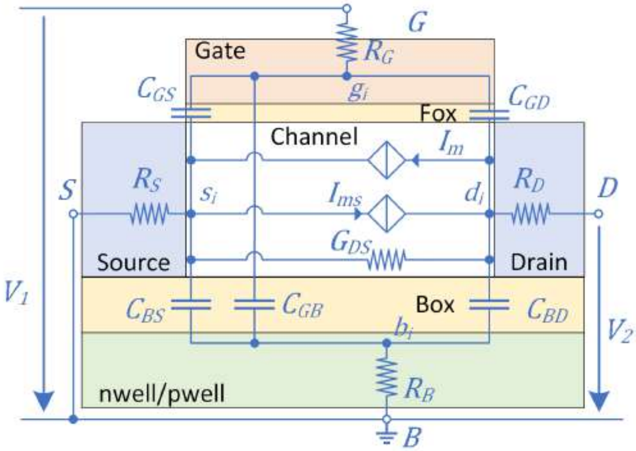


Fabio Sebastiano, Quantum Week, Oct. 12, 2020

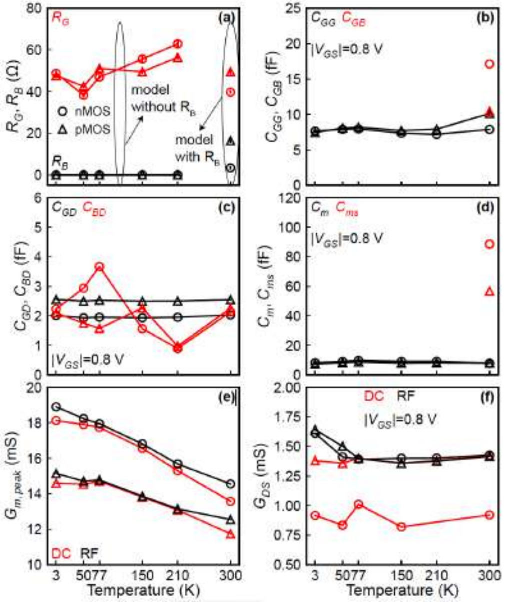
Extensive Modeling Campaigns (2)

- CMOS 0.16μm STMicroelectronics
- CMOS 40nm TSMC
- CMOS 28nm STMicroelectronics bulk/FDSOI
- CMOS 22nm FDSOI Global Foundries
- CMOS 16nm FinFET TSMC

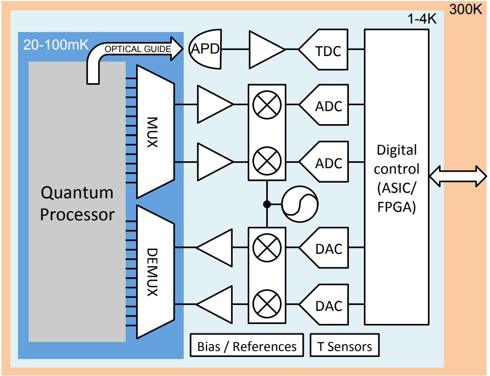
RF Modeling of CMOS 22nm FDSOI



H.C. Han et al., *ESSDERC* 2022



1. Digital Circuits
2. Radio-Frequency Circuits
   - Circulator
   - PLL
   - Mixer
   - Qubit readout
   - Qubit control



1. Digital Circuits

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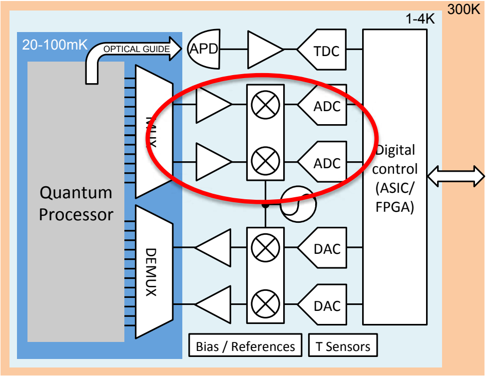
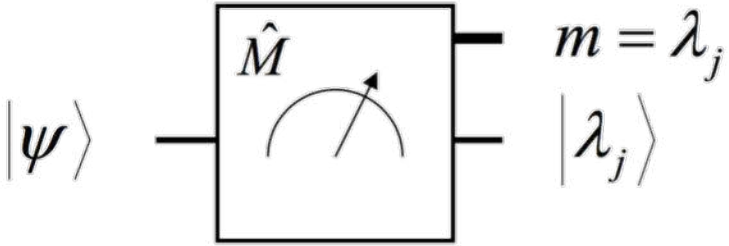


Qubit Readout: The Problem at Hand



The Design of QUADRO

- Target fidelity: 99.9%

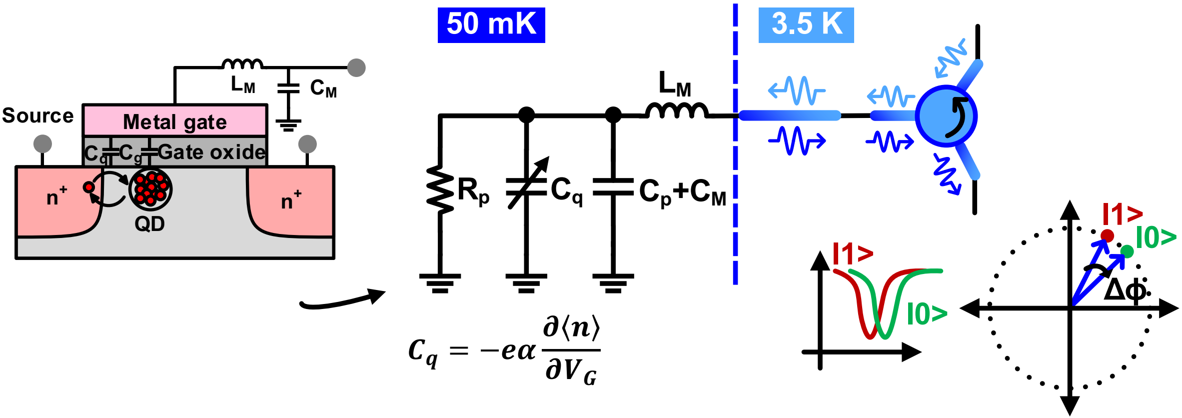
Jeroen V. Dijk, Thesis, 2021

	Value	Infidelity contribution to the read-out
Detuning energy		
nominal	83.2 mV (4.2 meV, 1.0 THz)	
error	0.24 mV (12 µeV, 2.8 GHz)	167×10^{-6}
	$\sigma = 0.24\,\mathrm{mV_{rms}}$	
	PSD = 0.24 µV/√Hz	
Tunnel coupling		
nominal	39 MHz (0.16 µeV)	167×10^{-6}
		$P_{\mathrm{charge}} = 99.967\,\%$

	Value	Infidelity contribution to the read-out
Charge sensor		333×10^{-6}
		$P_{\mathrm{sense}} = 99.967\,\%$

	Value	Infidelity contribution to the read-out
Quantum Point Contact		
signal	400 pA	
noise	$53\,\mathrm{pA_{rms}}$, PSD = 57 fA/√Hz	222×10^{-6}
Readout Circuit		
input-referred noise	$26\,\mathrm{pA_{rms}}$, PSD = 28 fA/√Hz	111×10^{-6}
		$P_{\mathrm{detect}} = 99.967\,\%$
$P_{\mathrm{charge}} \cdot P_{\mathrm{sense}} \cdot P_{\mathrm{detect}}$		$F = 99.9\,\%$

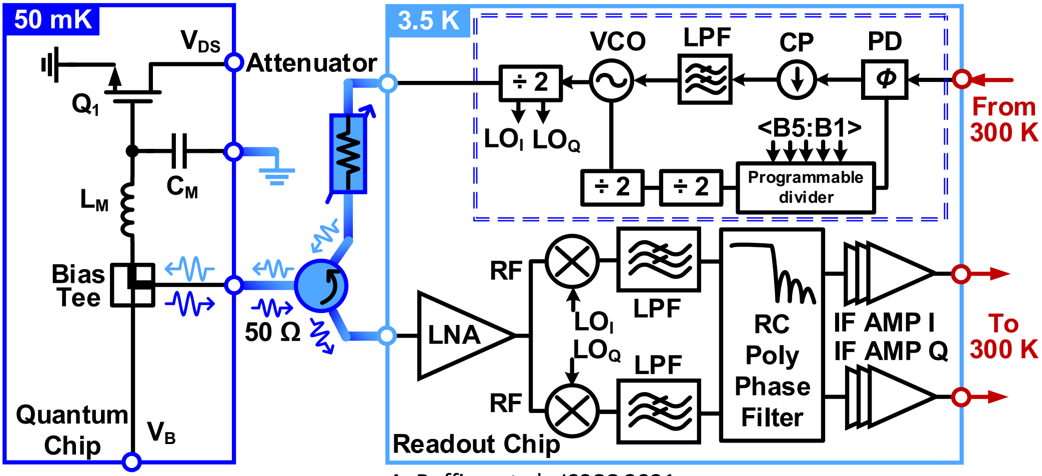
Readout Approach: Quantum Dot Reflectometry



$$C_q = -e\alpha \frac{\partial \langle n \rangle}{\partial V_G}$$

- A probing signal is coupled to an LC resonator.
- Depending on the state of the quantum dot (or qubit in general), additional quantum capacitance C_q causes a phase shift.
- This results in APSK modulation, to be read out.

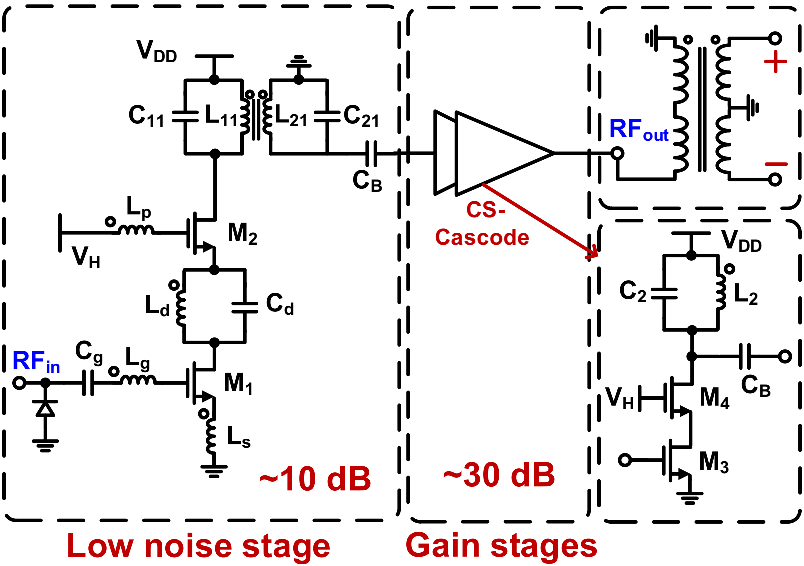
Initial Architecture



A. Ruffino et al., ISSCC 2021
Y. Peng et al., JSSC 2022

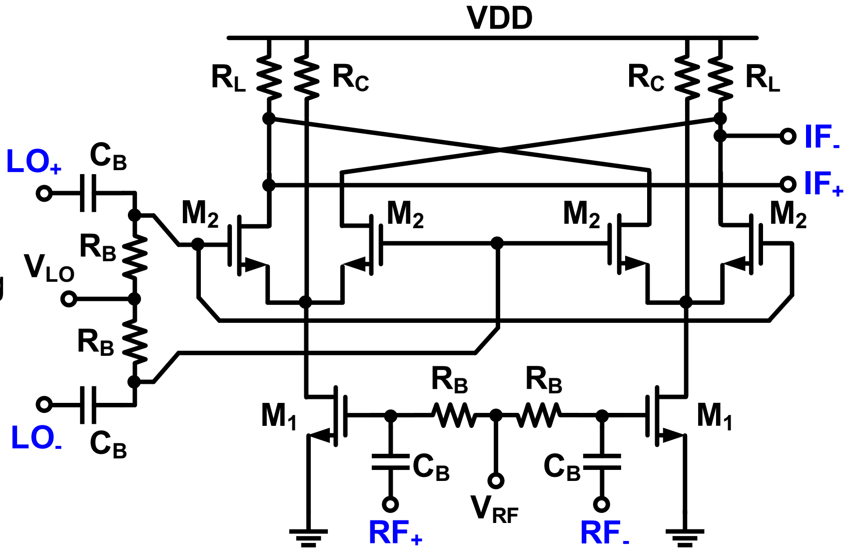
Low-Noise Amplifier

- Single-ended inductively degenerated common source LNA
- LC tank load for optimal noise impedance
- Transformer-coupled cascaded gain stages
- 40 dB gain
- 4.5 GHz - 8.5 GHz bandwidth



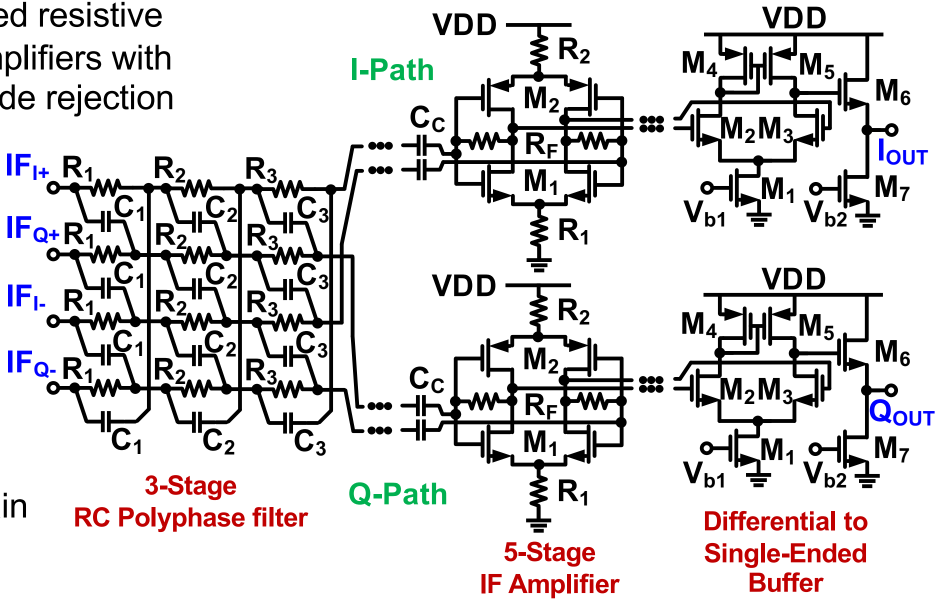
Mixer

- Single quadrature I/Q differential mixer for single-sideband (SSB) down-conversion
- Gilbert cell active mixer
- Resistor current bleeding for increased voltage headroom at low temperature
- 0.1-1.5 GHz IF with 4.9 GHz-6.5 GHz RF



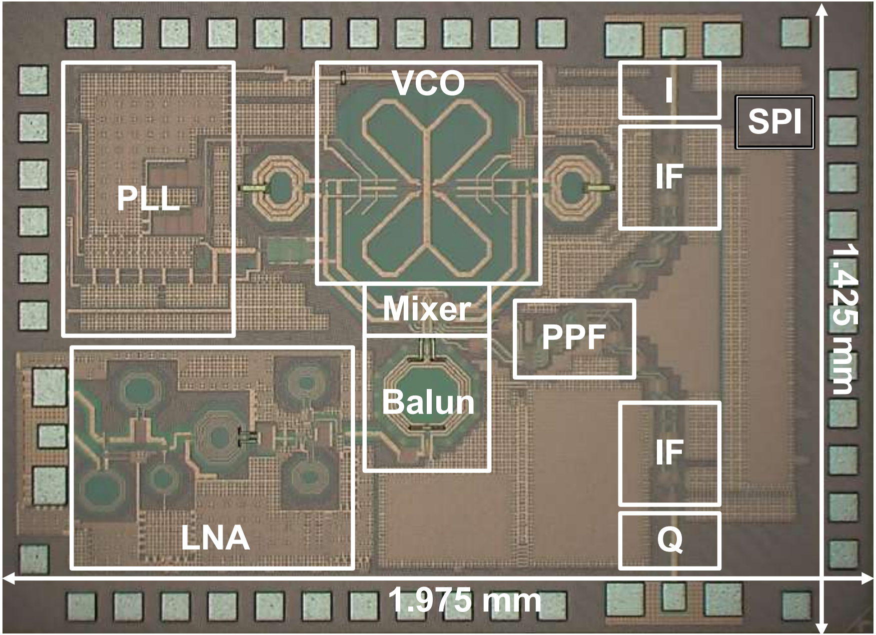
IF Chain

- Inverter-based resistive feedback amplifiers with common-mode rejection



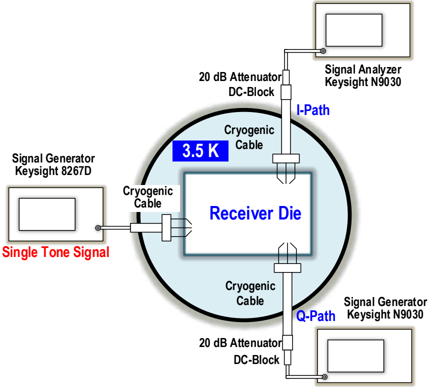
- 20-dB IRR
- I/Q 30-dB gain

The QUADRO Chip

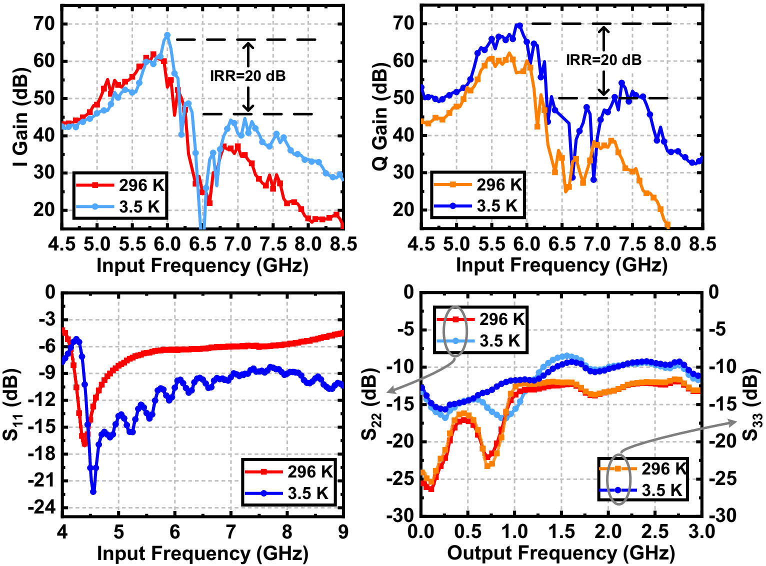


A. Ruffino et al., ISSCC 2021 – Y. Peng et al., JSSC 2022

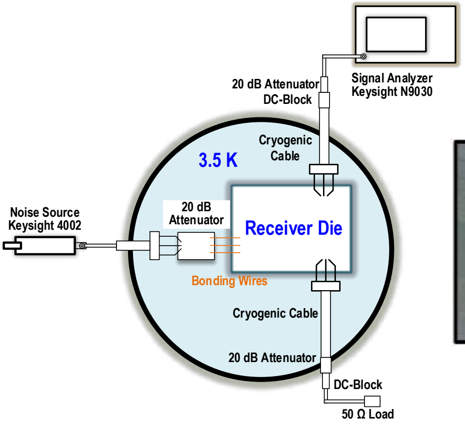
Measurement Setup

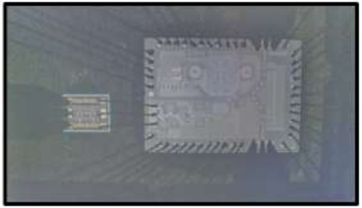


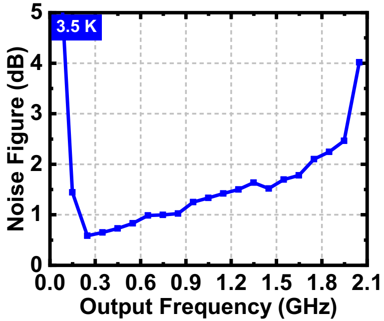
- 70-dB maximum conversion gain
- 1.4 GHz bandwidth
- Average 20-dB image-rejection ratio
- Better than -10 dB input and output match



LNA Noise Figure



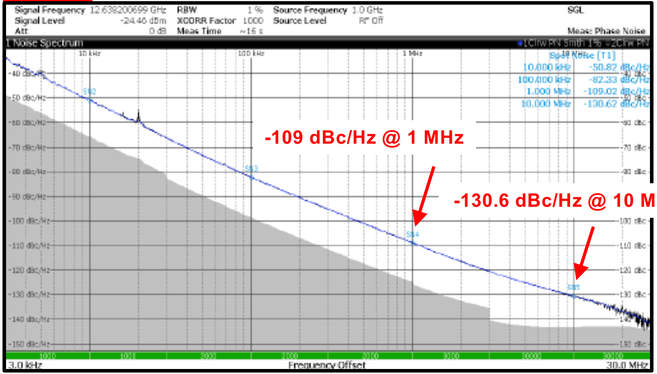




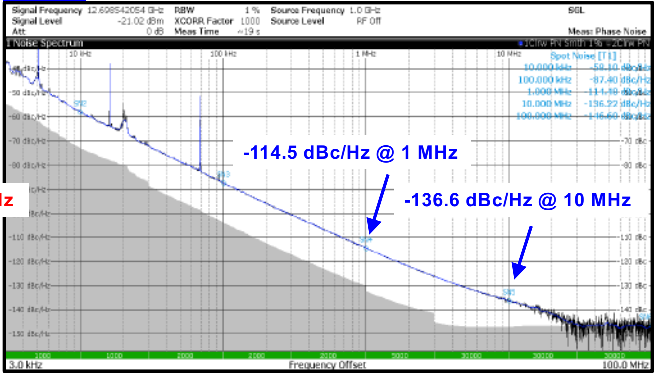
- Cold attenuator scalar SSB NF measurements
- 0.55 dB minimum noise figure
- Degradation at low and high frequency due to insufficient PPF image noise rejection
- Additional cryogenic LNA might be required for direct qubit readout

VCO Phase Noise

296 K

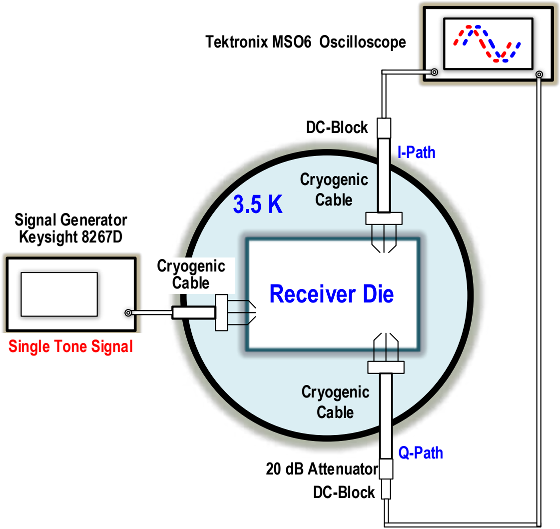


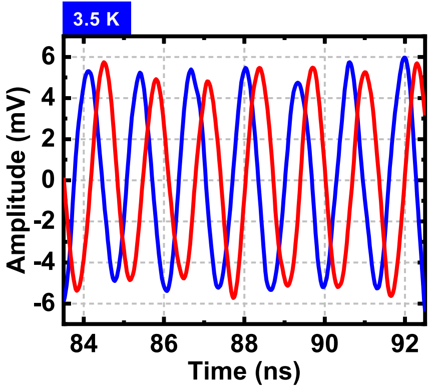
3.5 K



A. Ruffino et al., ISSCC 2021
Y. Peng et al., JSSC 2022

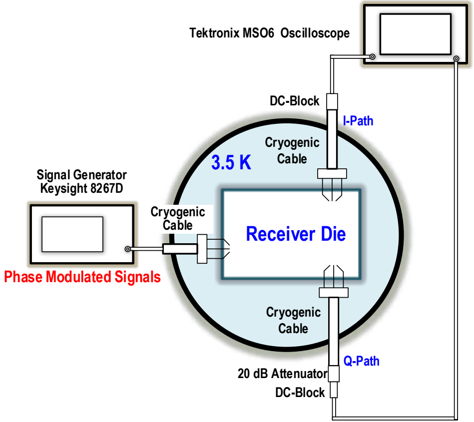
Time-Domain I/Q Measurements

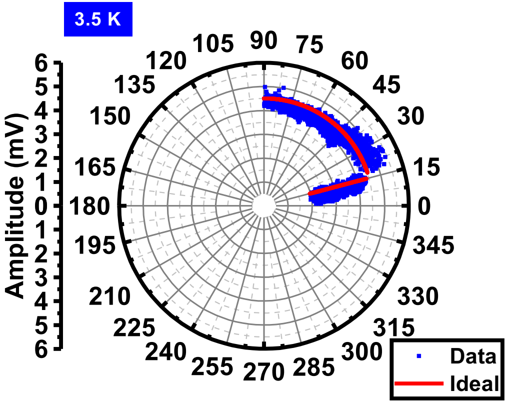




- Real-time I/Q output waveforms acquired at 3.5 K show 6° phase imbalance at center band (680 MHz IF frequency)

Polar Constellation Diagram

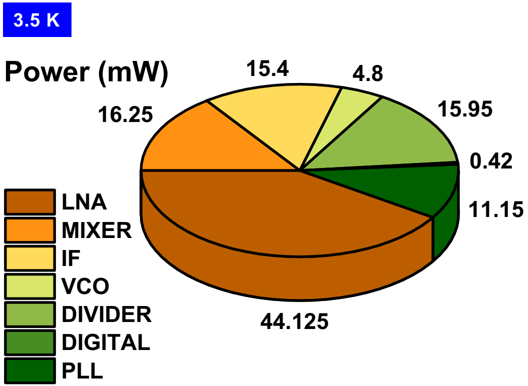




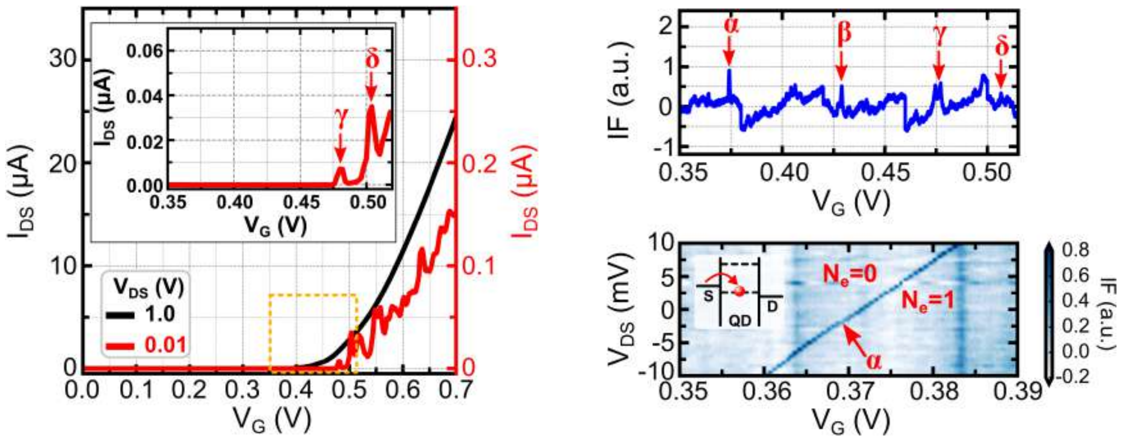
- A linear AM and PM signal is sent at the receiver input with a vector signal generator
- The downconverted I/Q output waveforms are sampled by an oscilloscope and baseband signals are reconstructed off-chip
- The I/Q receiver tracks the input signal in the polar constellation plot

Power Dissipation

- The chip consumes 108 mW at 3.5 K
- With 1.4 GHz bandwidth, considering 10 MHz qubit bandwidth and 10 MHz spacing, one can read 70 qubits with 1.5 mW/qubit



RF Reflectometry of QDs

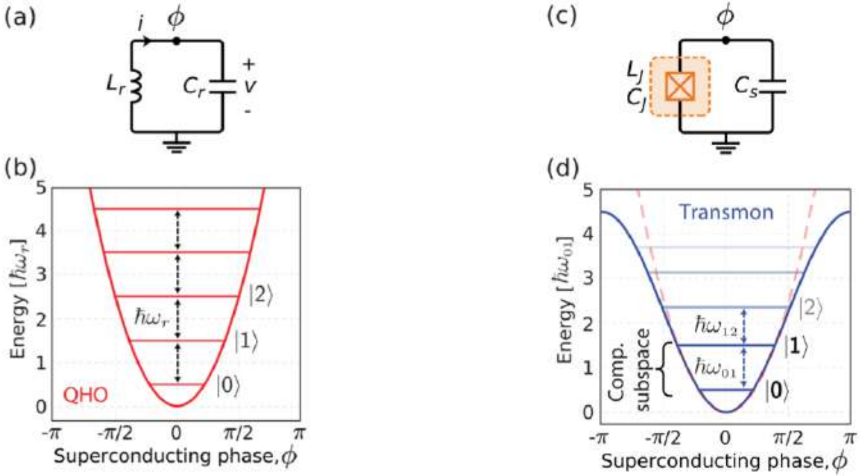


- At 50 mK, the 40-nm CMOS quantum dots show regular Coulomb oscillations in DC, which can also be resolved in RF reflectometry.

Superconducting Qubit Design

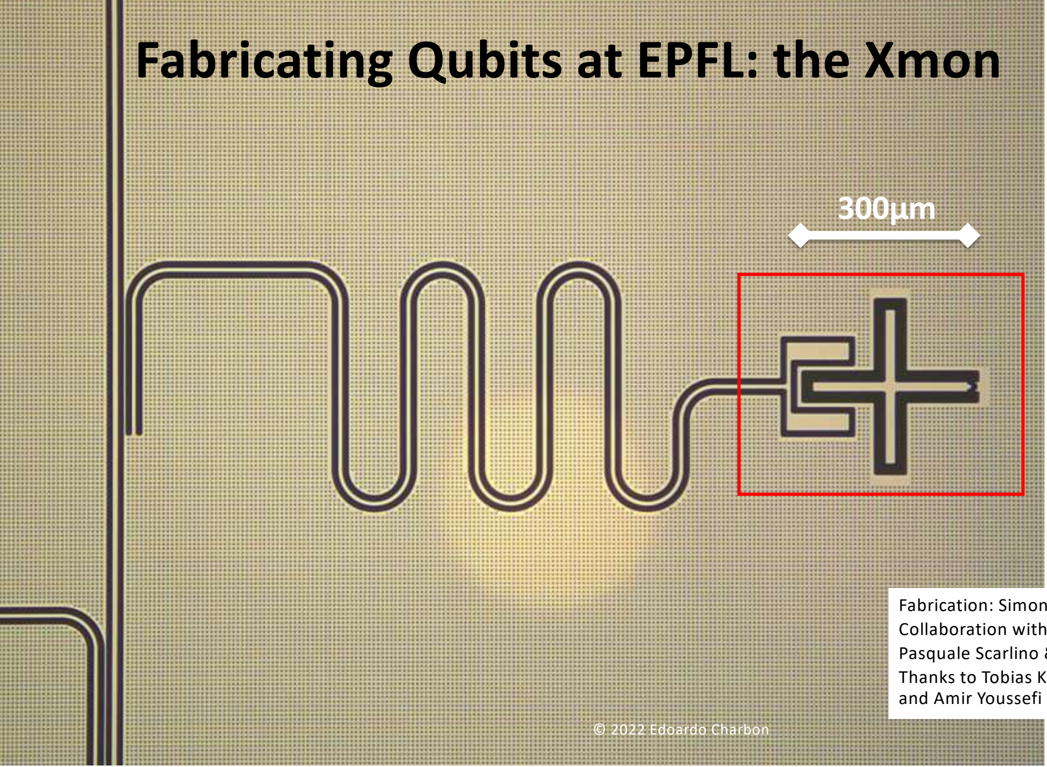
Anatomy of a SC Qubit (Transmon)

- Similar to a LC tank with a non-linear load (a double Josephson junction)



P. Krantz et al., A quantum engineer's guide to superconducting qubits, Appl. Phys. Rev. 6, 021318 (2019)

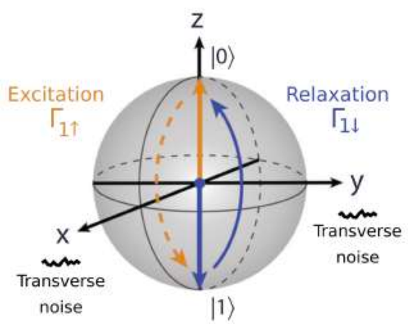
Fabricating Qubits at EPFL: the Xmon



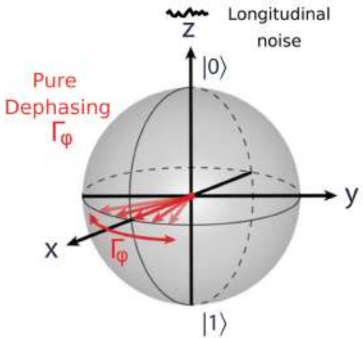
Fabrication: Simone Frasca
Collaboration with HQC Lab
Pasquale Scarlino & Marco Scigliuzzo
Thanks to Tobias Kippenberg, Shingo Kono and Amir Youssefi

Characterization of the Xmon

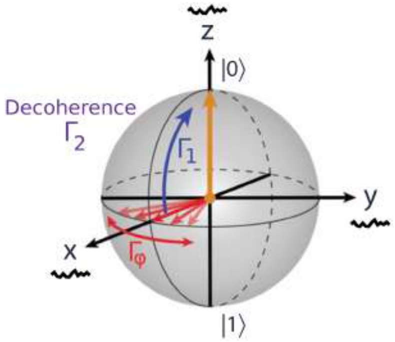
Relaxation Time = T_1



Dephasing Time = T_φ

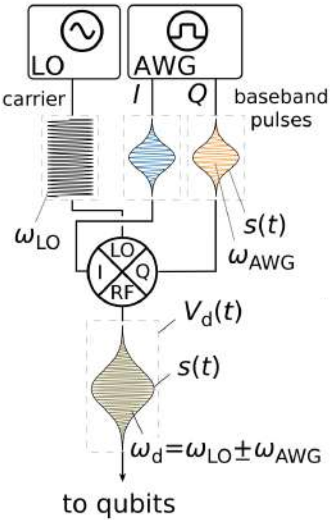


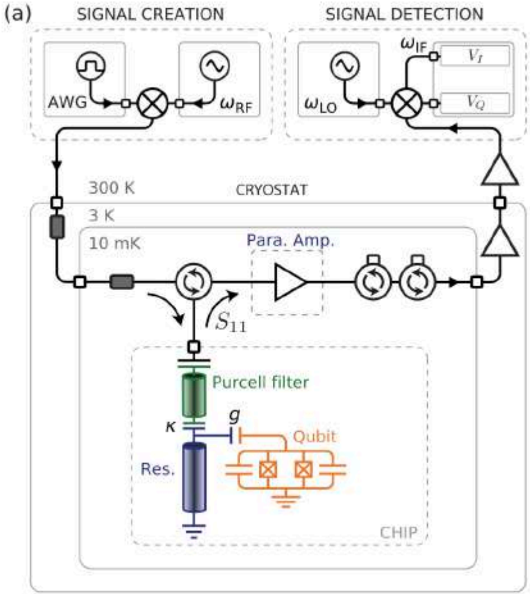
Decoherence Time = T_2



P. Krantz et al., A quantum engineer's guide to superconducting qubits, Appl. Phys. Rev. 6, 021318 (2019)

Characterization of the Xmon (2)

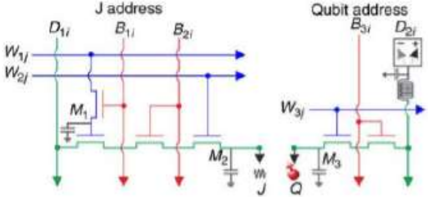


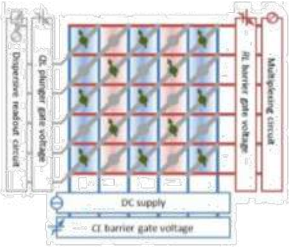


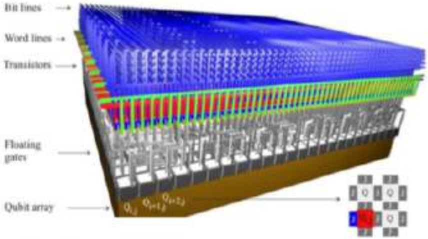
P. Krantz et al., A quantum engineer's guide to superconducting qubits, Appl. Phys. Rev. 6, 021318 (2019)

Trends

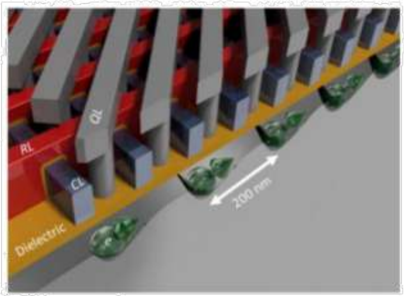
Proposals for Scalable Fault-Tolerant 2D Qubit Arrangements







M. Veldhorst *et al.* (UNSW),
***Nature Comm.* (2017)**

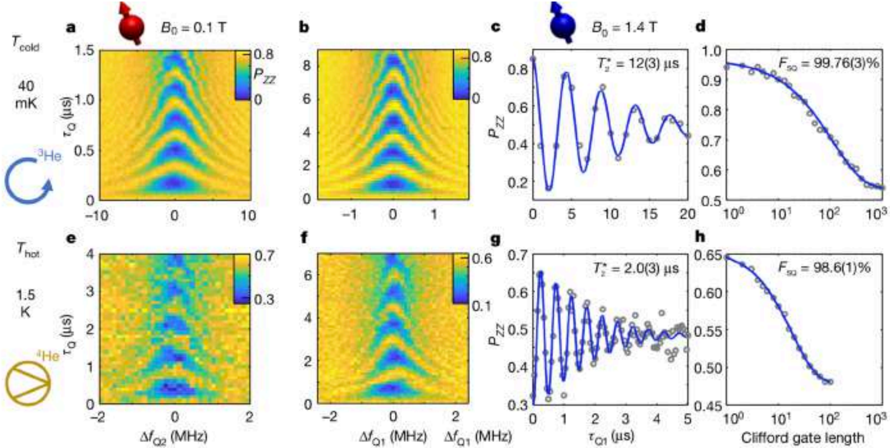


R. Li et al., arXiv 1711.03807 (2017)

Operation of a silicon quantum processor unit cell above one kelvin

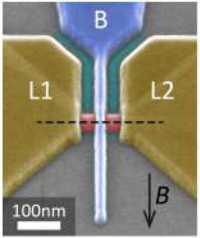
C. H. Yang[1✉], R. C. C. Leon[1], J. C. C. Hwang[1,6], A. Saraiva[1], T. Tanttu[1], W. Huang[1], J. Camirand Lemyre[2], K. W. Chan[1], K. Y. Tan[3,7], F. E. Hudson[1], K. M. Itoh[4], A. Morello[1], M. Pioro-Ladrière[2,5], A. Laucht[1] & A. S. Dzurak[1✉]

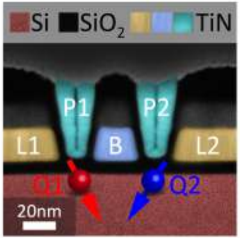
Nature 580, 2020
Courtesy: A. Dzurak



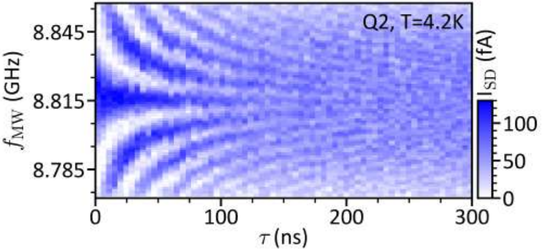
Silicon Quantum Dot Devices with a Self-aligned Second Gate Layer

Quantum dot hole spin qubit integrated in a bulk-Si FinFET

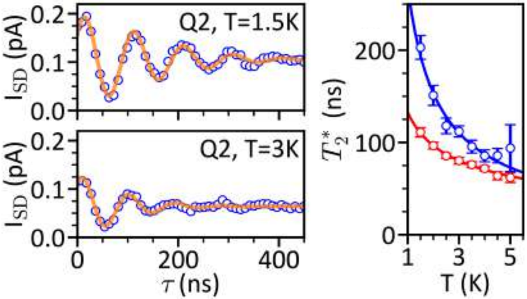




Ramsey fringes



Coherence



L.C. Camenzind et al., arXiv:2103.07369v1 (2021)

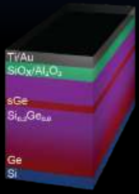
Courtesy: A. Kuhlmann

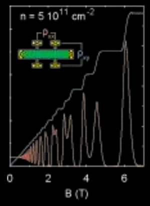
Courtesy: G. Scappucci

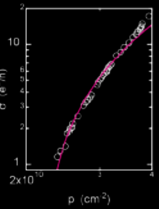
The germanium quantum information route

Scappucci group: materials ⟷ Veldhorst group: qubits

Strained Ge/SiGe on a Si wafer

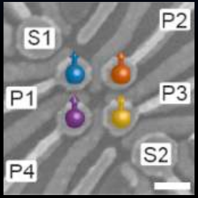




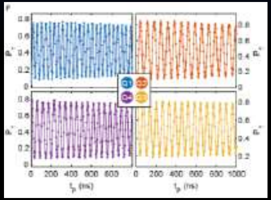


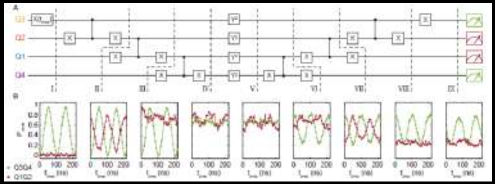
High mobility, low percolation density

Four-qubit germanium quantum processor



100 nm



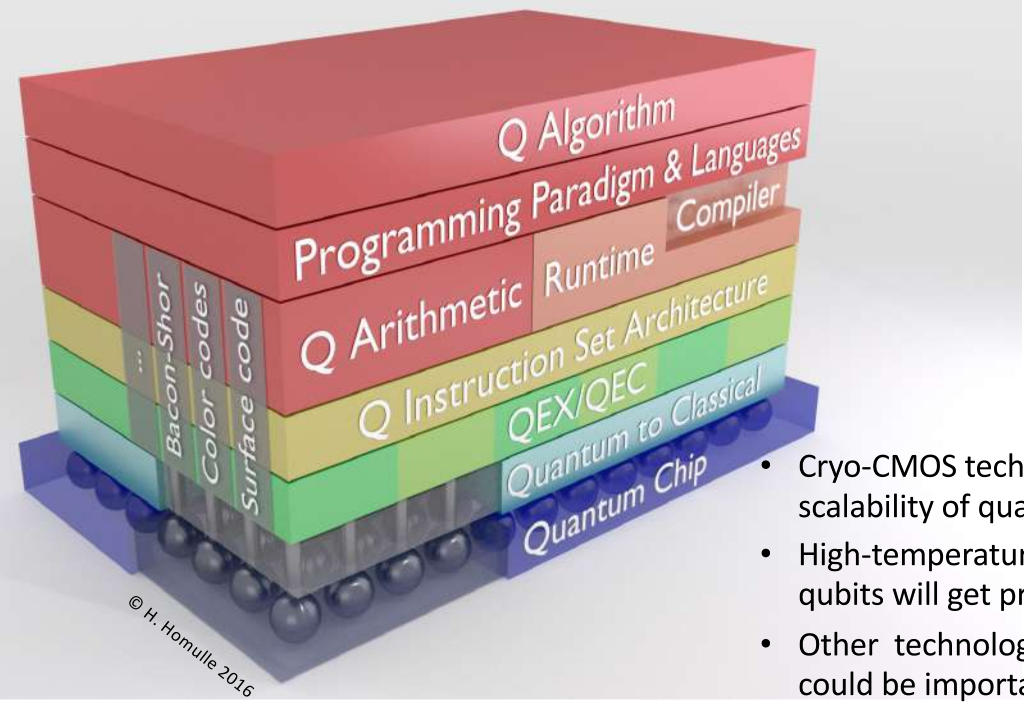


2x2 spin-qubit array 1,2,3,4 qubit gates

Coherent entanglement of 4-qubit state

Hendrickx et al. Nat. Comm (2018)
A. Sammak et al. Adv. Fun. Mat. (2019)
Hendrickx et al. PRB (2019)
Lodari et al. PRB (r) (2019)
Lawrie et al. APL (2020)
Lawrie et al. Nano Letters (2020)
Hendrickx et al. Nat. Comm (2020)
Hendrickx et al. Nature (2020)
Lodari et al. PRB (2020)
Lodari et al. ArxiV (2020)
G. Scappucci et al. ArXiv.(2020)
Van Riggelen et al. ArXiv (2020)
Hendrickx et al. ArXiv(2020)

QuTech
Creating the quantum future



Conclusions

- Cryo-CMOS technology is key to scalability of quantum computers
- High-temperature CMOS-compatible qubits will get prevalent
- Other technologies like 3D integration could be important enablers

Thank you http://aqua.epfl.ch

IceQubes 2019, 2021; next edition: 2023