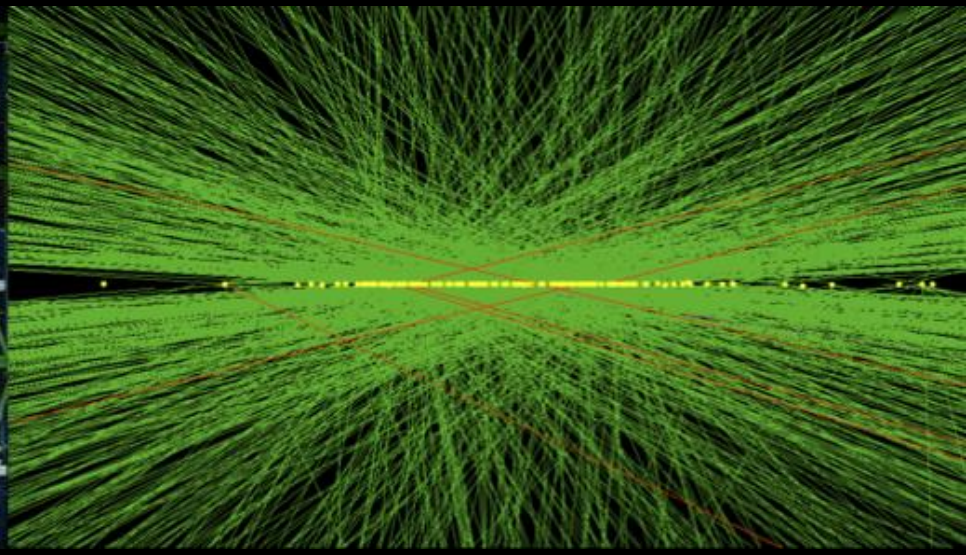

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Trigger Electronics & Data Acquisition

Sridhara Dasu

Original slides & graphics "stolen" from:
Wesley Smith, Sergio Cittolin, Tom Gorski, Ales Svetek,
Maria Cepeda, Sascha Savin, Varun Sharma, Piyush Kumar, Pallabi Das,
Isobel Ojalvo, Kevin Stenson, Phil Harris, …

The Scientific Process

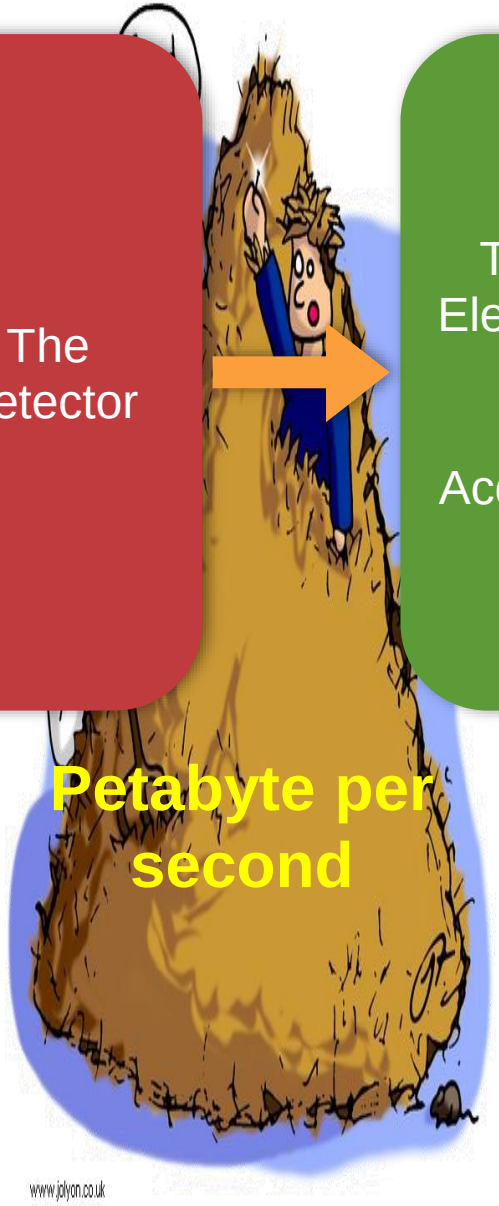
The Detector

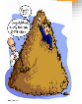
Trigger Electronics & Data Acquisition

Software & Computing

SCIENCE

Journal Publications



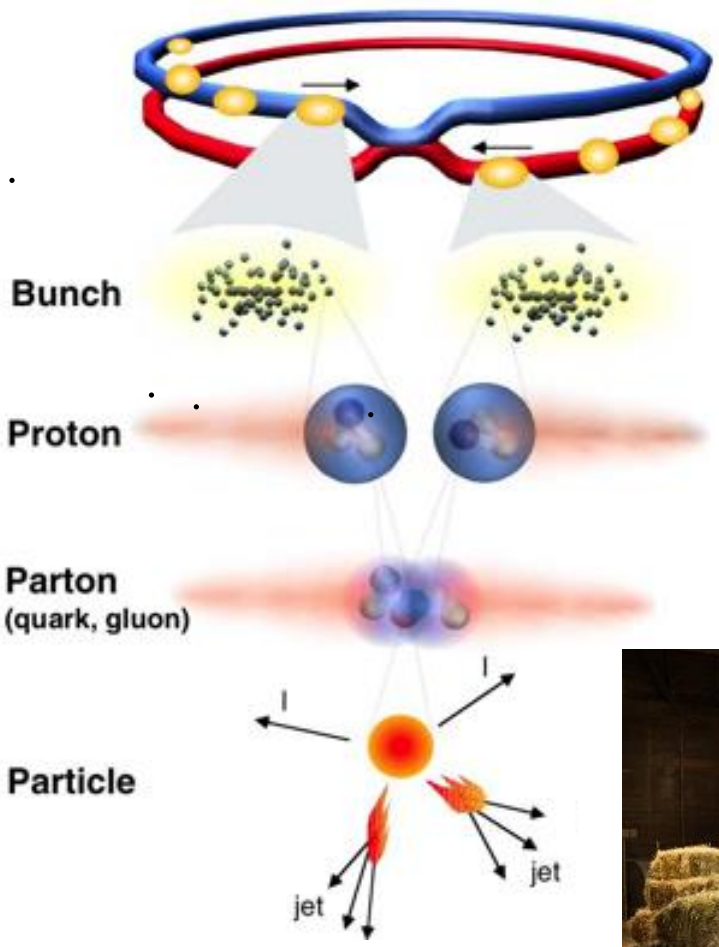


Petabytes get reduced to a social media post!

will.i.am @iamwill · Jul 4, 2012

Happy 4th of july to all americans...& happy "god particle" day to science enthusiast...congrats to all the scientist at cern...#willpower

Proton-Proton Collisions at the LHC



	Run-2	Run-1
Beam energy	6.5 TeV	4.0 TeV
Bunches/ beam	2556	1380
Protons/ bunch	2.5×10^{11}	2.2×10^{11}
N pp Collisions Created	$\sim 10^{16}$	3.5×10^{14}
N Higgs Events	$\sim 10^{4}$	~few 10^{2}

Fetch me my needle
buried in those
hay stacks –
And, do it
As Soon As Possible

1 event in 10 000 000 000 000 !

LHC Physics & Event Rates

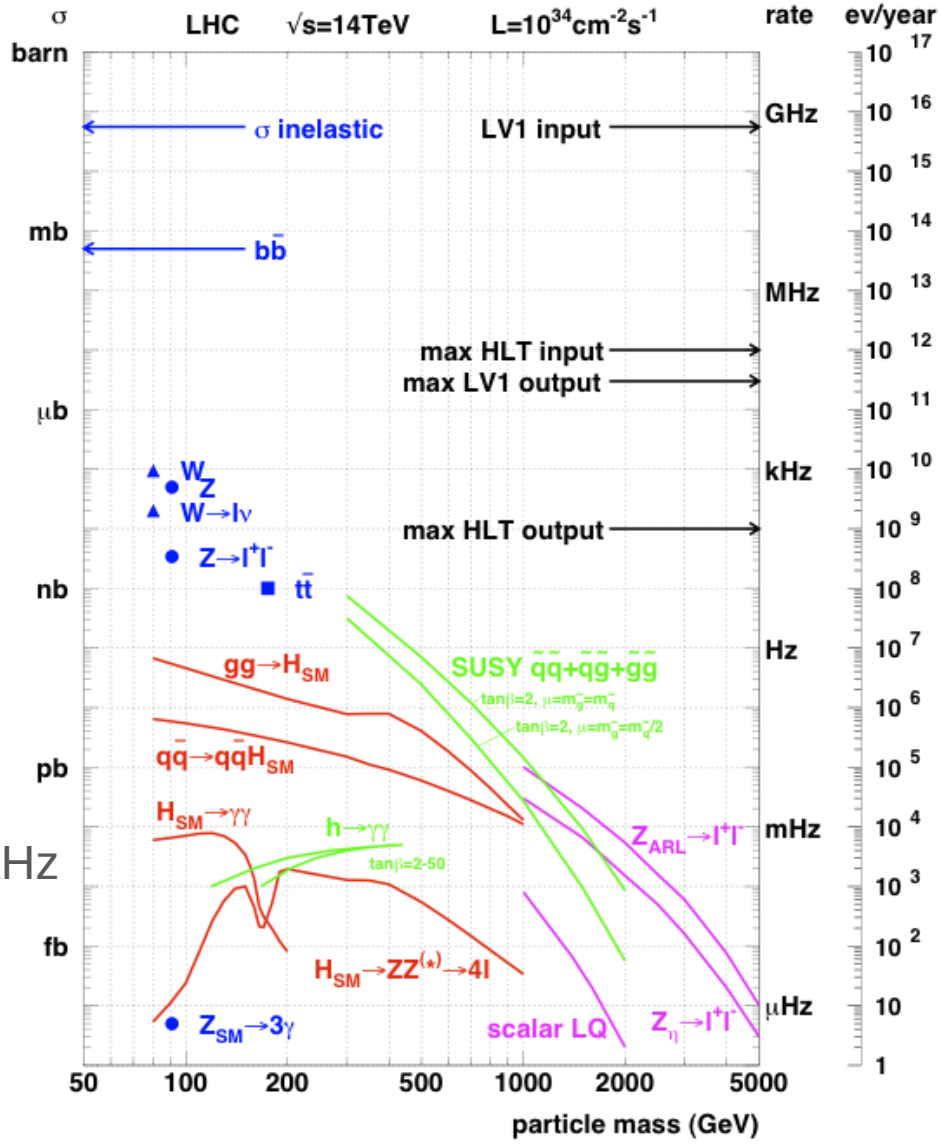
$L = 2 \times 10^{34} cm^{-2} s^{-1}$

- 50 pp events/25 ns crossing
  - ~ 1 GHz input rate
  - "Good" events contain ~ 50 background overlap
- 1 kHz W events
- 10 Hz top events
- < 10^4 detectable Higgs/year

Can store ~ 1000 Hz events

Select in stages

- Level-1 Triggers
  - 1 GHz (pp-interactions) to 100 kHz
- High Level Triggers
  - 100 kHz to 1000 Hz



(HL) LHC Physics – Trigger Challenge

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Electroweak Symmetry Breaking Scale

- **Higgs (125 GeV) studies and higgs sector characterization**
- **Quark, lepton Yukawa couplings to higgs**

Low ≅ 30 GeV

Low P_T γ, e, μ

Low P_T B, τ jets

New physics at TeV scale to stabilize higgs sector

- **Spectroscopy of new EWK produced resonances (SUSY or otherwise)**
- **Find dark matter candidate**

Multiple low P_T objects

Missing E_T

Multi-TeV scale physics (loop effects)

- **Indirect effects on flavor physics (mixing, FCNC, etc.)**
  - B_s mixing and rare B decays
- **Lepton flavor violation**
  - Rare Z and higgs decays

~ Dedicated triggers (CMS) or experiment (LHCB)

Low P_T leptons

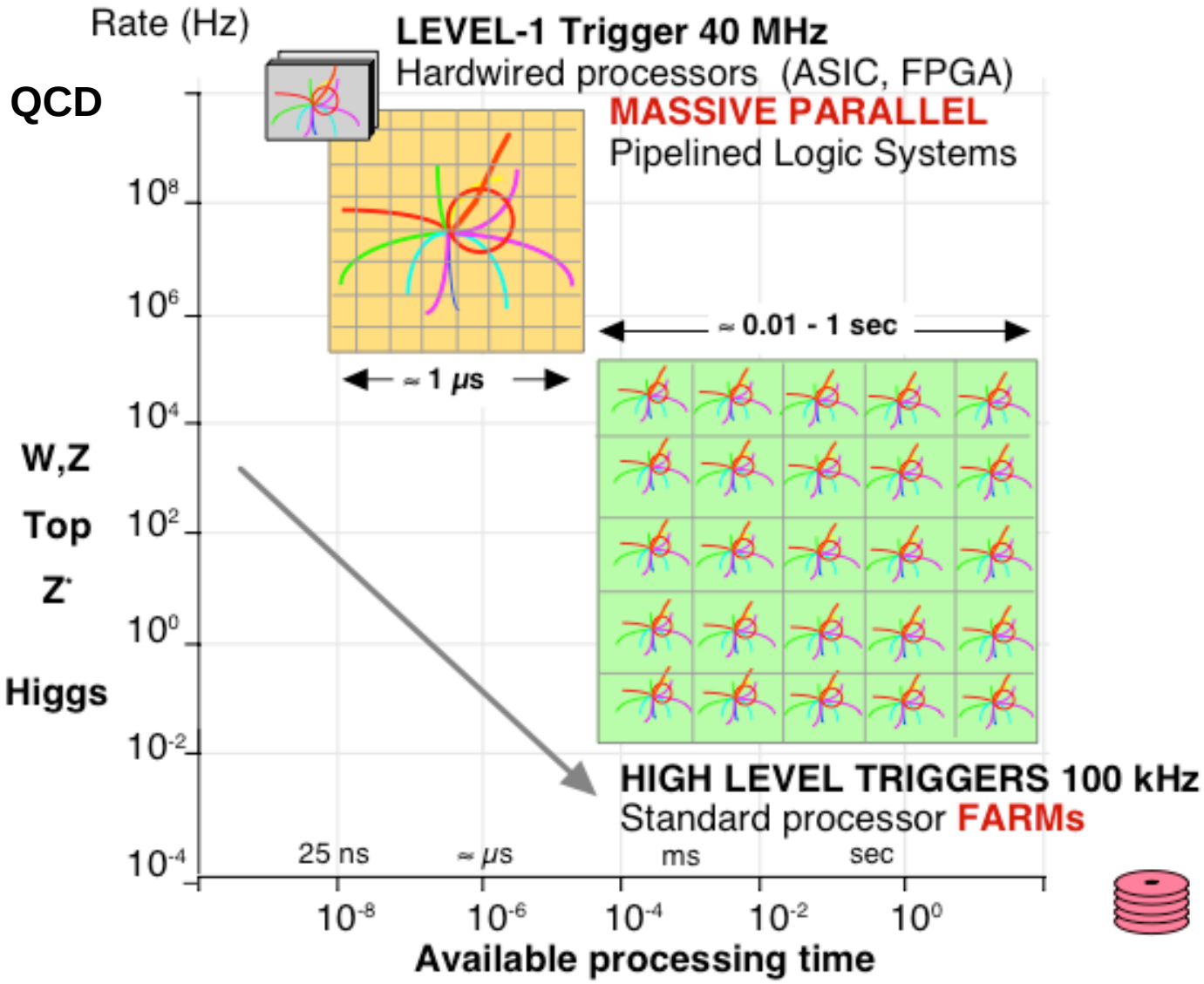
Planck scale physics

- **Large extra dimensions to bring it closer to experiment**
- **New heavy bosons**
- **Blackhole production**

High P_T leptons and photons

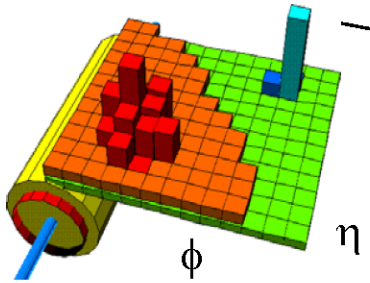
Multi particle and jet events

LHC Data Processing to Trigger



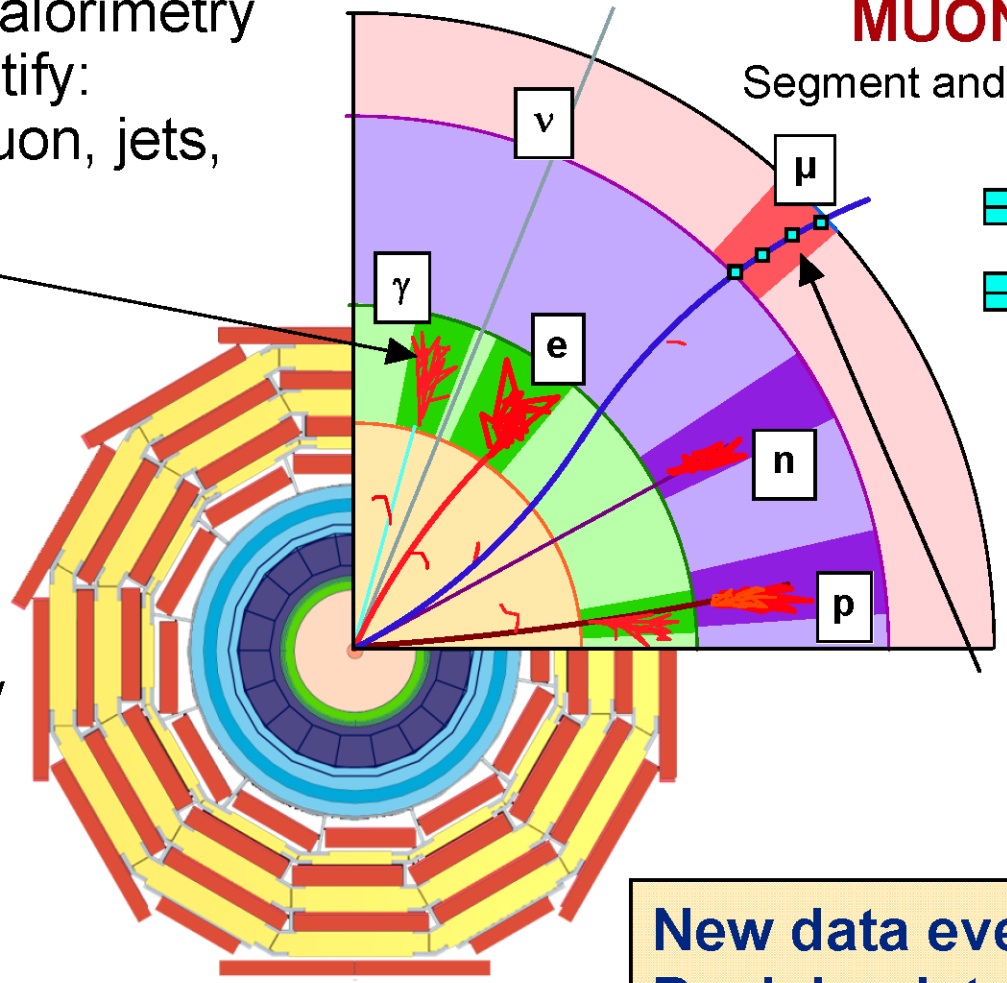
Level 1 Trigger Data

Use prompt data (calorimetry and muons) to identify:
High p_t electron, muon, jets, missing E_T



CALORIMETERs
Cluster finding and energy deposition evaluation

MUON System
Segment and track finding



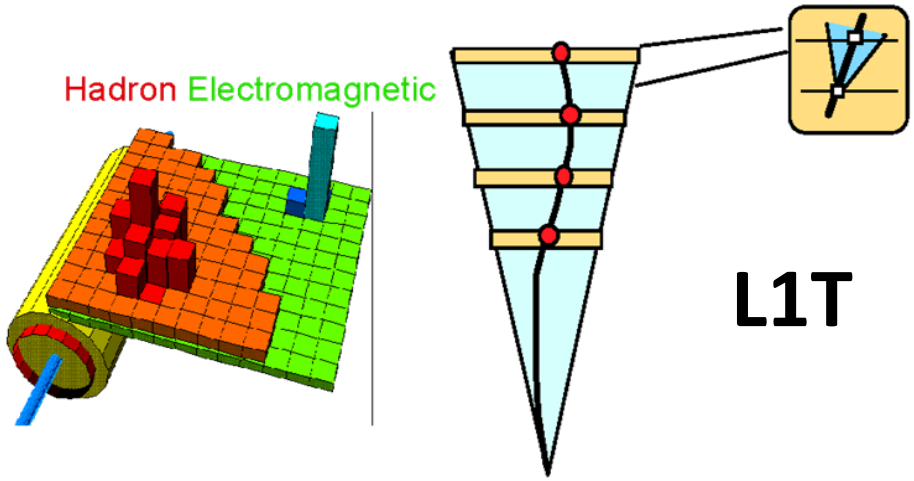
New data every 25 ns
Decision latency ~ μs

L1 @ LHC: Only Calorimeter & Muon

HLT@LHC: Key additional feature - Tracker

New tracker and level-1 track trigger envisioned for HL-LHC

- **Pattern recognition much faster/easier**

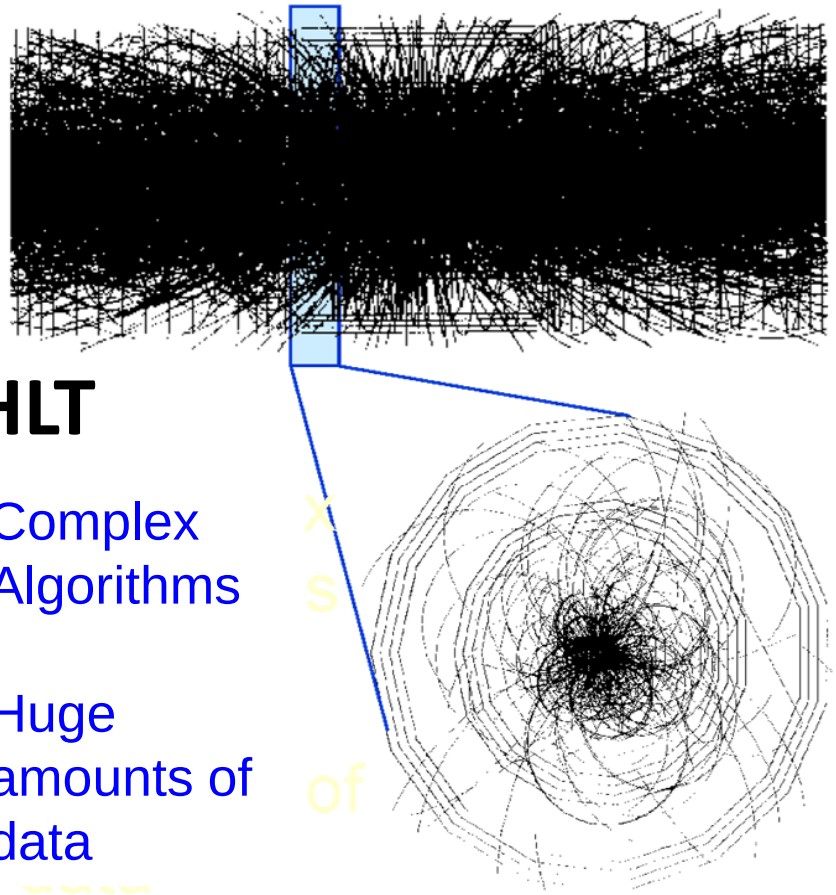


L1T

Simple Algorithms

Reduced amounts of data

- **Compare to tracker info**

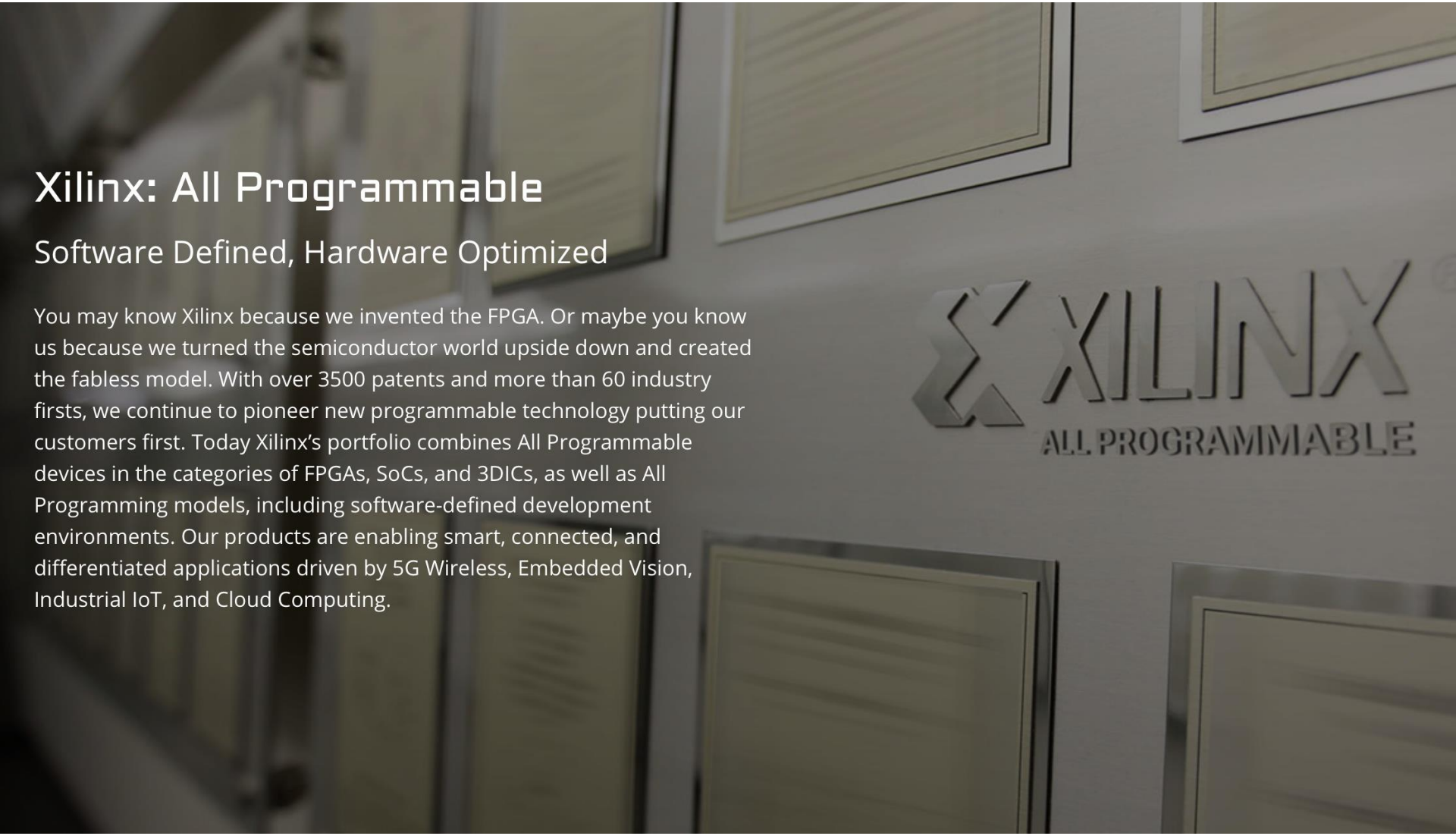


HLT

Complex Algorithms

Huge amounts of data

Xilinx Field Programmable Gate Arrays



Xilinx: All Programmable

Software Defined, Hardware Optimized

You may know Xilinx because we invented the FPGA. Or maybe you know us because we turned the semiconductor world upside down and created the fabless model. With over 3500 patents and more than 60 industry firsts, we continue to pioneer new programmable technology putting our customers first. Today Xilinx's portfolio combines All Programmable devices in the categories of FPGAs, SoCs, and 3DICs, as well as All Programming models, including software-defined development environments. Our products are enabling smart, connected, and differentiated applications driven by 5G Wireless, Embedded Vision, Industrial IoT, and Cloud Computing.

Xilinx FPGAs – Phase-1 Choice: V7 690T

Xilinx Multi-Node Product Portfolio Offering

Currently Deployed

HL-LHC Prototypes

45nm	28nm	20nm	16nm
SPARTAN-6	VIRTEX-7 KINTEX-7	VIRTEX UltraSCALE KINTEX UltraSCALE	VIRTEX UltraSCALE+ KINTEX UltraSCALE+

Cost-Optimized Portfolio

Spartan-7	Spartan-6
Artix-7	Zynq-7000

7 Series

Spartan-7	Artix-7
Kintex-7	Virtex-7

UltraScale

Kintex UltraScale	Virtex UltraScale

UltraScale+

Kintex UltraScale+	Virtex UltraScale+

	Spartan-7	Artix-7	Kintex-7	Virtex-7
Max Logic Cells (K)	102	215	478	1,955
Max Memory (Mb)	4.2	13	34	68
Max DSP Slices	160	740	1,920	3,600
Max Transceiver Speed (Gb/s)	--	6.6	12.5	28.05
Max I/O Pins	400	500	500	1,200

Key element - Multi-gigabit Opto-electronics

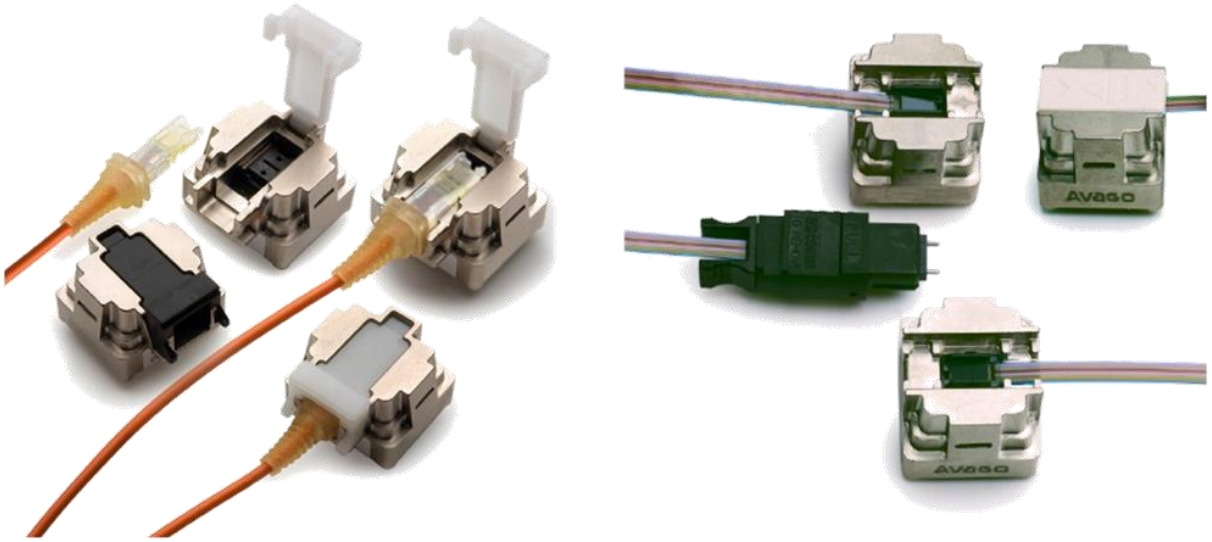


Figure 1. MiniPOD™ Transmitter and Receiver Modules with a) Round Cable and b) Flat Cable: shown with and without dust covers (White = Tx, Black = Rx).

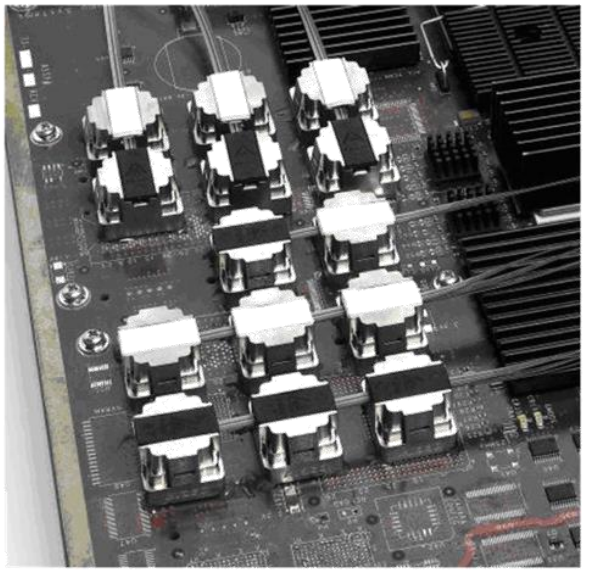


Figure 2. MiniPOD™ Transmitter and Receiver flat ribbon cable modules in a tiled arrangement example.

Key Product Parameters

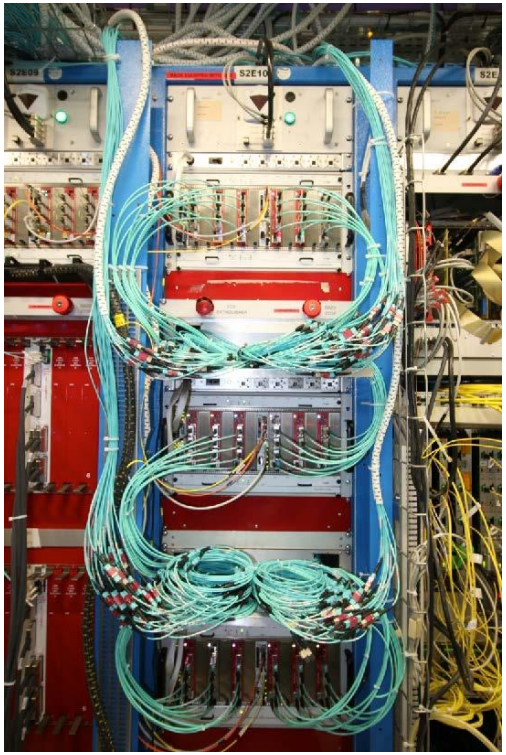
The Avago Technologies MiniPOD™ modules operate at 850 nm and are compliant to the Multi-mode Fiber optical specs in clause 86 and relevant electrical specs in annex 86A of the IEEE 802.3ba specifications.

Parameter	Value	Units	Notes
Data rate per lane	10.3125	Gbps	As per 802.3ba: 100GBASE-SR10 and nPPI specifications
Number of operational lanes	12		100GbE operation utilizes the middle ten lanes (Rx and Tx) of the 12 physically defined lanes
Link Length	100 150	m m	OM3, 2000 MHzMHz•km 50 µm MMF OM4, 4700 MHz•km 50 µm MMF

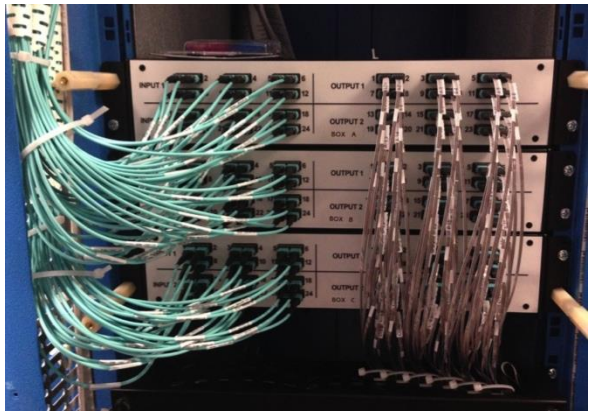
CMS Calorimeter Trigger Run-2

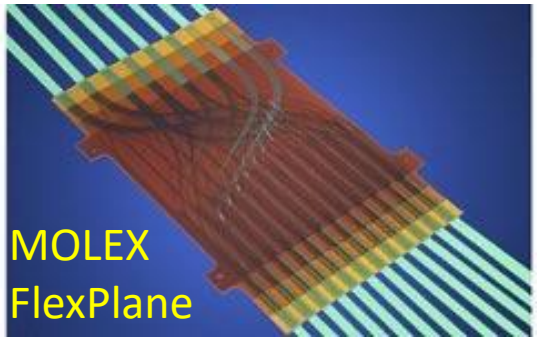
- Installed and commissioned in 2015, fully operational in 2016
  - Connections to CTP7 from Layer-1 patch panels completed in 2015
  - Connections from Layer-1 to Layer-2 via compact patch panel
    - 3 “pizza box” sized patch panels instead of full 56U rack with LC connectors
  - Layer 2 to demux to new μGT connected

Layer-1 CTP7

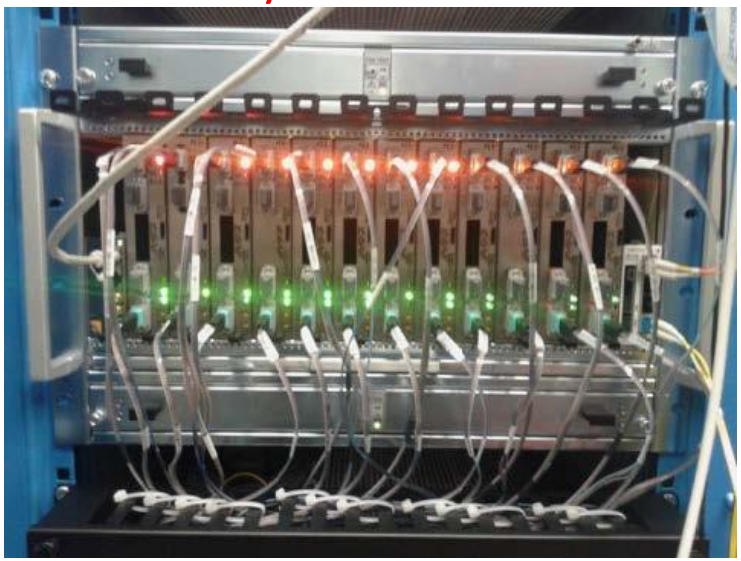


Layer-1 to Layer-2 Patch Panel

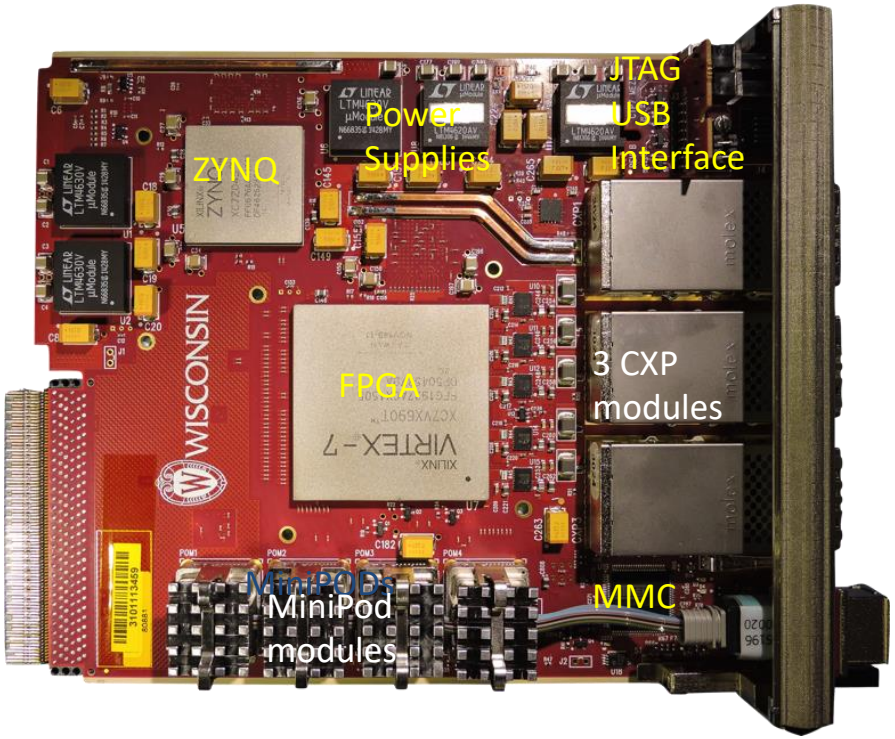


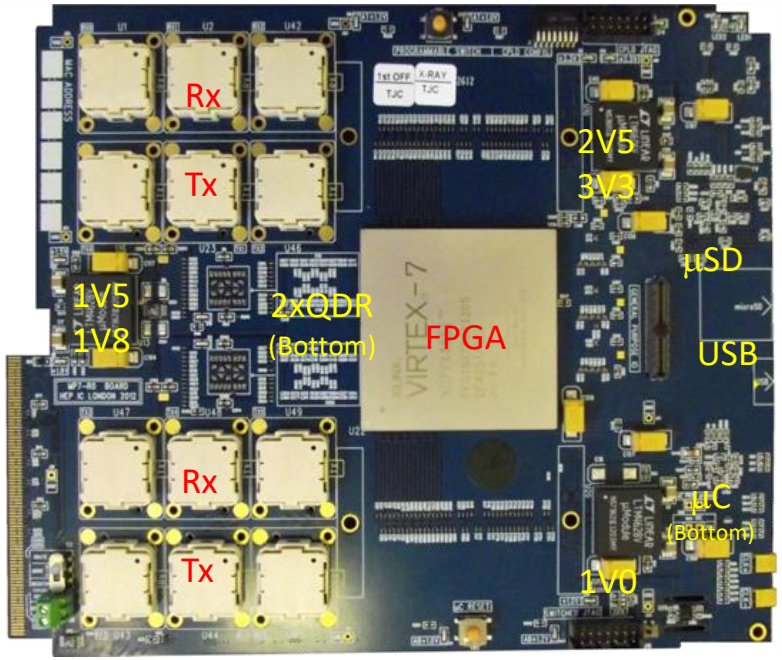


Layer-2 MP7



Level-1 Calorimeter Trigger Electronics



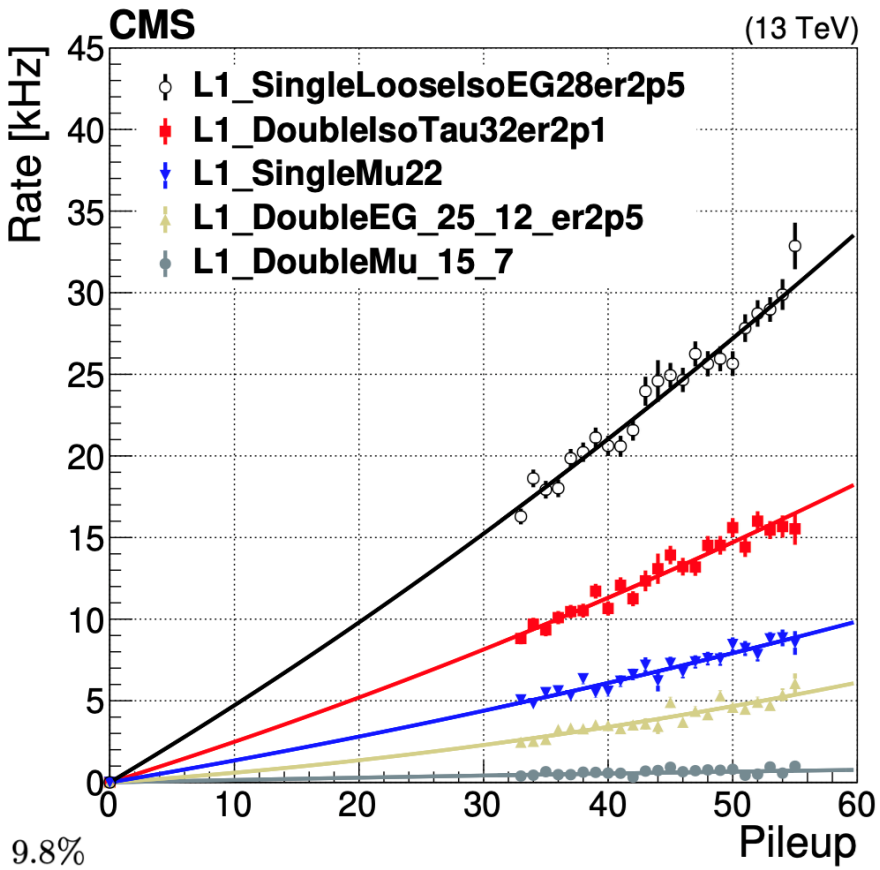


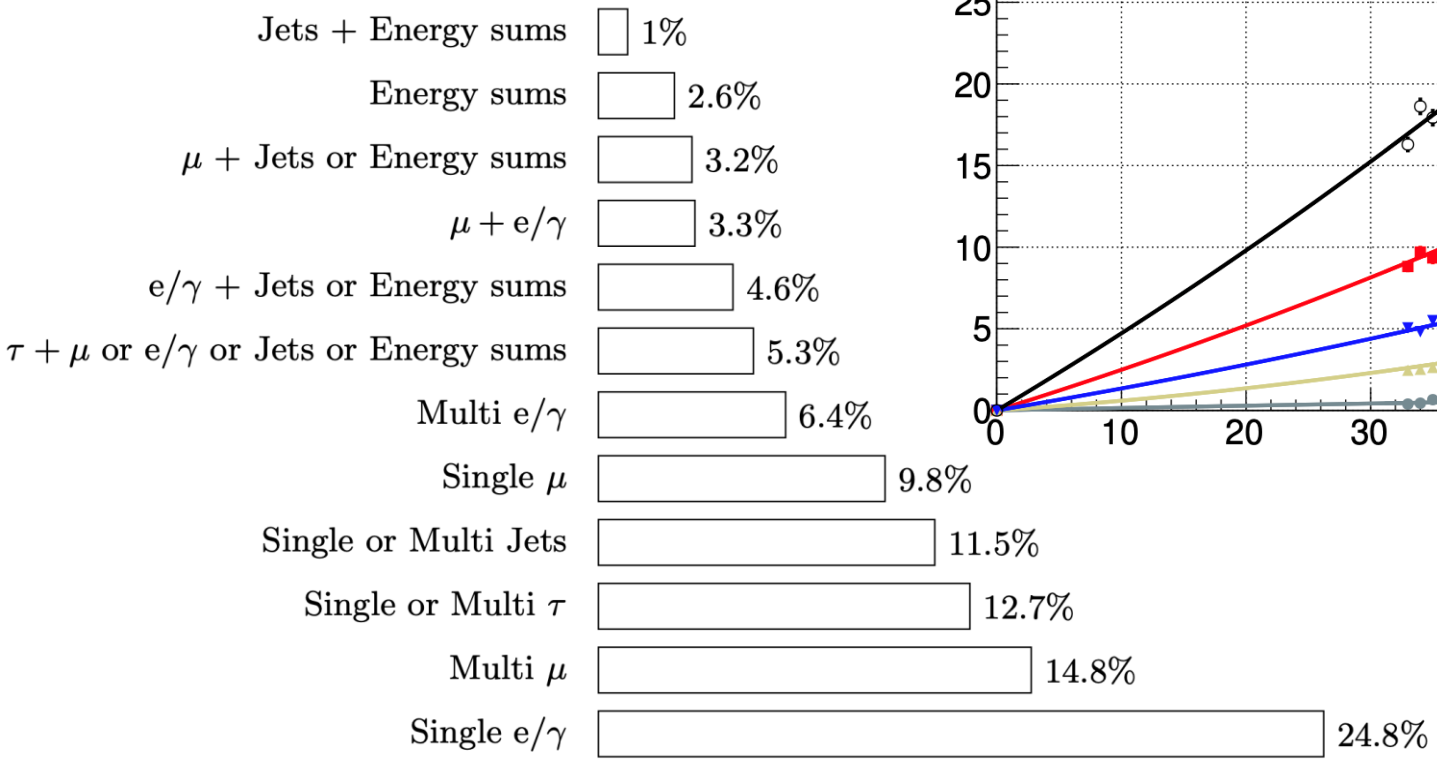
Calorimeter Trigger Processor(CTP7 – left), and Master Processor (MP7 - right)

- CTP7 (Layer-1) – µTCA Single Virtex 7 FPGA, 67 optical inputs, 48 outputs, 12 RX/TX backplane
  - Virtex 7 allows 10 Gb/s link speed on 3 CXP(36 TX & 36 RX) and 4 MiniPODs (31 RX & 12 TX)
  - ZYNQ processor running Xilinx PetaLinux for service tasks, including virtual JTAG cable
- MP7 (Layer-2) – µTCA Single Virtex 7 FPGA, up to 72 input & output links
  - Virtex 7 has 72 input and output links at 10 Gb/s
  - Dual 72 or 144MB QDR RAM clocked at 500 MHz

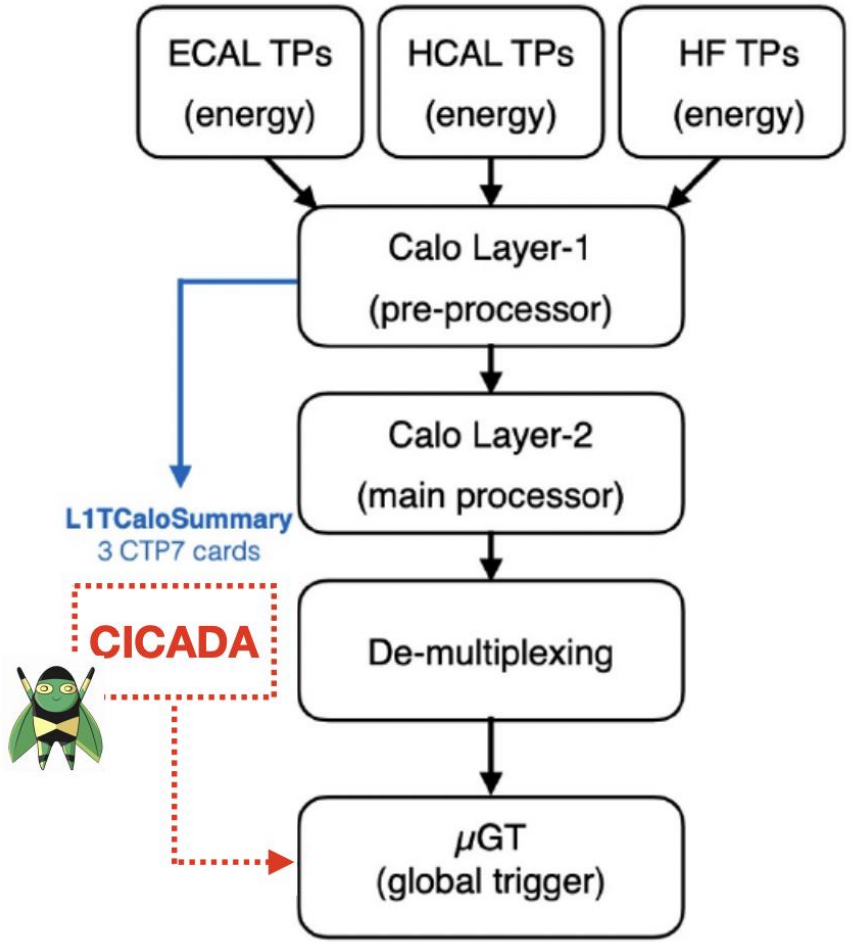
L1 Trigger Summary from Run-2,3

We capture the physics of interest within 100 kHz bandwidth, while discarding majority of 32 kHz of collisions

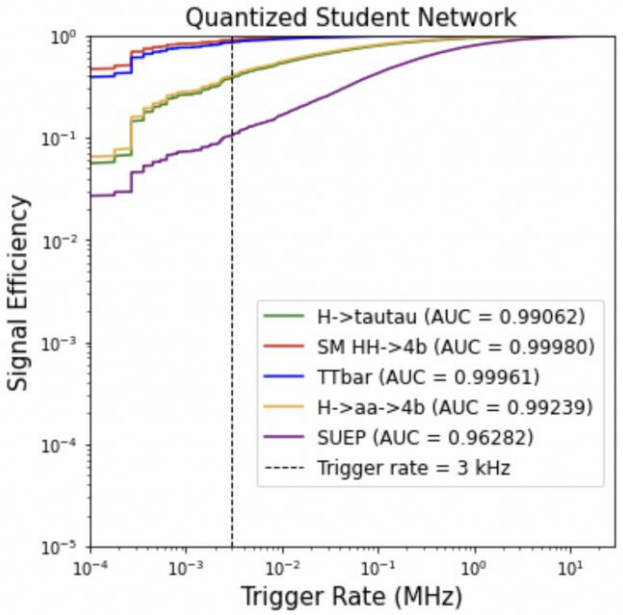




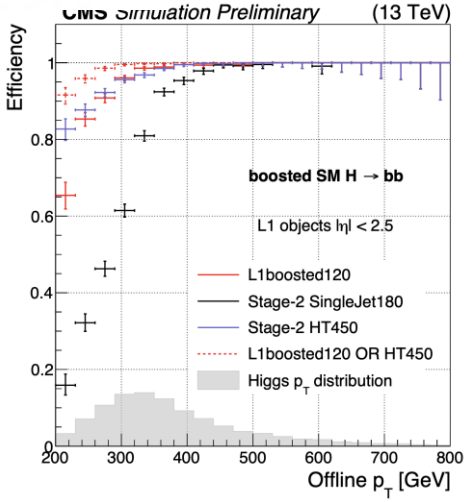
CICADA – Machine Learning in L1T



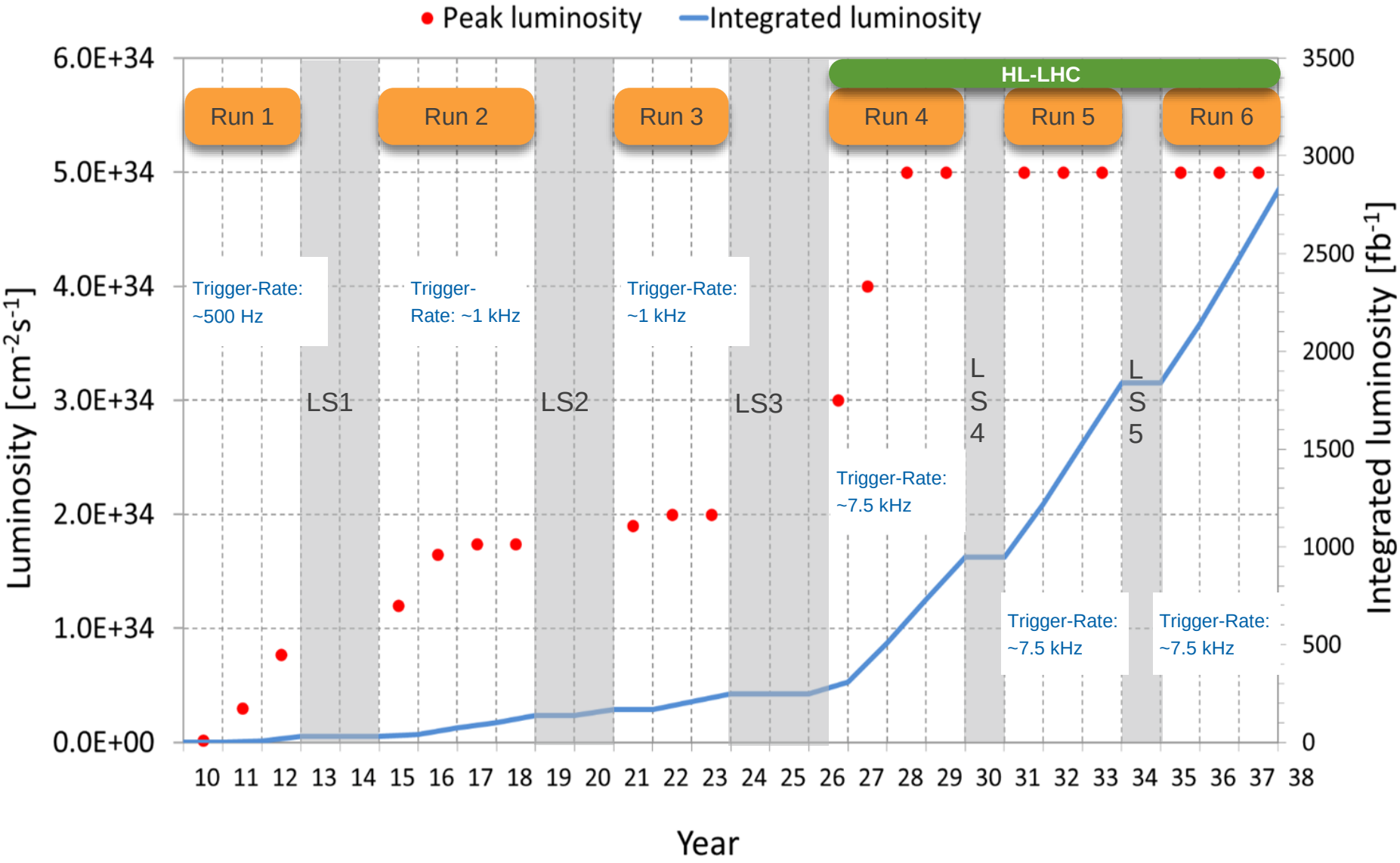
Unsupervised learning
"Anomaly Detection"
Ho-Fung Tsoi



Also includes new (but traditional) boosted object algorithm
Pallabi Das



LHC Now ➔ HL-LHC in the Future

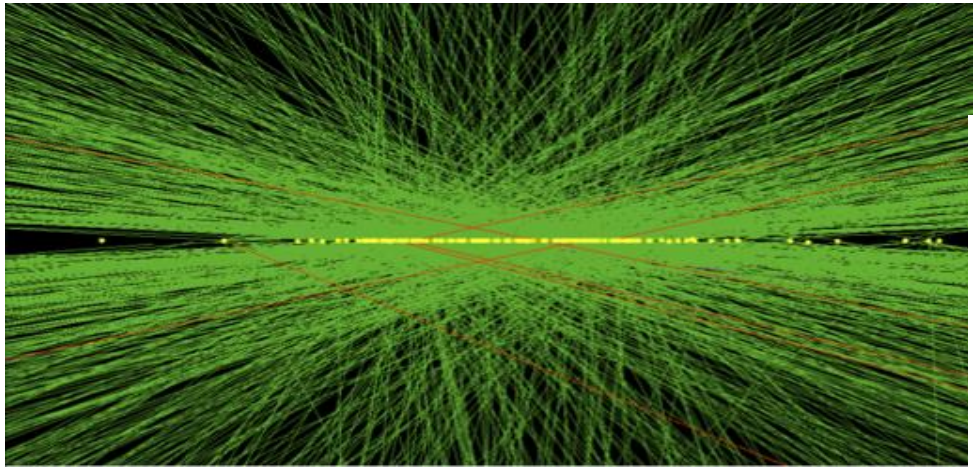


CMS will be on path to exabytes of data acquired in the HL-LHC era

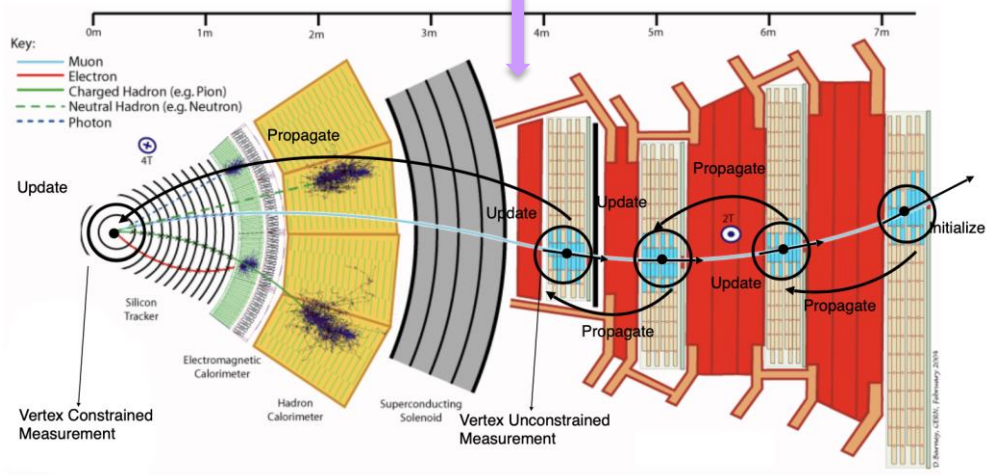
HLLHC Parameters

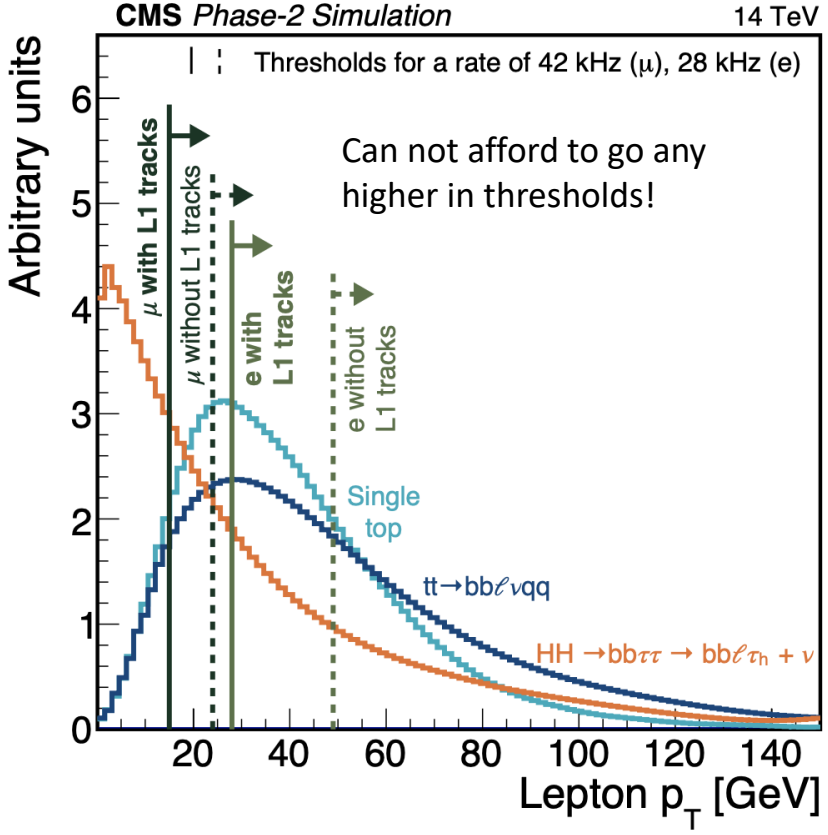
Parameter	Nominal LHC Design Report	HL-LHC 25 ns standard	HL-LHC 25 ns BCMS	HL-LHC 8b4e
Beam energy in collision [TeV]	7	7	7	7
$N_b[10^{11}]$	1.15	2.2	2.2	2.3
Number of bunches per beam	2808	2748	2604	1968
Beam current [A]	0.58	1.09	1.03	0.82
Minimum β^* [m]	0.55	0.2	0.2	0.2
ϵ_n [μm]	3.75	2.50	2.50	2.20
ϵ_L [eVs]	2.50	2.50	2.50	2.50
Peak luminosity with crab cavities $[10^{34}cm^{-2}s^{-1}]$	(1.18) Operating at 2x now	12.6	11.9	11.6
Levelled luminosity for $\mu = 140[10^{34}cm^{-2}s^{-1}]$	-	5.32 Expect Operating at 7.5x ultimately	5.02	5.03
(inelastic) collisions/crossing μ (with levelling and crab cavities)	27	140	140 μ=200	140
Maximum line density of pileup events during fill [events/mm]	0.21	1.3	1.3	1.3

Collisions (p-p) at HLLHC

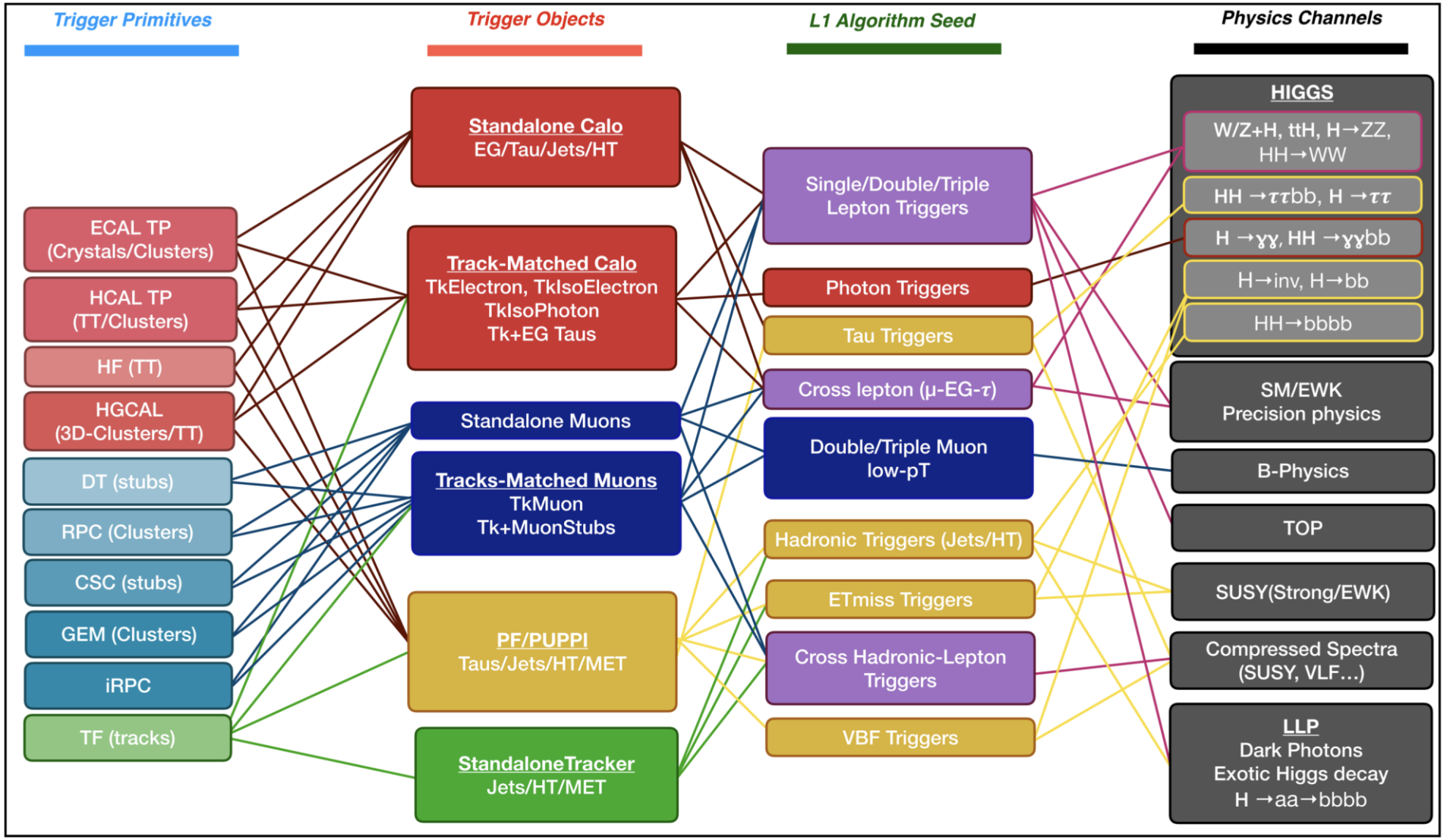


Selecting high P_T clusters and tracks

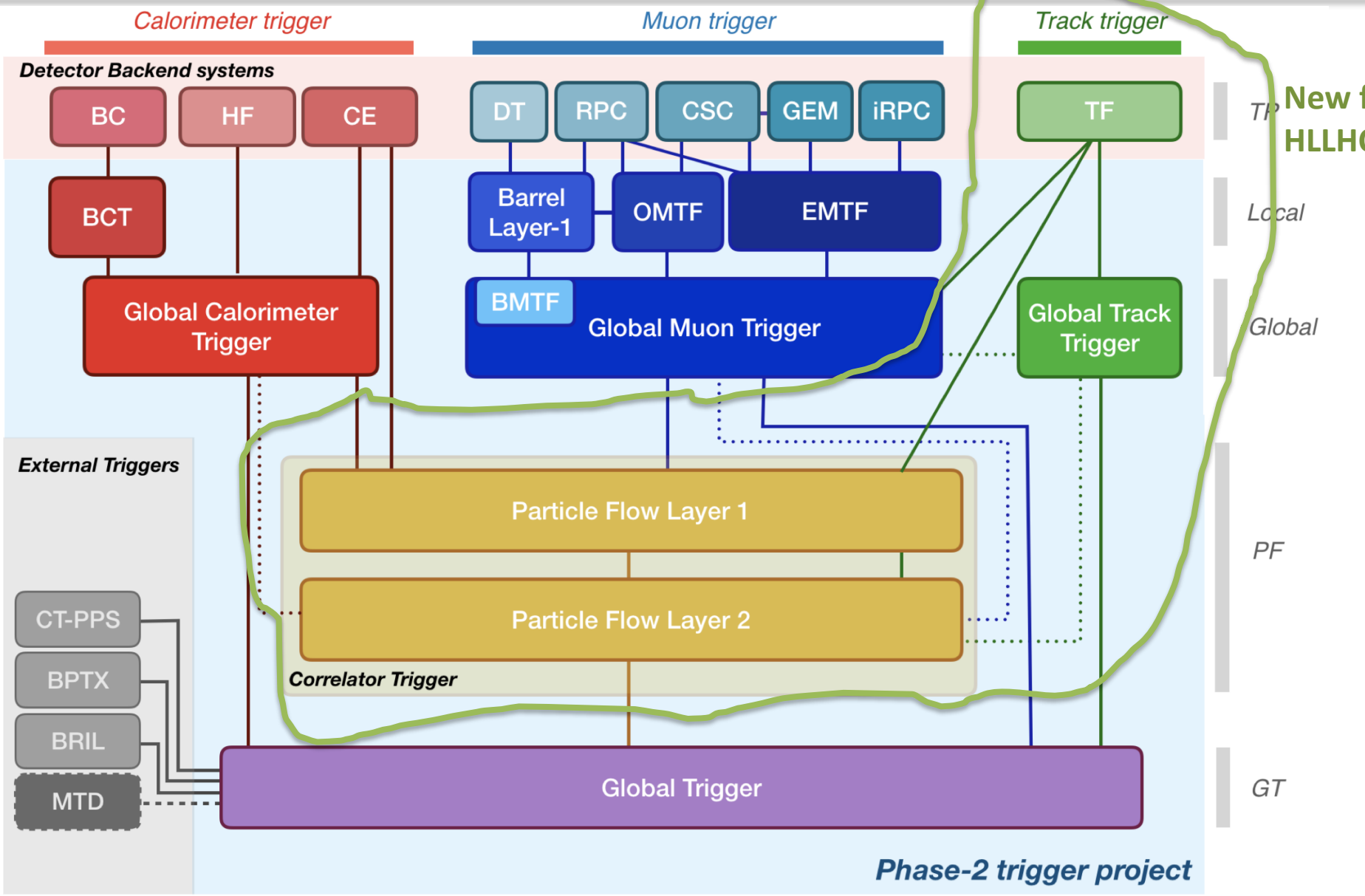




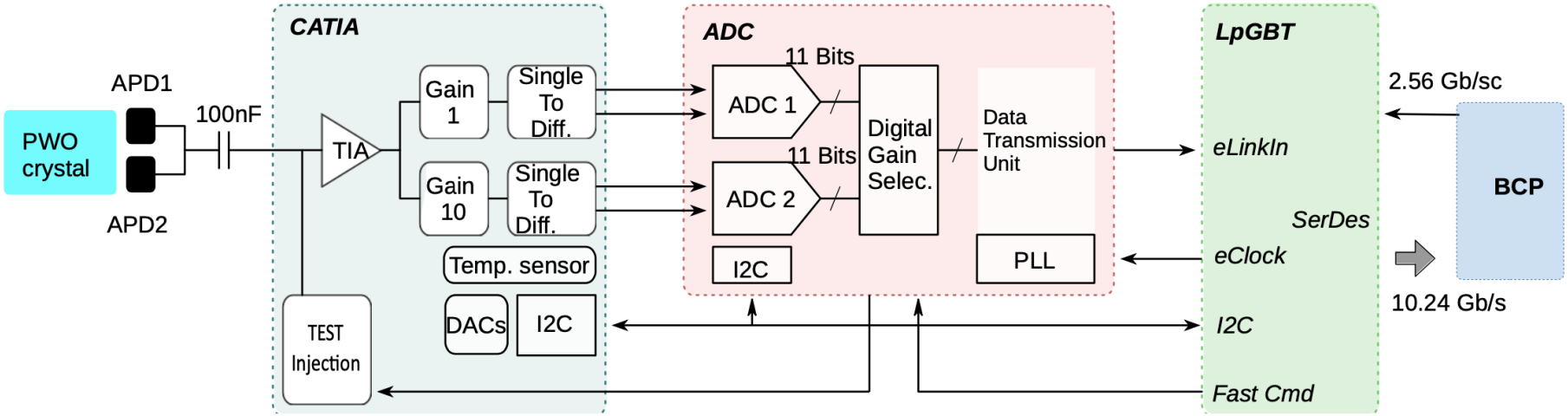
Triggers → Physics



CMS HLLHC Level-1 Trigger 2020

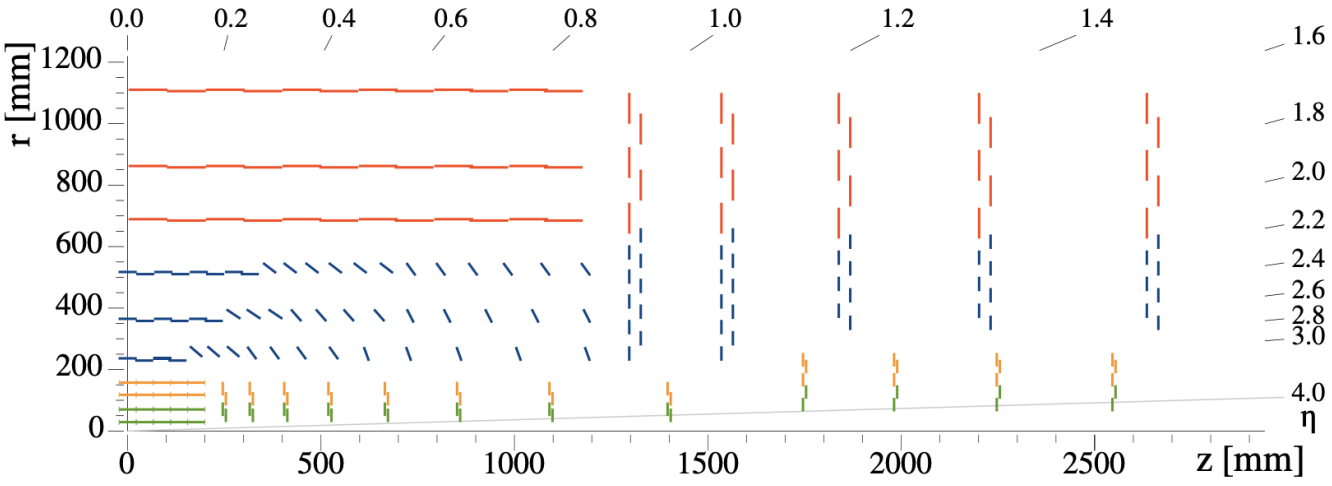


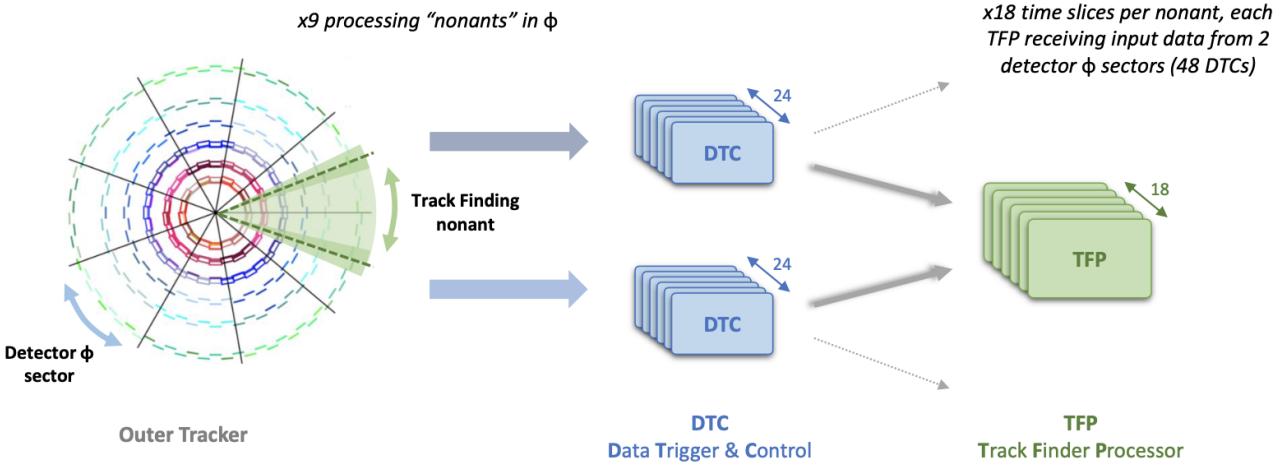
Getting the crystal data out (New for HLLHC)



There are 61200 crystals to be processed – packing 25 crystals per link out of BCP you still have 2448 links at 16 Gbps to contend in the calorimeter trigger path!

Getting the tracks out (New for HLLHC)





Outer tracker double layers allow track stub readout

Tracklets formed in TFP consistent with >2GeV P_T. Tracks propagated in-out, matched to form track candidates

Tracklets are then fit to make a track

Xilinx – Ultrascale+ Processors

Product Tables and Product Selection Guides

Cost-Optimized Portfolio

Spartan-7	Spartan-6
Artix-7	Zynq-7000

7 Series

Spartan-7	Artix-7
Kintex-7	Virtex-7

UltraScale

Kintex UltraScale	Virtex UltraScale

UltraScale+

Kintex UltraScale+	Virtex UltraScale+

	Kintex UltraScale+	Virtex UltraScale+	
Max System Logic Cells (K)	1,143	3,780	Times 2
Max Memory (Mb)	70.5	65,913	Many times
Max DSP Slices	3,528	12,288	Times 3
Max Transceiver Speed (Gb/s)	32.75	32.75	Times 2.5
Max I/O Pins	572	832	

Multi-gigabit-per-second serial links

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	Type	Max Performance[1]	Max Transceivers	Peak Bandwidth
Virtex UltraScale+	GTY	32.75	128	8,384 Gb/s
Kintex UltraScale+	GTH/GTY	16.3/32.75	44/32	3,268 Gb/s
Virtex UltraScale	GTH/GTY	16.3/30.5	60/60	5,616 Gb/s
Kintex UltraScale	GTH	16.3	64	2,086 Gb/s
Virtex-7	GTX/GTH/GTZ	12.5/13.1/28.05	56/96/16[3]	2,784 Gb/s
Kintex-7	GTX	12.5	32	800 Gb/s
Artix-7	GTP	6.6	16	211 Gb/s
Zynq UltraScale+	GTR/GTH/GTY	6.0/16.3/32.75	4/44/28	3,268 Gb/s
Zynq-7000	GTX	12.5	16	400 Gb/s
Spartan-6	GTP	3.2	8	51 Gb/s

HL-LHC

25 Gbps

LHC

10 Gbps

Key element - Multi-gigabit Opto-electronics

REVISION D

DO NOT SCALE FROM THIS PRINT

ESD SENSITIVE

TABLE 1: ASSEMBLY LENGTH LIMITS			
FIBER TYPE	HEAT SINK	MIN LENGTH (cm)	MAX LENGTH (cm)
-4	ANY	16	999
-5	-1,-2,-4,-5	12	100
	-3	12	48
-6	-1,-2,-4,-5	9	100
	-3	9	48

TABLE 2: LENGTH TOLERANCE	
ASSEMBLY LENGTH (cm)	TOLERANCE (cm)*
009-016	±0.16
017-999	±1%

* ROUNDED UP TO 2 DECIMAL PLACES

ECUO-B04-XX-XXX-0-X-1-X-XX

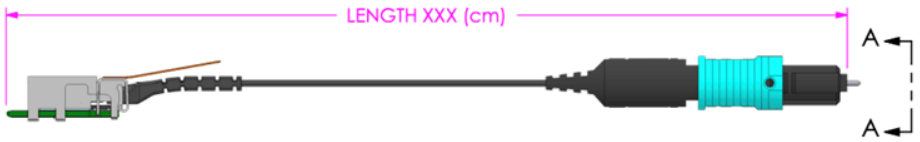
DATA RATE
-14: 14 Gbps
-25: 25.7 Gbps
-28: 28.1 Gbps

ASSEMBLY LENGTH
-XXX: LENGTH (cm) SEE TABLES 1, 2

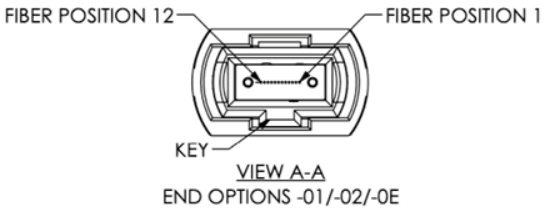
END OPTION
-01: MTP® MALE
-02: MTP® FEMALE
-07: MXC® INTERNAL PLUG
-0E: MPO PLUS® BAYONET MALE

HEAT SINK
-1: FLAT
-2: PIN FIN
-3: FLAT WITH GROOVE (SEE NOTE 2)
-4: PCIe® PIN FIN (-14 DATA RATE ONLY)
-5: 1.75 cm TALL PIN FIN (-25 & -28 DATA RATES ONLY)

FIBER TYPE
-4: AQUA LOOSE TUBE WITH BOOT
-5: BLACK JACKETED RIBBON WITH BOOT
-6: BLACK JACKETED RIBBON



PART NUMBER ECUO-B04-XX-XXX-0-1-5-01 SHOWN



VIEW A-A
END OPTIONS -01/-02/-0E

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS.
ALL DIMENSIONS ARE FOR REFERENCE ONLY

PROPRIETARY NOTE

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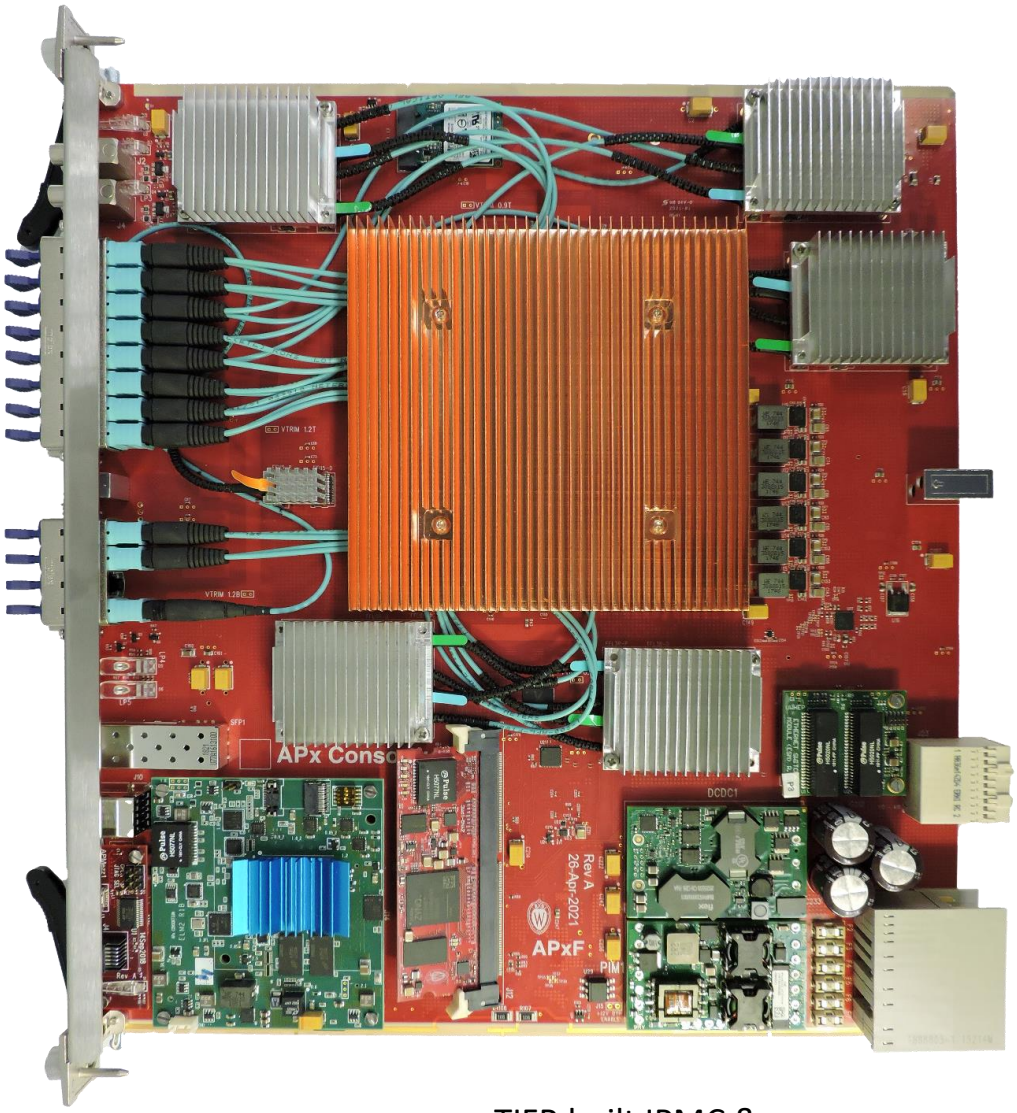
MATERIAL: DO NOT SCALE DRAWING SHEET SCALE: 1:1

DESCRIPTION: OPTICAL FIREFLY ASSEMBLY

DWG. NO. ECUO-B04-XX-XXX-0-X-1-X-XX

BY: JEAN W. 01/06/2016 SHEET 1 OF 6

Advanced Processor Prototype for HL-LHC



TIFR built IPMC &
ESM mezzanines

- Wisconsin APxF Board
- Xilinx VU13P or VU9P FPGA
- ZYNQ-IPMC
  (ATCA IPMI controller)
- ELM (ZYNQ-based
  embedded Linux endpoint)
- ESM (GbE switch)
- High efficiency heatsinks
- Front-panel inputs

25G Samtec Firefly positions loaded – 10x12 + 1x4
(124 25 Gbps links)

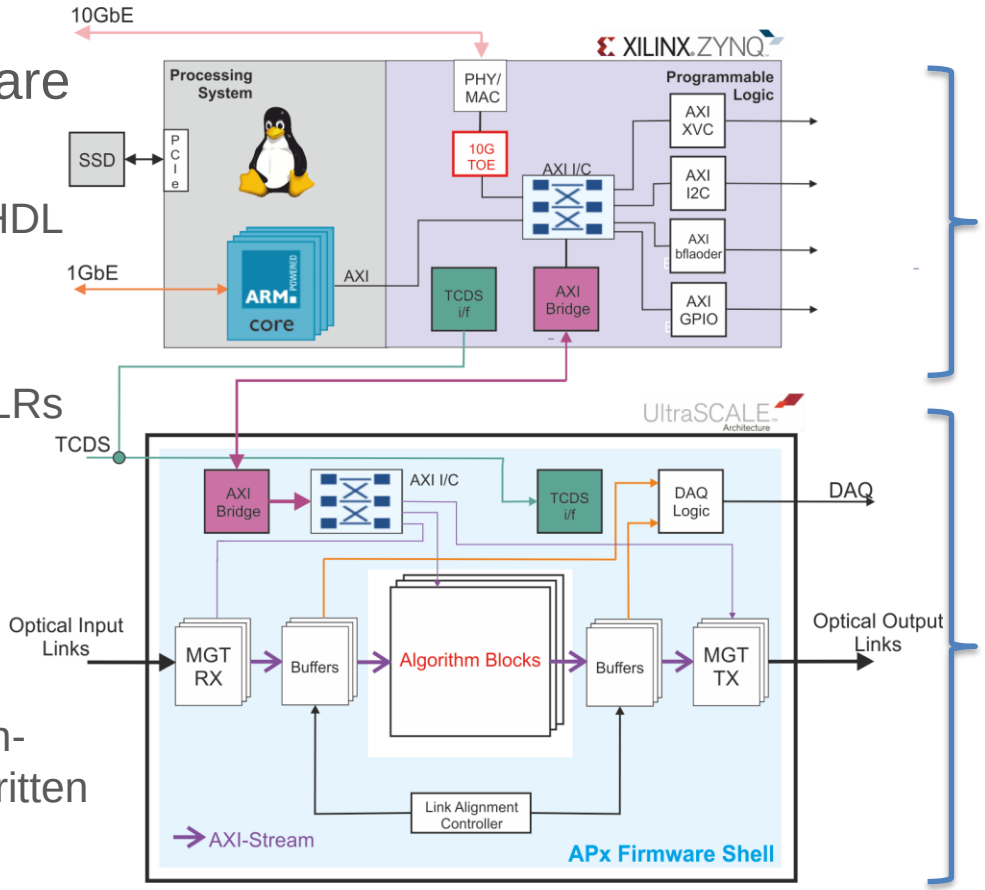
APx – Firmware/Software

A new paradigm for firmware development

- Core firmware written in VHDL by engineers
- Gigabit link support
- Data exchange between SLRs within chip
- Test buffers
- Clock and control

Physics

- Algorithmic firmware in high-level languages like C++ written by physicists



ELM:
Control endpoint, providing complete board overhead functionality

Processing FPGA:
- I/O
- data processor
- DAQ

APx-FS Resource Utilization

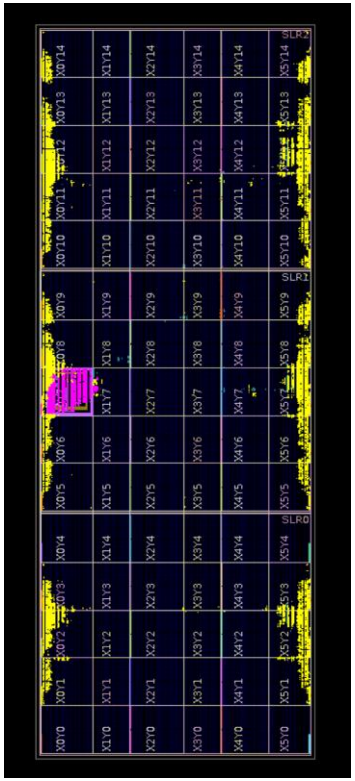
Utilization VU9P build Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	33309	1182240	2.82
LUTRAM	963	591840	0.16
FF	51563	2364480	2.18
BRAM	7	2160	0.32
IO	9	416	2.16
GT	102	104	98.08
BUFG	236	1800	13.11
MMCM	3	30	10.00

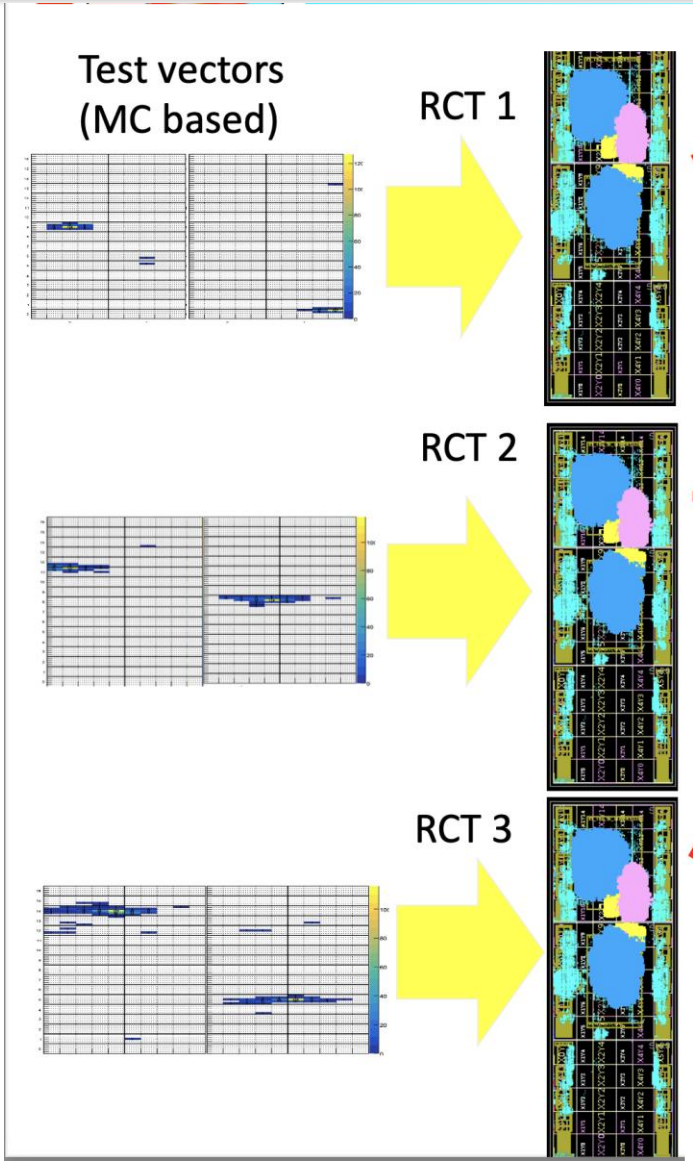
100x 25G GTY links w/ support infra

Central AXI infra with MGT-based Chip2chip core



APd1 VU9P FPGA floorplan

Calorimeter Firmware Tests



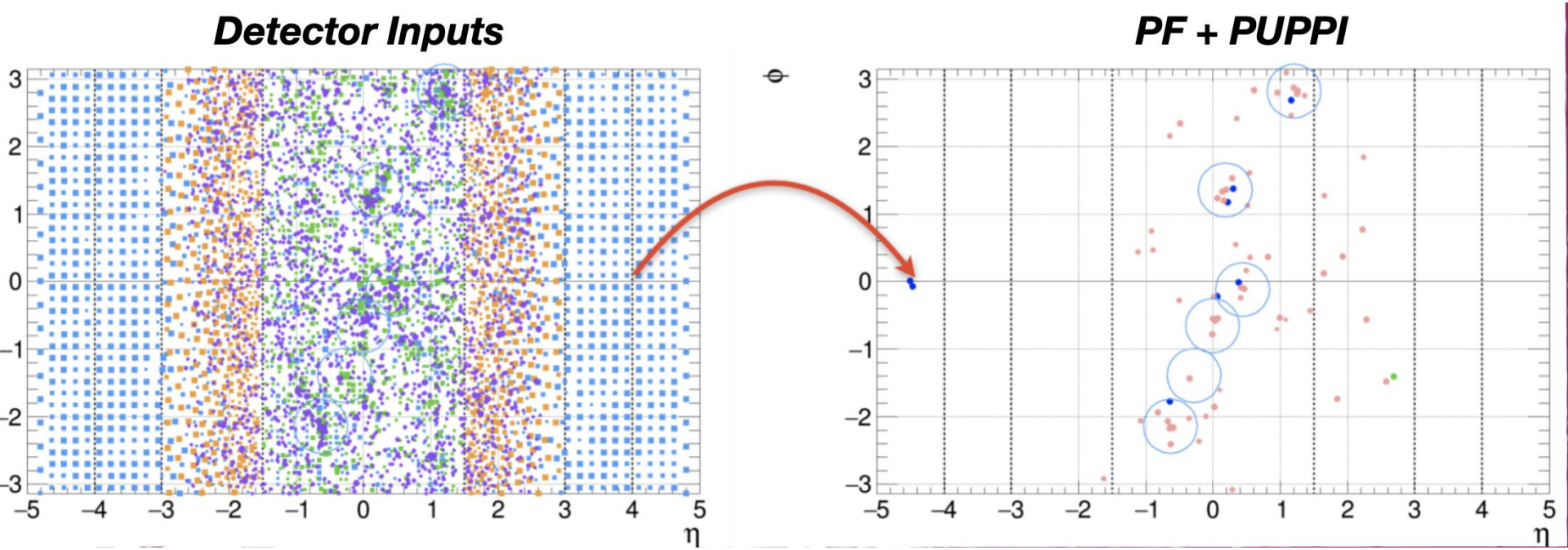
Test stand at Wisconsin

GCT HW output compared to expected

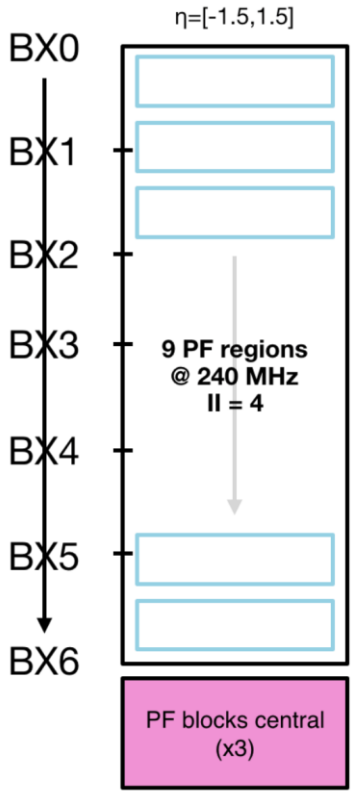
First time capturing real data in multiple card test!

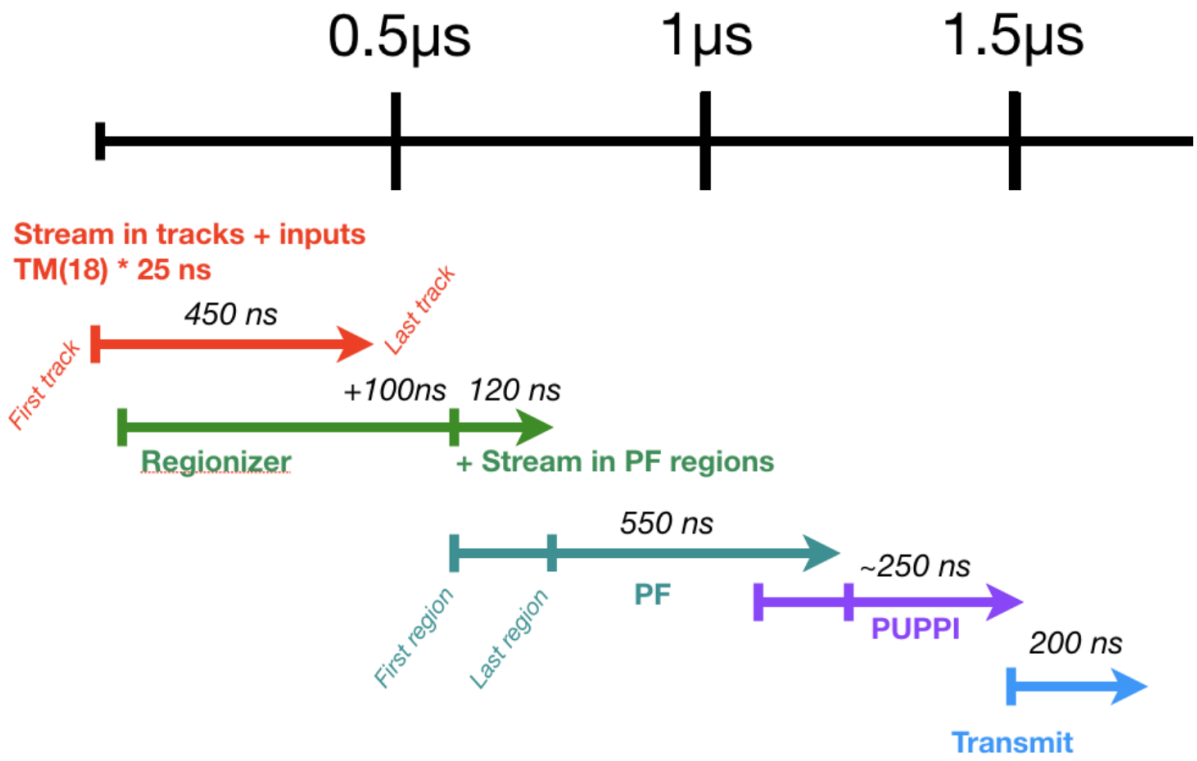
Firmware prepared and tests conducted by U of Hyderabad student Piyush Kumar

Particle Flow Reconstruction on FPGAs



Particle Flow Implementation

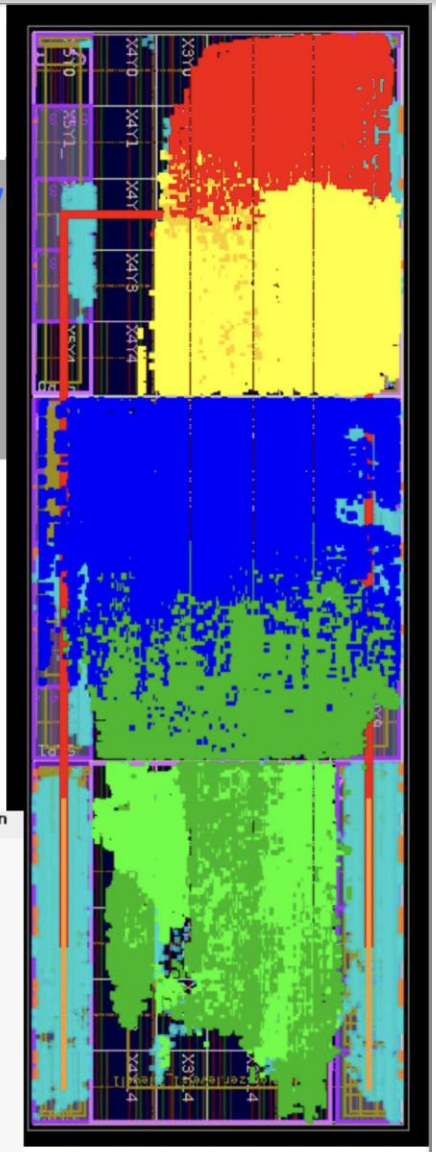


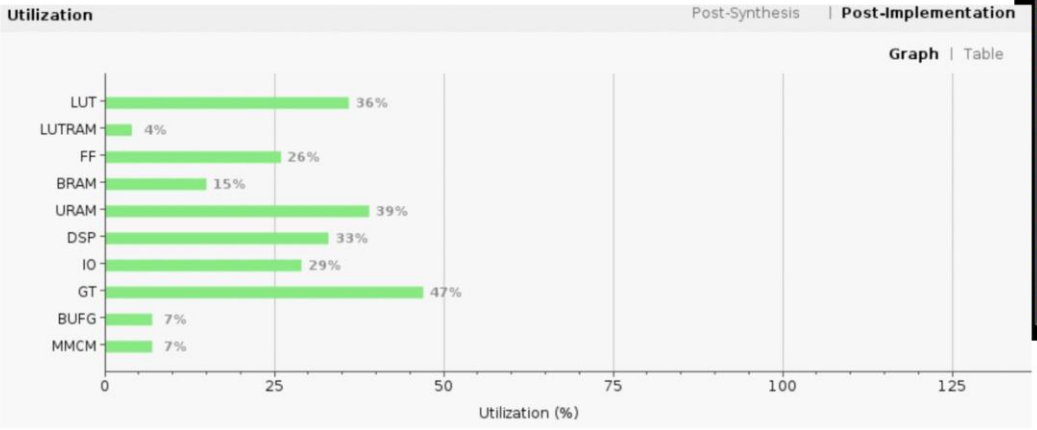


Particle Flow – Correlator Layer 1

- Five firmware pieces in main algorithm:
  - Common APx infrastructure
  - Regionizer
  - Particle Flow (PF)
  - PileUp Per Particle Identification (PUPPI)
  - Output sorting
- Meets timing with <50% resource use for VU9P-2 (plan to use VU13P-2).
- Latency of 1.1 μs is sufficient to meet the requirements
- Simulation and emulation match in single board tests.
- The most challenging firmware project we have, and it works!
- Additional algorithm to do e/γ preprocessing tested; not yet integrated

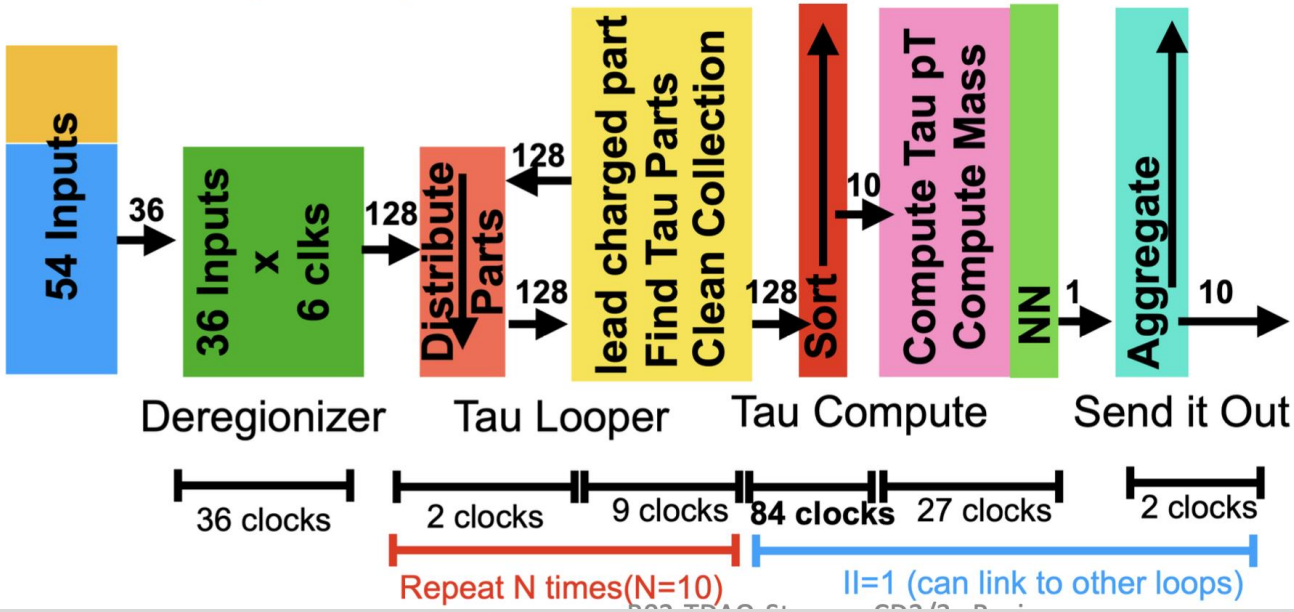
particle flow
PUPPI
output sort
regionizer 1
regionizer 2

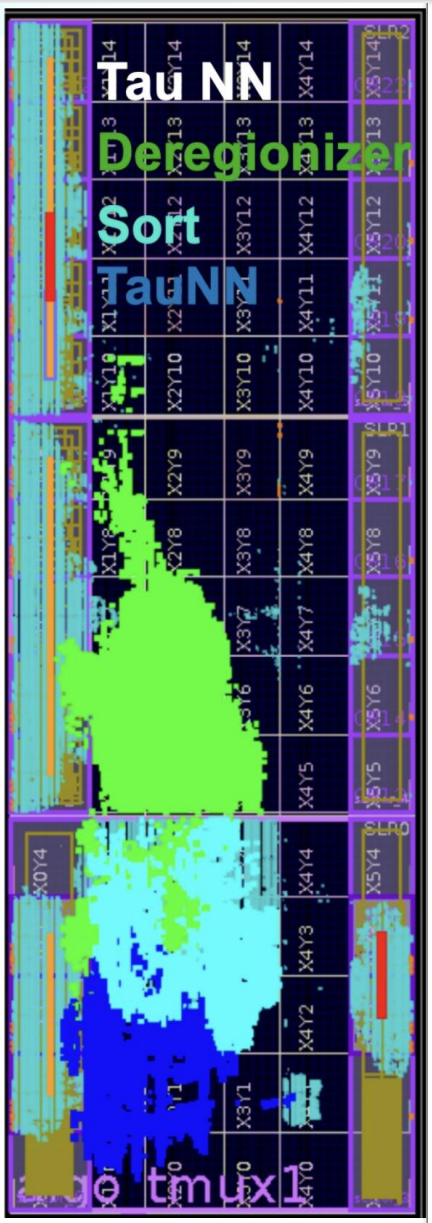




Particle Flow – Correlator Layer 2 τ_h

- τ reconstruction with neural net:
  - One of the first CL2 algorithms
  - Now uses redesigned firmware incorporating deregionizer code and seeded cone jet reconstruction before τ_h identification.
  - Meets timing
  - Latency of 1.0 μs is sufficient to meet requirements
  - Emulation matches and is in CMSSW with multi-vertex PUPPI capability.





Concluding Thoughts

We in HEP are not innovators of modern computing technologies but we are amongst those who push it the most.

A team of engineers and physicists have tamed the LHC data deluge with intelligent use of telecommunications and computing technologies to enable fundamental physics discoveries.

We continue to push the technologies to the limit.

Advances in telecommunications and computing technologies are continually adapted to track increasing data volumes.

Students and postdocs are getting good training, especially in operations and firmware, for potential careers in both academia and industry – We invite you to join us in the HL-LHC adventure!