# WP10.6.4 – Beam based feedback at FLASH Upgrade to mTCA

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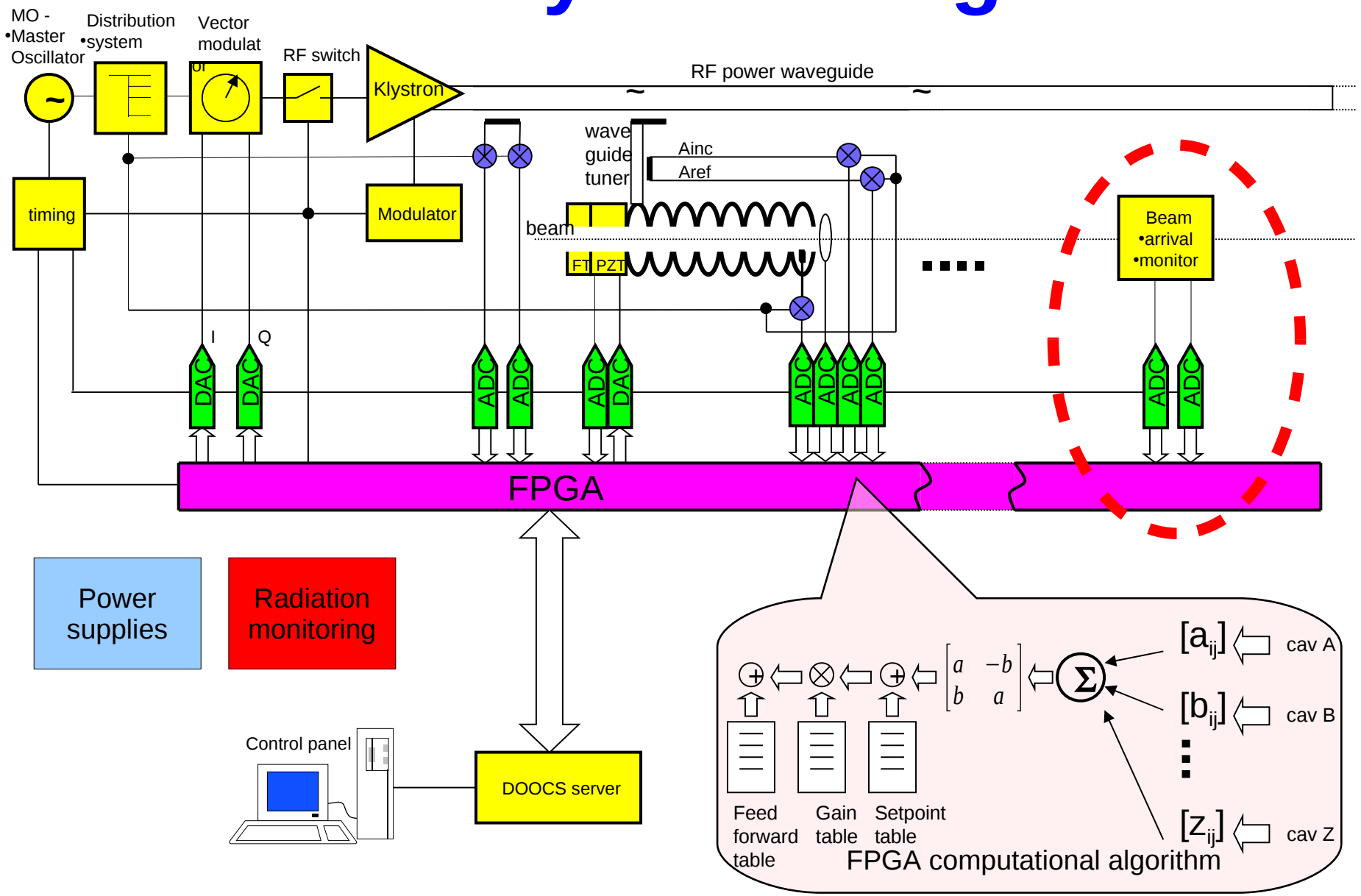
# Introduction

- BBF system generates correction for amplitude and phase of the RF filed, with respect of the beam
- There are 2 types of beam detectors in FLASH used for the feedbacks:
  - **BAM** - Bunch arrival time monitor for energy feedback
  - **PYRO** – for bunch compression feedback
- Pyro signal is slow in comparison with the BAM signal, and It has been moved to another system

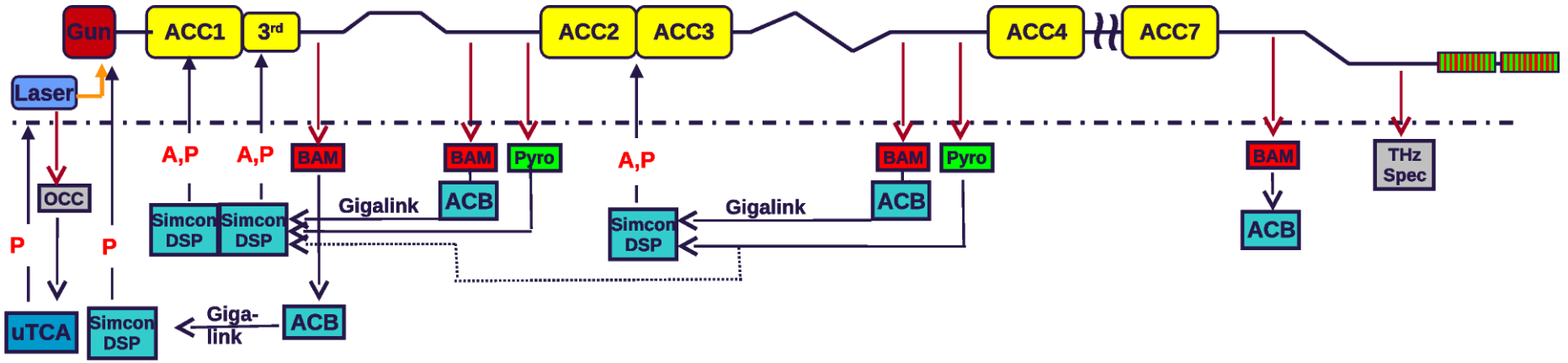
Most of the work has been focused on **energy feedback**

# LLRF System Diagram



# Actual status

- In the beginning of the 2011, the VME-based BBF system has been finally installed in the machine for permanent operation
- There are 4 BAMs and 2 PYROs



# Difficulties

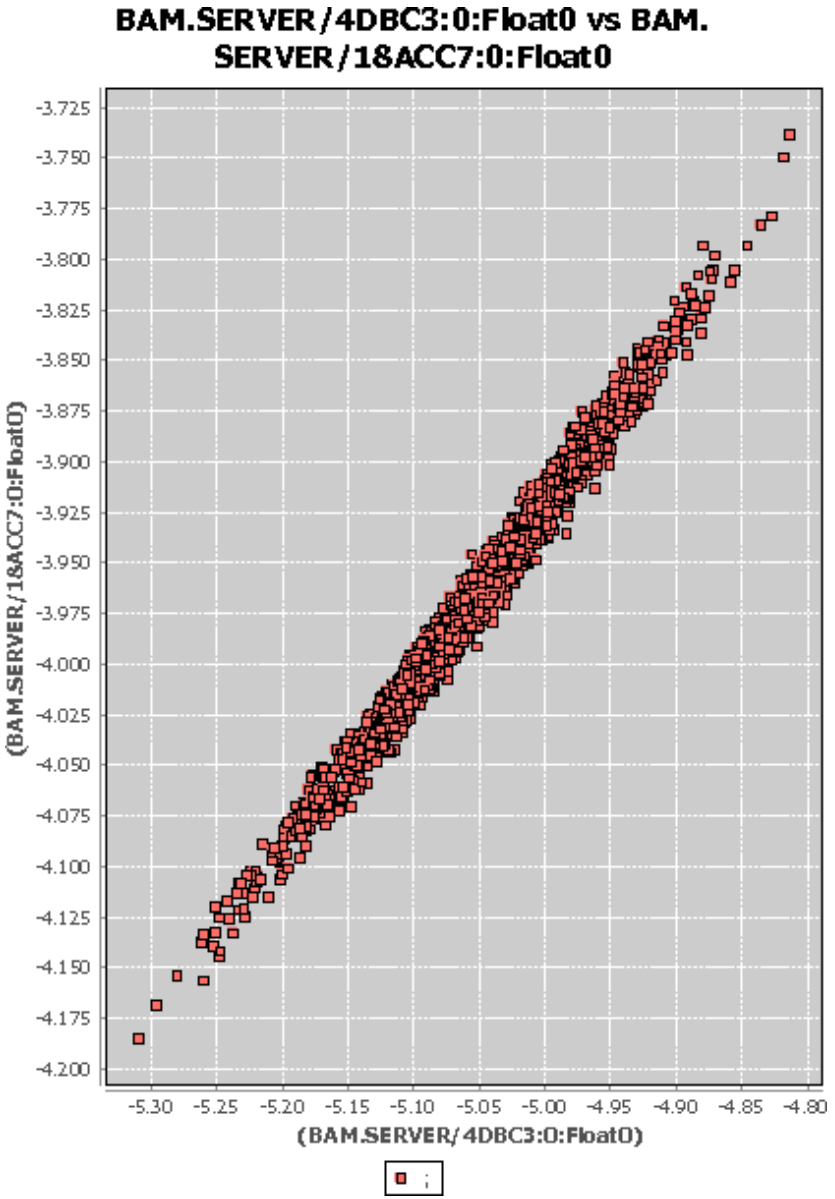
- For permanent installation, DOOCS DAQ system support was needed
- From the DAQ system, we found out that sometimes sent data was not consistent
- The reason of problem:
  - Solaris + DOOCS != Real-Time System
- The solution:
  - Each event was analyzed during processing, and was simply dropped – if it seems bad

# Difficulties

- Except DAQ problems, a lot of bugs have been fixed, and improvements added
- Clock input has been “re-wired” on the boards, to take clock directly from the optical fiber – it helped to solve problems with clock-to-trigger alignment
- A consensus between *request for new features* and *stability* has been achieved

# Results – Correlation of 2 BAMs

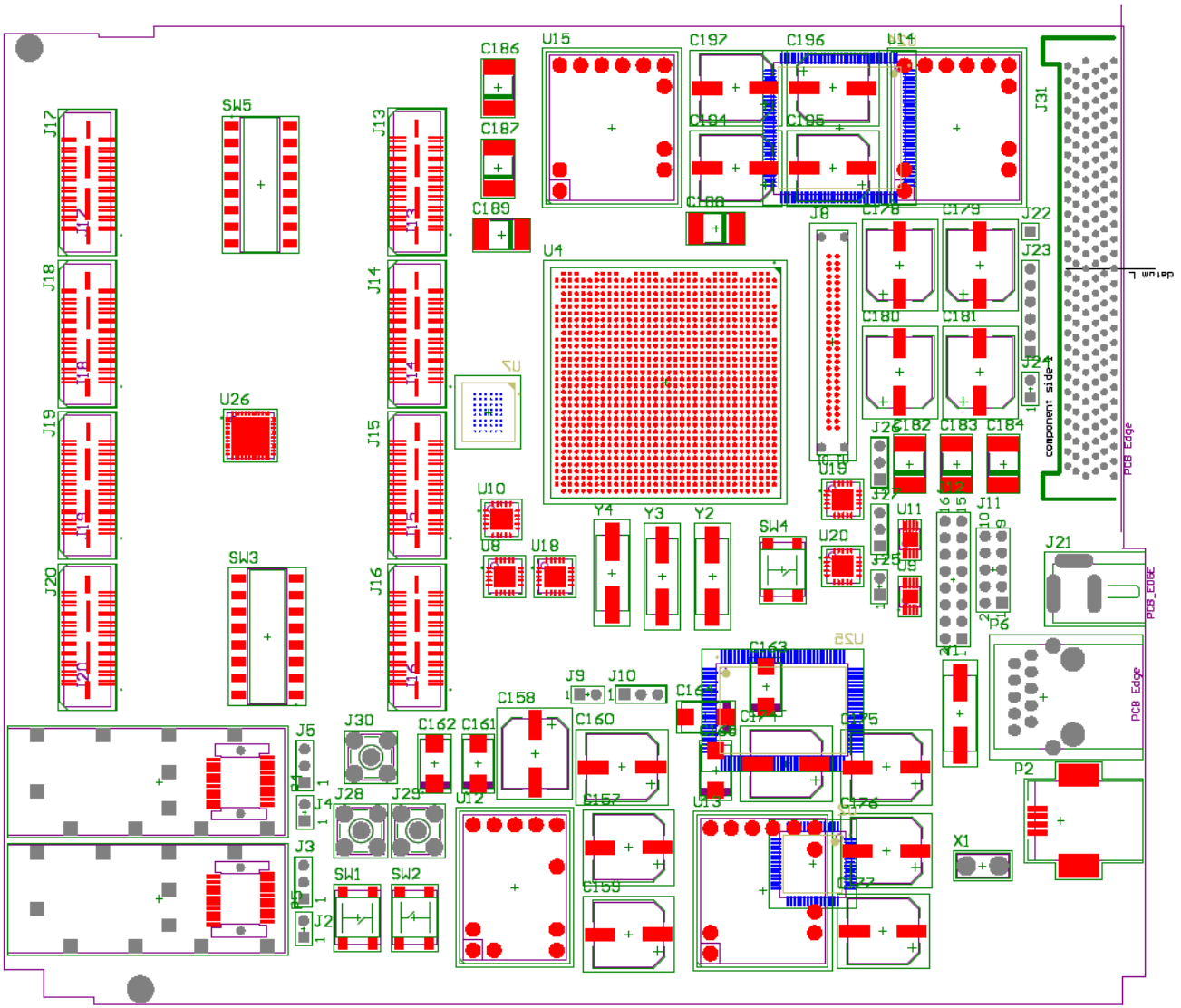
- After successful setting the system up, we have measured the correlation between 2 BAM detectors (at 4DBC3 and at 18ACC7 locations)



# New version of the system

- After successful installation of the VME system, we have started design works on new uTCA version of the board for processing BAM signals
- The main aims of this work are following:
  - Fix problems and limitations, which could not be avoided in existing system (216 MHz sampling)
  - Build system in uTCA form factor, which guaranties compatibility with rest of the LLRF system

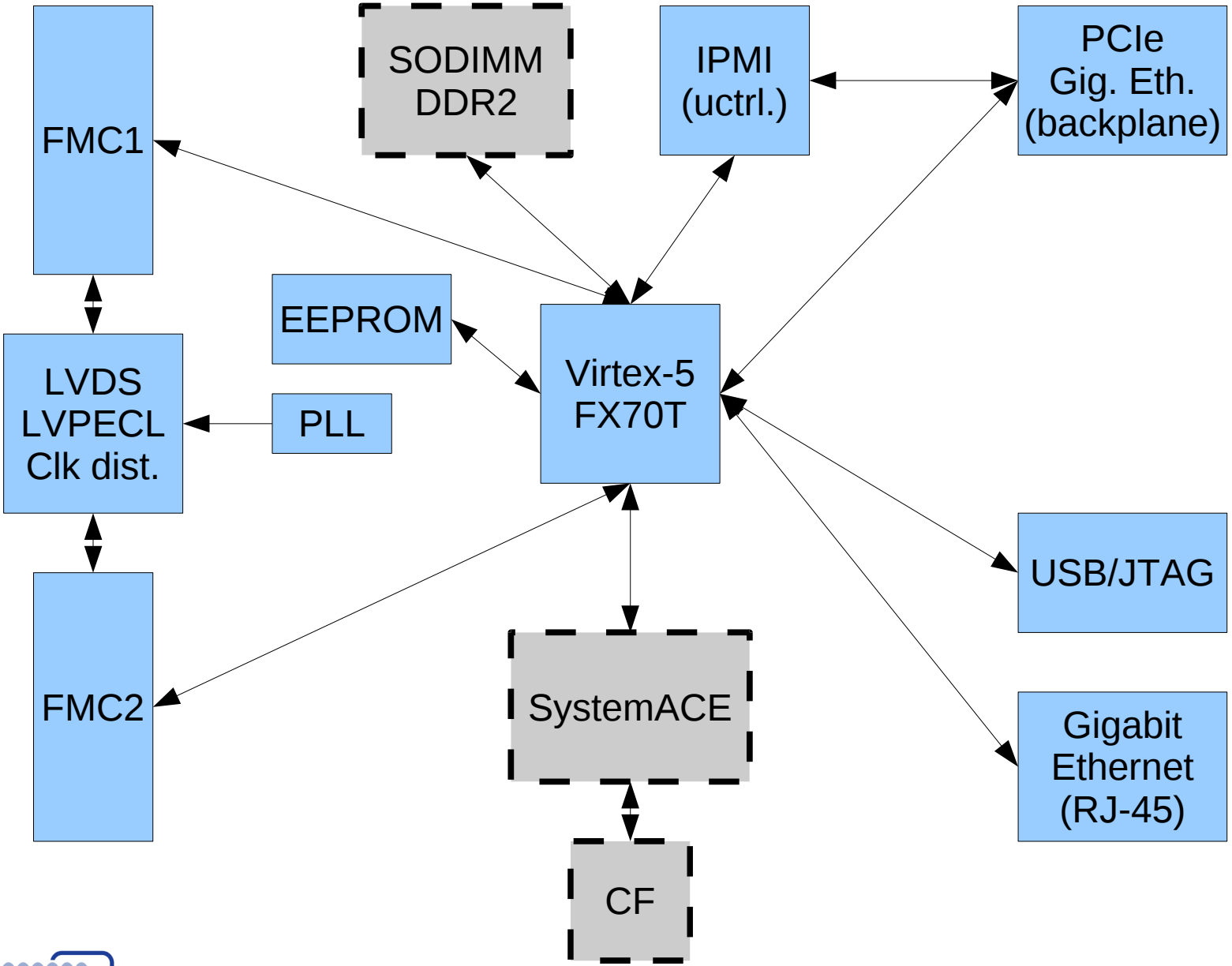
# First vision



# Main Features

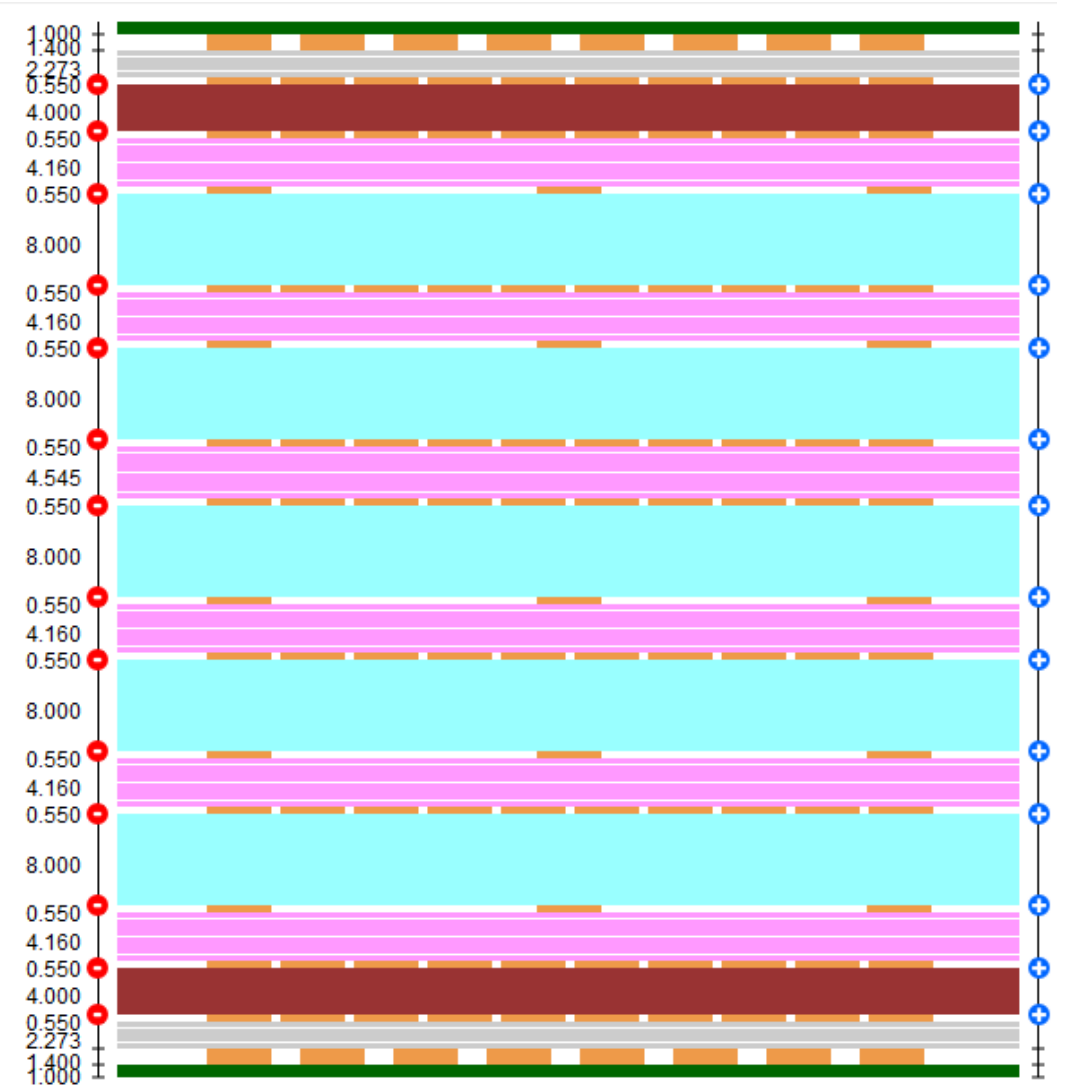
- **uTCA** form factor
- **AMC.4** compatible (xTCA for Physics std.)
- Carrier for **2 FMC** slots
- Up to **4 ADC** channels
- Up to **16 bits** per ADC (diff. pair each)
- PLL to generate clock up to **1GHz** for ADCs
- Low-noise clocks (**LVDS** and **LVPECL)** provided for each ADC
- Clocks for ADCs will have **phase shifting**
- **PCIe** & **IPMI** compatible

# Block diagram



# PCB layer stack

- 16 layers (7 signal, 9 planes)
- 2.3mm pressed thickness (with cutting when needed)
- FR408 high frequency material
- 4 mills tracks (6 mills spacing)
- 100 Ohm differential pairs on inner layer
- Blind vias from top to second and third planes (bottom and top)
- No buried vias
- Stack has been designed and simulated Polar and Isostack software
- Stack has been accepted by the manufacture company as „safe”



# Actual status

- What is already done:
  - Concept of the board has been worked out
  - All partial schematics done
  - PCB production technology chosen
  - 95% of components ordered
- What we are currently doing:
  - Integrating all partial schematics - connecting signals to FPGA (according to the chosen PCB technology)
  - We are about to start routing

# The End

Thank You !