# Analog signal conversion and clock distribution in the uTCA based LLRF system

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**WP10.6 - LLRF at FLASH**

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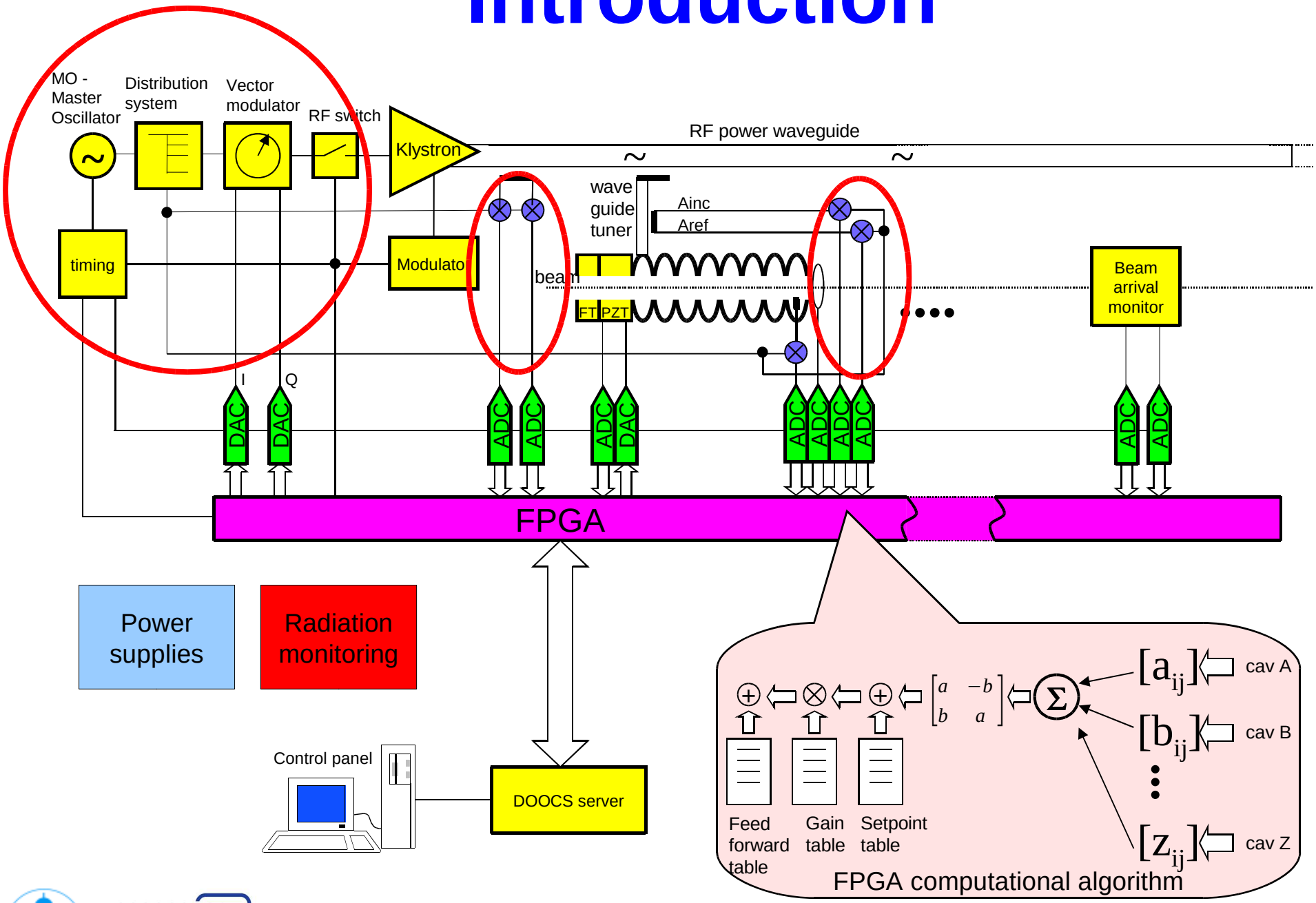
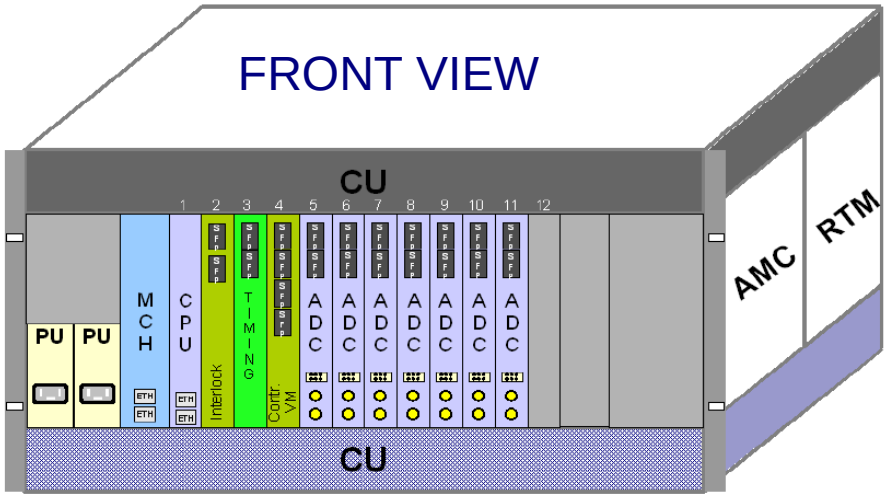
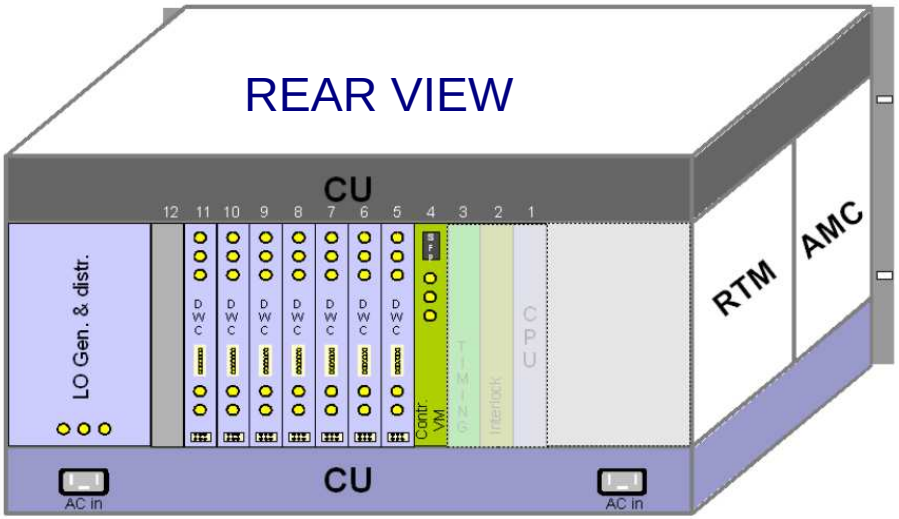
# Introduction



# LLRF

- The new LLRF system concept: compact design in uTCA crate
- Both AMC (front) and uRTM (rear) modules are used
- Many RF signals must be distributed inside of the crate (minimum external connections)
- This increases performance and reliability but creates technical difficulties
- The distribution scheme and special cards fulfilling all requirements have to be designed



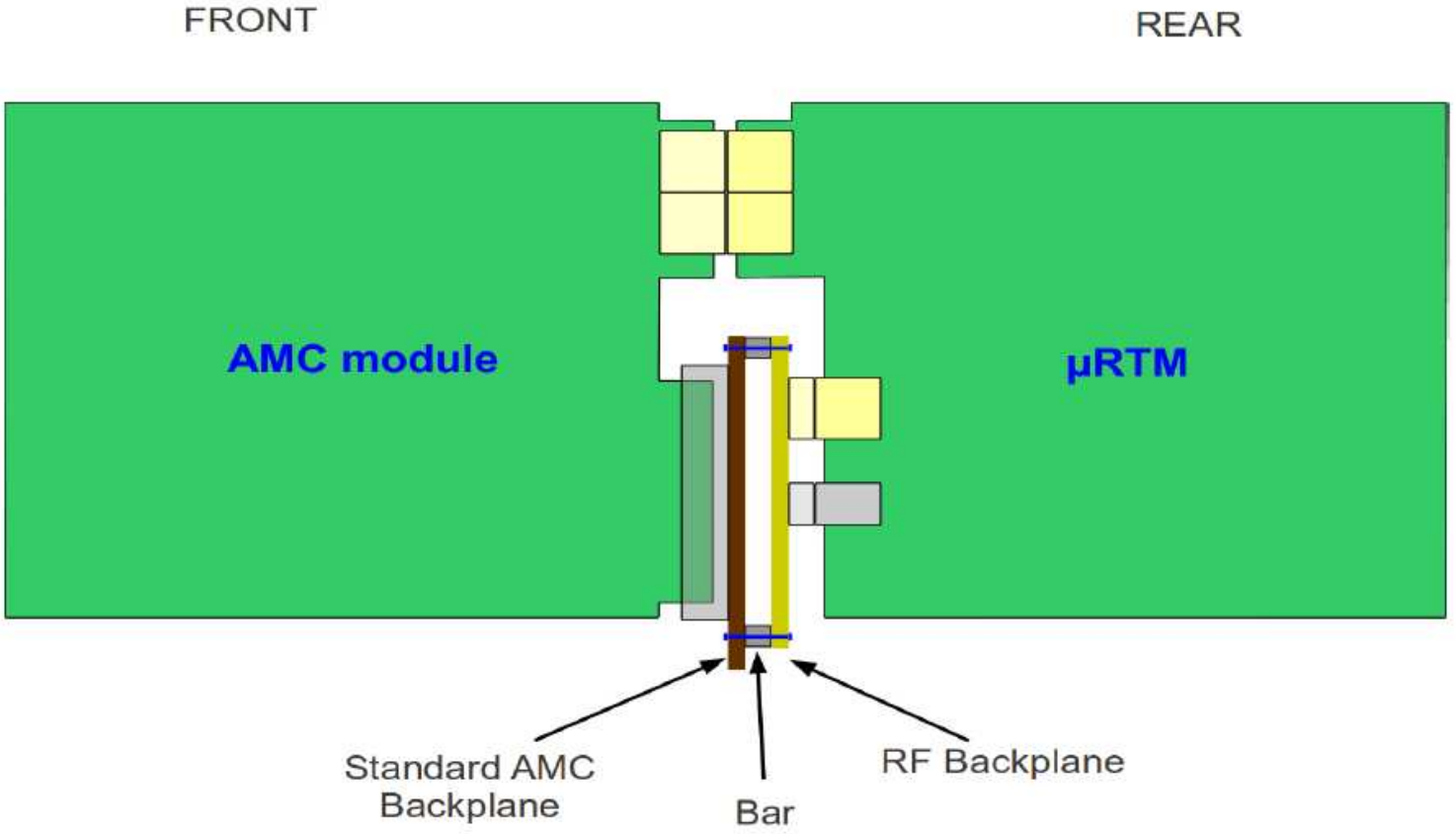

Courtesy of T. Jeżyński

# Physical layout of components – RF Backplane for Analog Signals

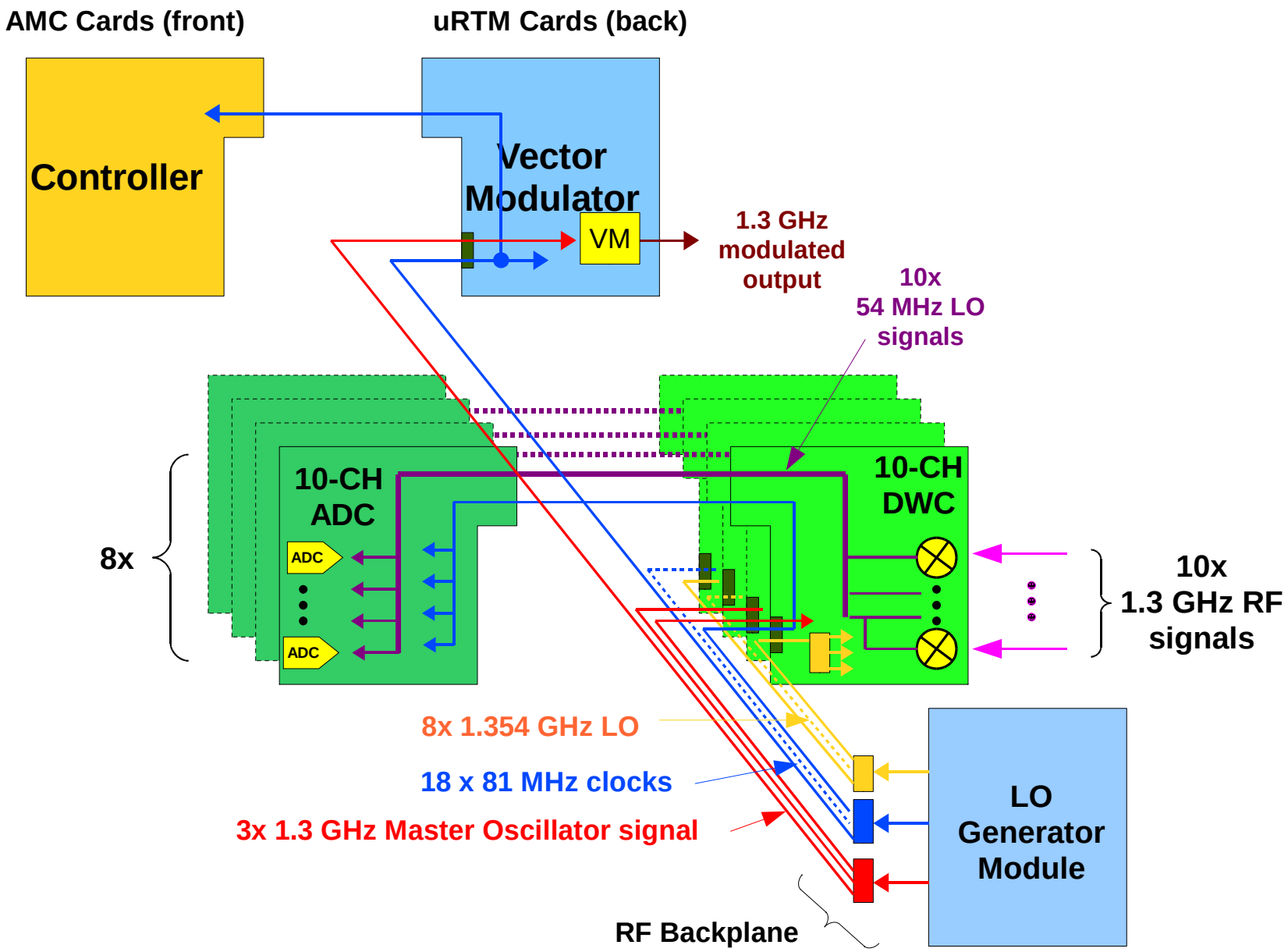
- Standard uTCA crate was modified to fulfill LLRF requirements

AMC Modules:
- Controller
- ADC card

uRTM Modules:
- Mutichannel downconverter
- Vector Modulator



# Analog signal flow concept in the uTCA Crate



# RF Backplane for uTCA (uRFB)

Objectives:

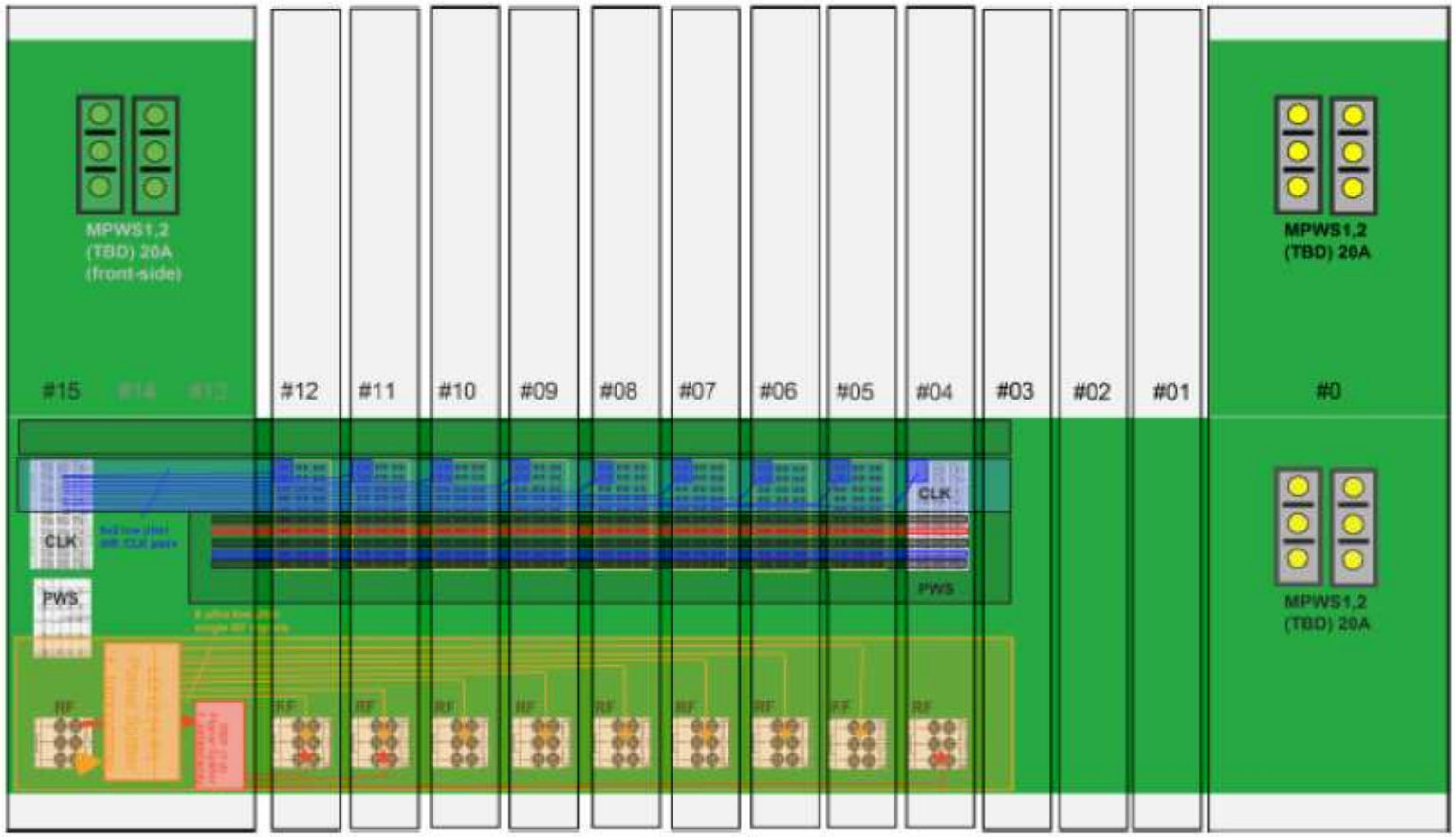
- Distribute analog signals in the crate
- Distribute high performance power supply

Signals

- 9 x 1354 MHz LO
- 18 x differential 81 MHz clocks
- 3 x 1300 MHz Master Oscillator
- Analog power supply (+/- 7V) for each uRTM

# RF Backplane Concept

- Entry slot for the signals on the left side in spare uTCA crate area
- “As passive as possible” - to reduce additive jitter and other interference from active components




Courtesy of T. Jeżyński

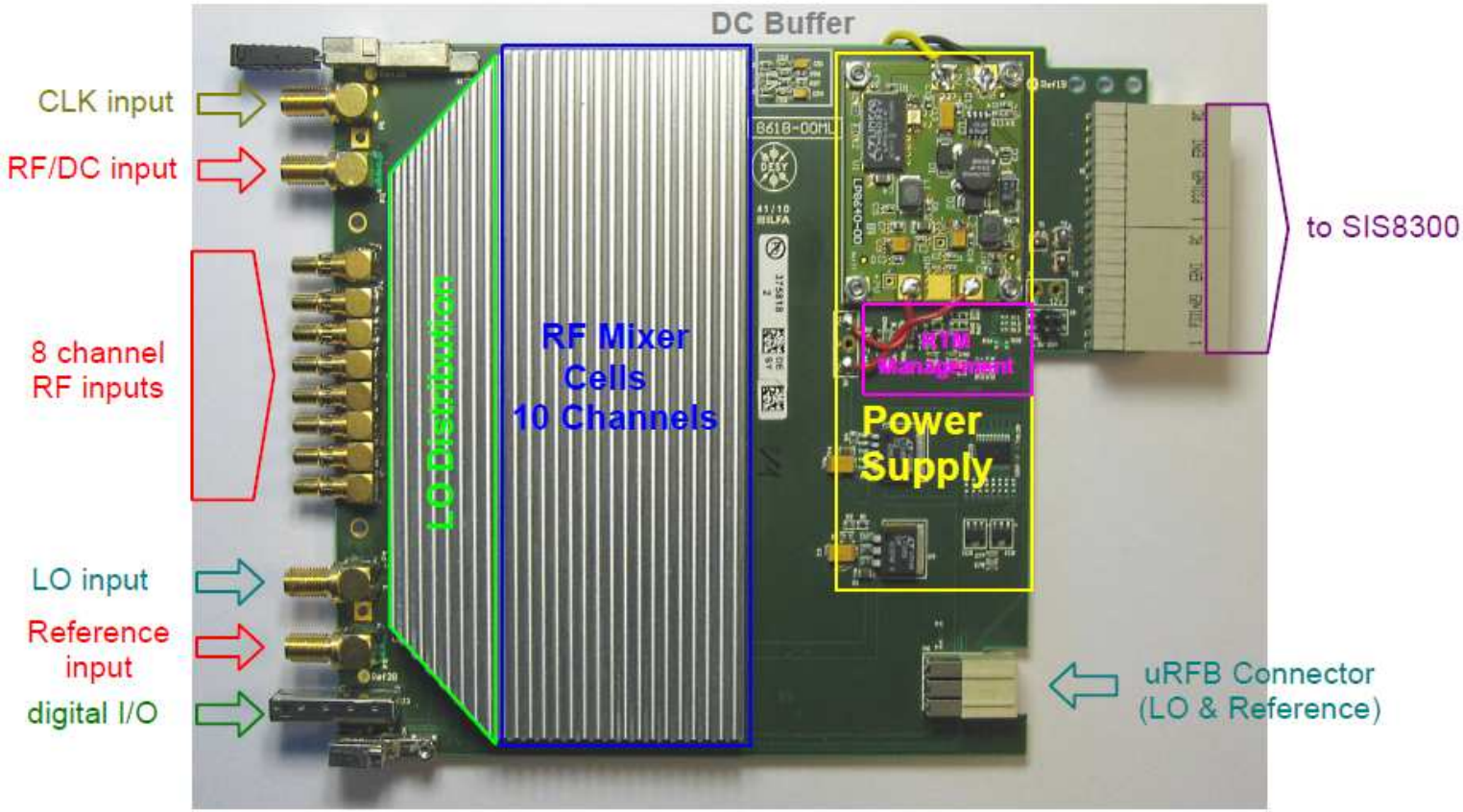
# Board Design and Current Status

- There was significant development on the backplane during first 18 months of the EuCARD program.
- Ability of reaching the performance was demonstrated on the ATCA platform
- The uTCA version is in the final design stage
- In June 2011 first tests are expected

# RTM Downconverter (DWC)

- 10-channel downconverter module
- Change the cavity frequency (1.3 GHz) down to 54 MHz IF signal
- Very high performance required (linearity, low crosstalks, low noise contribution)
- RF Backplane compatible
- Minimum cable connections (LO distribution on board)
- The next generation of the module was developed and successfully tested in 2010/beginning of 2011 (Deliverable 10.6.7)

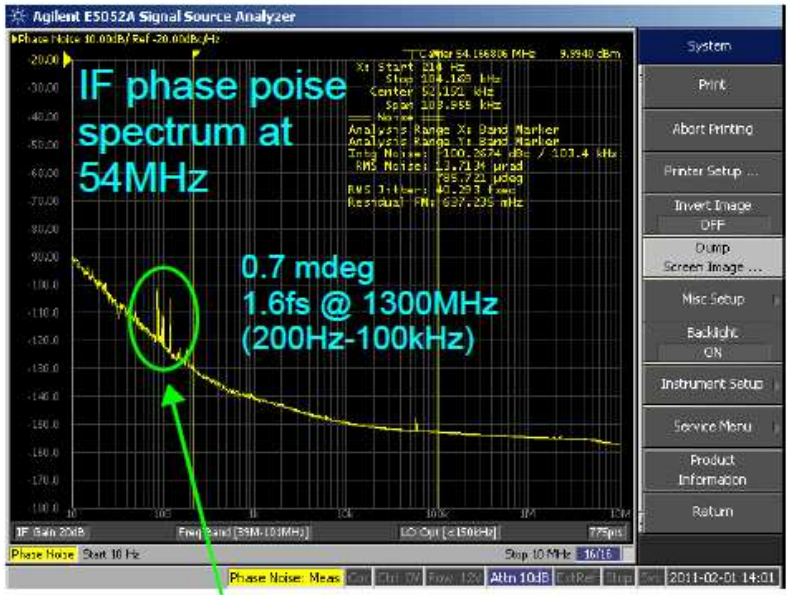
# RTM DWC Board




Courtesy of Jan Piekarski and Matthias Hoffmann

# RTM DWC – First Measurement Results

- No disturbances from the crate (power supply, MCH, CPU)
- IF phase noise spectrum at 54MHz
- 0.7mdeg or 1.6fs @1300MHz (200Hz-100kHz)
- Tested in ELMA and Schroff crate



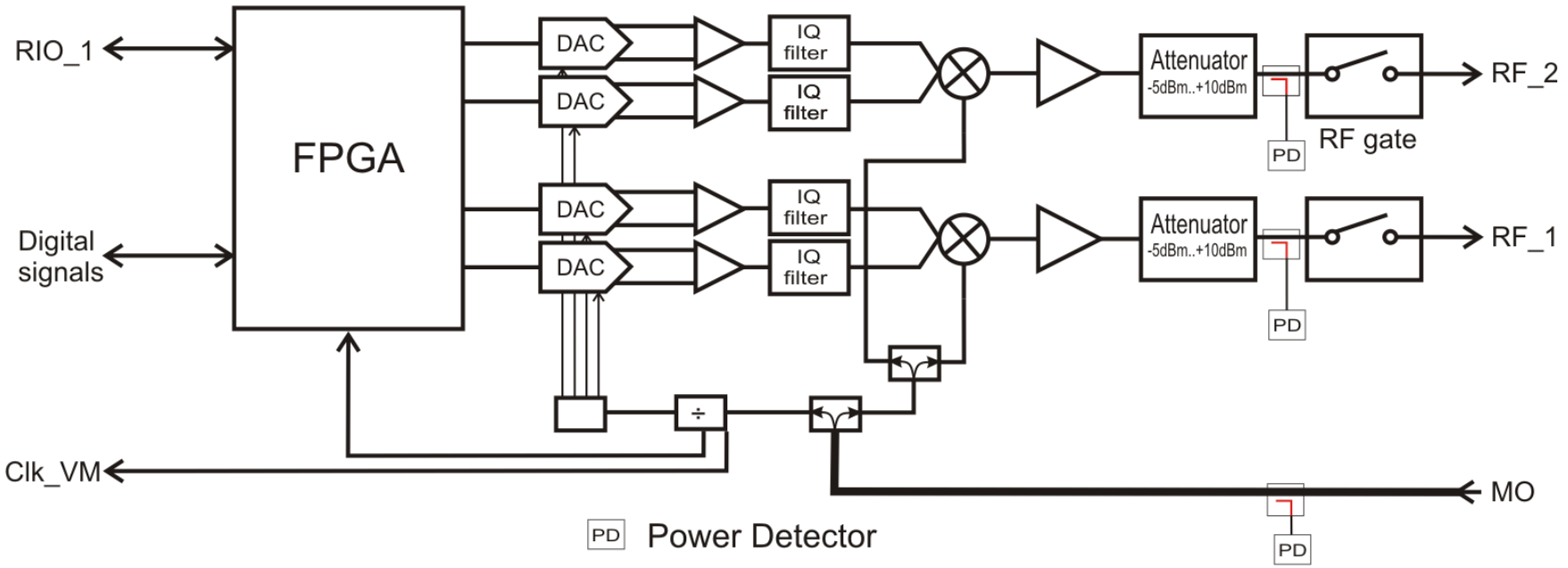

LO-Box Power Supply


Courtesy of Matthias Hoffmann

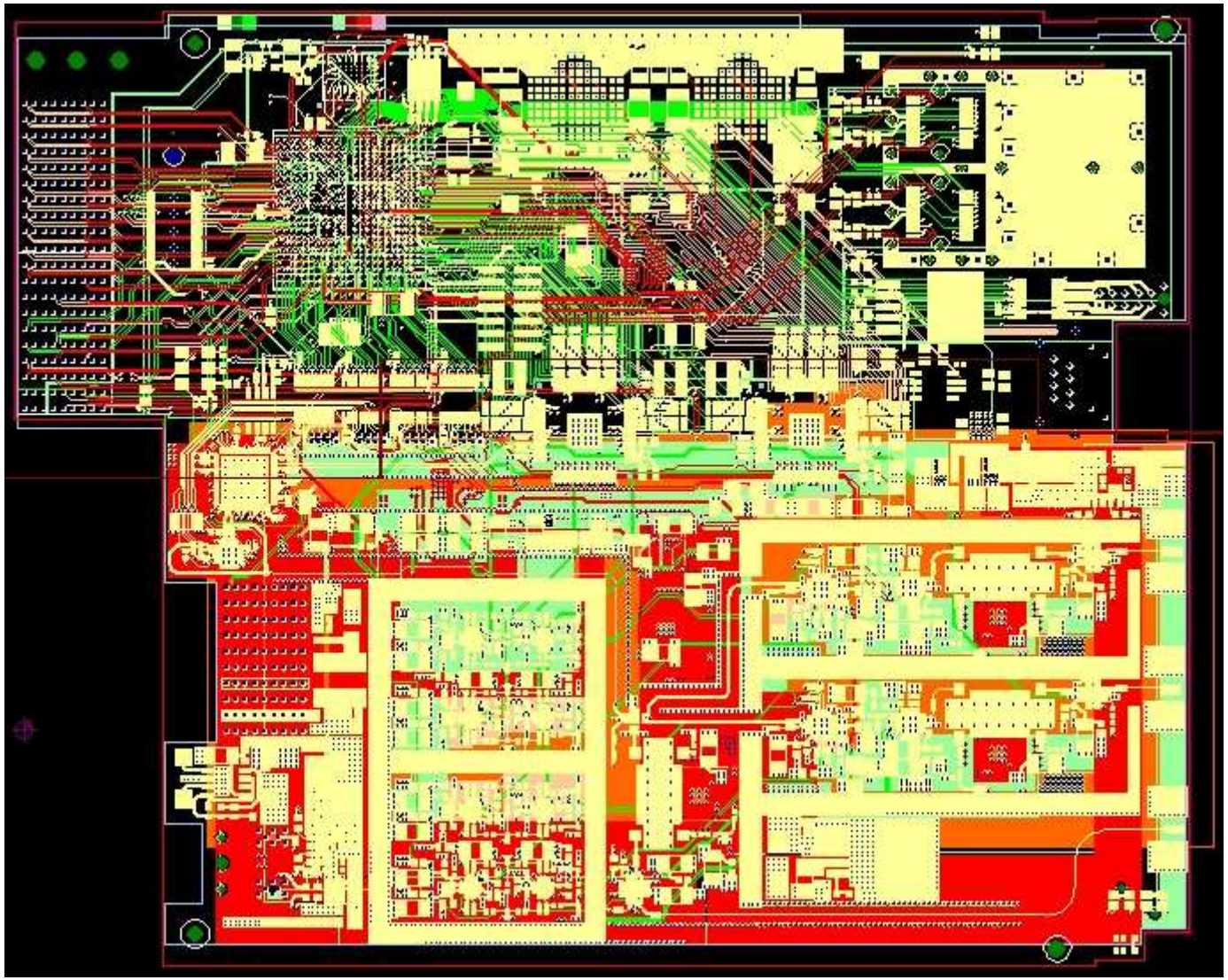
# uRTM Vector Modulator

- Designed for modulation of the klystron input signal
- Driven directly from AMC digital controller and compatible with the RF Backplane distribution
- Assumed minimum front panel connections
- Two-channel device
- Operation frequency range of 216 MHz to 3.9 GHz (for various applications in the machine)
- Prototype was successfully tested during first 12 months for the ATCA based LLRF system

# RTM Vector Modulator Concept



# RTM Vector Modulator – project status



- 10-layer board
- Last design stage
- Production expected in end of May 2011
- Deliverable 10.6.8

# Summary

- The RF Backplane is in last design stage. Proof of principle was done in the previous reporting period on the ATCA design prototypes
- The uRTM DWC was built and successfully tested. New revision is prepared to clean minor layout errors and increase functionality
- The uRTM Vector Modulator version is in preparation for production. Prototype was successfully tested in 2009/2011

Thank You for attention!