EuCard

Firmware Development for xTCA based LLRF System at FLASH

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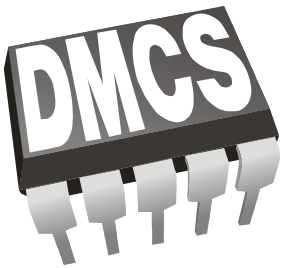

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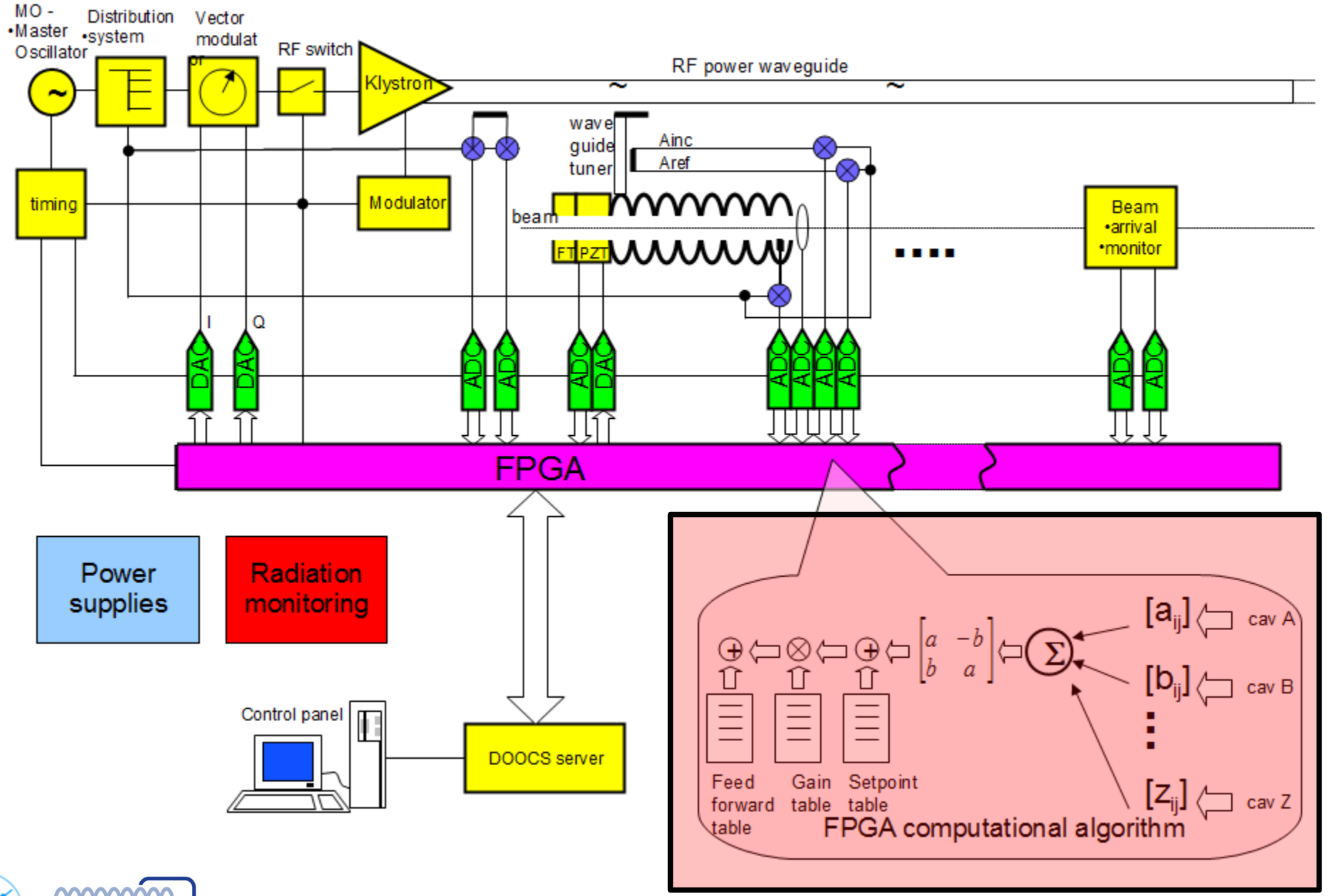
Agenda

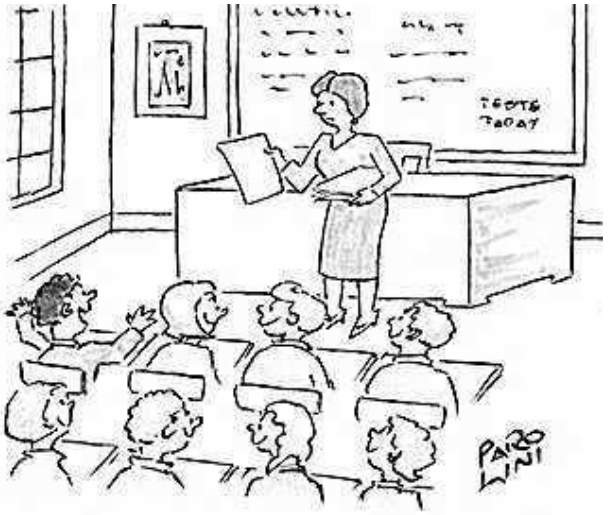
1. Introduction
2. Implemented firmware modules
3. Requirements of VME vs uTCA
4. Migration to uTCA
5. Optimization
6. Current Status
7. Summary

Introduction



Introduction

- Several years of work on LLRF system firmware
- VME based LLRF system @ FLASH
- Development of xTCA based LLRF system
- New system = new challenges



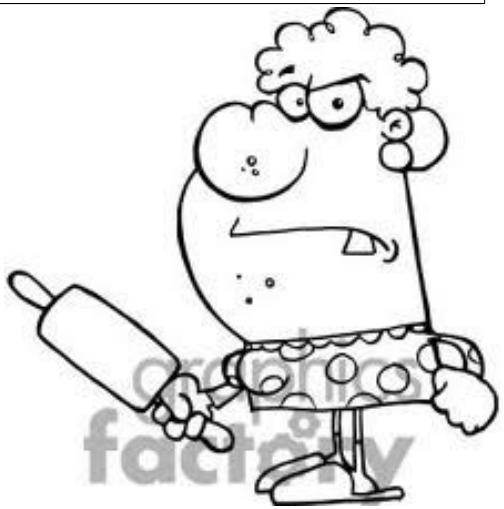
Implemented firmware modules

- Basic RF control
  - feedforward
  - feedback
  - data acquisition/communication
- Beam based feedback
- Machine protection system interface
- Status monitoring
- Communication links

Requirements of VME vs uTCA

aspect	VME	xTCA	differs in
architecture	centralized	distributed	latency,resources, bandwidth,distribution
communication	VME bus	PCIe, GBe	complexity, error protection
components	< 2005	NOW	technology, max frequency
FLASH needs	on the limit	new possibilities	

To boldly go where no man has gone before



Migration to uTCA

- Porting of the modules to the new hardware
- Communication protocols implementation
- Algorithm and resource distribution
- Redundancy (which modules, where)
- Flow control (event dispatching, interactions)
- Lab tests (cavity simulator)
- FLASH tests

Current Status/Future

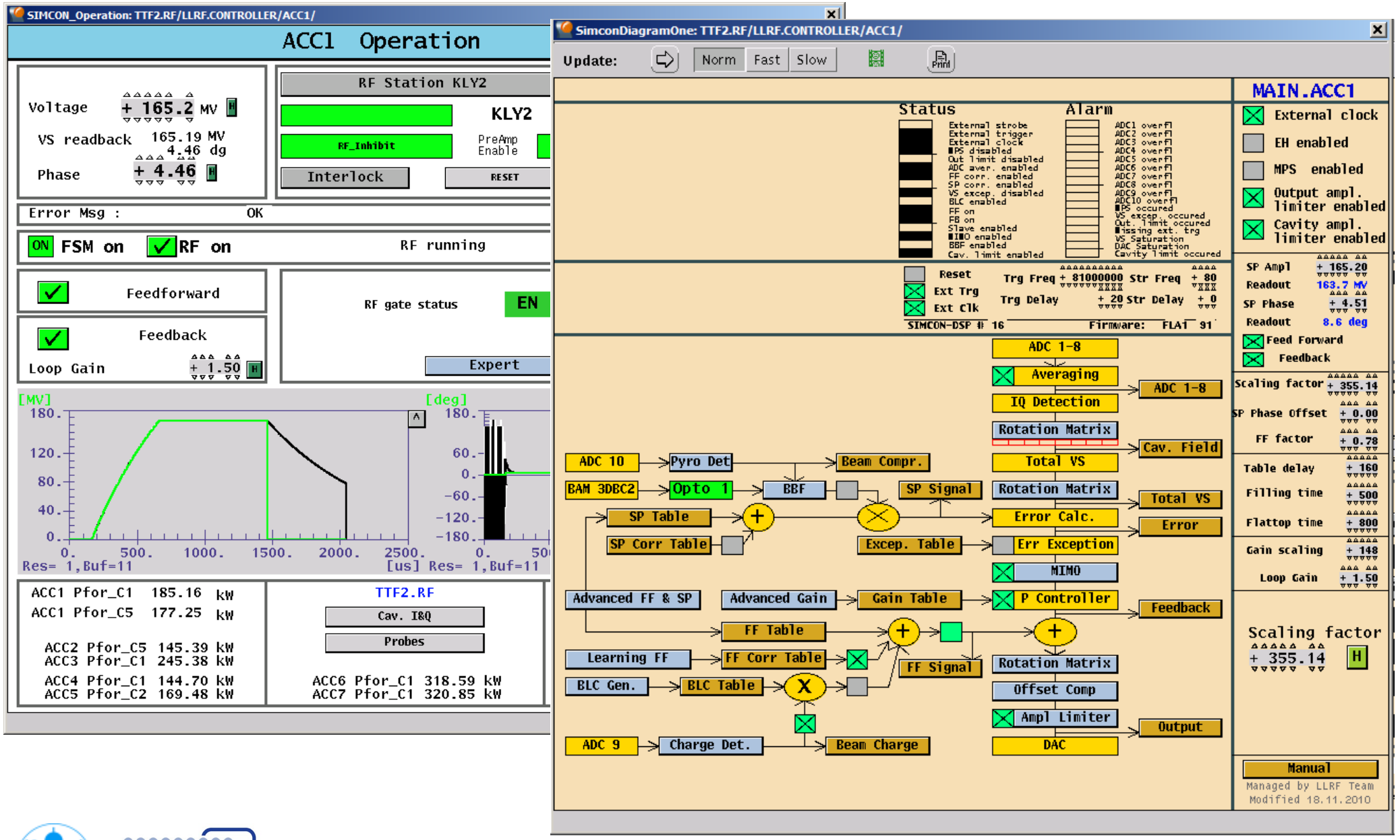
- Initial algorithm distribution has been done
- PCIe and Gbe modules implemented
- Low Latency Link Modules implemented
- First test of ATCA based system have been done

- **Add functionality**
- **Optimization of the firmware**

Optimization

- **Modules** – adjustment of implemented modules to accommodate new features available in FPGA (faster arithmetic units, serdes blocks, dedicated logic etc.)
- **Distribution** – after initial tests adjustment of the structure should be done
- **Flow control**

Summary


SIMCON_Operation: TTF2.RF/LLRF.CONTROLLER/ACC1/
ACC1 Operation
Voltage + 165.2 MV
VS readback 165.19 MV
4.46 dg
Phase + 4.46
RF Station KLY2
KLY2
RF_Inhibit
PreAmp Enable
Interlock
RESET
Error Msg : OK
ON FSM on
RF on
RF running
Feedforward
Feedback
Loop Gain + 1.50
RF gate status
EN
Expert
[MV]
[deg]
Res= 1,Buf=11
[us] Res= 1,Buf=11
ACC1 Pfor_C1 185.16 kW
ACC1 Pfor_C5 177.25 kW
ACC2 Pfor_C5 145.39 kW
ACC3 Pfor_C1 245.38 kW
ACC4 Pfor_C1 144.70 kW
ACC5 Pfor_C2 169.48 kW
TTF2.RF
Cav. I&Q
Probes
ACC6 Pfor_C1 318.59 kW
ACC7 Pfor_C1 320.85 kW
SimconDiagramOne: TTF2.RF/LLRF.CONTROLLER/ACC1/
Update:
Norm
Fast
Slow
Print
Status
Alarm
Reset
Ext Trg
Ext Clk
Trg Freq + 81000000
Str Freq + 80
Trg Delay + 20
Str Delay + 0
SIMCON-DSP 4F 16
Firmware: FLA1 91
ADC 1-8
Averaging
IQ Detection
Rotation Matrix
Cav. Field
Total VS
Error
ADC 10
Pyro Det
Beam Compr.
BAM 3DBC2
Opto 1
BBF
SP Signal
SP Table
SP Corr Table
Excep. Table
Err Exception
MIMO
Advanced FF & SP
Advanced Gain
Gain Table
P Controller
Feedback
FF Table
Learning FF
FF Corr Table
FF Signal
BLC Gen.
BLC Table
Offset Comp
Ampl Limiter
Output
ADC 9
Charge Det.
Beam Charge
DAC
MAIN.ACC1
External clock
EH enabled
MPS enabled
Output ampl. limiter enabled
Cavity ampl. limiter enabled
SP Ampl + 165.20
Readout 163.7 MV
SP Phase + 4.51
Readout 8.6 deg
Feed Forward
Feedback
Scaling factor + 355.14
SP Phase Offset + 0.00
FF factor + 0.78
Table delay + 160
Filling time + 500
Flattop time + 800
Gain scaling + 148
Loop Gain + 1.50
Scaling factor
+ 355.14
H
Manual
Managed by LLRF Team
Modified 18.11.2010