# Innovative approach to modern readout system development

- Design of DAQ using SciCompiler and Open FPGA.
- FERS-5200: a distributed Front-End Readout System for multidetector arrays.

CAEN Tools for Discovery

*A. Abba, C.Tintori, F. Caponio, A. Cusimano, L.Ferrentino,*
*V.Arosio, Y. Venturini,*
*L. Colombini, T. Masini, G. Cerretani*

NI Nuclear Instruments

# SCI-COMPILER

Scientific Firmware Compiler

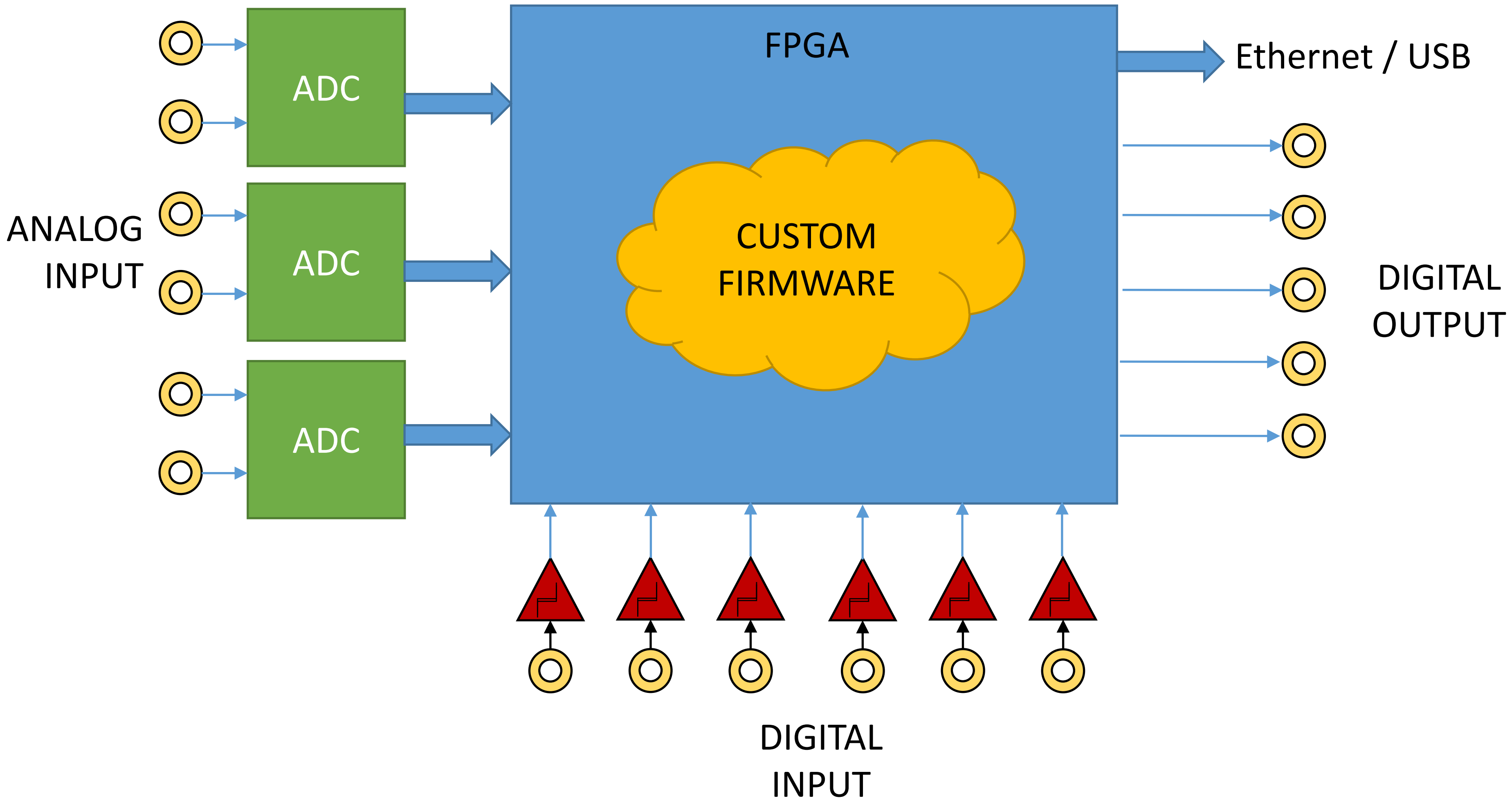
designed for CAEN digital acquisition systems

CAEN
*Tools for Discovery*

Nuclear Instruments

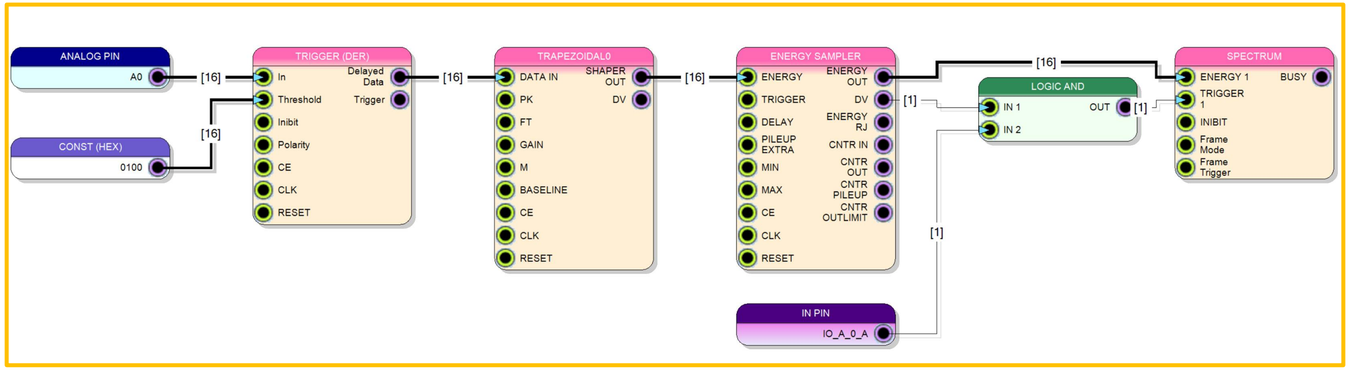
# Modular Electronics readout systems

# Replace modular Electronics with FPGA

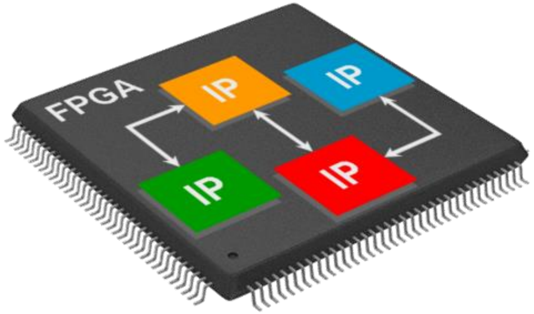


# CAEN Solution: OpenFPGA digitizers + SciCompiler firmware generator

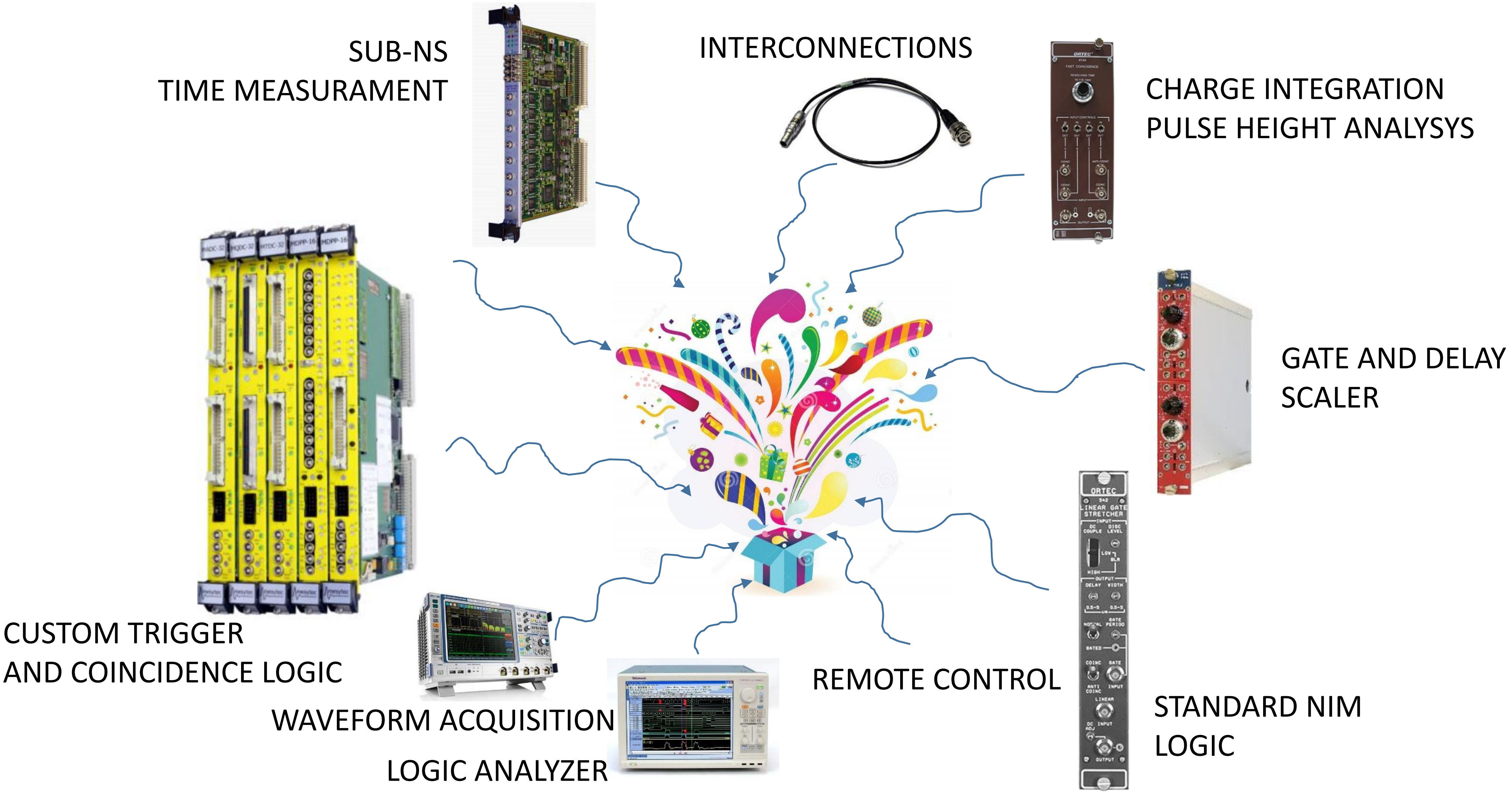

OpenFPGA Digitizers



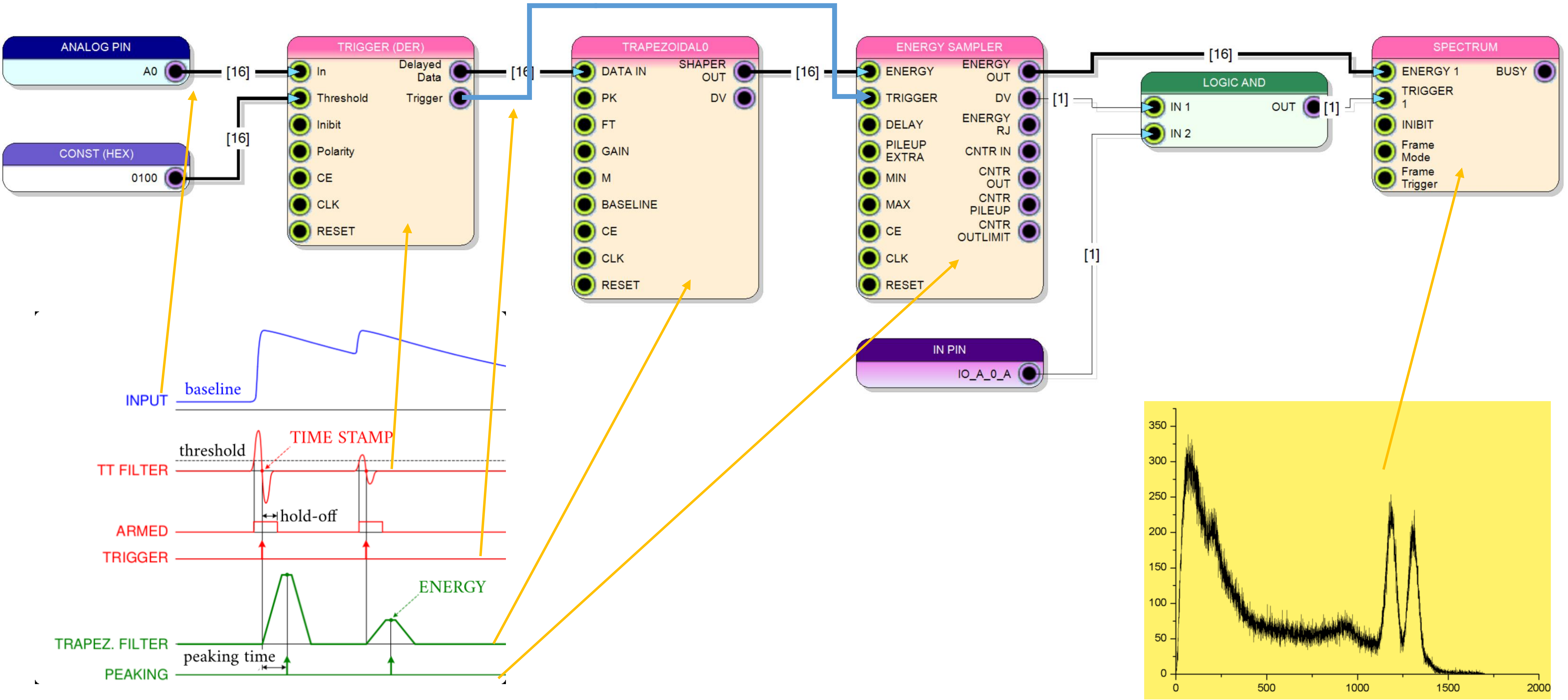

SCI-COMPILER



# Real Time FPGA processing without VHDL

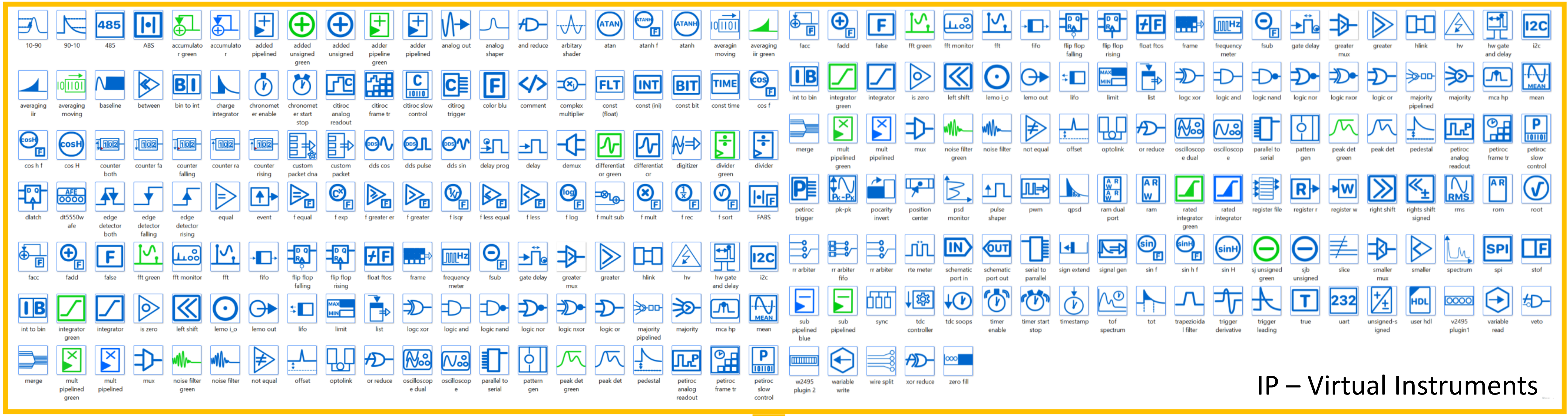


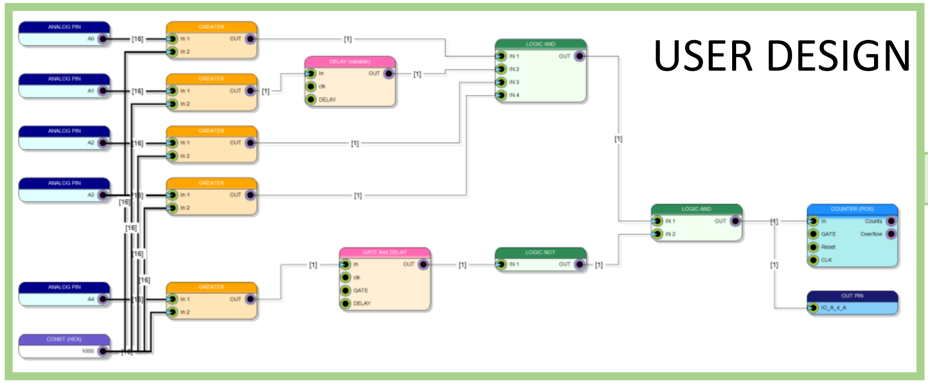
# Implementation of PHA

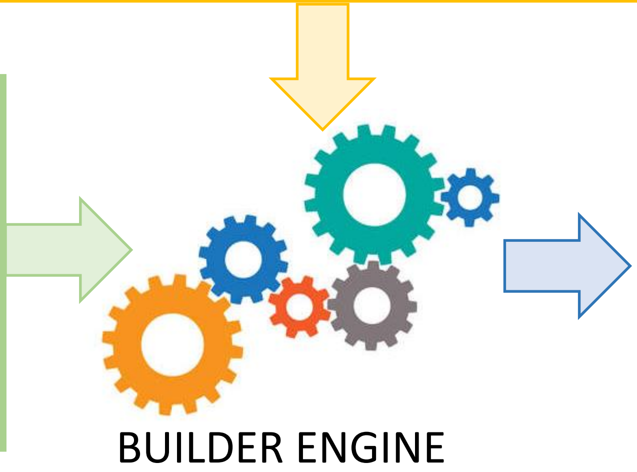


# All hardware devices in a single software

# SciCompiler: ip integrator software



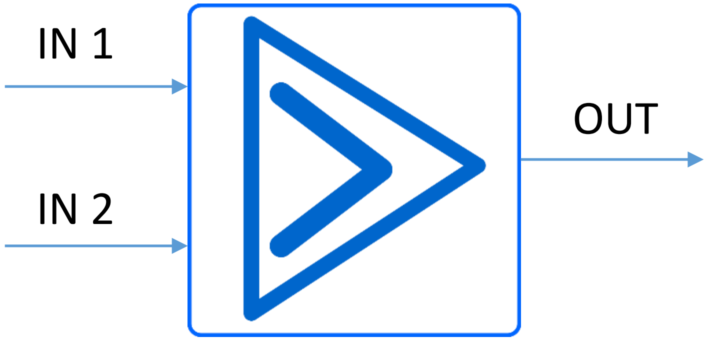




```
architecture Counter_Arch of AAC2M2P1 is begin

  count_proc : process(CP,SR,PE,CEP,CET) begin
    if (SR='0') then Q <= "0000";
    elsif rising_edge(CP) then
      if PE = '0' then Q <= P; --Load
      elsif CET = '1' and CEP = '1' then Q <= Q+1; -- count
      end if;
      if CET = '1' and Q = "1111" then TC <= '1'; -- Terminal count
      else TC <= '0';

      end if;
    end if;
  end process count_proc;
```

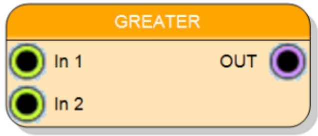

www.scicompiler.cloud

# What is an IP

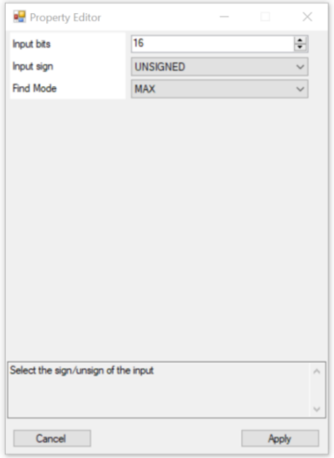
## SYMBOL




## COMPONENT




## PROPERTY WINDOW

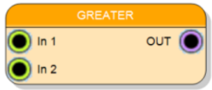



## GUIDE

**Greater**

Components ›› Comparator ››

V2495 DT5550




The block implements a digital comparator that determines if the first input is greater than the second input. The comparison between the two inputs, which are two vectors of the same size representing numbers expressed in binary notation, is done bit by bit starting from the MSB and proceeding towards the LSB. When an inequality between two bits is found, if the considered bit of the first input vector is 1 and the correspondent bit of the second input vector is 0 it means that the first number is greater than the second. In this case the output of the block is a 1, otherwise it is a 0, meaning that the first input number is smaller than the second input number.

| **In 1** | VECT | Size: 1...32 |
|---|---|---|

*First Input signal*

| **In 2** | VECT | Size: 1...32 |
|---|---|---|

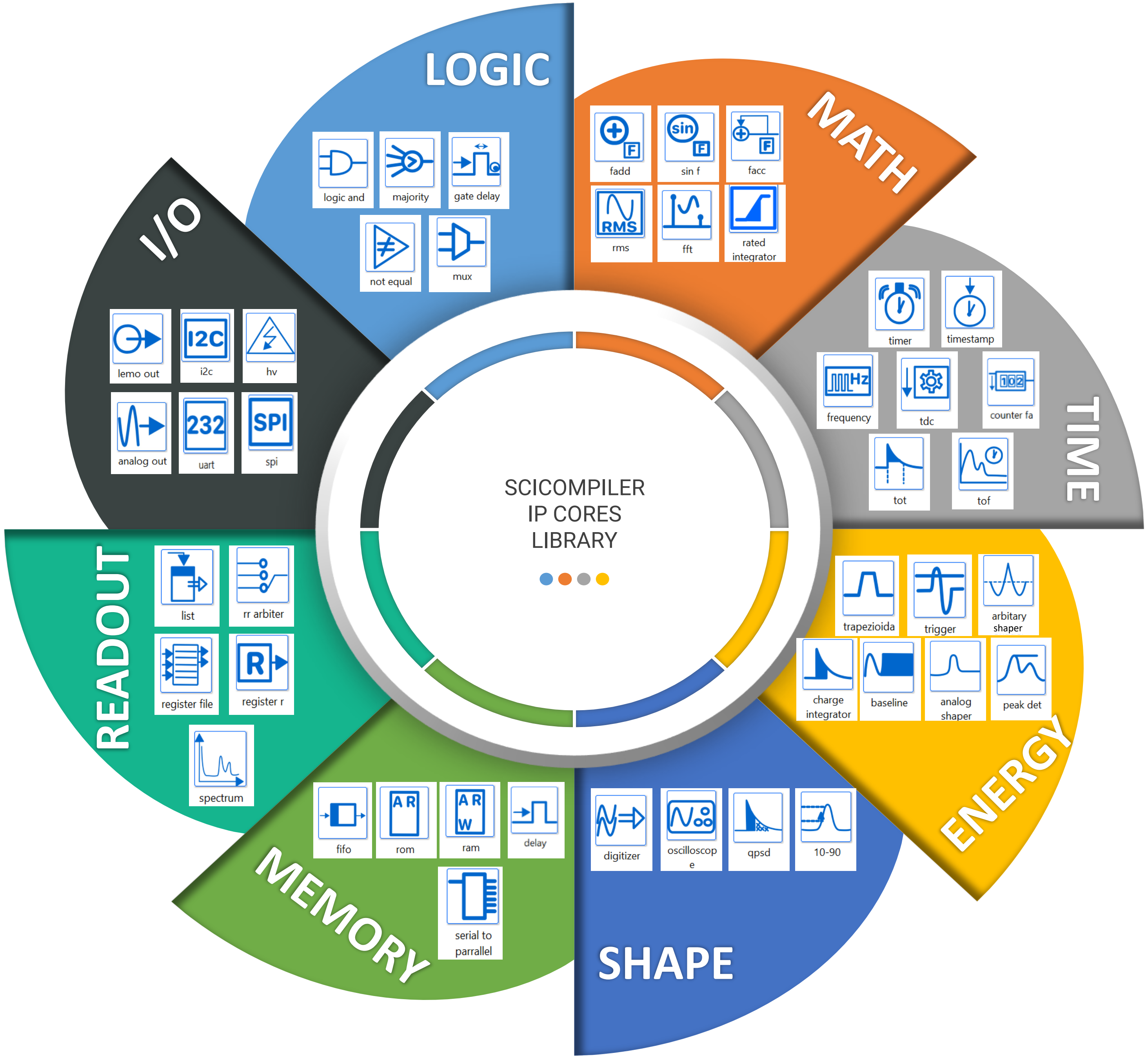
*Second Input signal*

| **OUT** | VECT | Size: 1 |
|---|---|---|

*Output signal consisting of a 1 if the first input is greater than the second, in a 0 otherwise*

## IMPLEMENTATION

```
entity comparator is
    Generic (IN_SIZE : integer := 16;
             OPERATION : STRING := "equal";
             IN_SIGN : STRING := "signed";
             REGISTER_OUT : STRING := "true"
             );
    Port ( in1 : in STD_LOGIC_VECTOR (IN_SIZE-1 downto 0);
           in2 : in STD_LOGIC_VECTOR (IN_SIZE-1 downto 0);
           clk : in STD_LOGIC;
           comp_out : out STD_LOGIC);
end comparator;

architecture Behavioral of comparator is
signal i_out : std_logic := '0';
begin

IF_equal:
   if OPERATION = "equal" generate
      begin
         i_out <= '1' when in1=in2 else '0';
   end generate;


IF_notequal:
   if OPERATION = "not_equal" generate
      begin
         i_out <= '0' when in1=in2 else '1';
   end generate;
```

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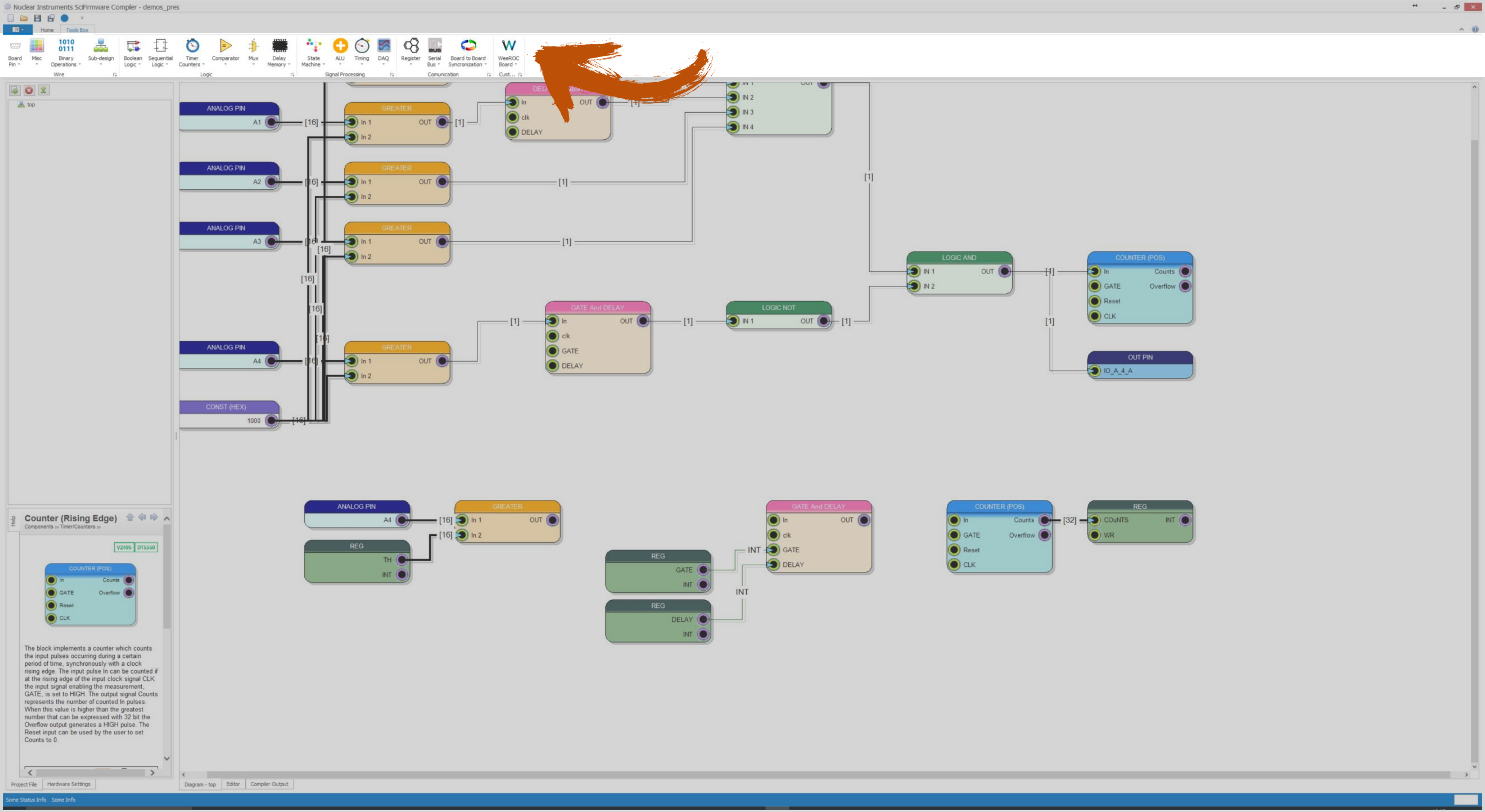
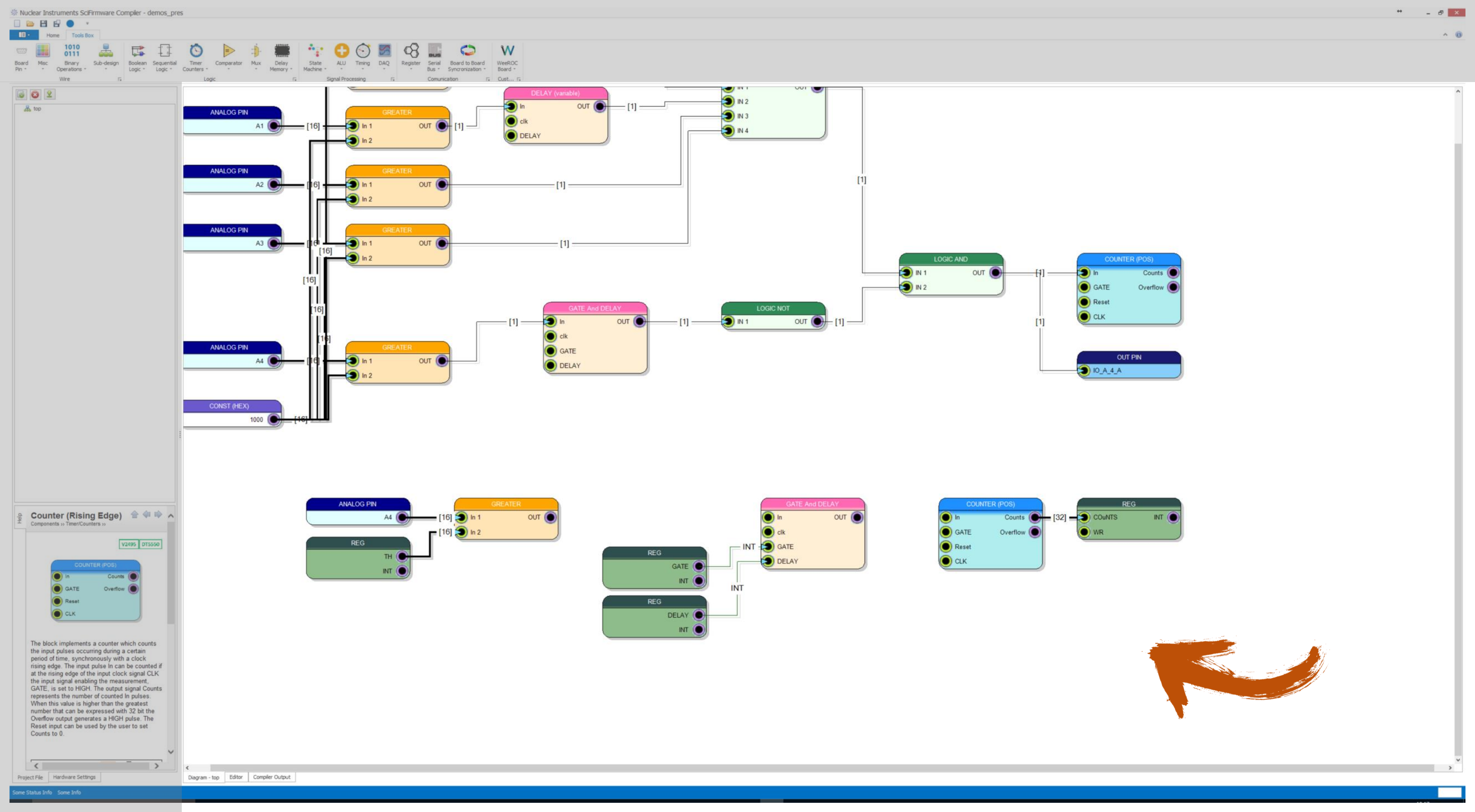

Nuclear Instruments SciFirmware Compiler - demos_pres
Home
Tools Box
Board Pin
Misc
1010 0111
Binary Operations
Sub-design
Wire
Boolean Logic
Sequential Logic
Timer Counters
Comparator
Mux
Delay Memory
Logic
State Machine
ALU
Timing
DAQ
Signal Processing
Register
Serial Bus
Board to Board Syncronization
Comunication
WeeROC Board
Cust...
top
ANALOG PIN
A1
A2
A3
A4
GREATER
In 1
In 2
OUT
CONST (HEX)
1000
[16]
[1]
In
clk
DELAY
GATE
IN 2
IN 3
IN 4
GATE And DELAY
LOGIC NOT
IN 1
LOGIC AND
COUNTER (POS)
Counts
Overflow
Reset
CLK
OUT PIN
IO_A_4_A
REG
TH
INT
[32]
COuNTS
WR
Counter (Rising Edge)
Components » Timer/Counters »
V2495
DT5550
The block implements a counter which counts the input pulses occurring during a certain period of time, synchronously with a clock rising edge. The input pulse In can be counted if at the rising edge of the input clock signal CLK the input signal enabling the measurement, GATE, is set to HIGH. The output signal Counts represents the number of counted In pulses. When this value is higher than the greatest number that can be expressed with 32 bit the Overflow output generates a HIGH pulse. The Reset input can be used by the user to set Counts to 0.
Project File
Hardware Settings
Diagram - top
Editor
Compiler Output
Some Status Info
Some Info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Home
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Binary Operations
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top
ANALOG PIN
A1
A2
A3
A4
CONST (HEX)
1000
GREATER
In 1
In 2
OUT
DELAY (variable)
In
clk
DELAY
IN 2
IN 3
IN 4
GATE And DELAY
GATE
LOGIC NOT
IN 1
LOGIC AND
COUNTER (POS)
Counts
Overflow
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OUT PIN
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Hardware Settings
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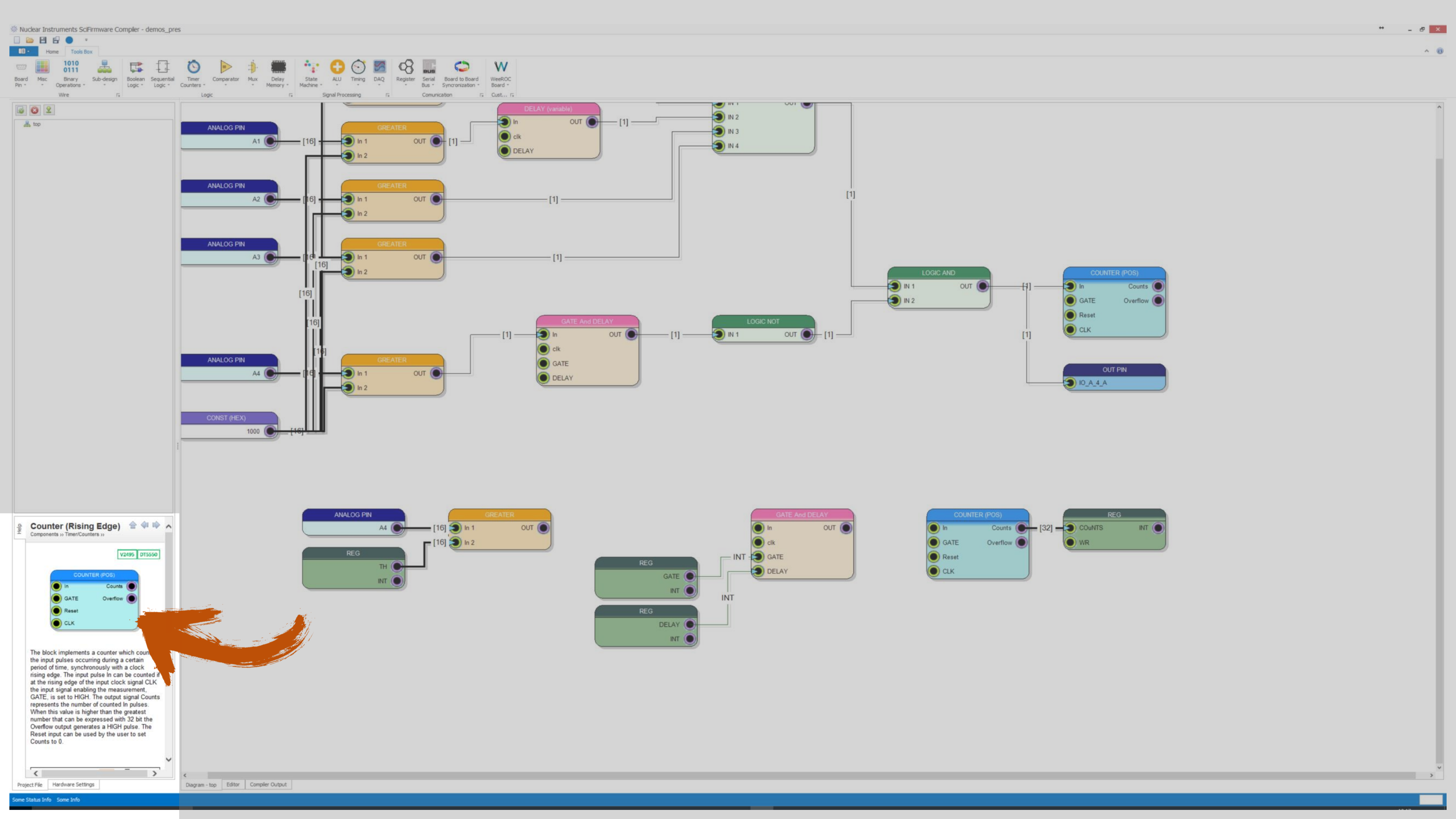
Editor
Compiler Output
Some Status Info
Some Info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Home
Tools Box
Counter (Rising Edge)
Components ›› Timer/Counters ››
V2495
DT5550
COUNTER (POS)
In
Counts
GATE
Overflow
Reset
CLK
The block implements a counter which coun
the input pulses occurring during a certain
period of time, synchronously with a clock
rising edge. The input pulse In can be counted if
at the rising edge of the input clock signal CLK
the input signal enabling the measurement,
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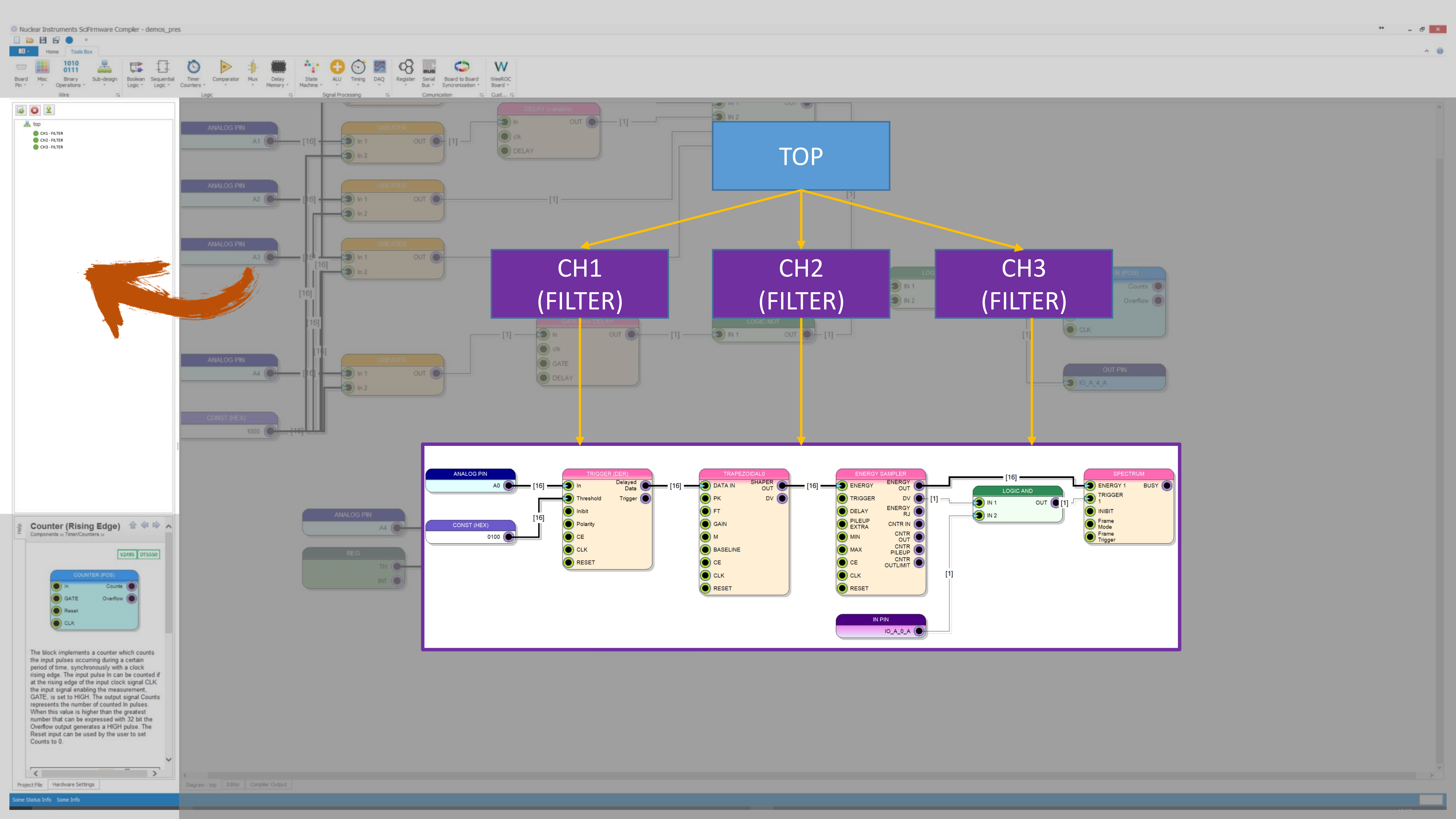
Counts to 0.
Project File
Hardware Settings
ANALOG PIN
GREATER
DELAY (variable)
GATE And DELAY
LOGIC NOT
LOGIC AND
COUNTER (POS)
OUT PIN
IO_A_4_A
CONST (HEX)
1000
REG
Diagram - top
Editor
Compiler Output
Some Status Info
Some Info


Nuclear Instruments SciFirmware Compiler - demos_pres
Home
Tools Box
top
CH1 - FILTER
CH2 - FILTER
CH3 - FILTER
TOP
CH1
(FILTER)
CH2
(FILTER)
CH3
(FILTER)
ANALOG PIN
CONST (HEX)
TRIGGER (DER)
TRAPEZOIDAL0
ENERGY SAMPLER
LOGIC AND
SPECTRUM
IN PIN
Counter (Rising Edge)
COUNTER (POS)
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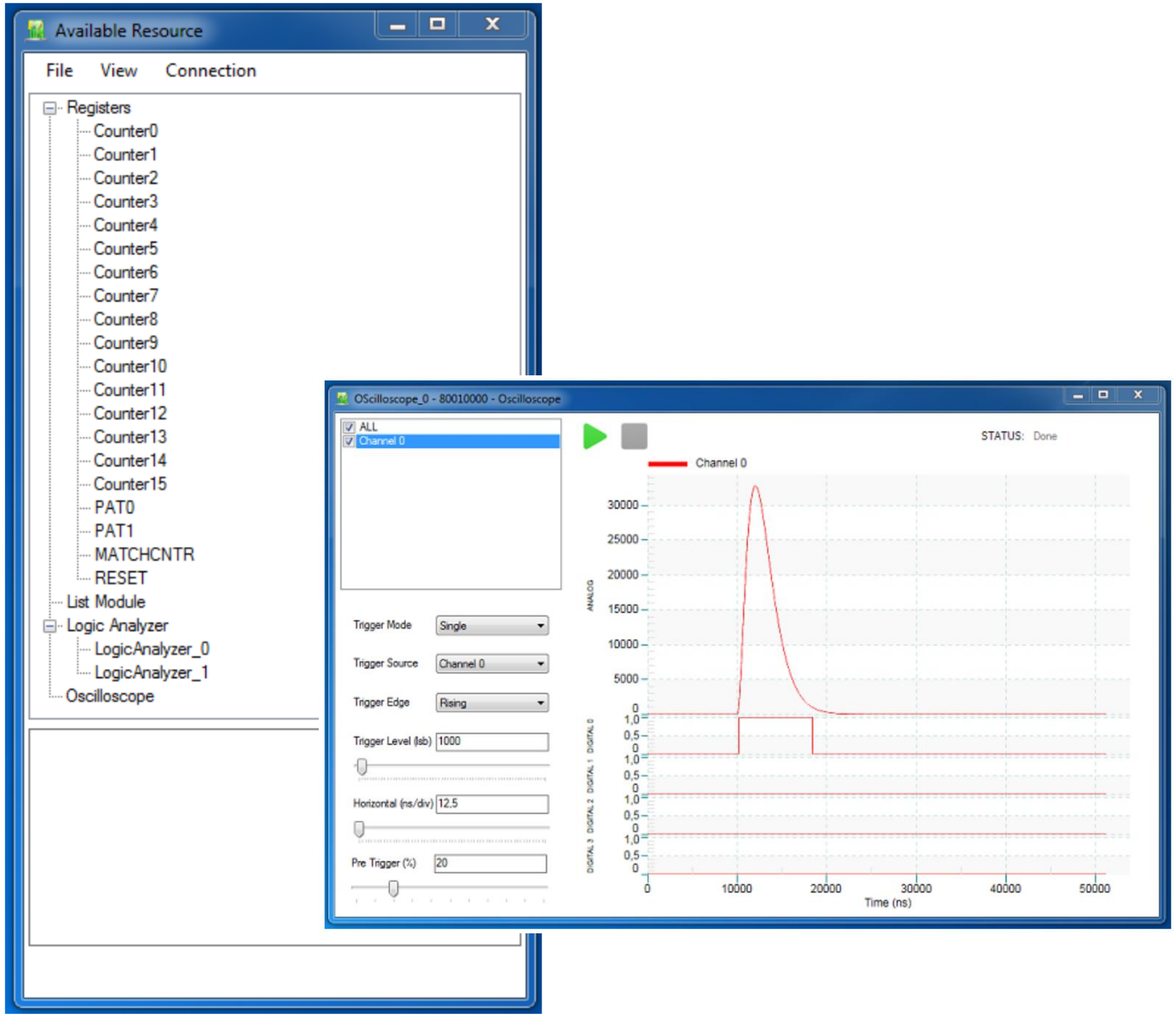
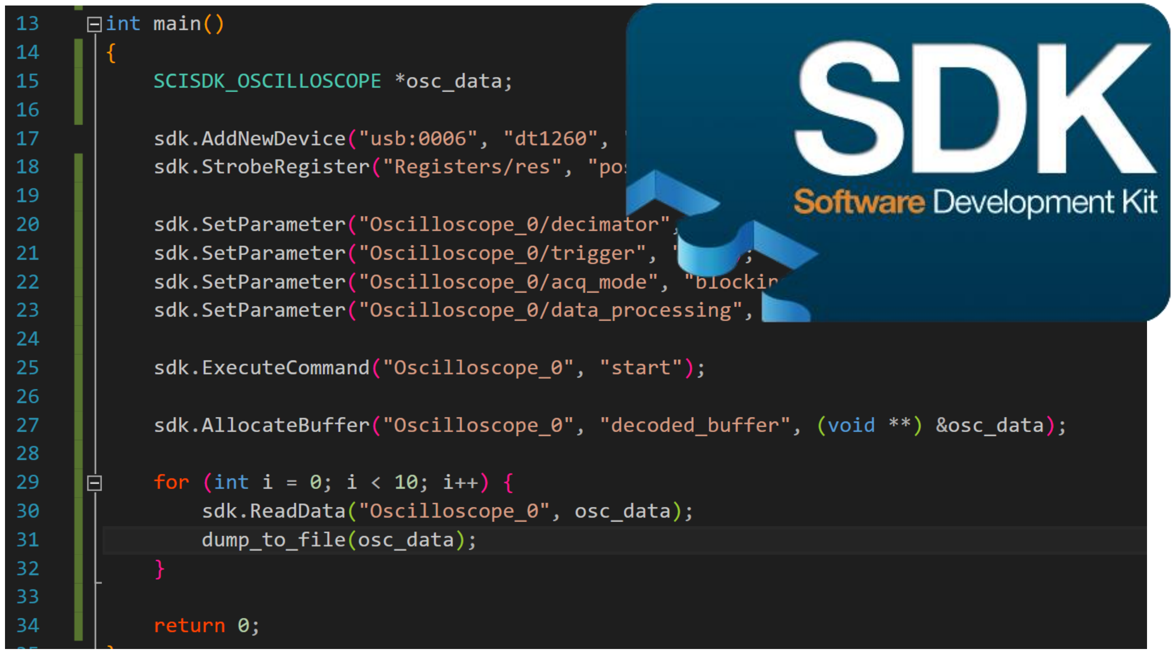
Project File
Hardware Settings
Some Status Info
Some Info

# Data readout – Resource explorer and SDK



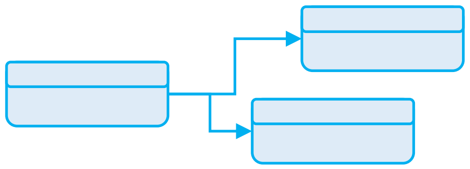




python™ VB.NET

# Resource Explorer Web Interface


www.scicompiler.cloud

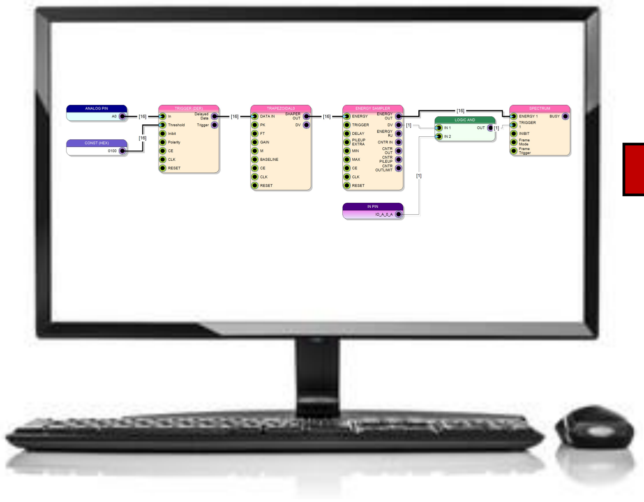
# Remote Compile Service based on MyCAEN Cloud

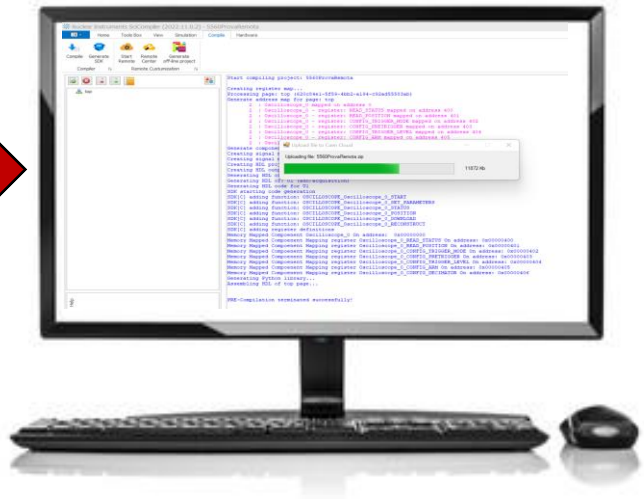


Design entry with SciCompiler

Upload project on the cloud

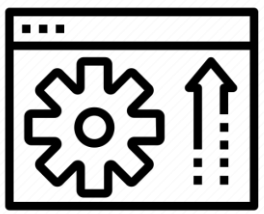
Remote Compile on MyCaen



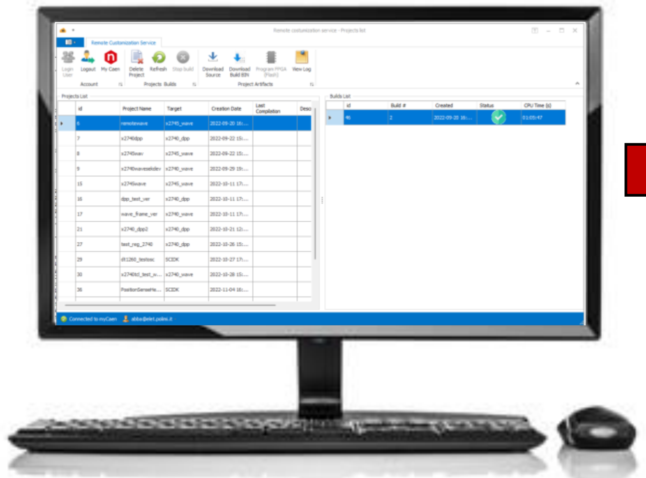


# Remote Compile Service based on MyCAEN Cloud

Download the firmware compiled

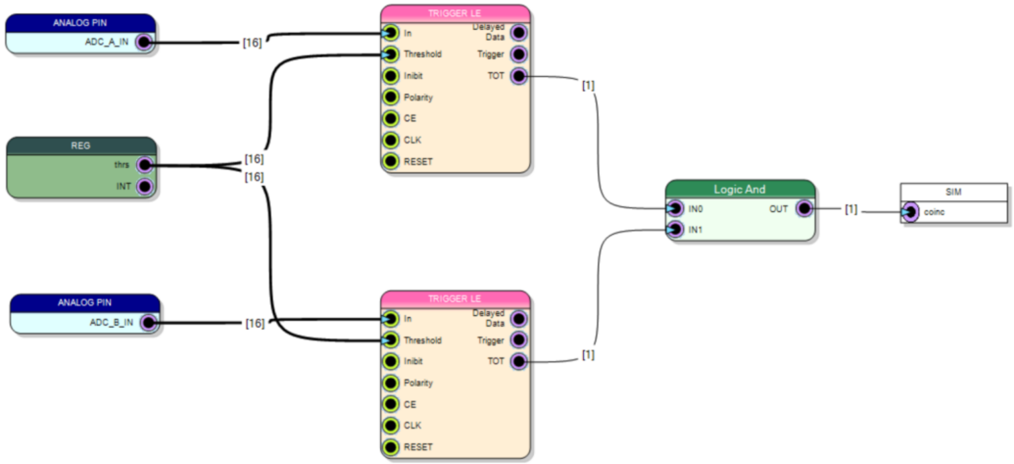


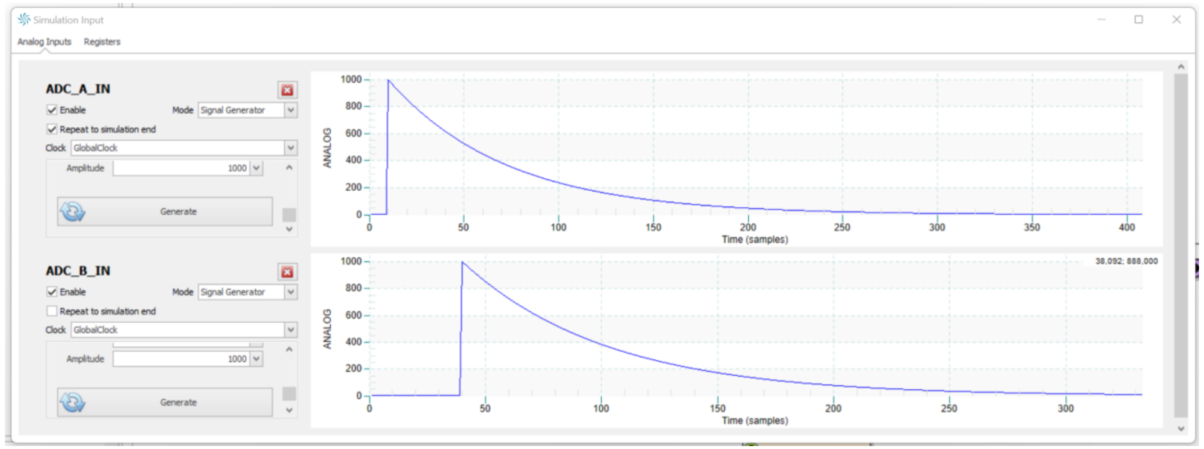
Install the firmware on the device



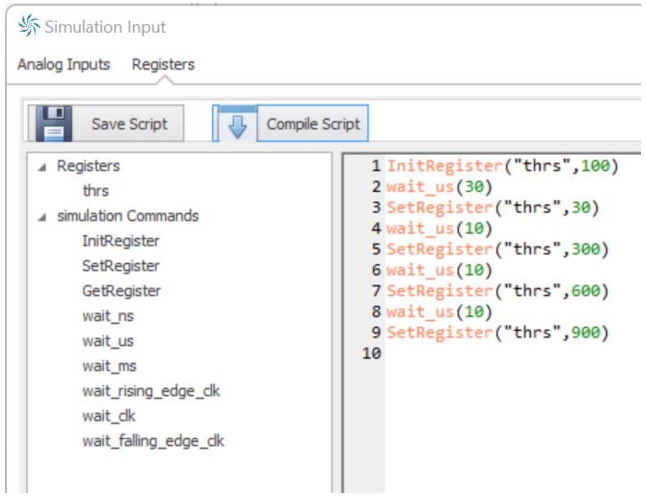

# Integrated simulation

- Save your time → Compile can require hours, simulation few seconds
- Simpler debug → You can inspect any net and signal
- Better test coverage → You can insert critical signal to check how firmware perform



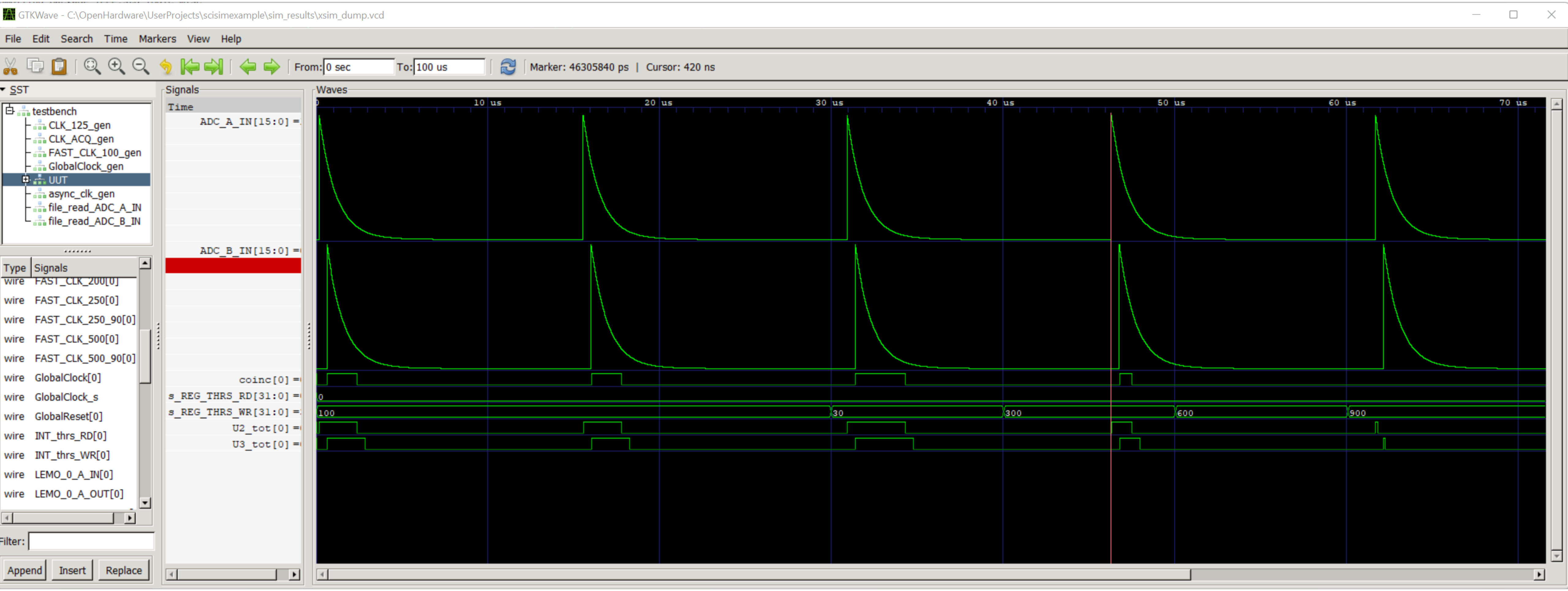




Generate analog signal to replace ADC data stream

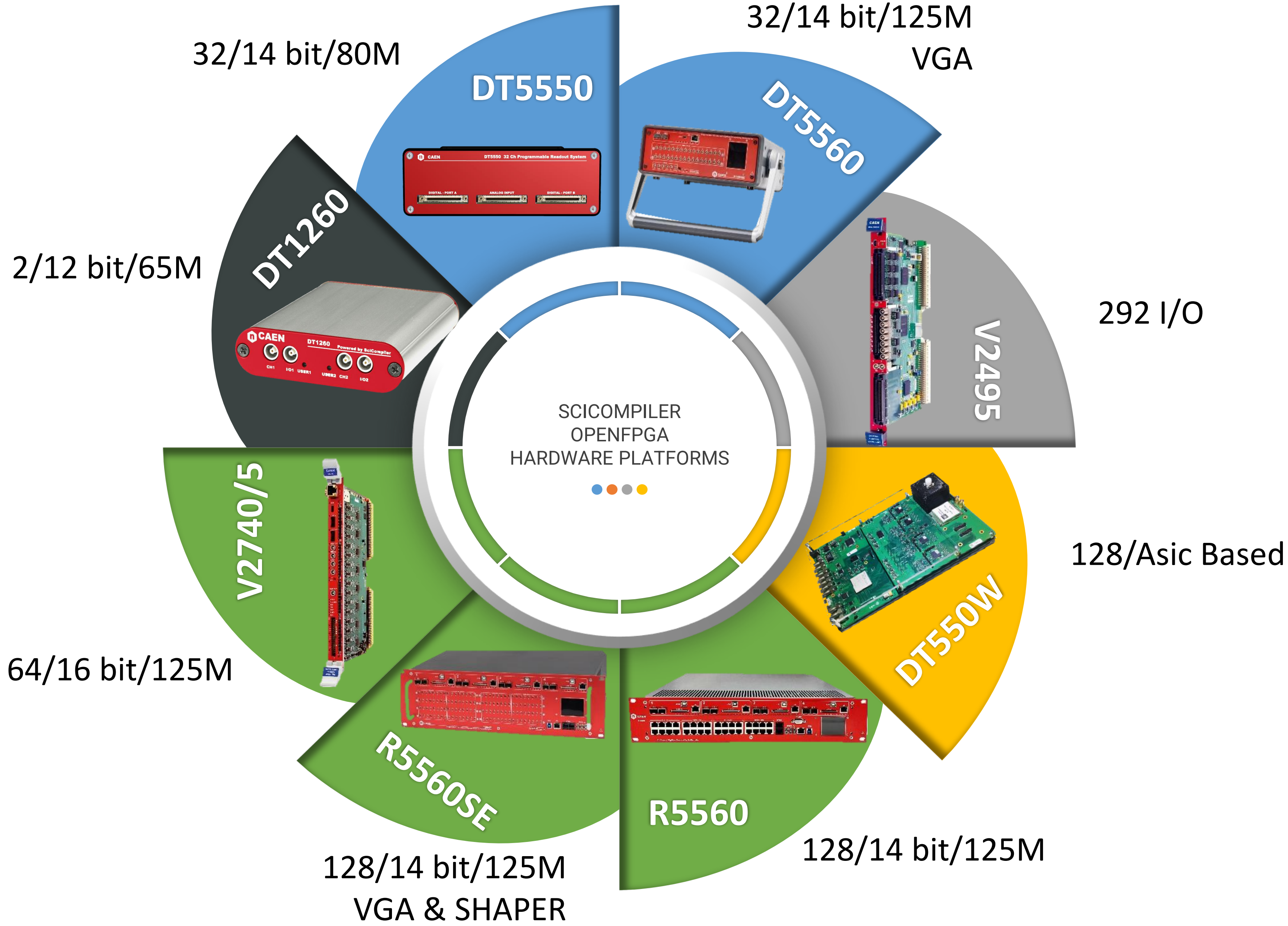



Write script to simulate Register RW

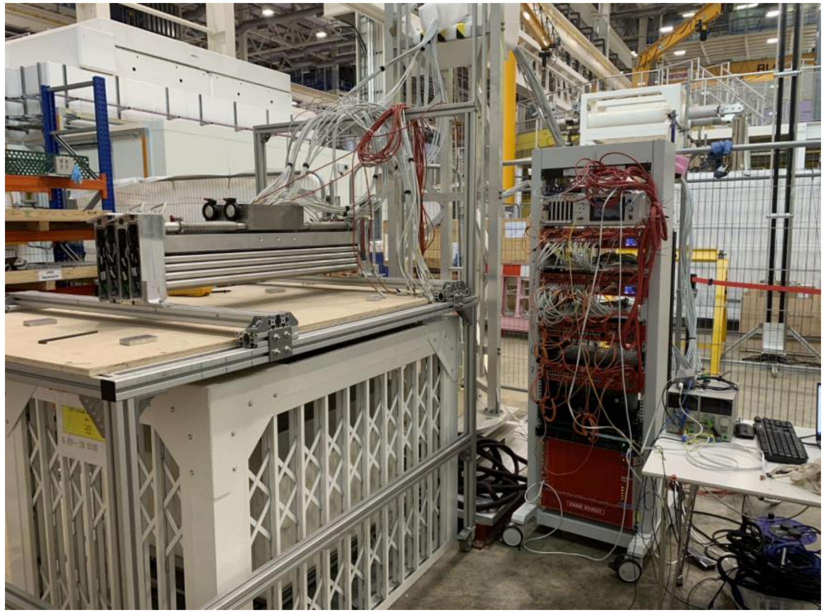
# Integrated simulation

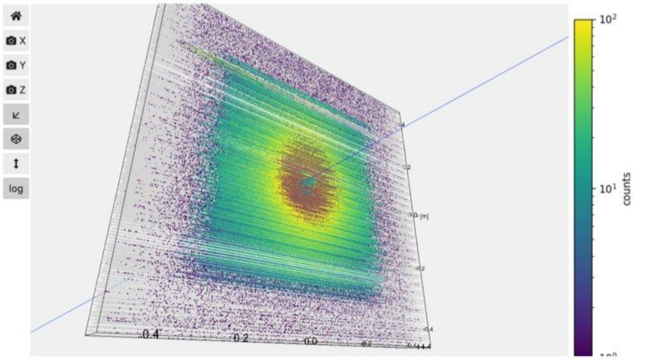


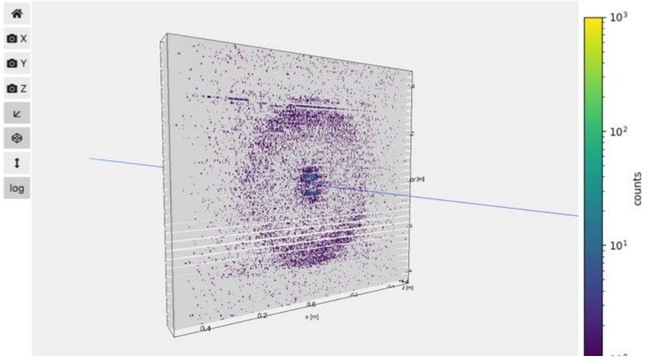

DT5550
DT5560
V2495
DT550W
R5560
R5560SE
V2740/5
DT1260
SCICOMPILER
OPENFPGA
HARDWARE PLATFORMS


SCICOMPILER
OPENFPGA
HARDWARE PLATFORMS
DT5550
32/14 bit/80M
DT5560
32/14 bit/125M
VGA
V2495
292 I/O
DT550W
128/Asic Based
R5560
128/14 bit/125M
R5560SE
128/14 bit/125M
VGA & SHAPER
V2740/5
64/16 bit/125M
DT1260
2/12 bit/65M

# ESS - LOKI SANS Readout – 2300 channels



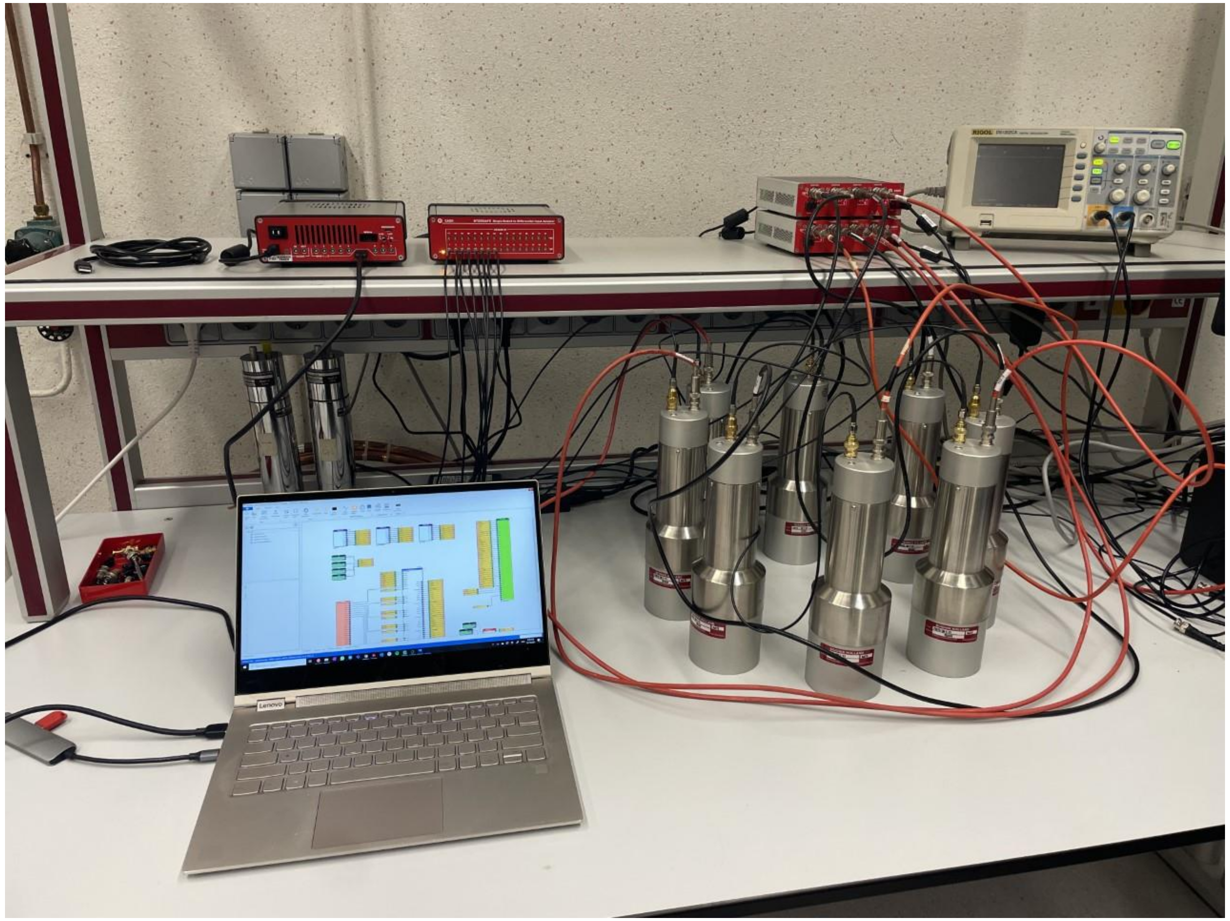




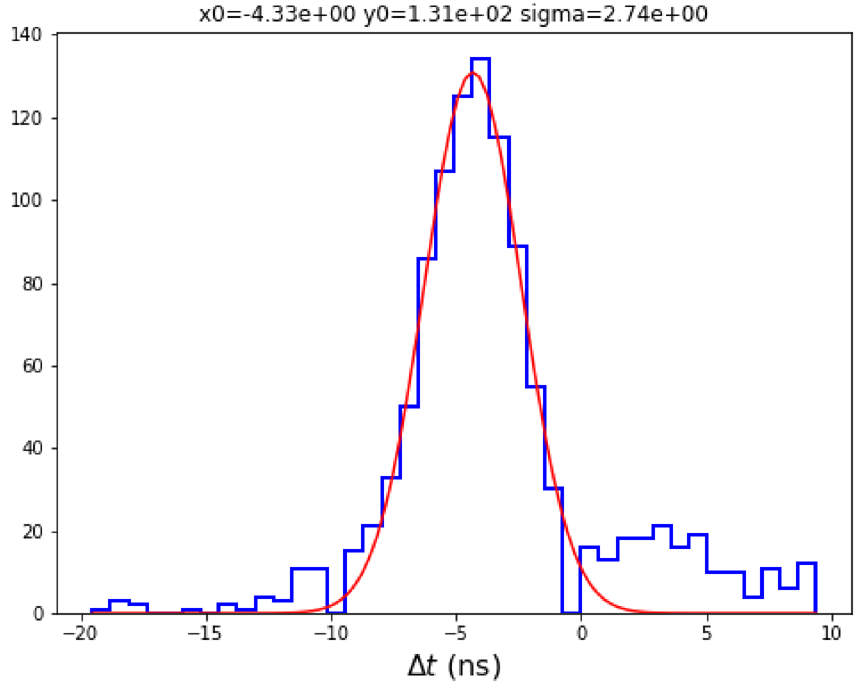
Real time processing from 2300 channels to readout straw tubes for LOKI experiment @ ESS.
ESS BIFROST, MIRACLES and VESPA are using R5560 and SciCompiler for readout

*Davide Raspino - ISIS*

# Sub-ns Time of flight measurament with DCFD



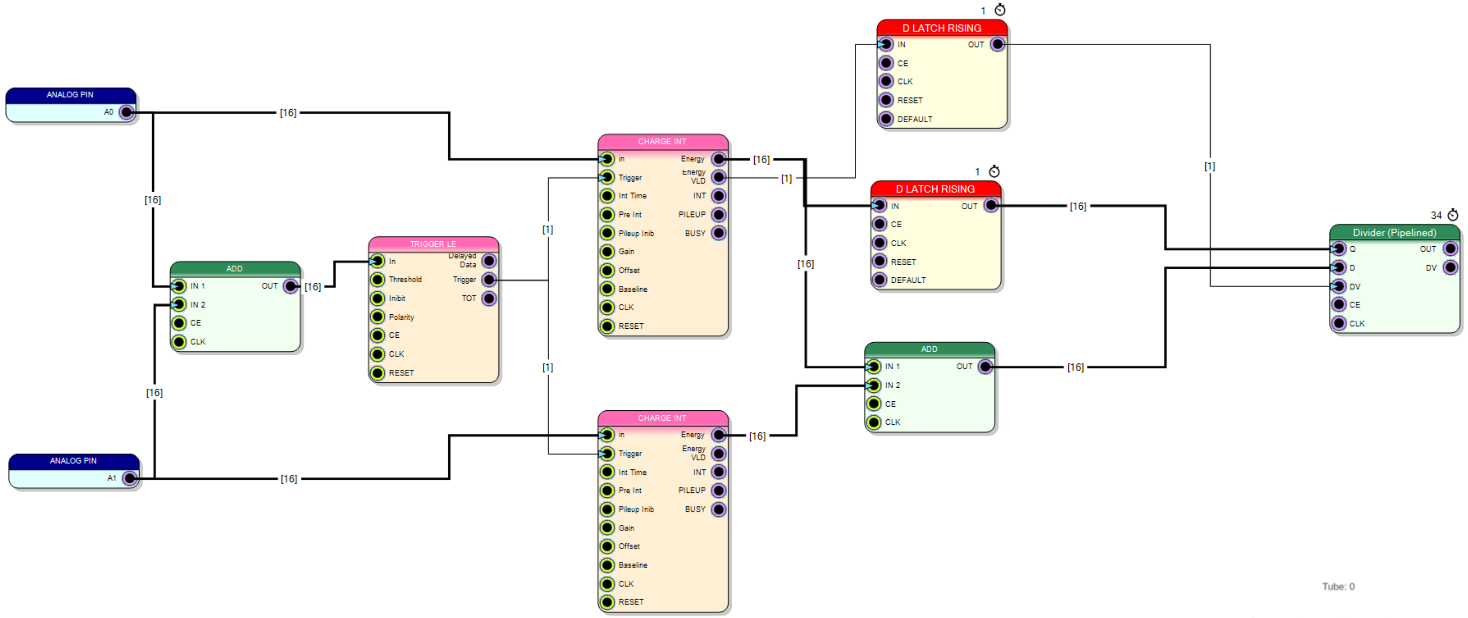
Sub-ns time of flight of correlated gamma measurement using DT5550, PMTs and a custom firmware developed using SciCompiler

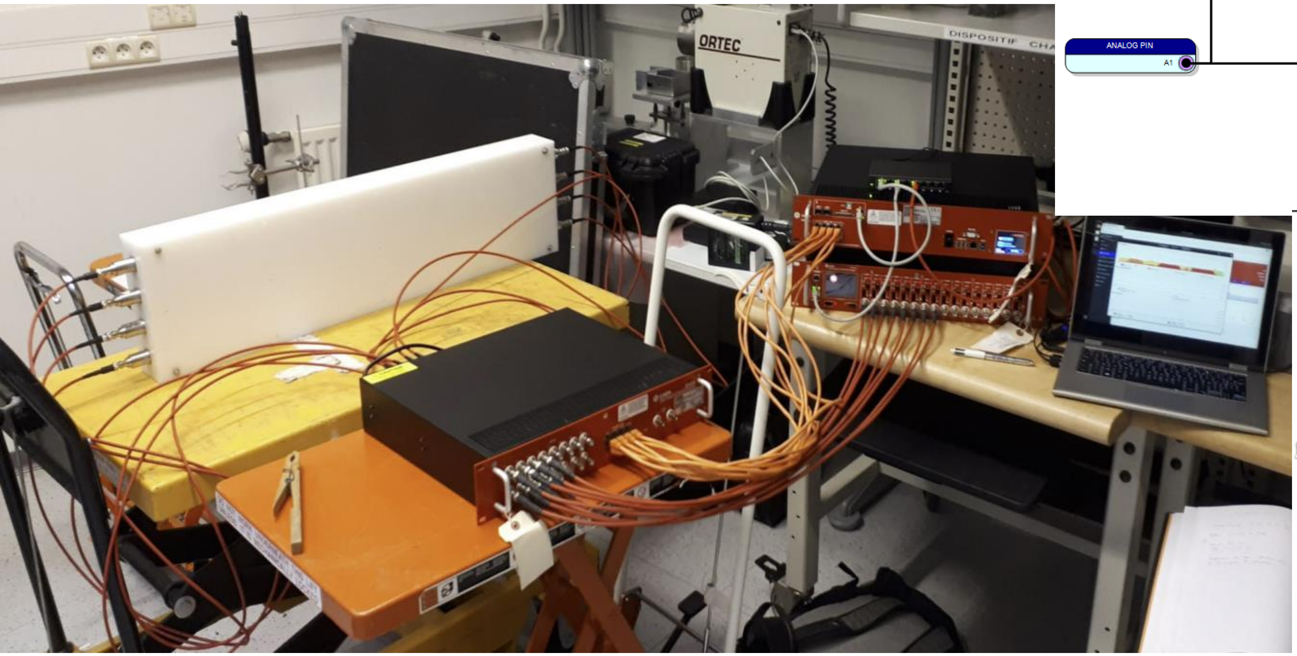


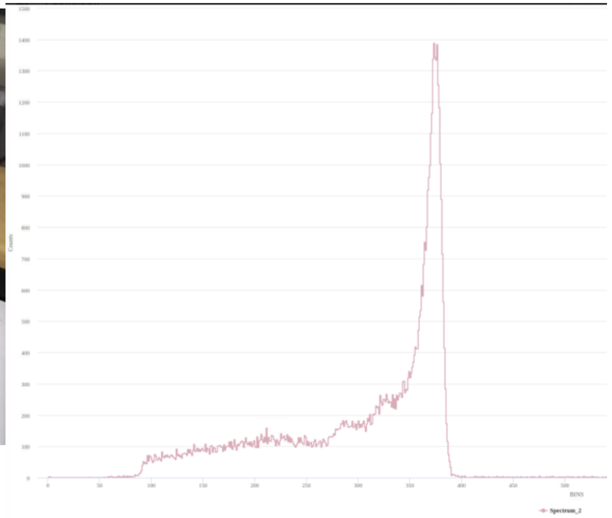

*Auke Colijn - Nikhef*

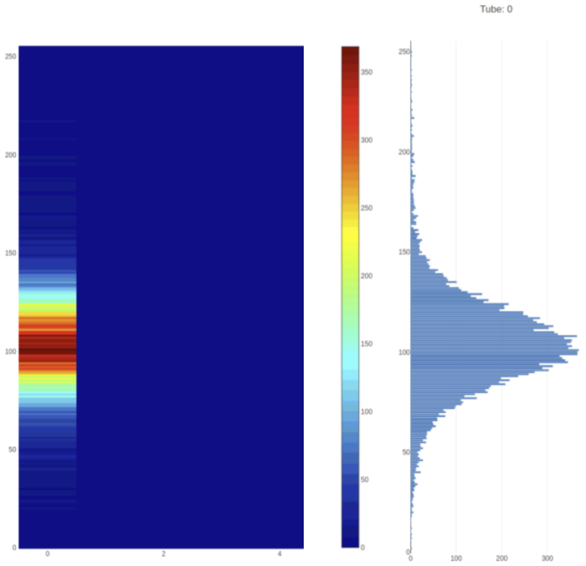
# Position sense He3 tube

Real time calculation of neutron interaction point using He3 tubes. 32 channels realtime center of mass and energy spectrum calculation.



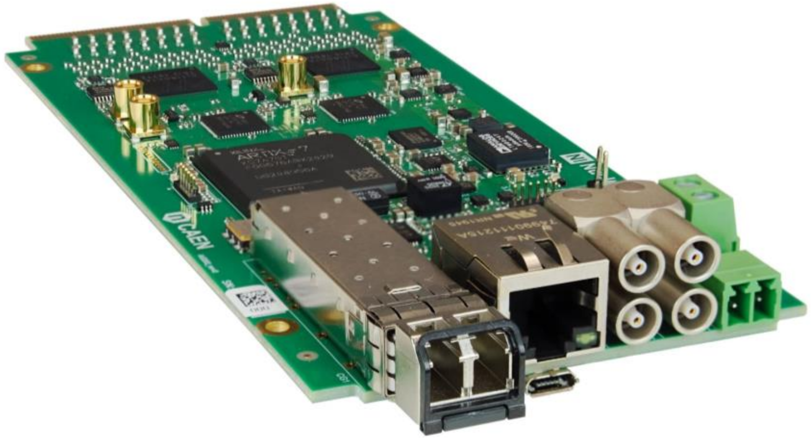






picture from IRSN

# FERS-5200: a distributed Front-End Readout System for multidetector arrays




CAEN Tools for Discovery

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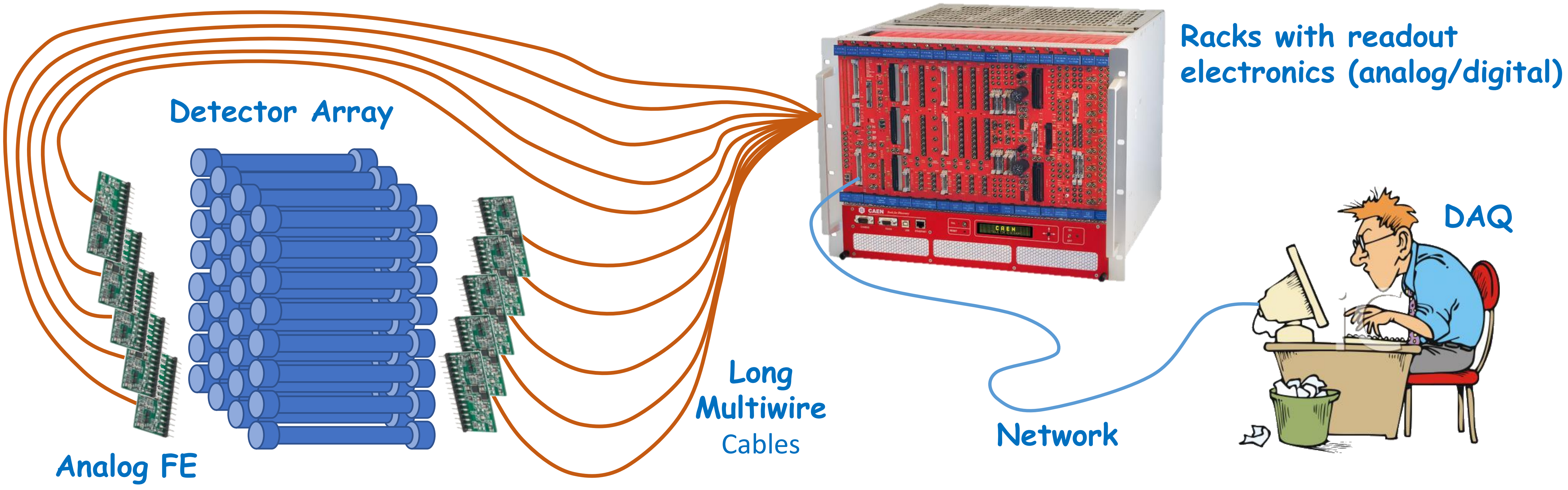
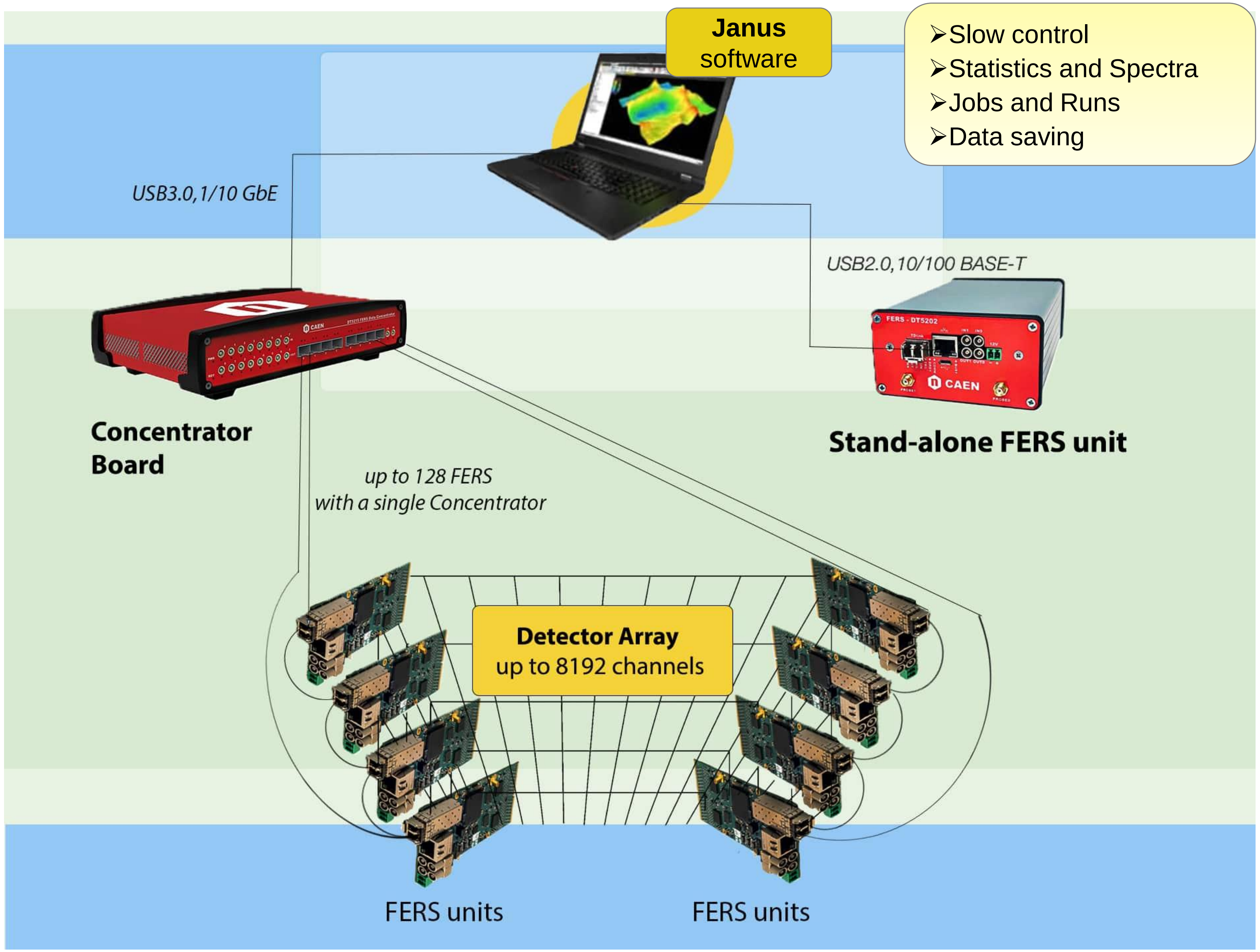
# The old way: rack electronics

- Front End Preamplifiers close to the detectors
- Long cables bring analog signals to readout electronics (ADC, TDC, etc.) in racks
- **PROBLEMS**: Signal attenuation, noise pick-up, ground loops, cost of cables, geometry constraints



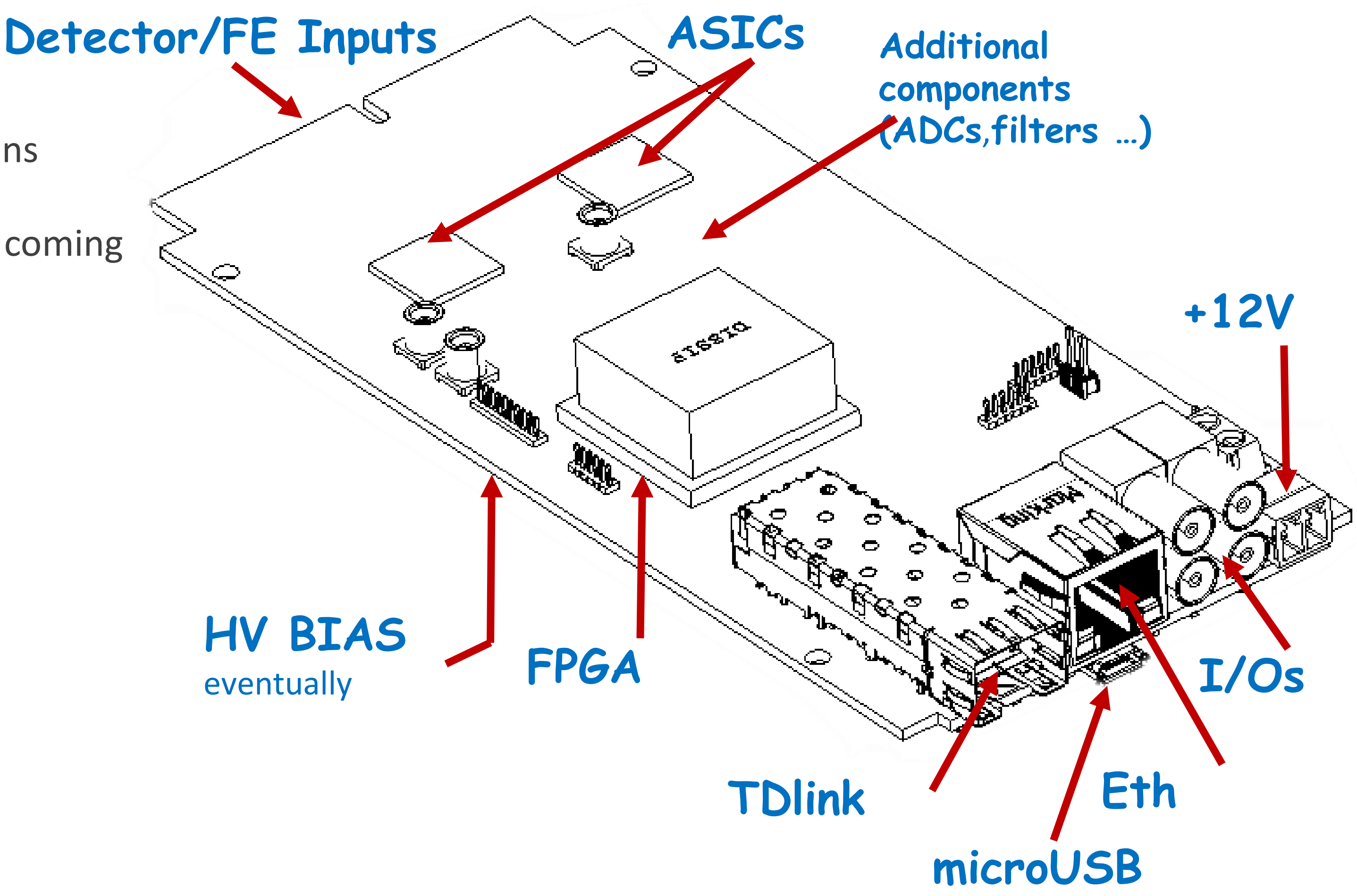
# State of the Art: FERS-5200

- **Modular and Distributed** readout of large arrays of detectors
- **Compact** FERS units based on *ASICs* → front-end + digital
- **Concentrator Board** to manage multiple FERS units
- **TDlink**: 4.25 GB/s Optical link providing Readout, Slow Control, Synchronization → **Easy-scalability**
- **Janus** software to control the whole system and make standard DAQ

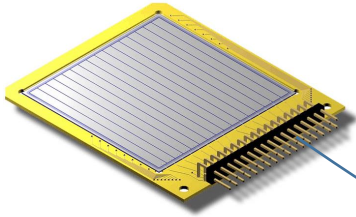


# FERS unit – how it is done

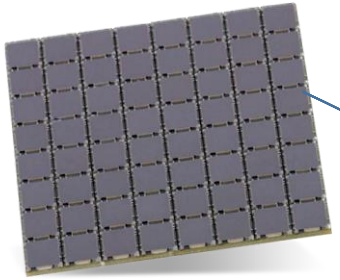
- Compact PCB - 17 x 8 cm
- Readout through **ASICs** tailored for specific applications
- FPGA implements the "processing center" for data coming from ASICs
- Embedded **High Voltage** for detector biasing**,** when requested by the application
- Different readout protocols: USB, Ethernet, TDLink




# FERS-5200 “flavours”

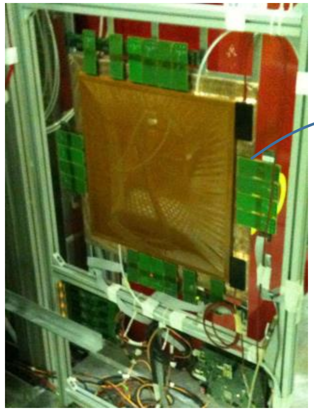


**Silicon Strip Detectors**

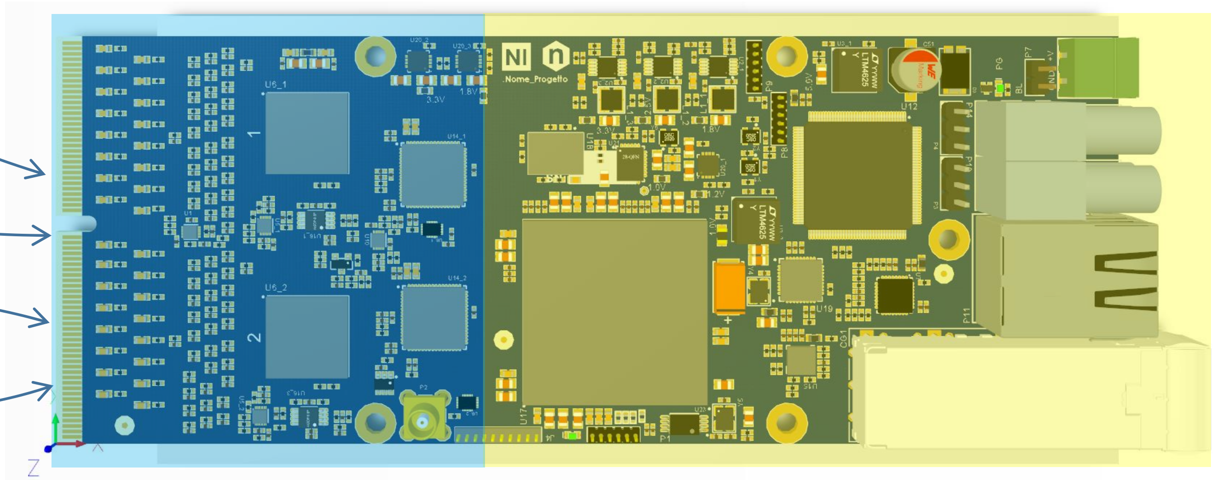


**SiPM**

**Multi- wire chambers**



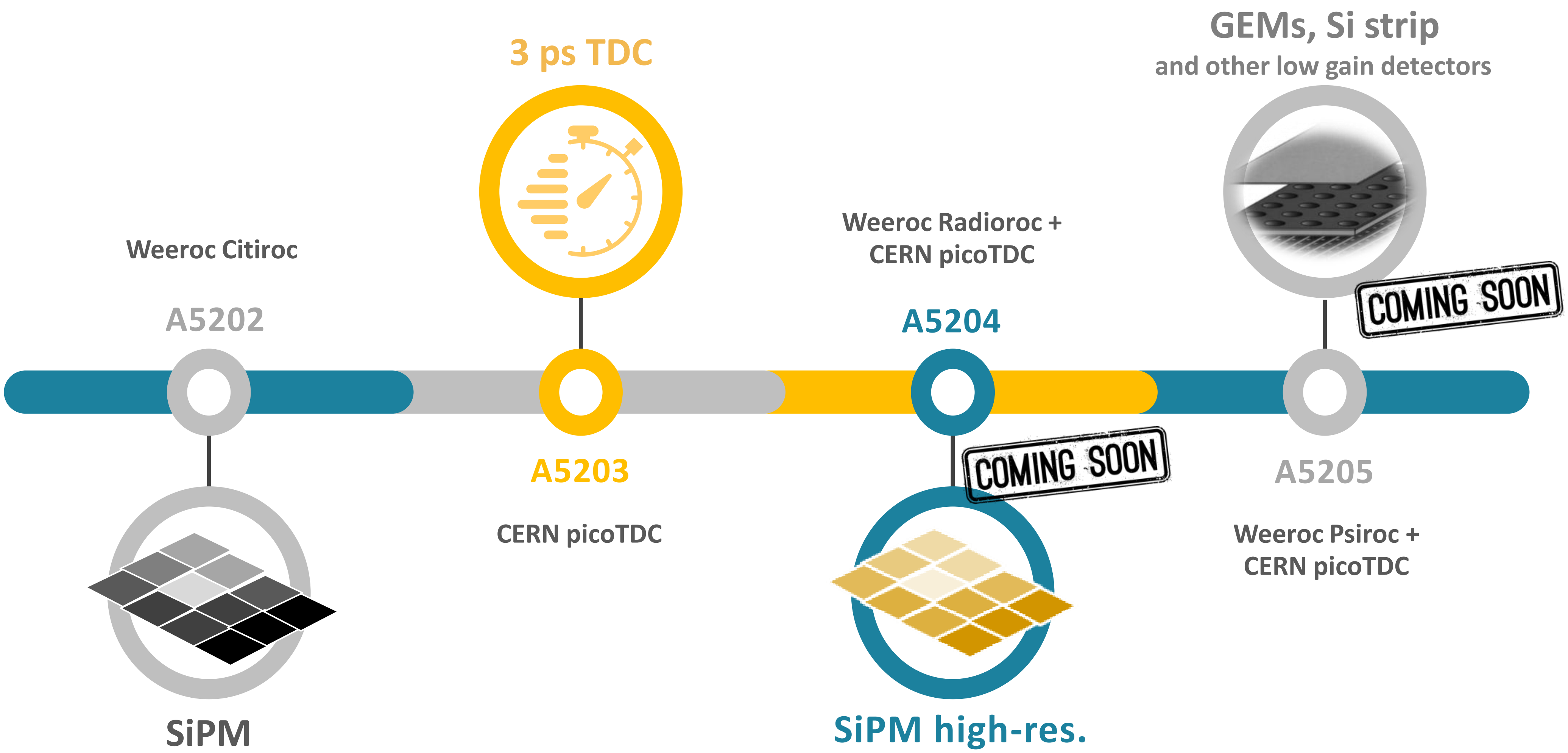
**Micromegas, GEMs**



**APPLICATION -SPECIFIC** **COMMON INFRASTRUCTURE**

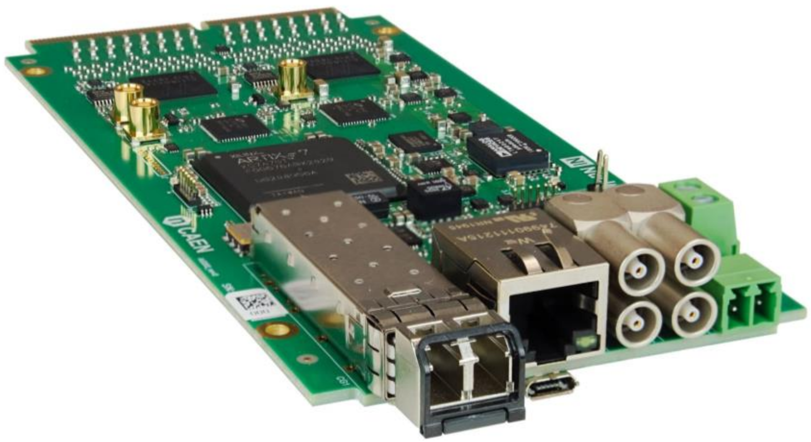
**Same infrastructure, different Front-Ends**
quick integration of different ASICs

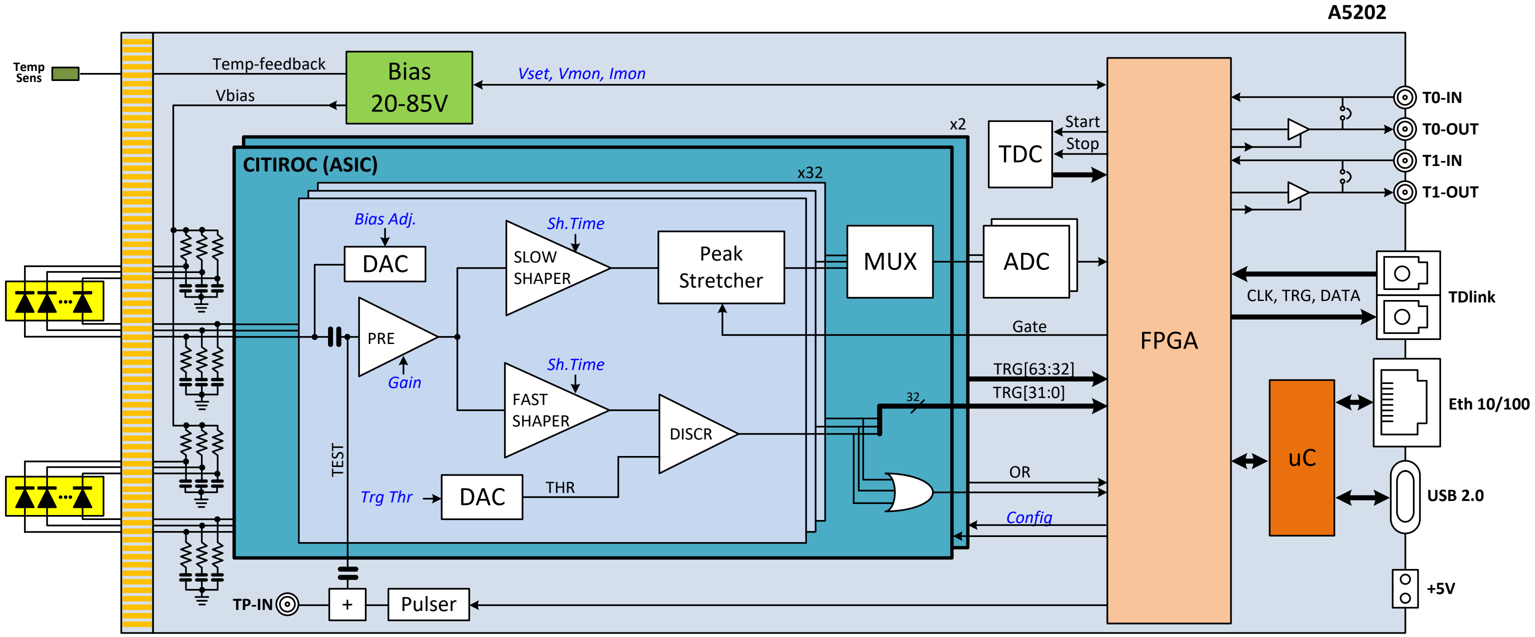
# FERS Roadmap



# A5202: 64 channel SiPM readout

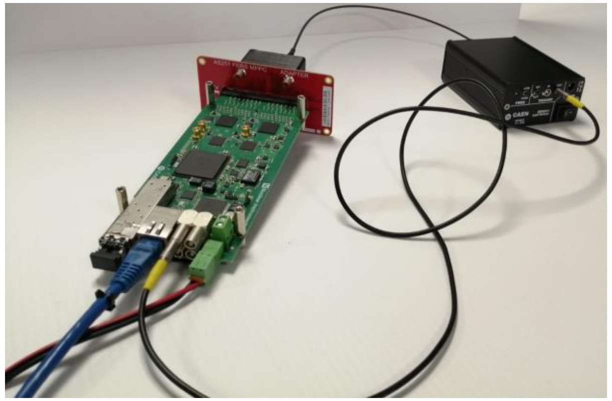
- 64-channels SiPM readout, based on analog chain + **Peak Sensing** strategy (Weeroc **Citiroc-1A**)
- Embedded 20-85 V module for SiPM **bias**
- **Single photoelectron** energy resolution and **0.5 ns** event timestamp resolution
- Readout modes: photon counting, spectroscopy (PHA), event timestamping

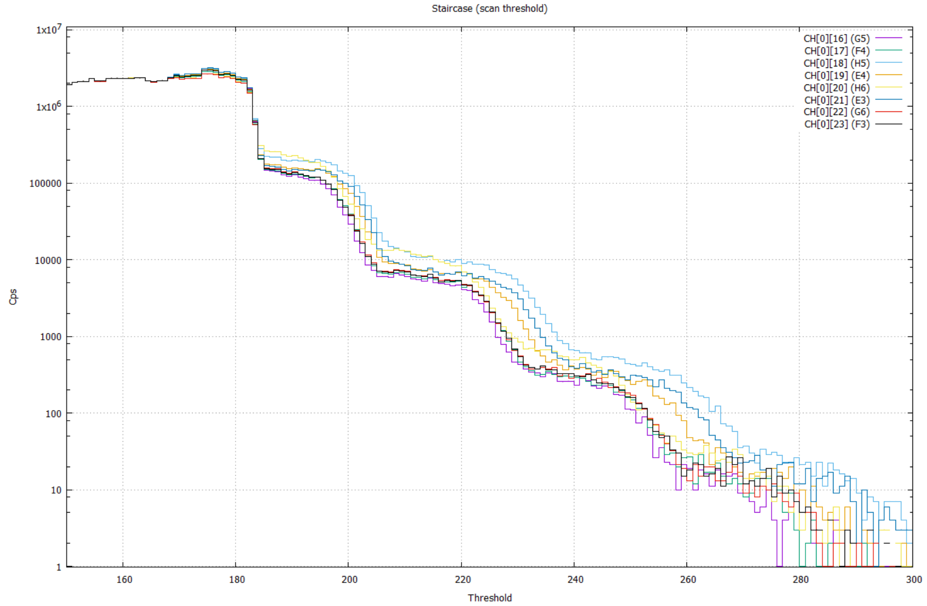




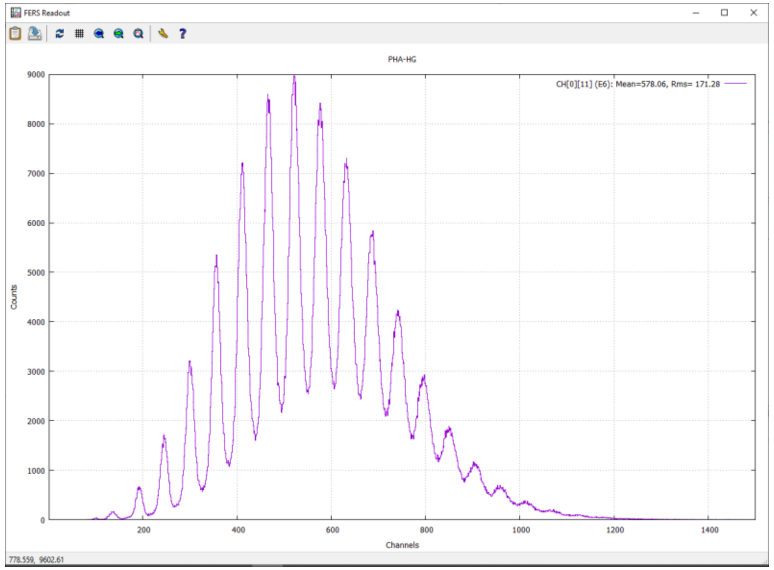
# Qualification of A5202

- One A5202 board
- SiPM Matrix Hamamatsu S13361-3050AE-08
- CAEN SP5601 LED Driver

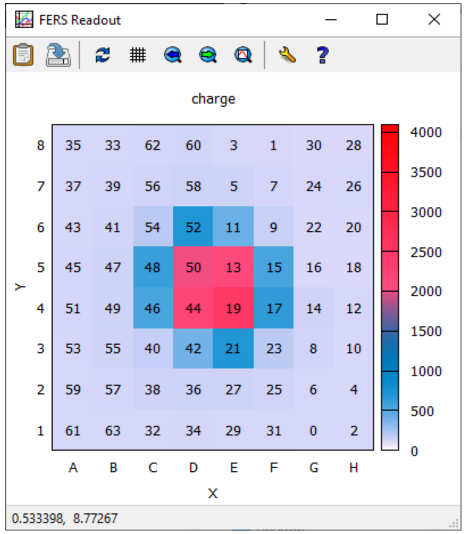





Staircase

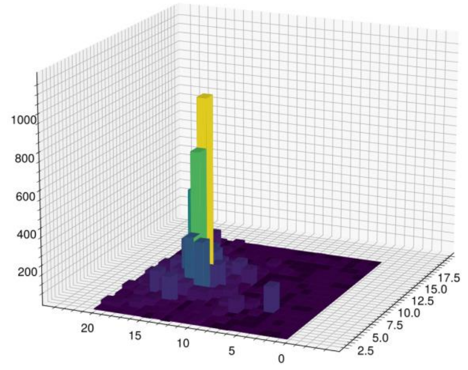


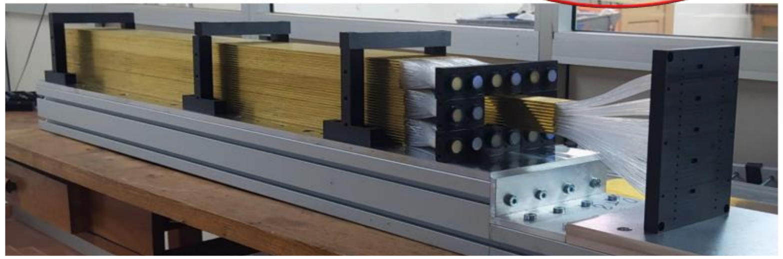

SiPM spectrum with photopeaks




Imaging

# Use cases

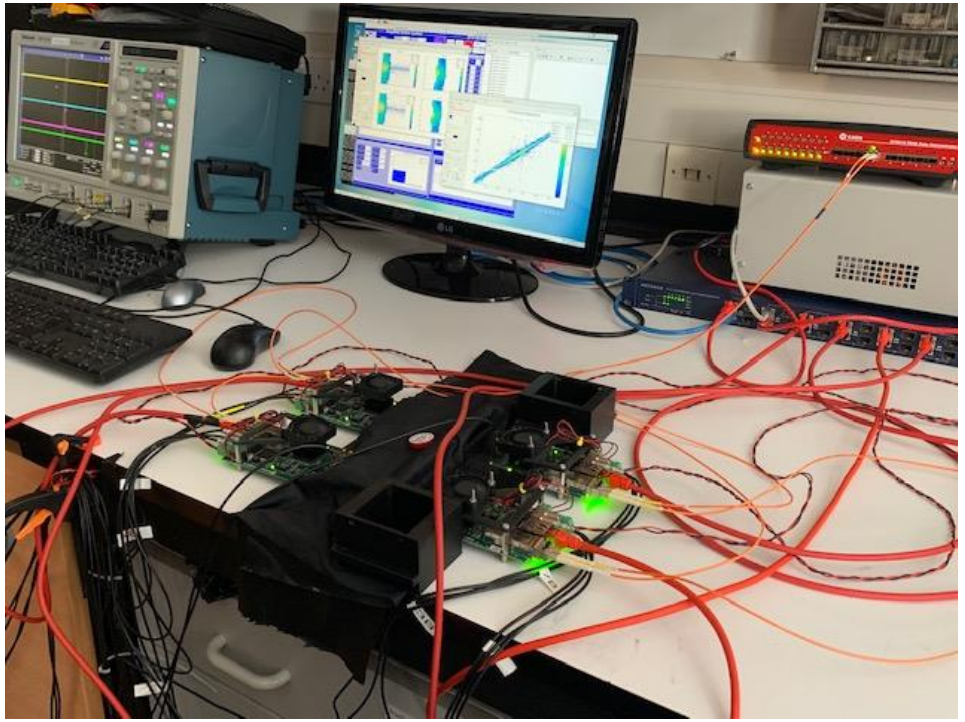


FERS in dual readout calorimetry
R. Santoro, Calor 2020

- Development and testing of **dual readout highly granular calorimeter**, exploiting SiPM and CAEN A5202

- **320 SiPMs** read out using **five CAEN A5202**

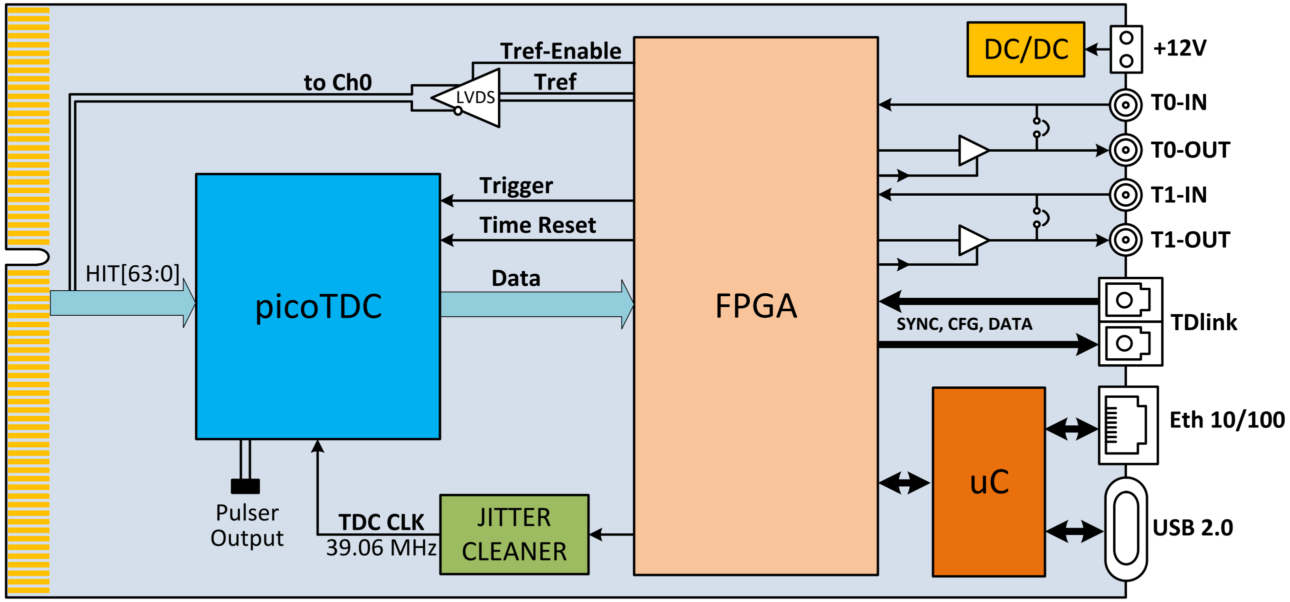


FERS for cosmic ray tomography
**Muon tomography scanner**, suitable for **nuclear waste characterization,** by Lynkeos Technology (Scotland)

First-of-a-kind muography for nuclear waste characterization
D. Mahon *et al.*
Philos. Trans. R. Soc. A, 377 (2018), p. 0048,
10.1098/rsta.2018.0048

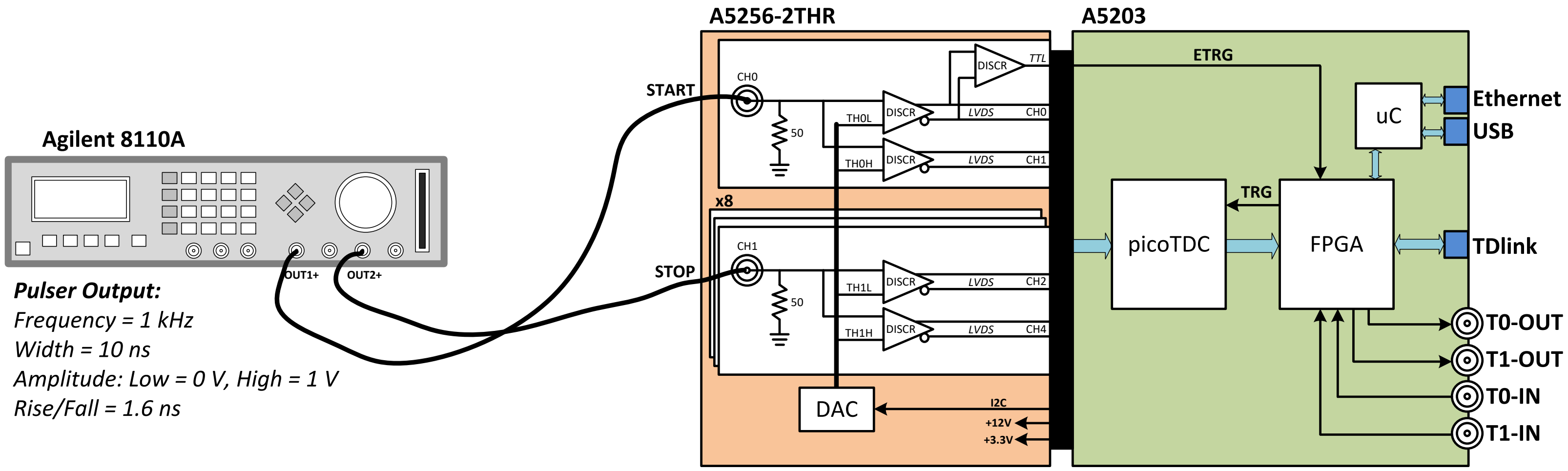
# A5203: 64 channel 3 ps TDC

- 64-channels **TDC** unit for extremely high-resolution applications housing CERN **picoTDC** ASIC
- Timing resolution LSB = 3.125 ps, **RMS typ. 7 ps**
- **LVDS**-compliant input → possible coupling with external discriminator output or custom front-end
- Acquisition of rising/falling edge timestamps → **ToA** and **ToT**



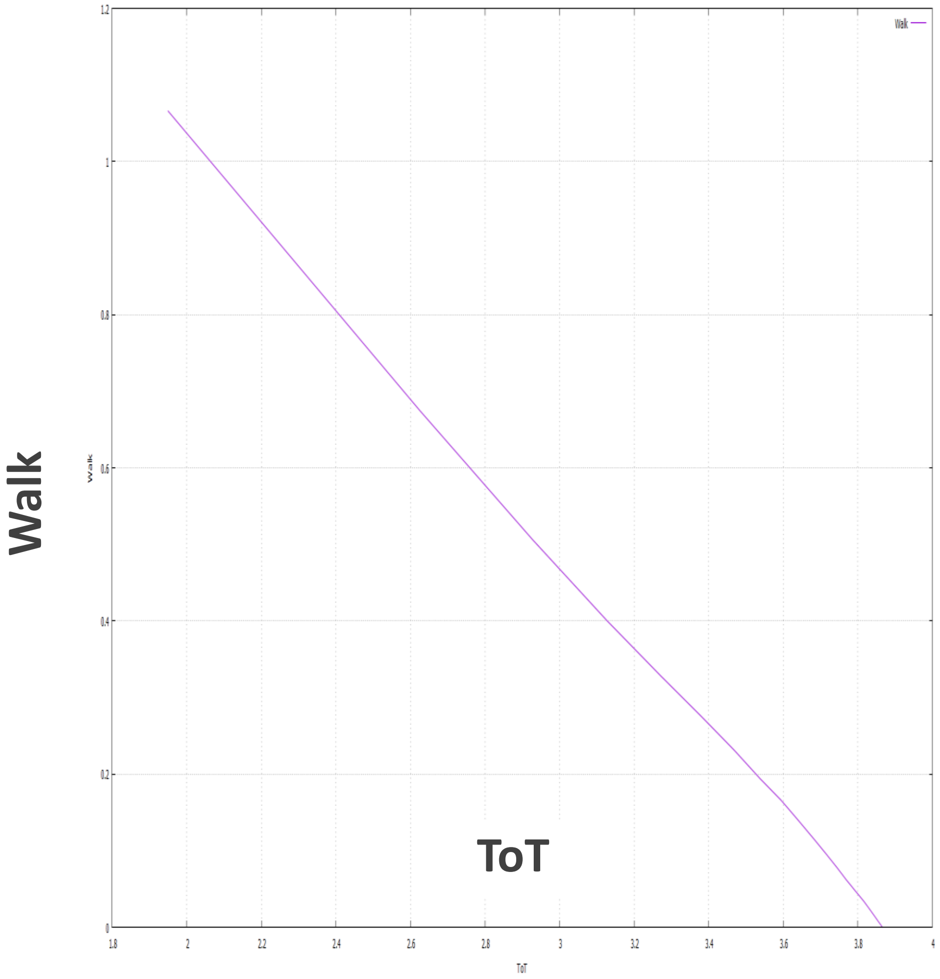
# Timing Resolution with fixed amplitude (1)

**Setup:**
A5203: 64 ch. picoTDC
A5256: 16+1 ch. Dual Threshold Fast Discriminator
Agilent A8110A: Dual Pulse Generator (1V, 0.8 ns rising edge)

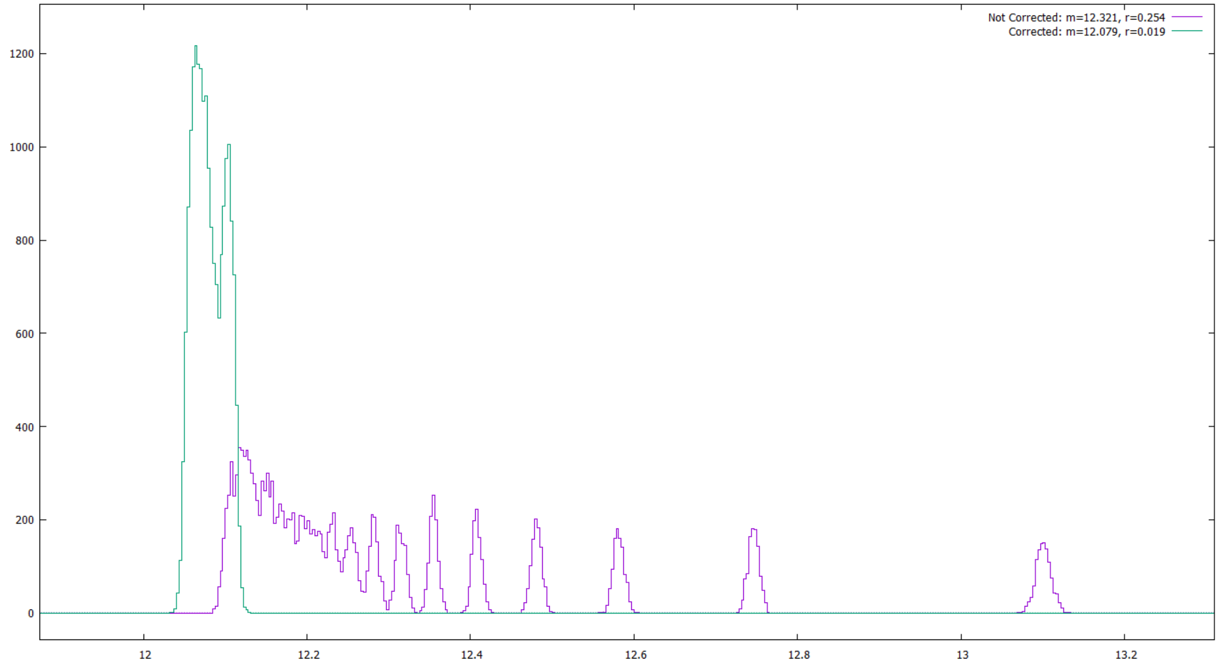



| | Low Thr | | High Thr | |
|---|---|---|---|---|
| | Mean | RMS | Mean | RMS |
| **deltaT (start-stop)** | 4.7 ns | 5 ps | 4.9 ns | 6 ps |
| **ToT** | 10.6 ns | 6.5 ps | 10.2 ns | 5.5 ps |

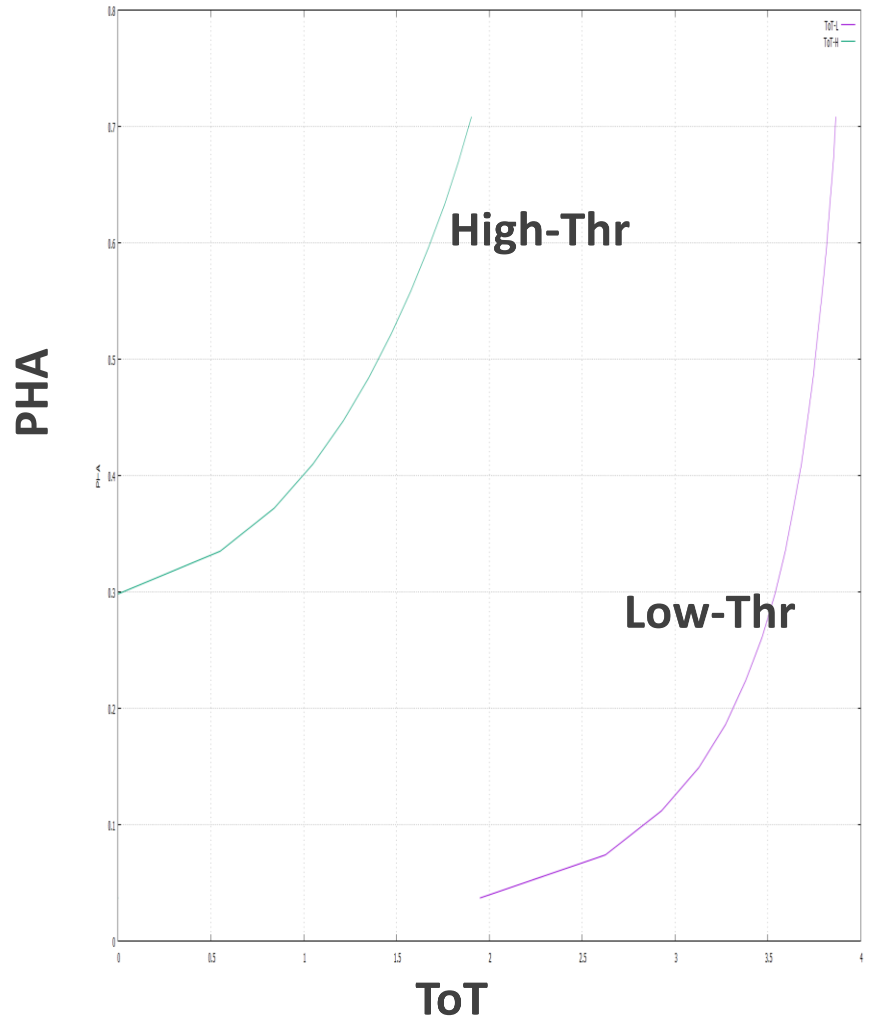
# Walk correction




**Amplitude Sweep from 35 mV to 750 mV:**
Low Thr. = 30 mV, High Thr. = 300 mV
ΔT = 254 ps RMS (no correction)
Use sampled waveform to calculate **ToT-Walk** curve
ΔT = 19 ps RMS (after correction)



# Amplitude Reconstruction

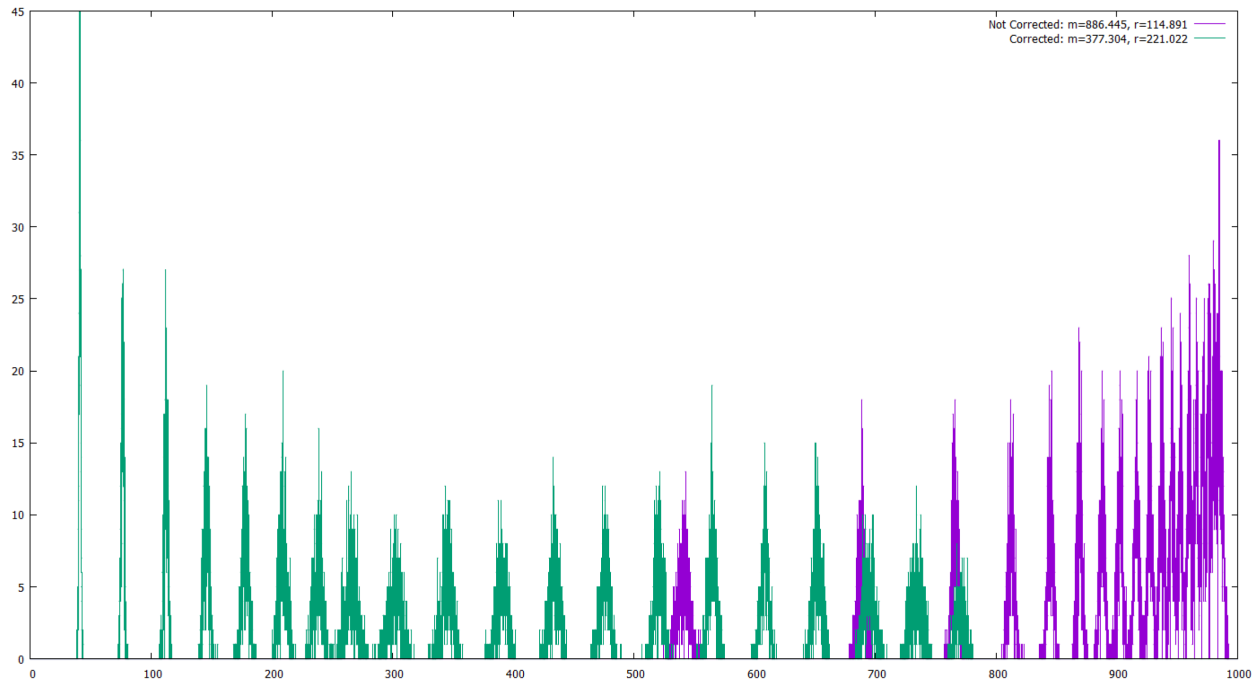



**Amplitude Sweep from 35 mV to 750 mV:**

Low Thr. = 30 mV, High Thr. = 300 mV

Use sampled waveform to calculate **ToT-PHA** curve

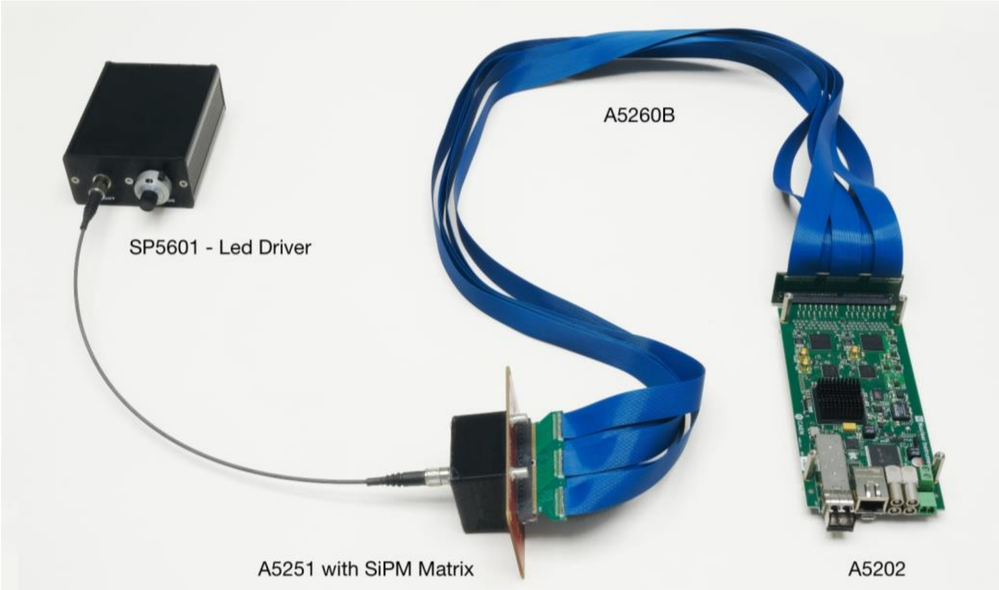
Double Threshold helps in linearization

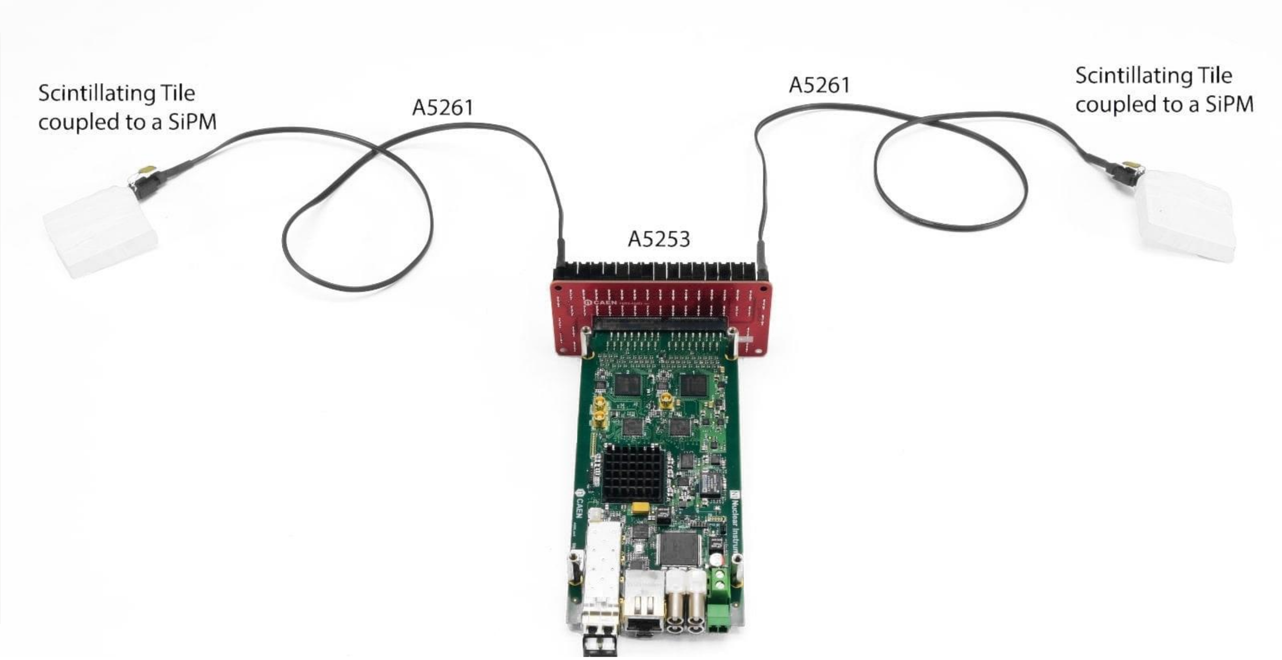


# FERS Cables

- **Micro-coaxial extension cable** for detector remoting
- Detached electronics simplifies the connection to **cold detectors**
- **Edge connector**: optimal fit for feed-through **flanges**
- Different types of interchangeable end connectors + custom made easily
- Easy fitting of **geometrical constraints**

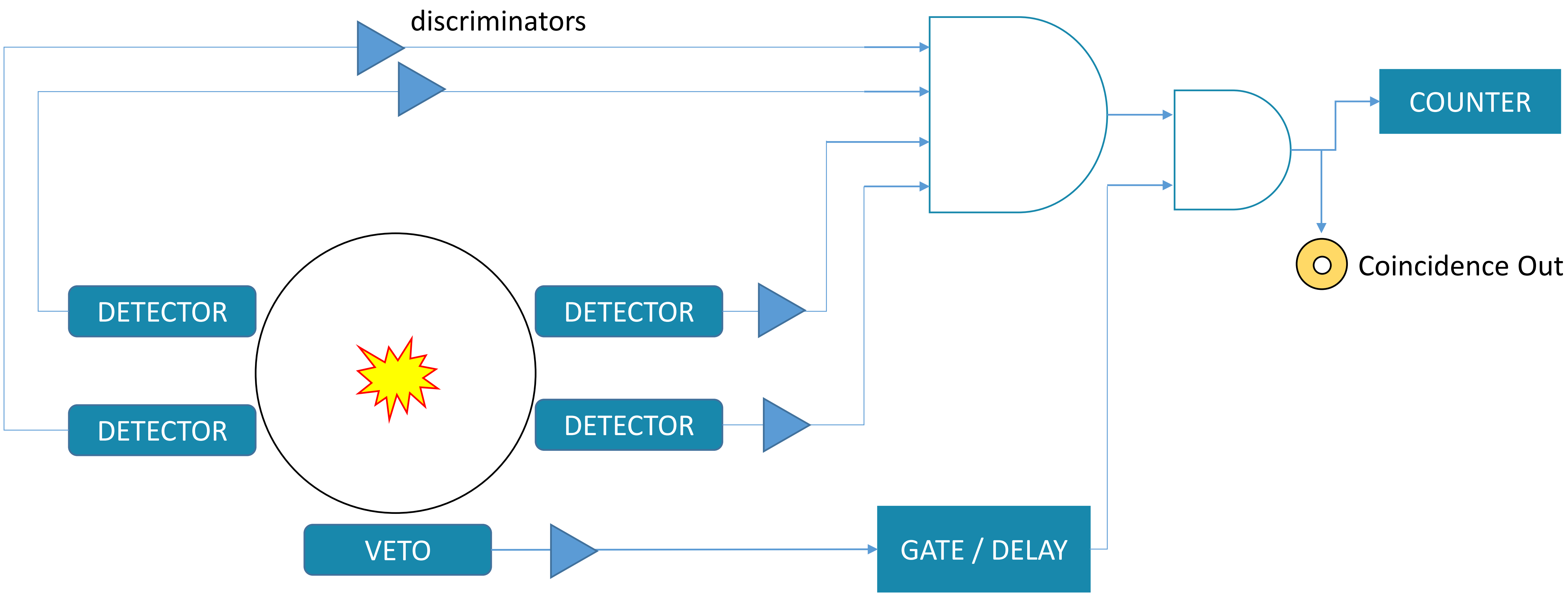

- 2.54 mm strip
- Hamamatsu footprint
- SensL footprint
- single SiPM footprint
- LEMO with discriminator



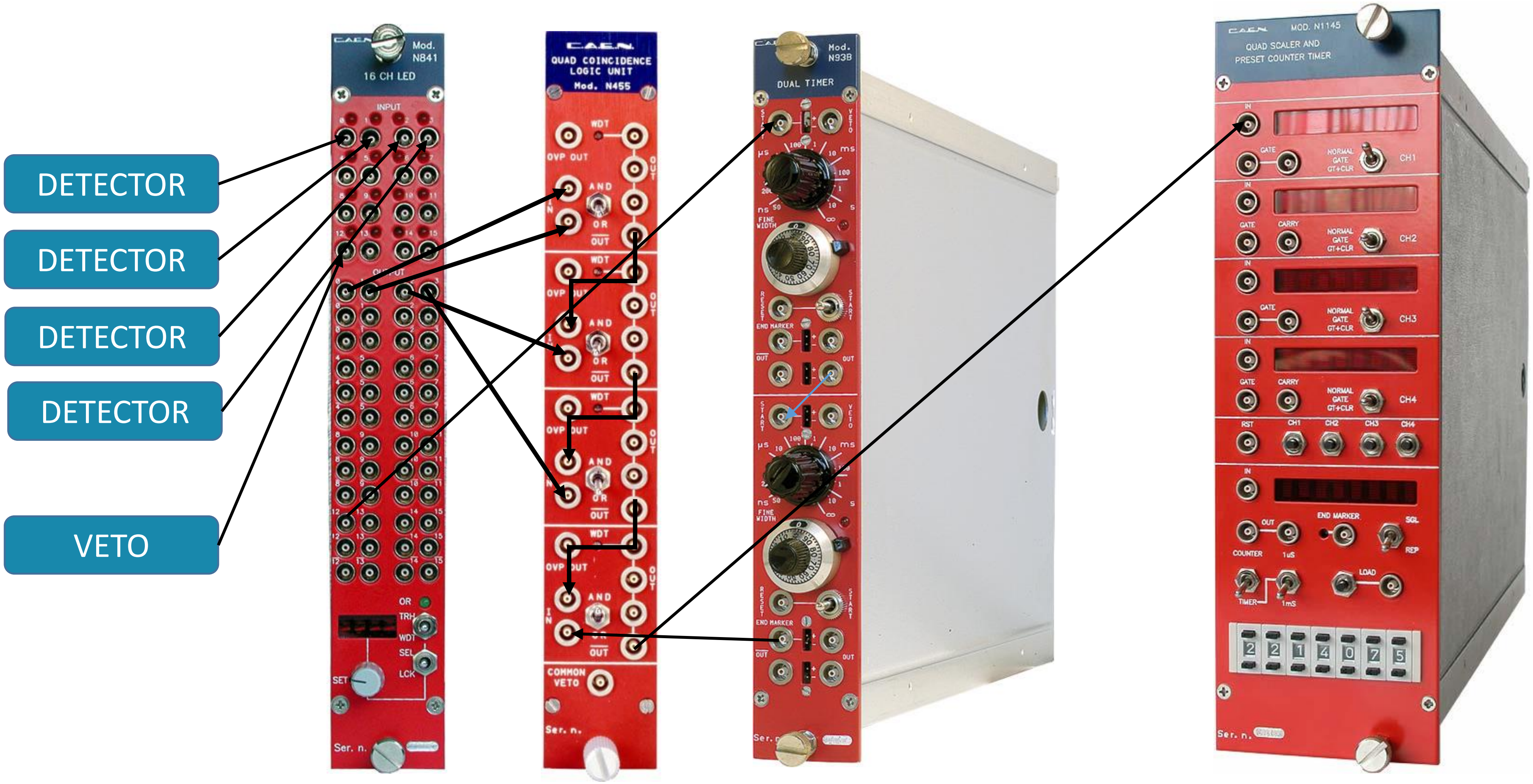



# Backup Slides

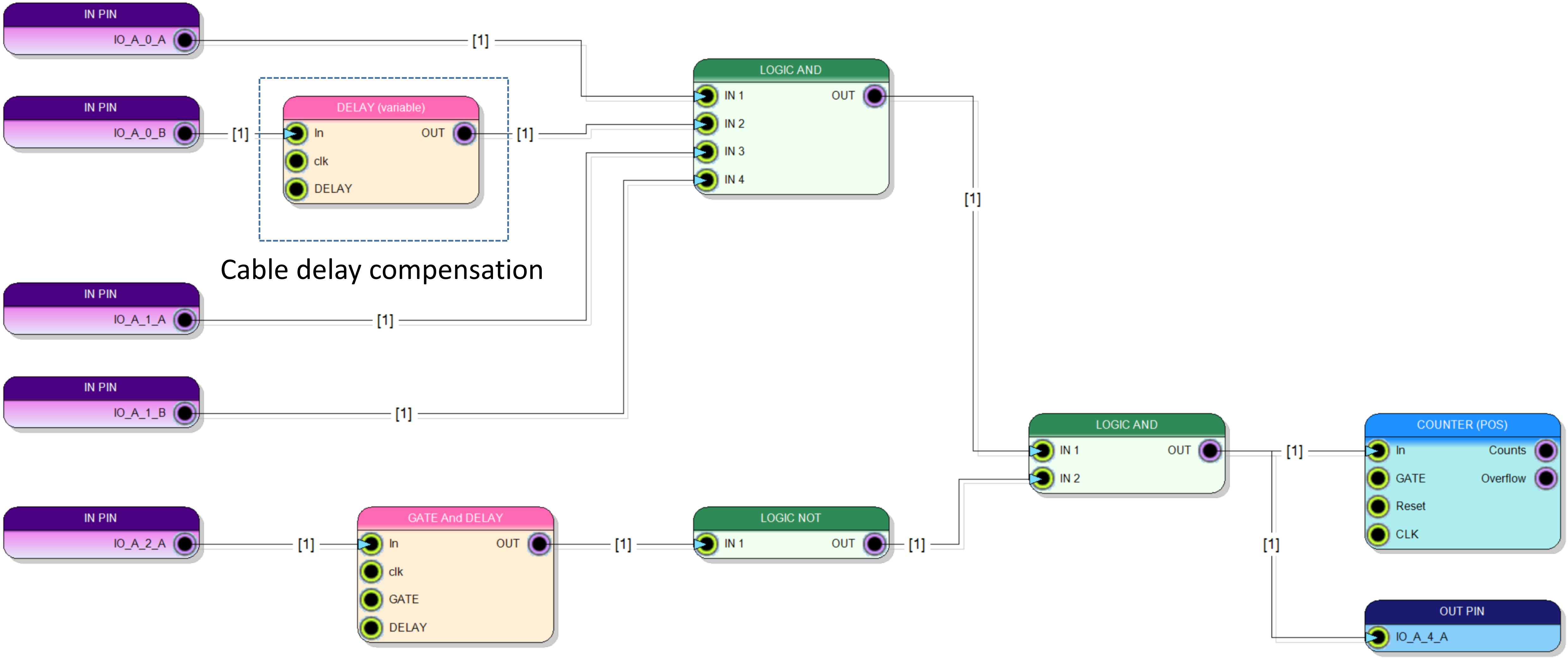
# Example: 4 coincidence event counter with VETO



# Let’s do with NIM modules…



# Let’s do the same just dran&drop virtual instruments and cables




Cable delay compensation

# DT1260 – SciCompiler Development Kit


- 2 Analog Input Channels
- Single ended input on LEMO connector
- 65 MSPS, 12 bit simultaneous sampling ADC.
- 2Vpp input dynamic
- Channel by channel indipendent offset
- DC Coupling: programmable AC shaper
- 1K/50R input impedance
- Integrated PHA and PSD signal processing
- Integrated QDC signal processing

- 1x FPGA based on Spartan 7 FPGA
- USB 2 readout
- 2 Digital I/O on LEMO connector
- Desktop form factor
- Designed for SCI-Compiler
- Ideal for: SiPM, PMT, HpGE, Silicon and He3 Detectors

# DT5560 SE – 32 Channel openFPGA digitizer for labs

- 32 Analog Input Channels
- Single ended input on LEMO connector
- 125 MSPS, 14 bit simultaneous sampling ADC.
- 20mVpp to 10Vpp input dynamic
- Channel by channel indipendent offset
- DC/AC Coupling: programmable AC shaper
- 1K/50R input impedance
- Integrated PHA and PSD signal processing
- Integrated QDC signal processing
- 1x FPGA based on Xilinx Zynq SOC. Possibility to install 7030, 7035 Xilinx Zynq
- 1 Gbps ethernet + USB 2 readout
- Desktop form factor
- Compatible with SCI-Compiler
- Ideal for: SiPM, PMT, HpGE, Silicon and He3 Detectors

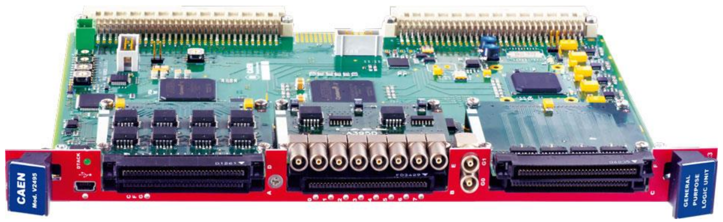
# R5560/SE – 128 channels digitizer for medium/large experiments



- 128 Analog Input Channels
- R5560:
  - Differential Input on low cost RJ45 connector
- R5560SE:
  - Single ended input on MCX connector
  - 20mVpp to 10Vpp input dynamic
  - Channel by channel indipendent offset
  - DC/AC Coupling: programmable AC shaper
- 125 MSPS, 14 bit simultaneous sampling ADC.

- 4 x 32 LVDS pair  or 4x64 single ended I/O (256 I/O)
- 4x FPGA based on Xilinx Zynq SOC. Possibility to install 7030, 7035 Xilinx Zynq for a total logic up to 1.4 million of LUT
- Ready to use Linux image for all 4 Zynq SoC
- 4x 1 Gbps Ethernet interface  connected to Zynq PS for fast data readout
- 8x 6.7 Gbps optical link (80 Gbps) connected to Zynq PL for extreme fast data readout.

# Mixed signal and ASIC based platforms



CAEN V2495

Fully programmable advanced digital logic platform

- Altera Cyclone V FPGA
- 162 input channels
- 130 output channels
- Several Expansion interface
- USB2, VME, LAN


CAEN DT5550

Fully programmable advanced mixed signal logic platform

- Xilinx Kintex 7 FPGA
- 32 Analog Inputs, 80MSPS 14 bit
- 106 digital I/O, CMOS (1.8, 3.3V) or LVDS
- USB 3

CAEN DT5550W

ASIC Development System.

- Citiroc and Petiroc support
- Xilinx Kintex 7 FPGA
- 8 Analog Inputs, 80MSPS 14 bit
- 220 digital I/O
- USB 3
- Carry board for 4 WeeROC Petiroc 2 ASICs

weeroc

# FERS models

**A5202: 64 ch. SiPM readout (READY)**

- Based on **Citiroc** ASIC
- Preamp, Fast shaper + Discrim, Slow shaper + Peak Sensing + Mux ADC
- High Voltage (up to 80 V) for SiPM biasing
- Acq modes: spectroscopy (PHA), photon counting, timing list mode (ToA + ToT)
- Single photon detection (threshold at 1/3 p.e.). Timing resolution = ~0.3 ns RMS.

**A5203: 64/128 ch. TDC (READY)**

- Based on **picoTDC** ASIC
- Start-Stop timing resolution = ~5 ps RMS (tested with pulser, 0.8 ns rising edge, 1 Vpp)
- Acq. modes: Common Start, Common Stop, Trigger Matching, Streaming (Leading, Trailing, ToT)
- Extension board (A5256) with fast discriminators (16+1 channels)

**A5204: 64 ch. SiPM readout (2023)**

- Based on **Radioroc** + **picoTDC** ASICs
- Similar to A5202, with improved timing resolution = 55 ps FWHM (on single photon)

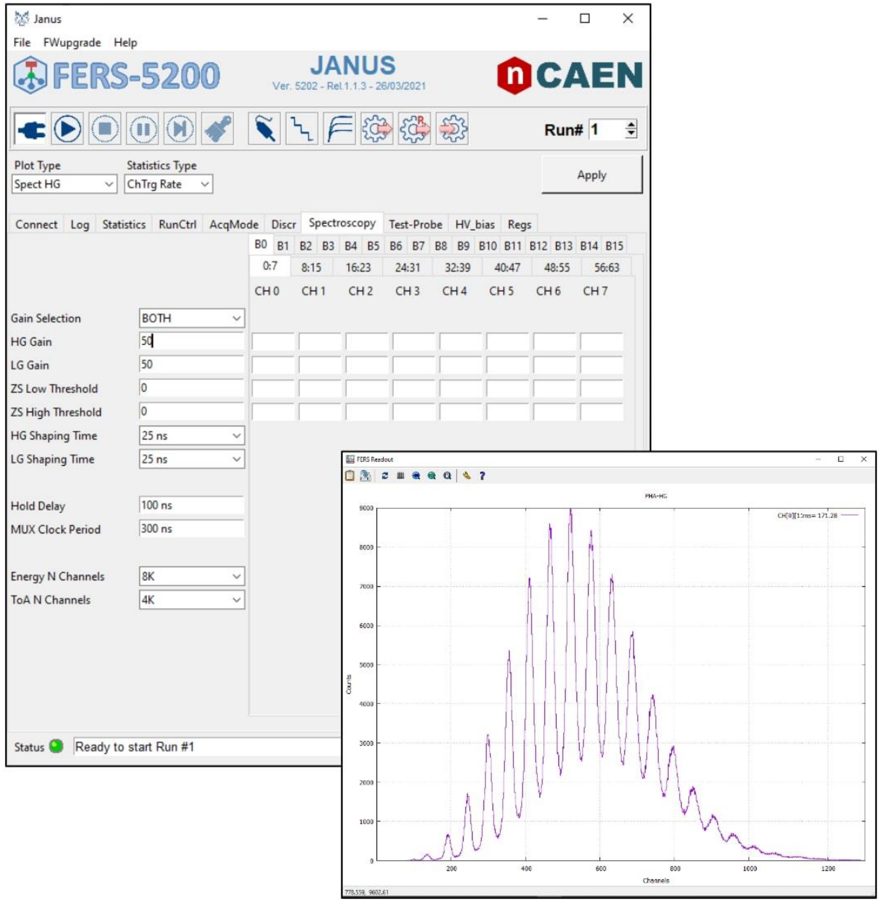
**A5205: 64 ch. SSD, GEM, PIN diodes readout (2023)**

- Based on **Psiroc** + **picoTDC** ASICs
- Programmable gain: 125 mV/pC up to 4 V/pC. Min trigger threshold = 0,5 fC
- Pos/Neg inputs. Dynamic range up to 5 pC with PHA, 100 pC with ToT
- Timing res = 150 ps RMS @ $Q_{IN}$=4 fC
- Linearized ToT for high rate, high-res energy and ps timing!

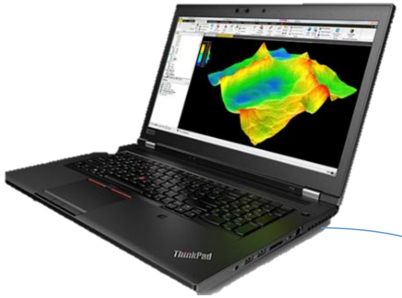
# Janus Software

CAEN **Janus software** is free and available for FERS multi-board control and data acquisition:

- Model-dependent GUI for a quick and easy start
- **Open-Source** for user customization
- High Voltage fully controllable by the software
- Management of the acquisition parameters of all connected boards
- Multi parametric Jobs and Runs with time or counts preset
- Data saving of lists in **.bin**, **.txt** format
- Statistics and Spectra visualization

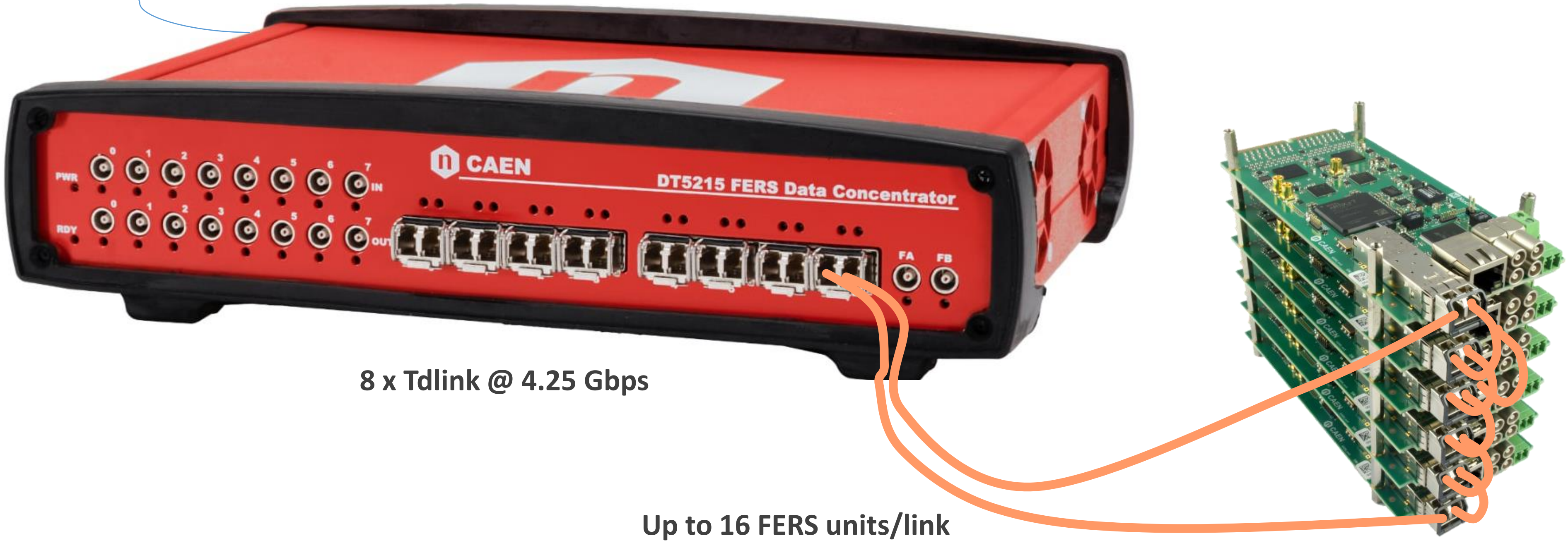


# DT5215 – Concentrator Board



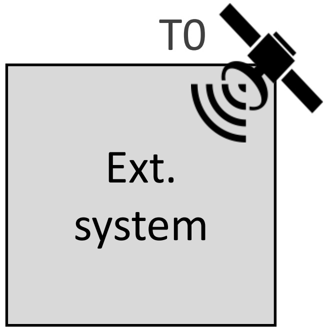
**Readout Interface**
- 1/10 Gbps Ethernet
- USB-3.0

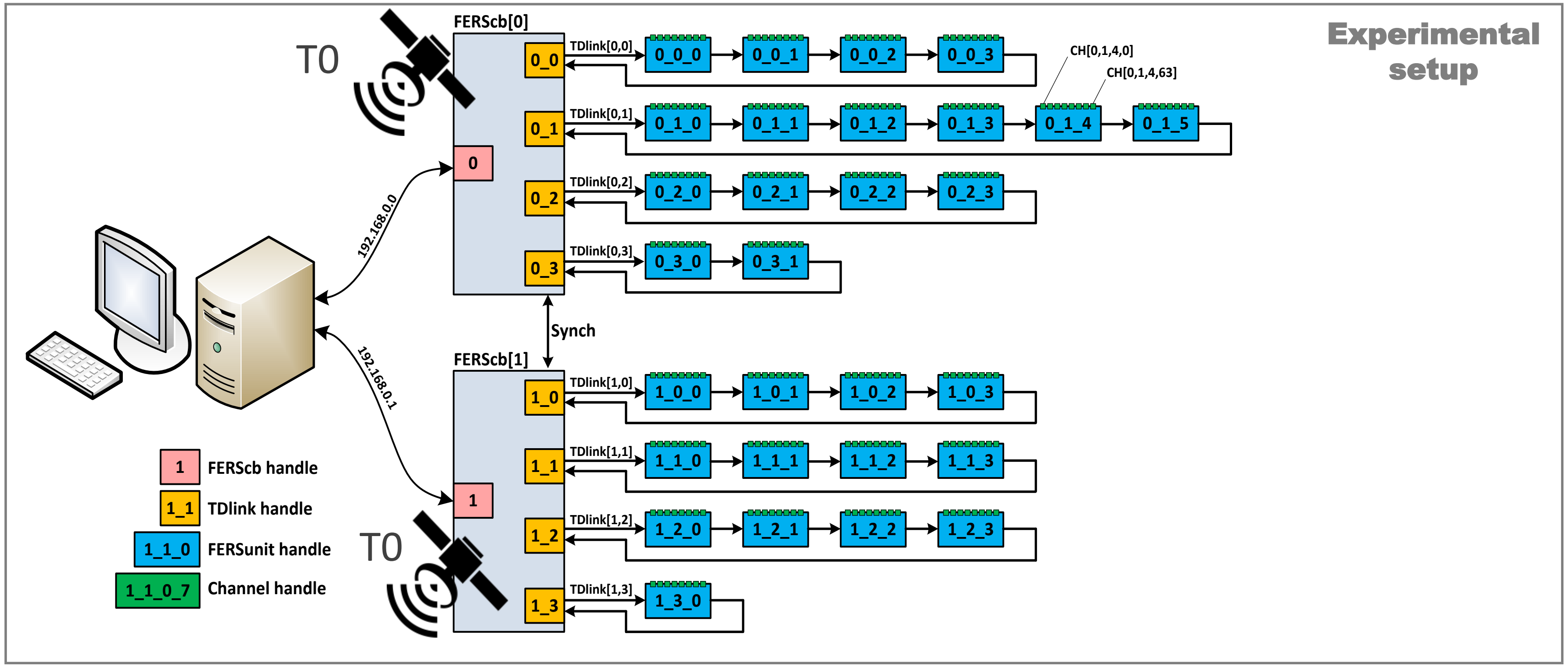
**Zynq Ultrascale SoC – FPGA and ARM**
- Readout process management
- Event sorting
- Event Building



# The key point: TDLink protocol

- **CAEN proprietary protocol TDlink**: 4.25 Gb/s over **optical fiber** providing *Readout*, *Slow Control*, *Sync* and *Clock* at once
- Allows **alignment of the timestamps with external systems** too – for example GPS



# x5202: acquisition modes

- **Spectroscopy Mode (PHA)**:
  - A/D conversion of the pulse height (preamp + shaper + peak hold + mux + 14 bit ADC)
  - Common trigger (int. or ext.)
  - Zero suppression with programmable thresholds
  - Max trigger rate = 100 kHz (dead time = ~10 µs per trigger)

- **Counting Mode** (e.g. photon counting in SiPMs):
  - Counters fed by fast discriminator signals
  - Simultaneously latched at programmable time frames and saved to memory (MCS mode)
  - Counting rate up to ~20 Mcps/ch

# x5202: acquisition modes

- **Timing Mode** (List of Tstamps and/or Time over Threshold):
  - Independent hit recording: channel ID + timing (0.5 ns resolution)
  - Common start or common stop (int/ext T-ref signal)
  - Gating mode
  - Optionally, **ToT** (0.5 ns resolution) provided for low resolution PHA: Charge Resolution = 1.5%
  - Max total hit rate = ~50 Mcps/board

- **Spectroscopy and Timing mode** (List of PHA + Tstamps and/or ToT)

**COMING SOON**

# A5202: readout modes

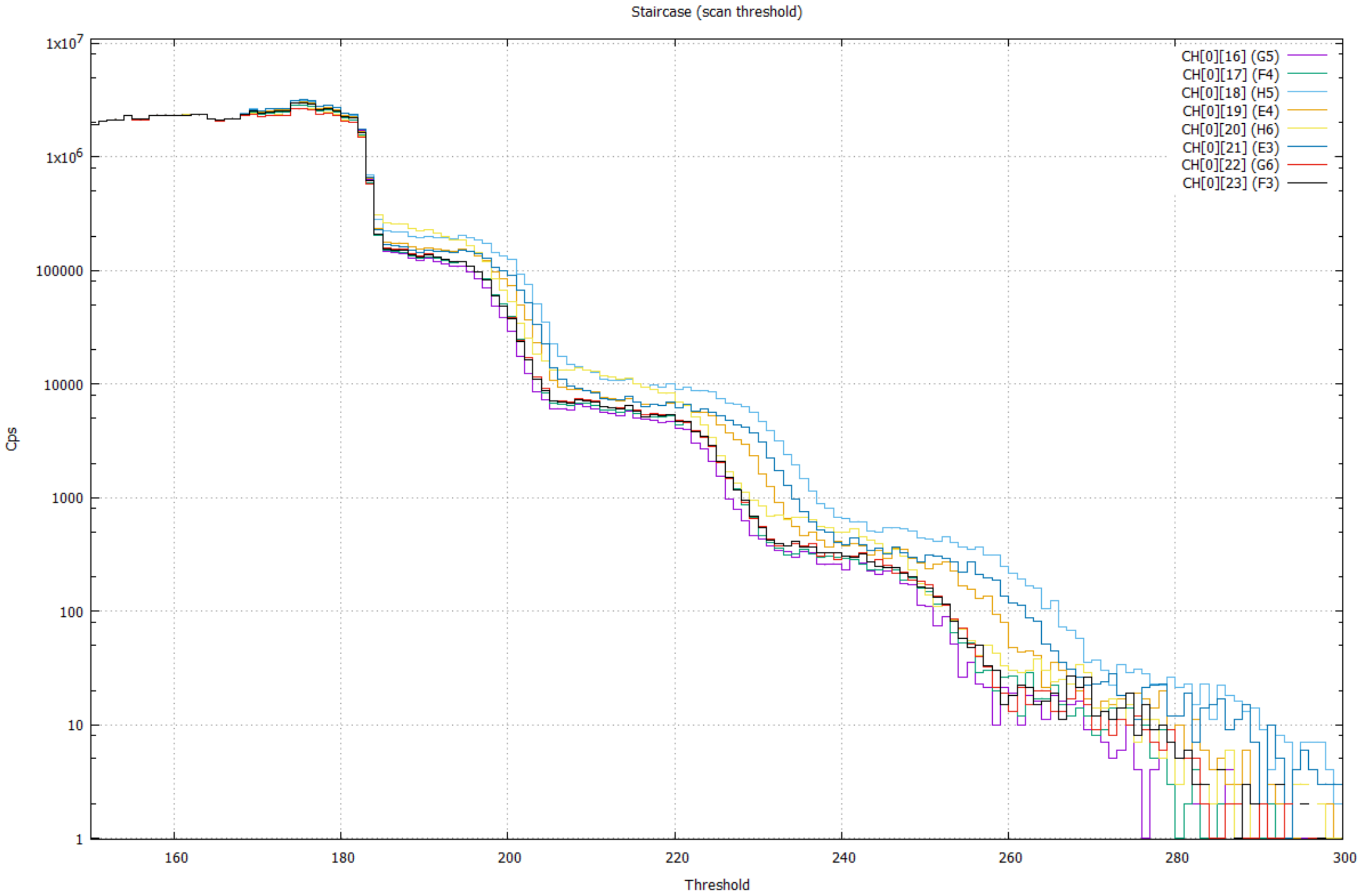
- **Common Trigger Mode**
  - **FERS units**: generate a trigger request (typically OR of channel discriminators)
  - **Data Concentrators**: receive and combine requests from all units and generate the **Global Trigger**
  - **Event Building** and data reduction takes place in the ARM processor of the Data Concentrator

- **Trigger-less Mode (independent channel acquisition)**
  - **FERS units**: each channel pushes data asynchronously, typically at different rates
  - No trigger and data correlation in HW. Events reconstruction in DAQ.

# SiPM readout with A5202 – Staircase

Example for the trend of the number of events triggered as a function of the threshold:

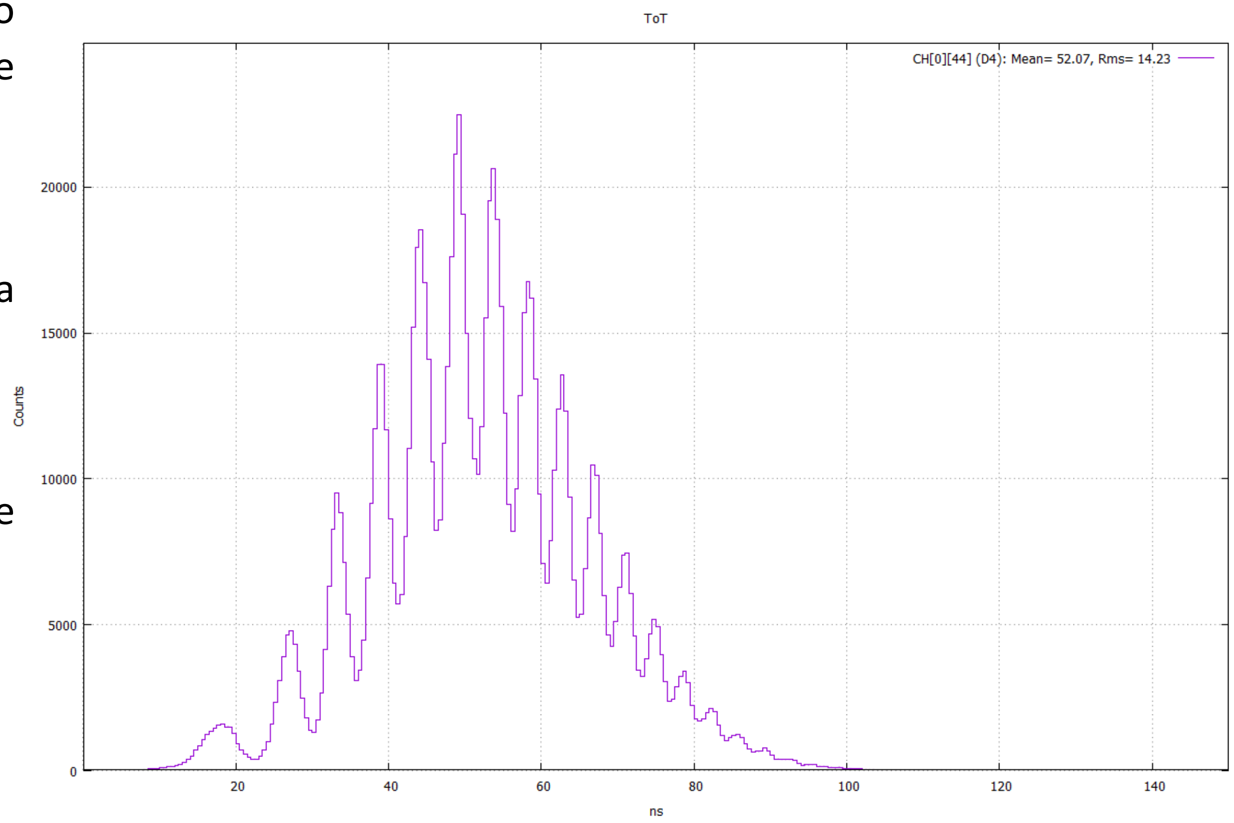
- ➢ No LED Driver used → Dark Count Rate only
- ➢ Each stair correspond to a different number of photoelectrons triggered



# SiPM readout with A5202 – ToT

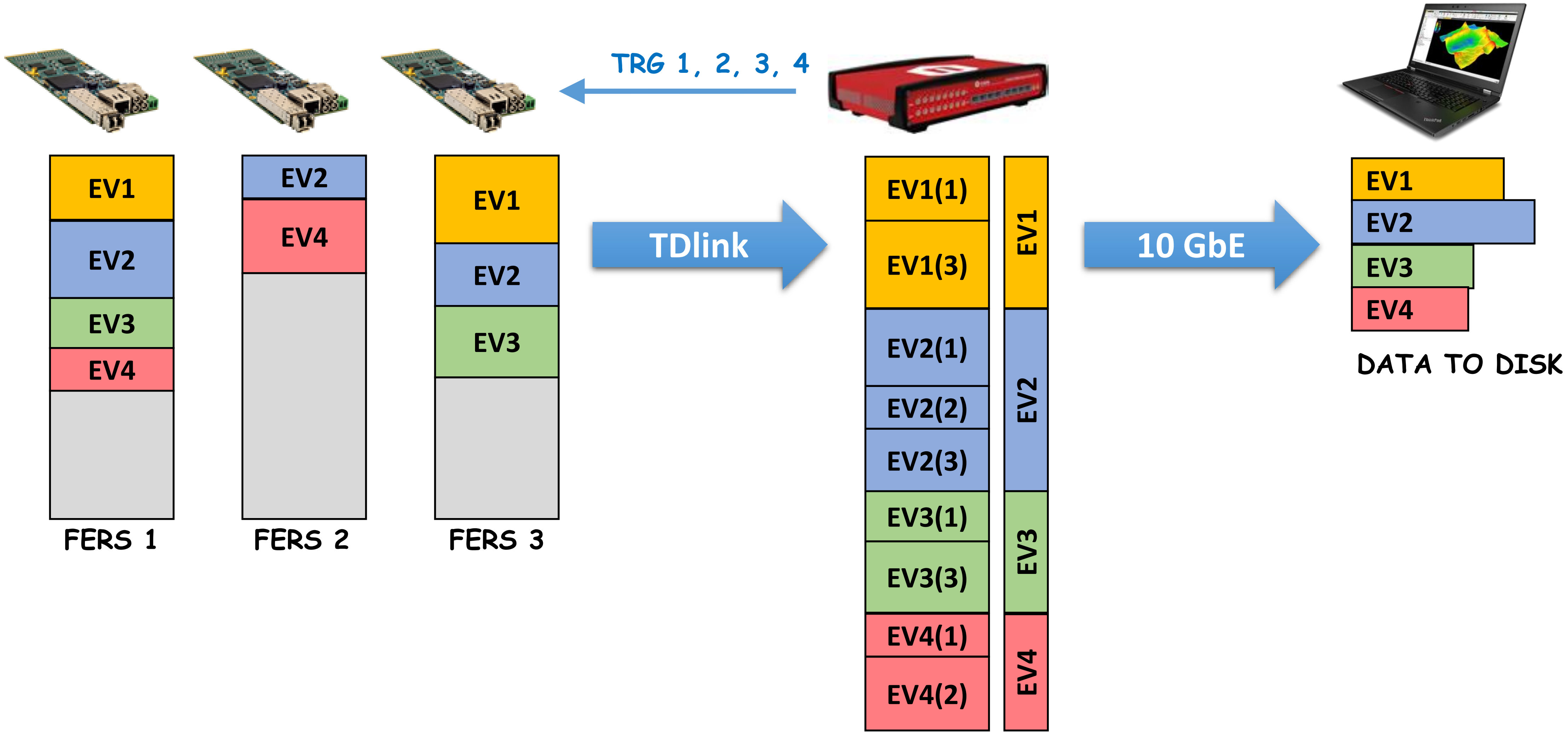
The Time over Threshold (ToT) of the pulse allows to reconstruct the energy information as well with some advantages:

- Greater dynamics to higher amplitude signals w.r.t. PHA
- Independent channel acquisition (trigger-less data streaming)
- Lower dead time → Higher acquisition Rate
- Photopeaks clearly visible and well resolved despite the lower resolution (~ 1/3) w.r.t. PHA using the same setup



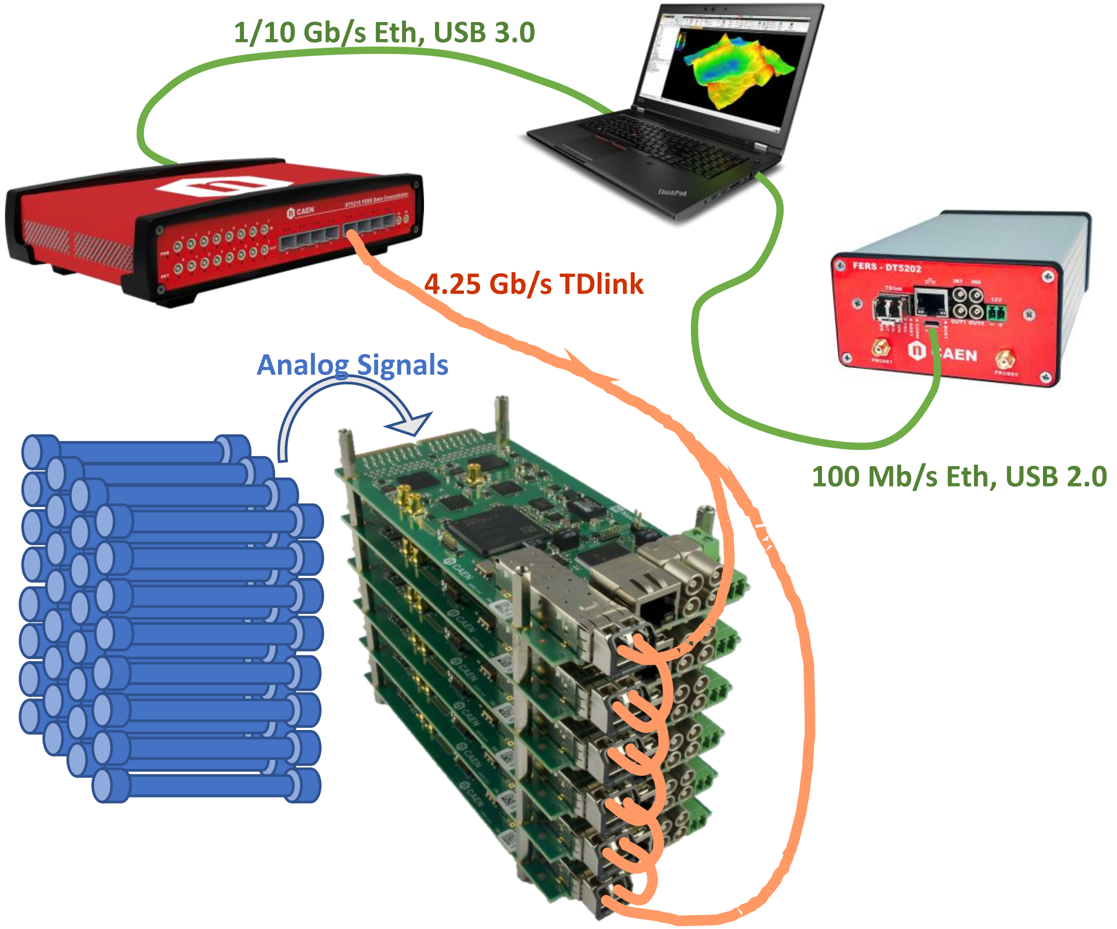

SiPM ToT spectrum with the clearly visible photopeaks

# In-built sparse event readout

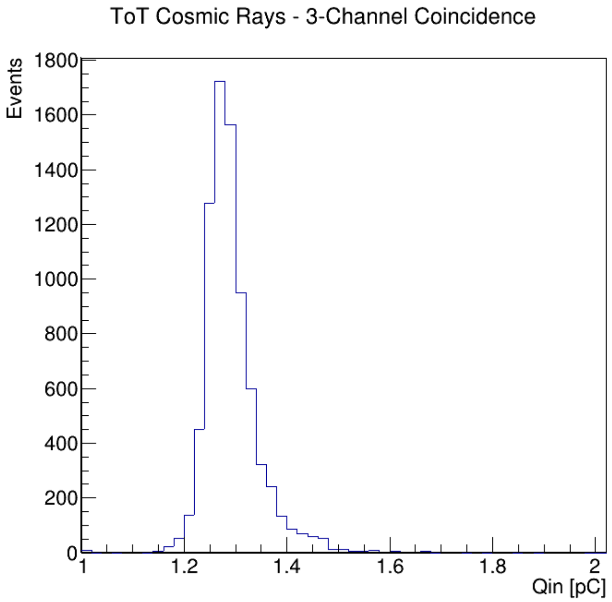


# FERS-5200

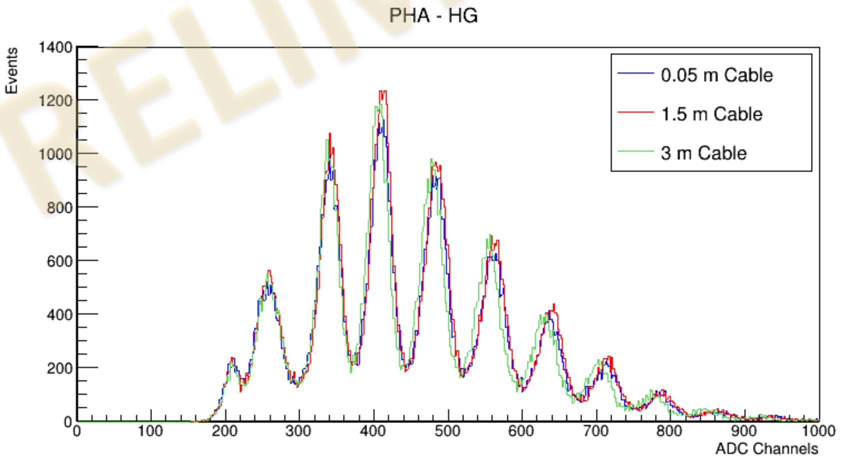
- **Modular** readout of large arrays of detectors
- **Compact** and **dense** FERS units based on **ASICs**: front-end + digital
- Dedicated protocol developed for **distributed systems**
- **Easy-scalability** of systems through daisy-chain of **fibers**
  1 FERS unit = 64/128 ch
  1 Concentrator = 8k/16k channels
- Stand Alone version for **Evaluation** => scale up to 10k/100k channels with same electronics



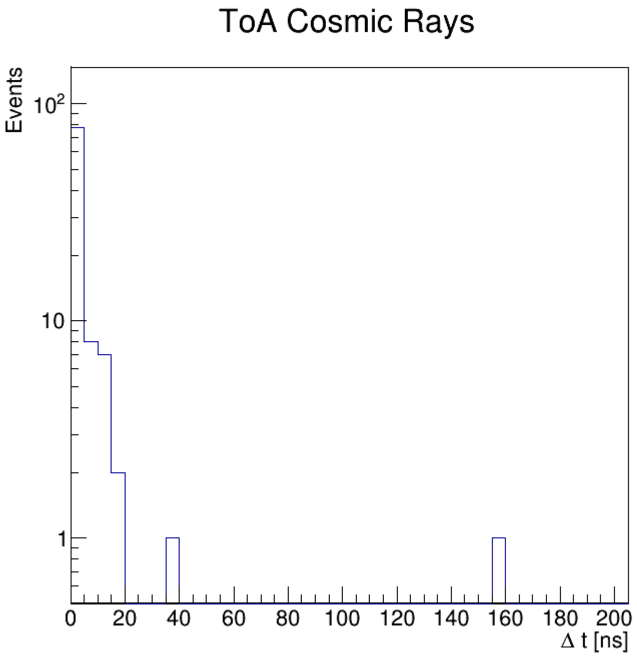
# Work in progress




Landau distribution of Cosmic Rays in ToT mode



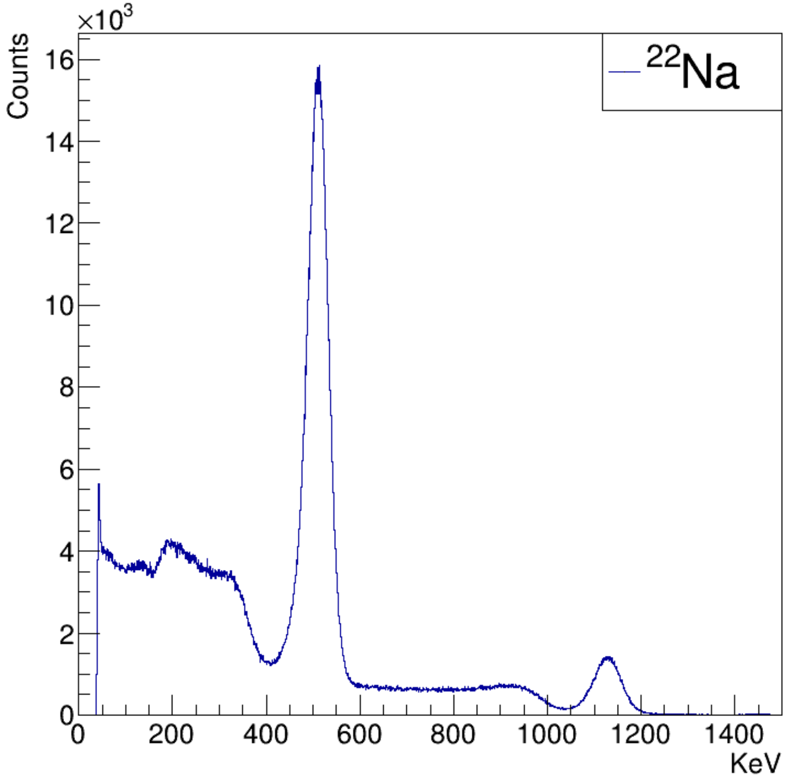

Energy loss along a cable with remote SiPM



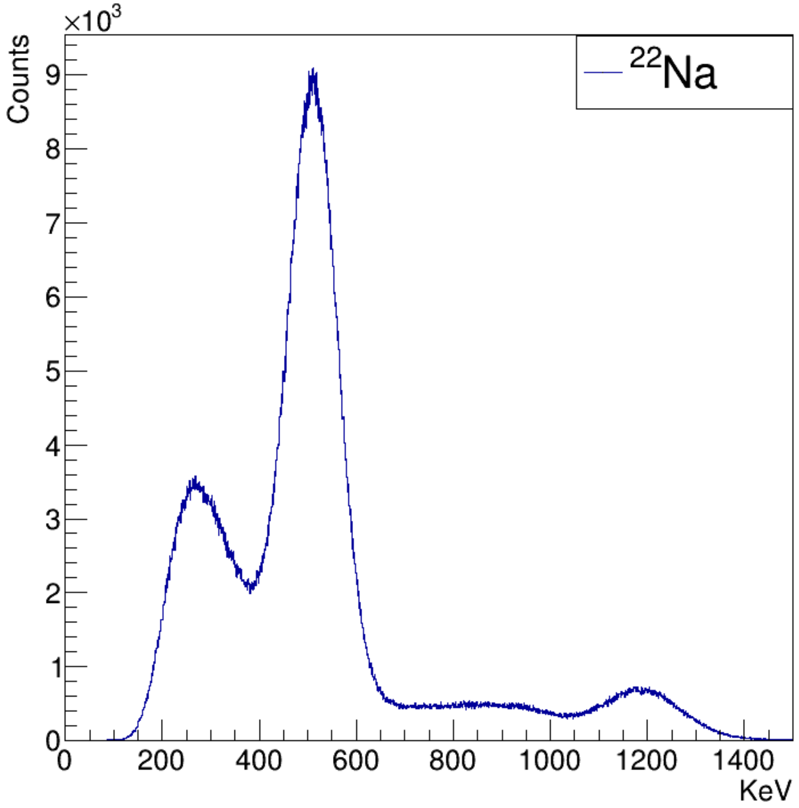

Muon lifetime with plastic scintillators

# Spectroscopy

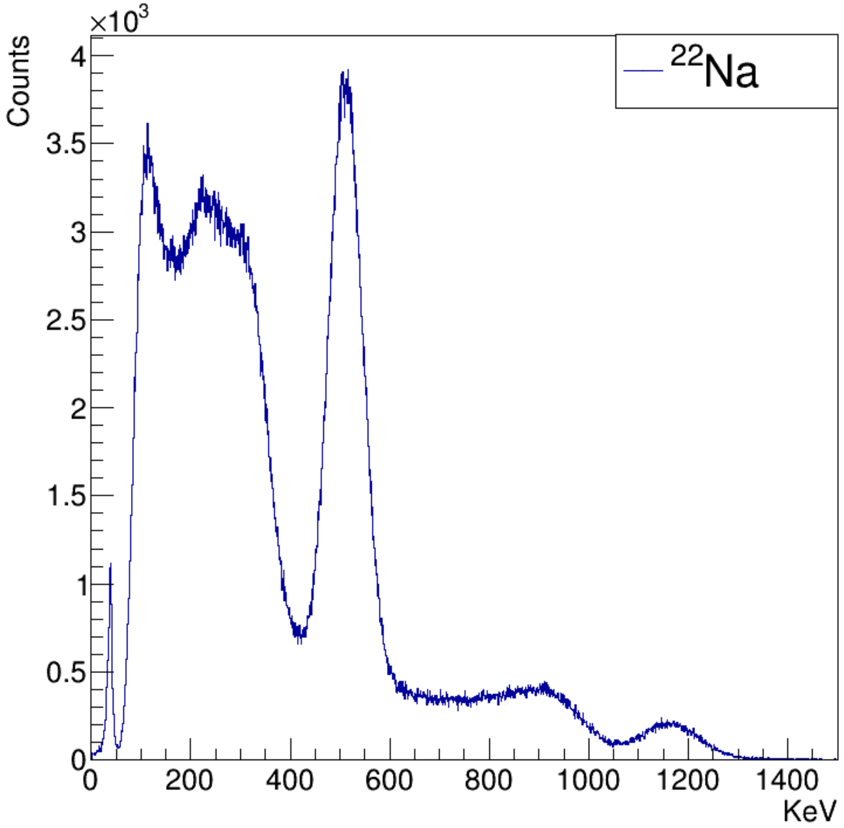
Lyso




BGO



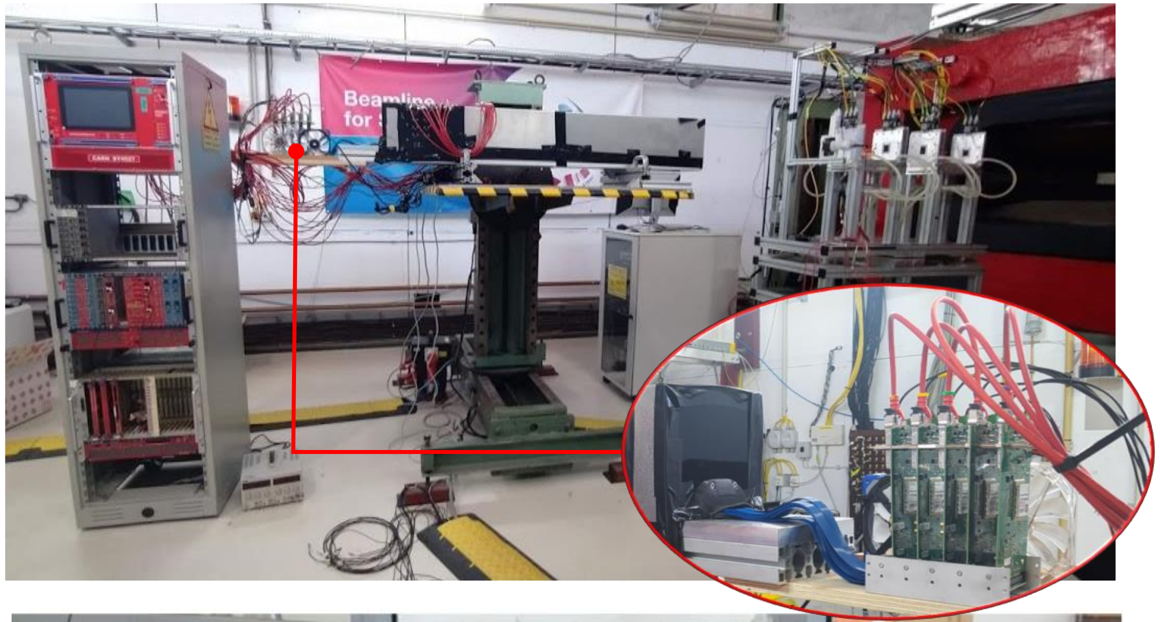

CsI

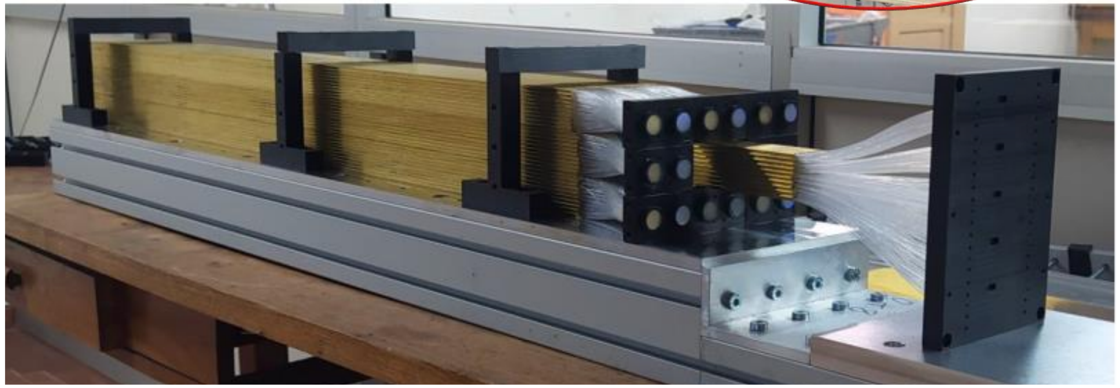


# Case history

# FERS in dual readout calorimetry

- Development and testing of **dual readout highly granular calorimeter**, exploiting SiPM technology and CAEN A5202 board.
- **320 SiPMs** read out using **five CAEN A5202**
- Successful qualification of a module on beam with EM shower containment @Desy (June 2021) and @CERN (August 2021)
- Plans to **scale-up the system** to handle more SiPMs for hadronic containment

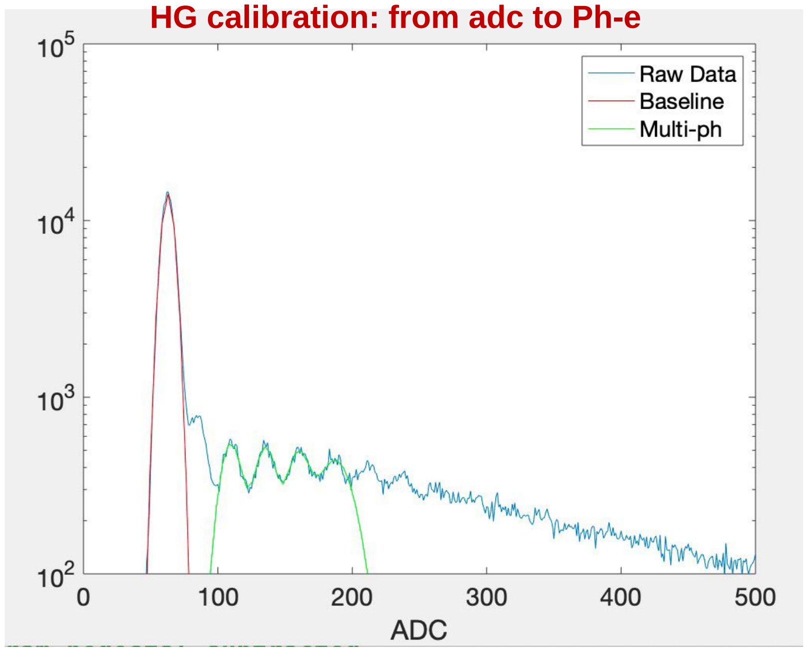


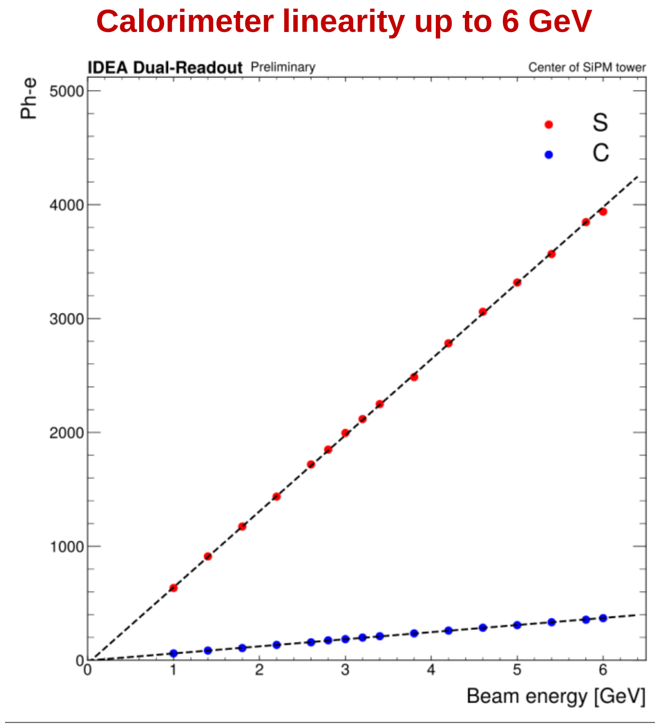


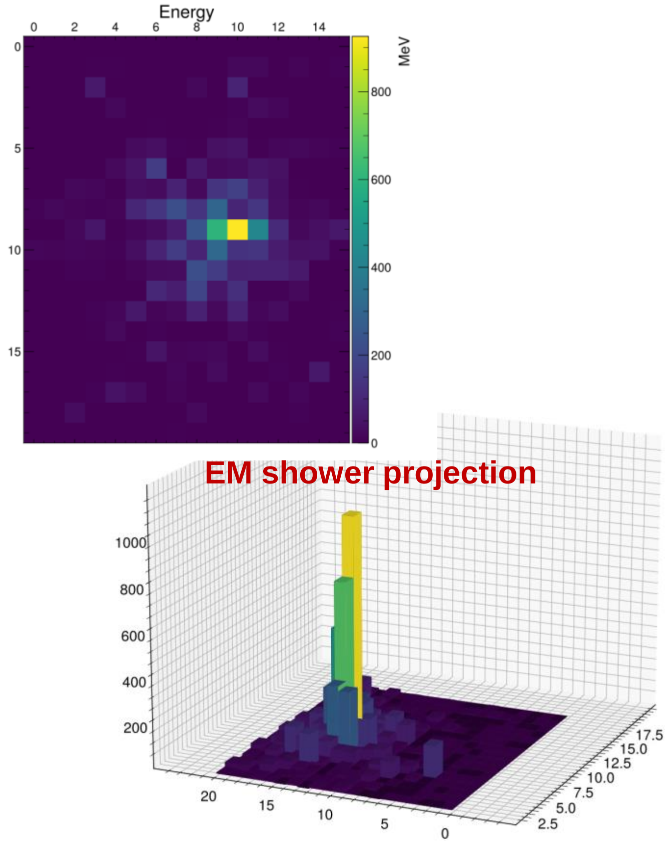
**Talk "SiPMs for dual-readout calorimetry"**
*R.Santoro – Università dell'Insubria*
Session 5 - Calorimeter Technologies for Future Colliders 1

# FERS in dual readout calorimetry

CAEN A5202 demonstrated to work for SiPM calibration and lead to excellent results in the linearity of the calorimeter response and EM shower containment



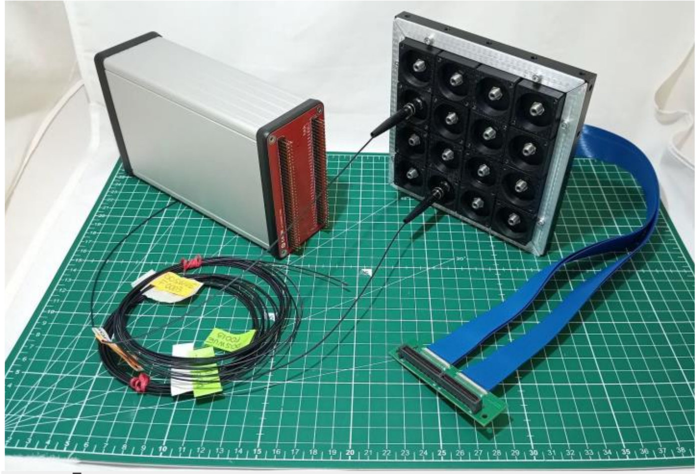



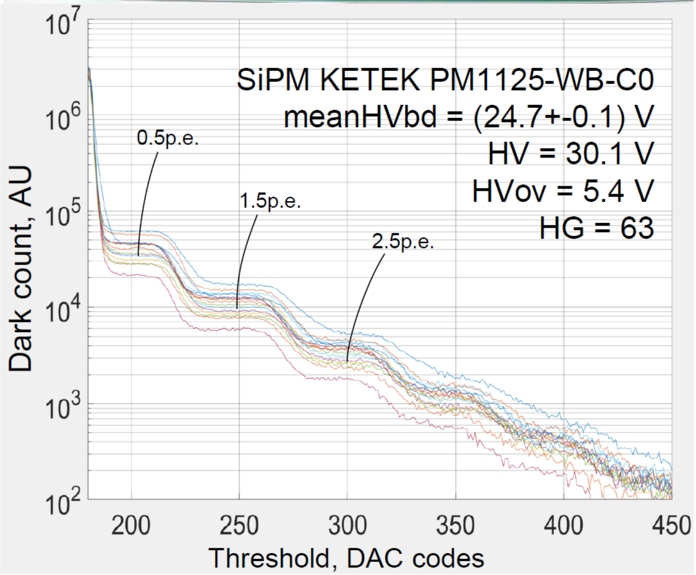

Courtesy of R. Santoro

https://indico.ihep.ac.cn/event/14967/contribution/1/material/slides/0.pdf

# FERS in ORIGIN project

- **Biomedical application:** real-time, in-vivo dosimeter imaging for oncological brachytherapy treatment
- **Standalone** desktop version DT5202 used  to readout 16/32 PMMA fibers with scintillators in their tip
- CAEN DT5202 demonstrated to have a good imaging resolution and uniformity among channels
- Close staircases, clearly-resoluted p.e. and negligible noise

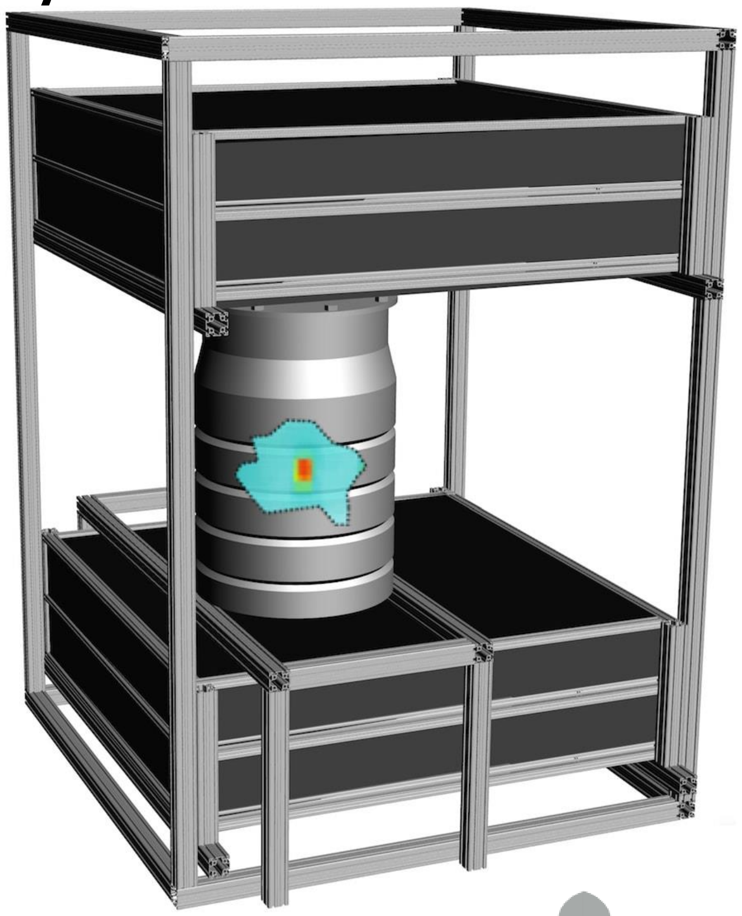





See NSS-MIC 2021 poster "Qualification of a Silicon Photomultiplier scalable readout system" (#912)

# FERS in cosmic ray tomography

- **Muon tomography scanner**, suitable for **nuclear waste characterization,** by Lynkeos Technology (Scotland)
- First design with MA-PMTs detectors and MAROC chip readout
- Device successfully deployed at Sellafield site (UK)
- Upgrading to **SiPMs** detectors in 2021 – readout electronics based on FERS



First-of-a-kind muography for nuclear waste characterization
D. Mahon *et al.*
Philos. Trans. R. Soc. A, 377 (2018), p. 0048, 10.1098/rsta.2018.0048

LYNKEOS TECHNOLOGY LTD

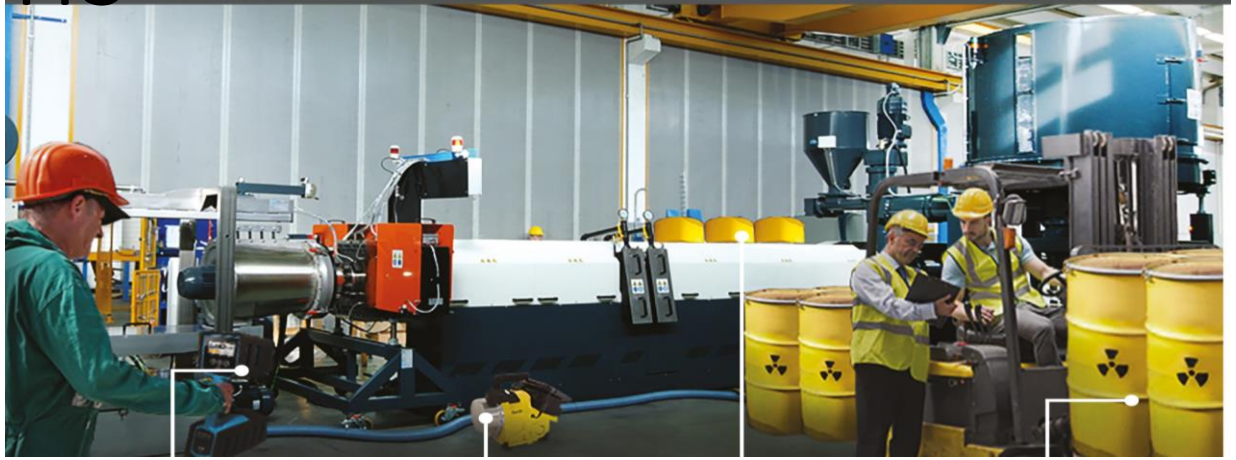
# FERS in D&D operations

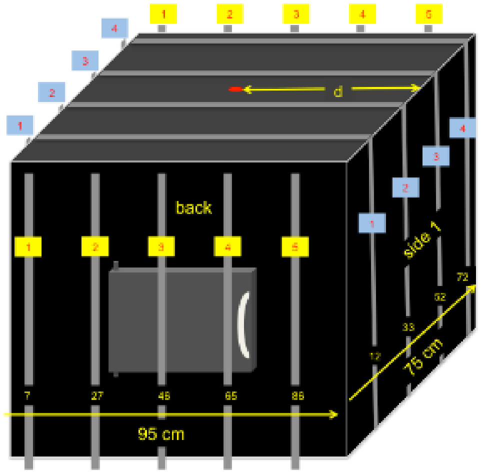
- **CAEN** is the coordinator of the **MICADO** project, aiming at developing reference processes and instrumentation for cleaning and decommissioning operations in nuclear power plants

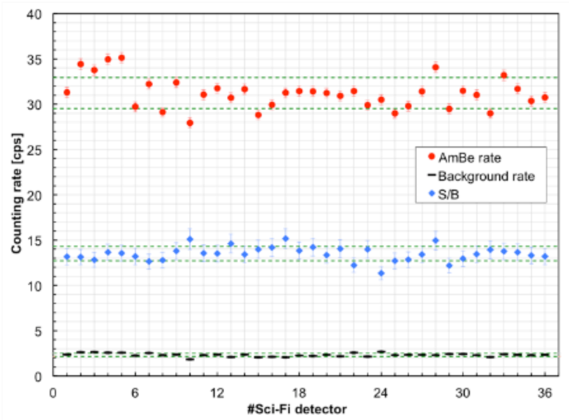
- Detection system for gammas and neutrons, based on SciFi & SiLiF detectors

- **SciFi** readout with **FERS** electronics (SiLiF with CAEN V2740)

- Thanks to the **modular** structure, the instrument can be used for the radiological monitoring of the waste during storage

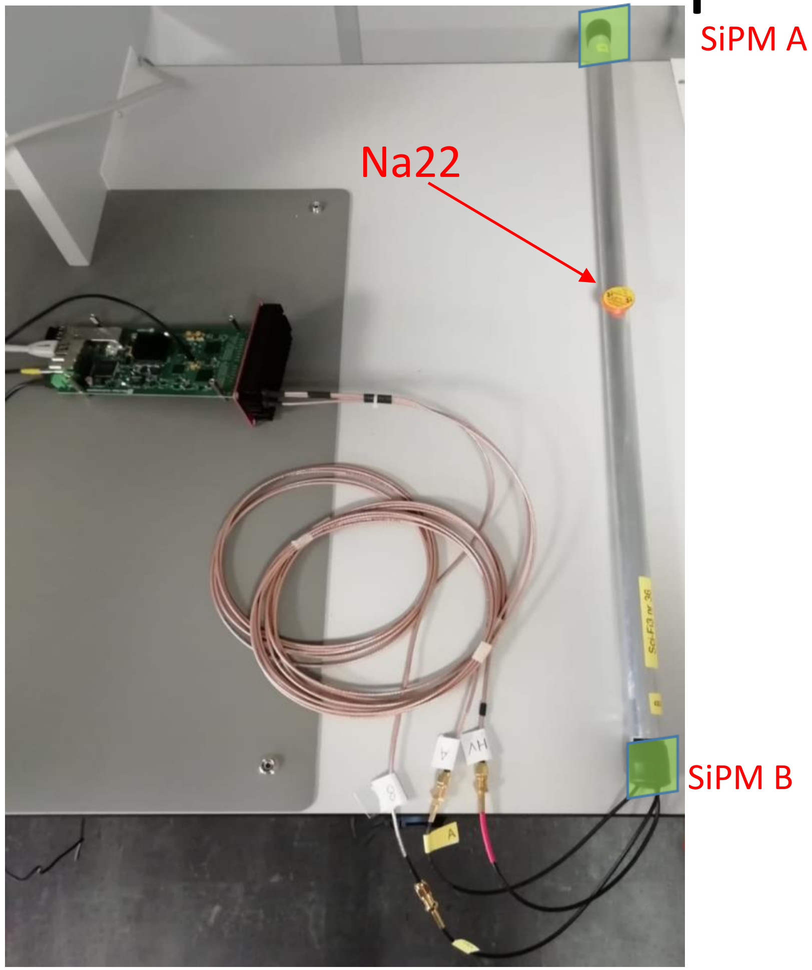




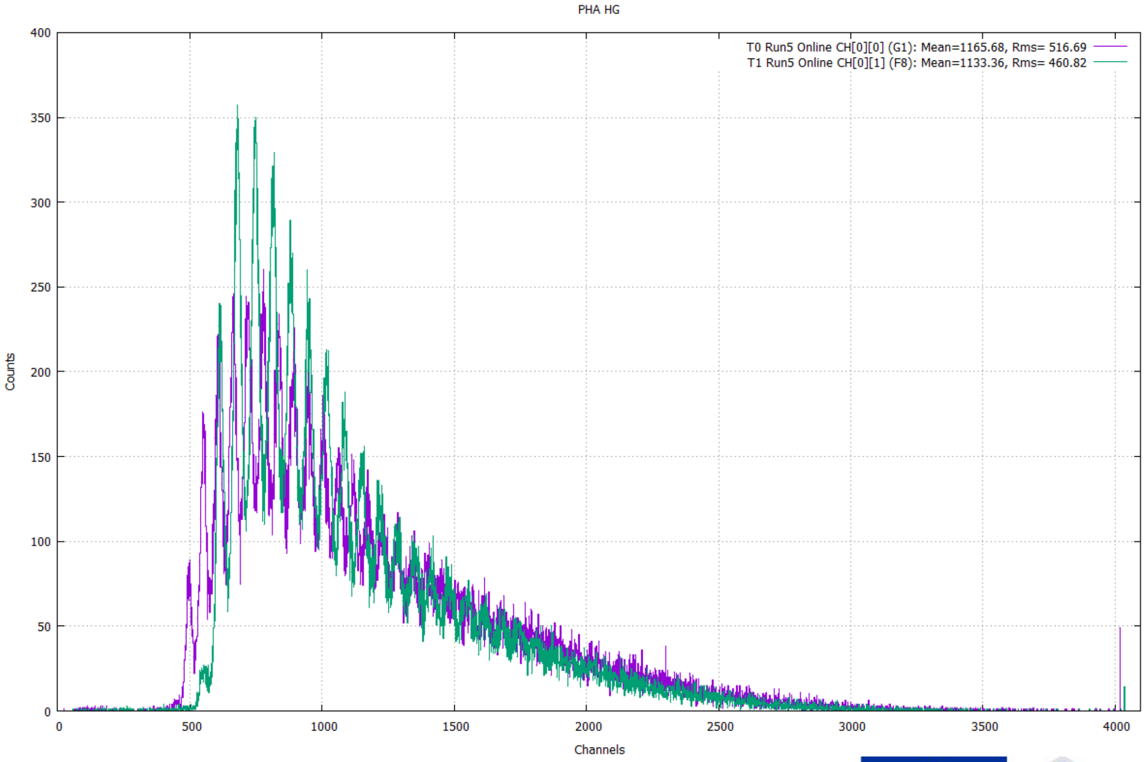




https://www.micado-project.eu/

# FERS in D&D operations




- Readout of **SiPM-coupled SciFiGamma bar** using A5253 adapter
- Coincidence trigger

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