



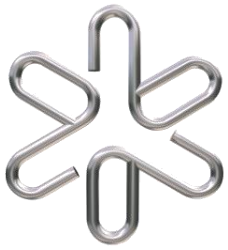
High Energy Physics and Instrumentation with the LHC-CERN



Radiation Effects in Electronic Devices

N. H. Medina

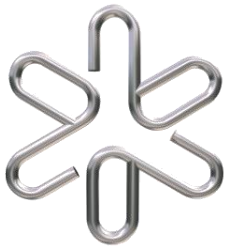
Instituto de Física da Universidade de São Paulo



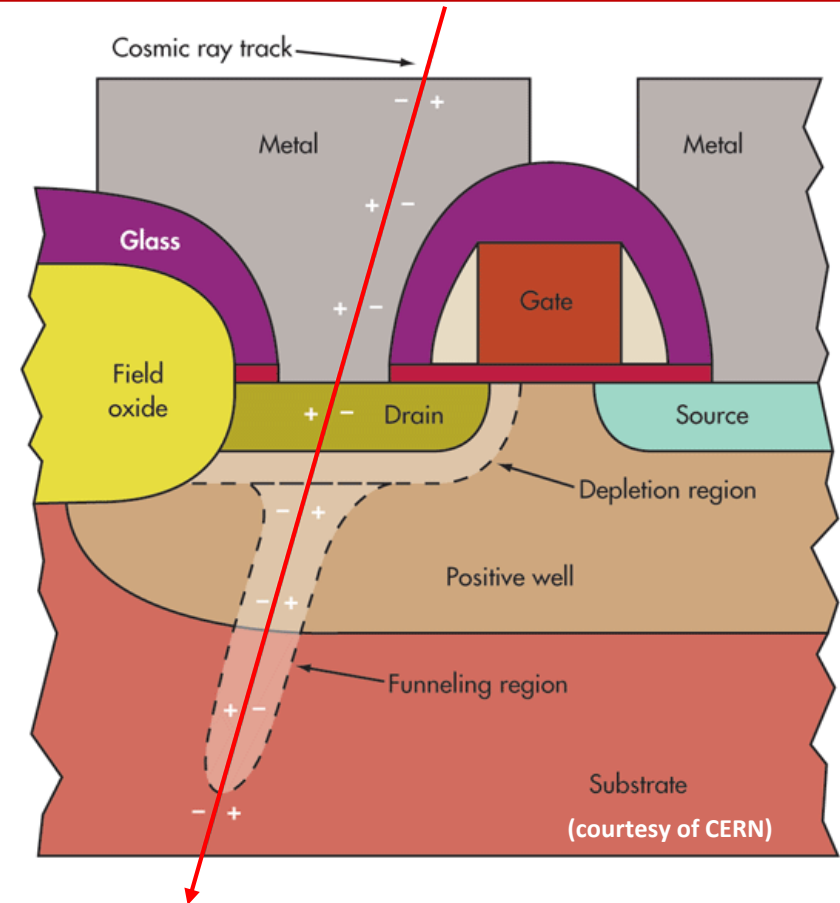
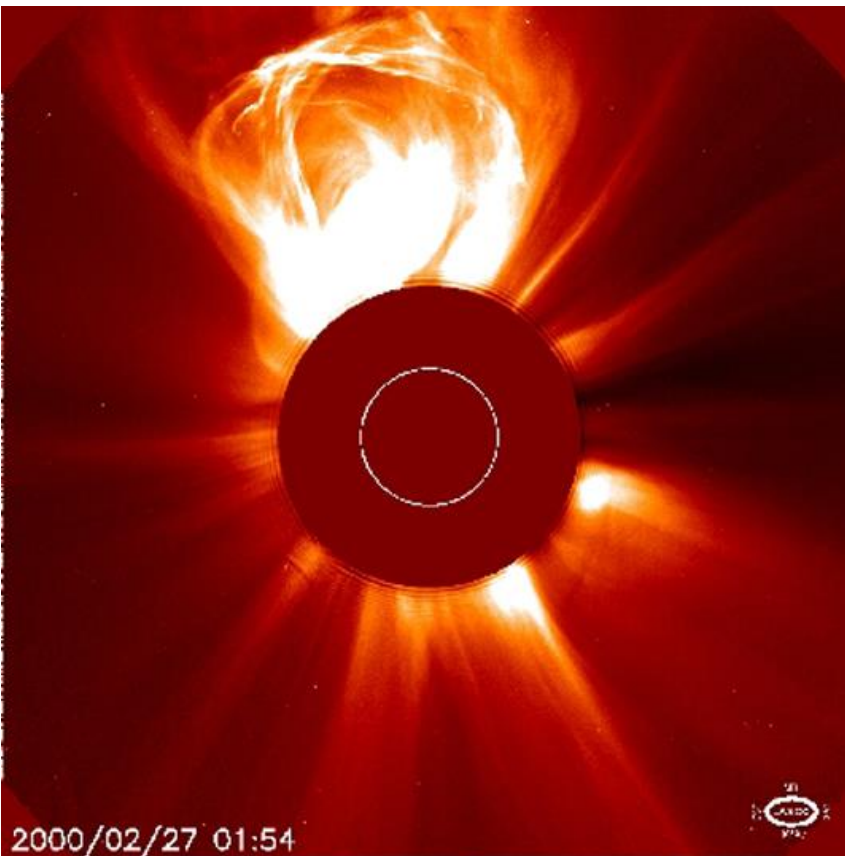
OUTLINE



- *Radiation effects in electronic components*
- *Measurement examples.*
- *New beam line for Applied Nuclear Physics*



Coronal Mass Ejection

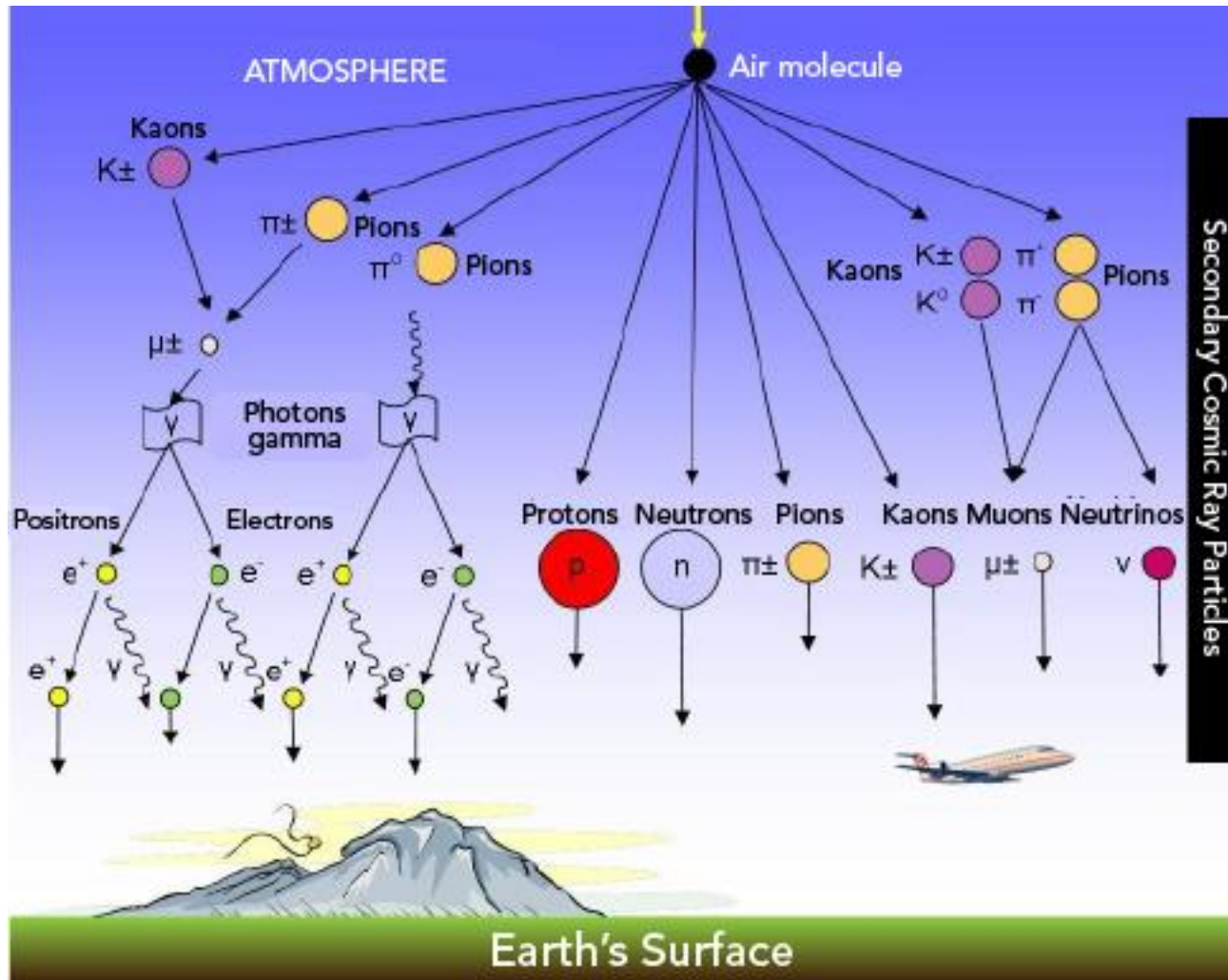


A Coronal Mass Ejection (CME) blasts into space a billion tons of particles traveling millions of km/h, impacting any planet or spacecraft in its path.

Credit: A coronal mass ejection on Feb. 27, 2000 taken by SOHO LASCO C2 and C3 (SOHO ESA & NASA) and Rudolf R. Bühler

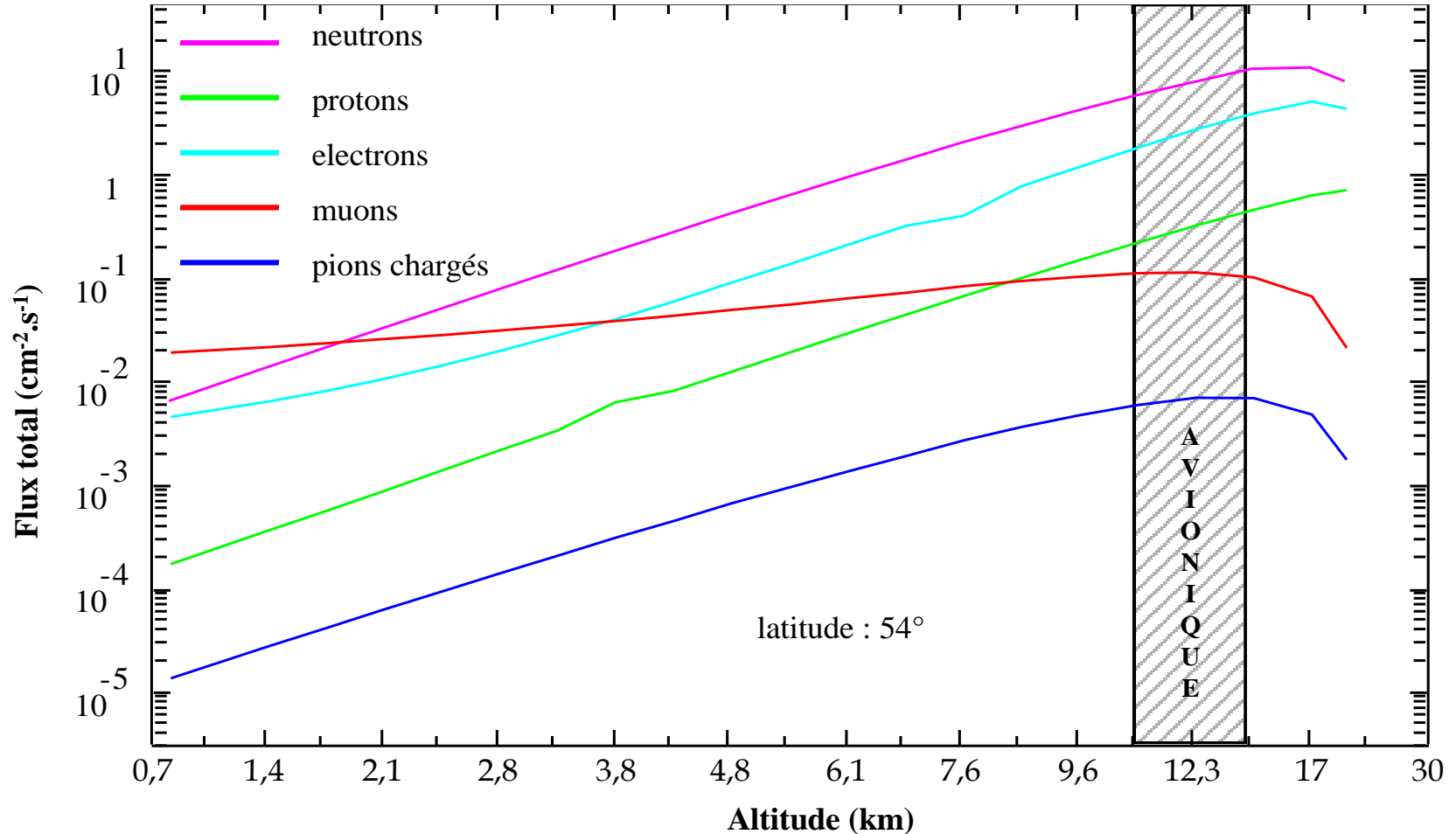


Neutron production in Atmosphere



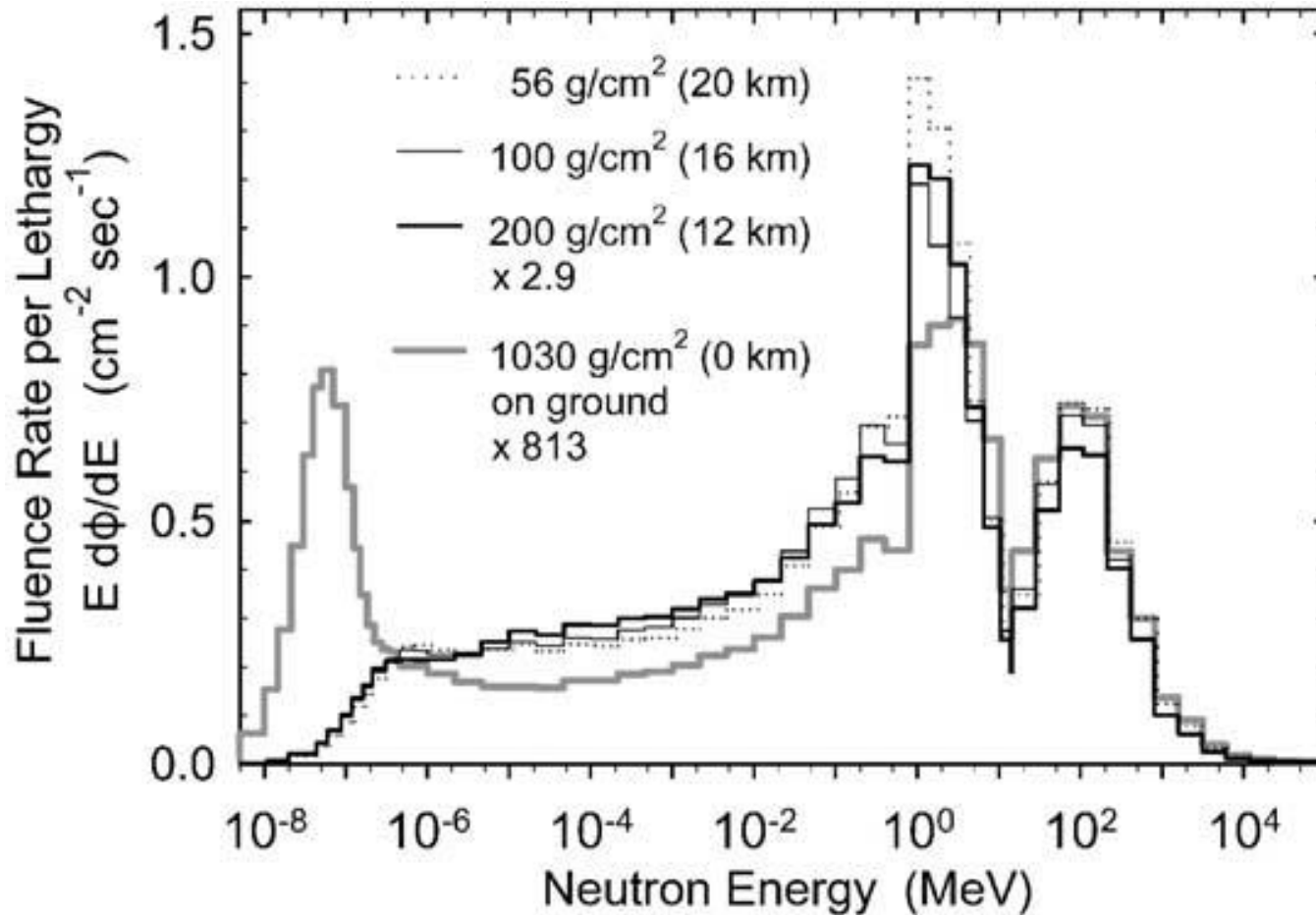


Charged Particles and Neutron Flux





Neutron fluence at different altitudes





Neutron Flux Simulation inside the MAGNEX Experimental Hall



A dedicated simulation was performed with the FLUKA code in order to evaluate the radiation spectra and fluence as a function of the topology of the detectors inside the MAGNEX experimental hall at LNS.

Four radiation sources were considered :

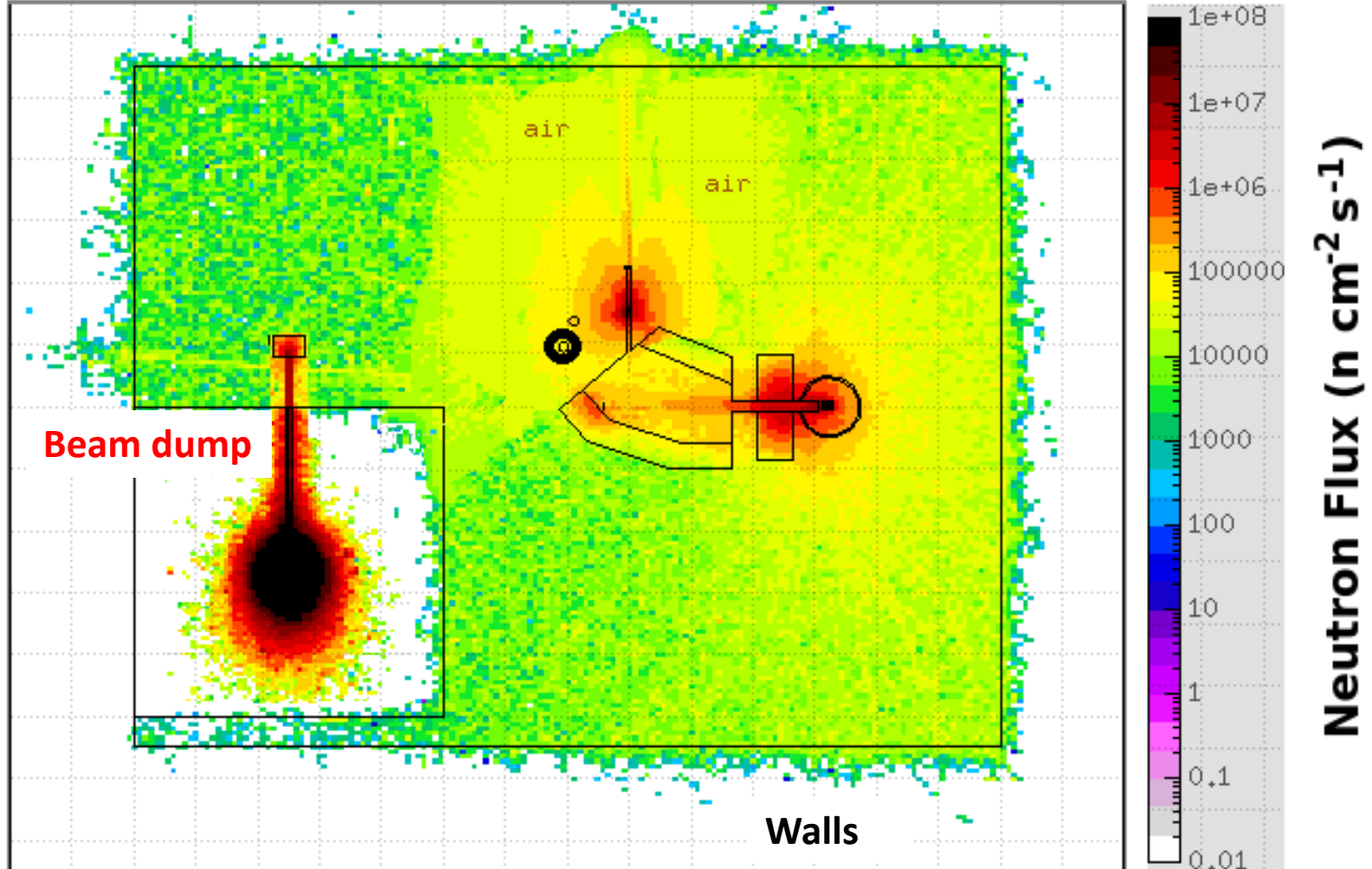
- **Beam-target interaction;**
- **Leakage** along the transport of beam line;
- **Beam - beam stopper** interaction.
- **Secondary radiation** induced by neutron interactions with the material inside the experimental hall, including its walls, floor and ceiling.

The ^{20}Ne beam interaction with a ^{76}Ge target with ^{12}C backing was simulated

Fully stripped ^{20}Ne beam with an energy of **60 MeV/A** and a current of **85 e μ A**
The beam dump is inside a concrete bunker.

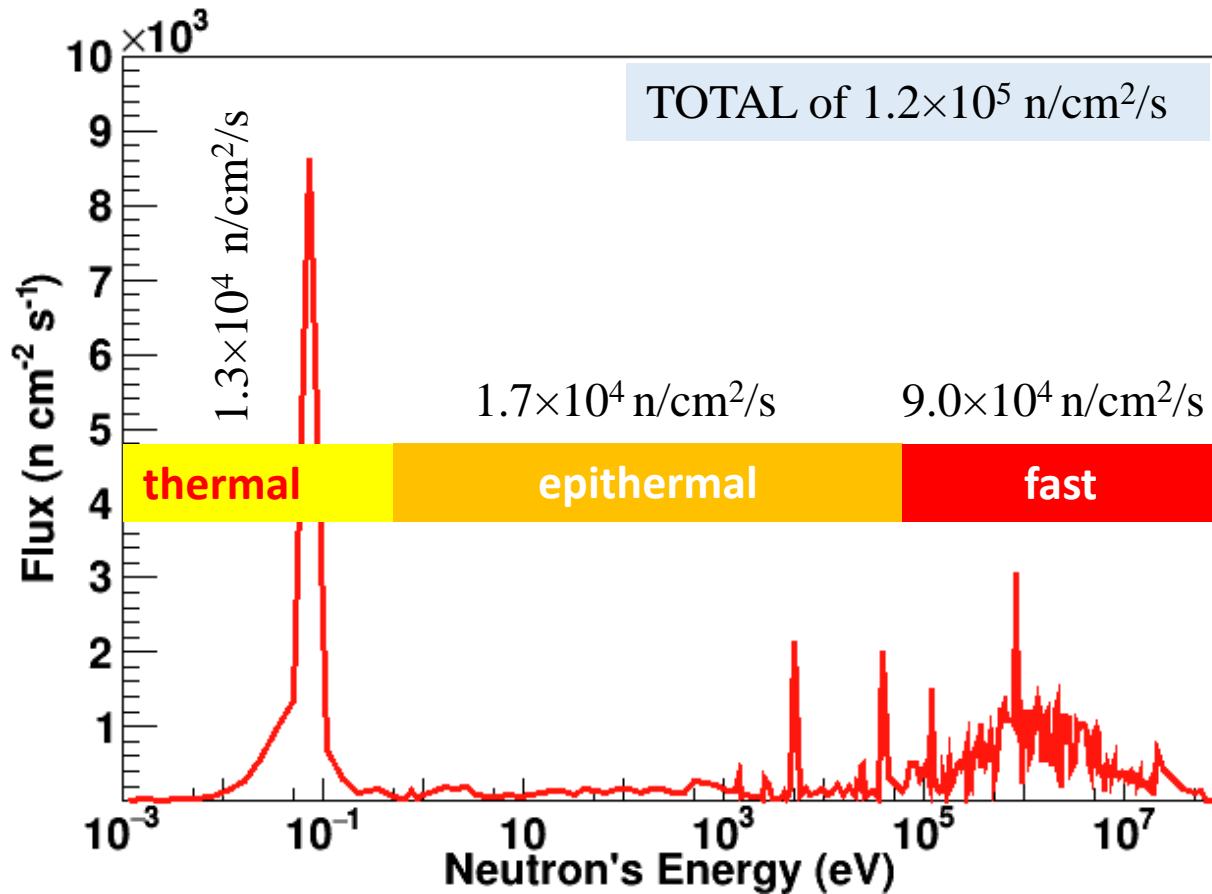


Neutron Flux inside the MAGNEX Experimental Hall

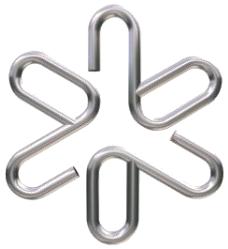




Simulated Neutron Energy Spectrum

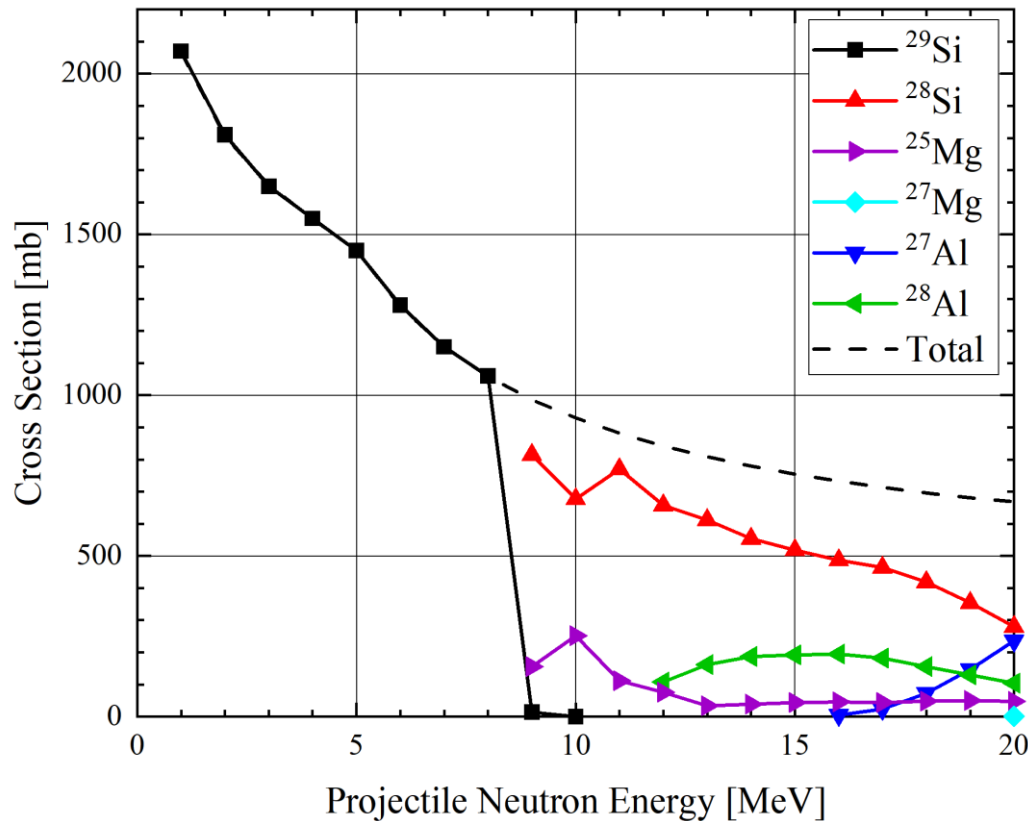


Neutron energy spectrum obtained via FLUKA simulations for the region where the MAGNEX focal plane detector is located



Neutron-induced Nuclear Reactions

Fusion-evaporation Monte Carlo Calculations

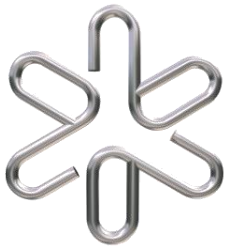


neutron + ^{28}Si $E=14$ MeV

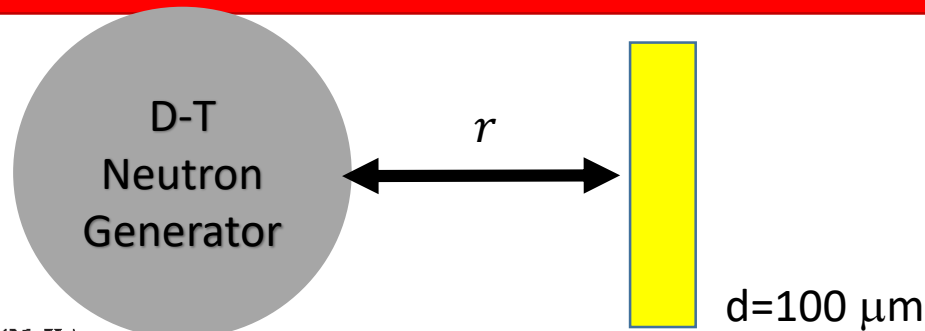
$n + ^{28}\text{Si} \rightarrow n + ^{28}\text{Si}$ Elastic scattering

$n + ^{28}\text{Si} \rightarrow p + ^{28}\text{Al}$

$n + ^{28}\text{Si} \rightarrow \alpha + ^{25}\text{Mg}$



Silicon Surface Barrier Detector



Neutron rate (4π): $1.58(5) \times 10^8 \text{ n/s}$

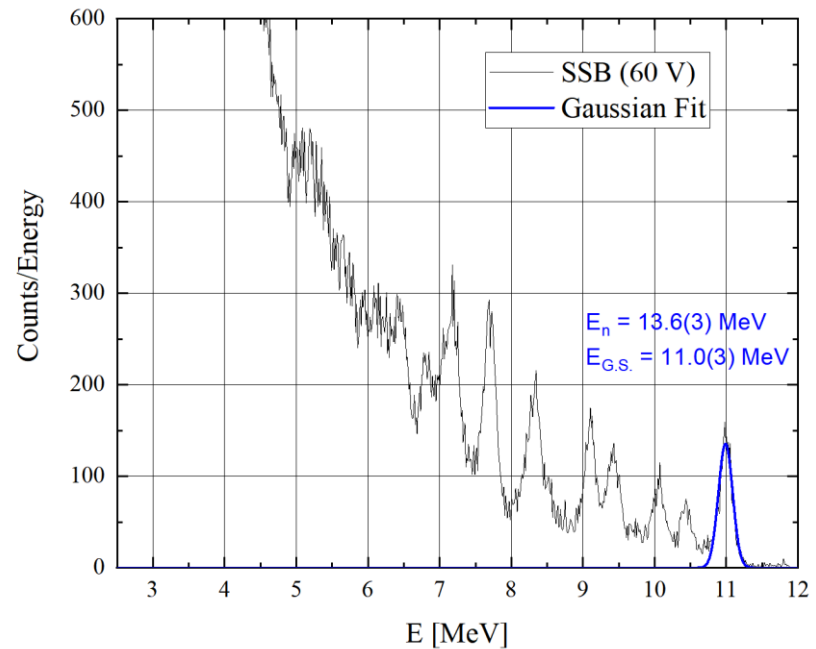
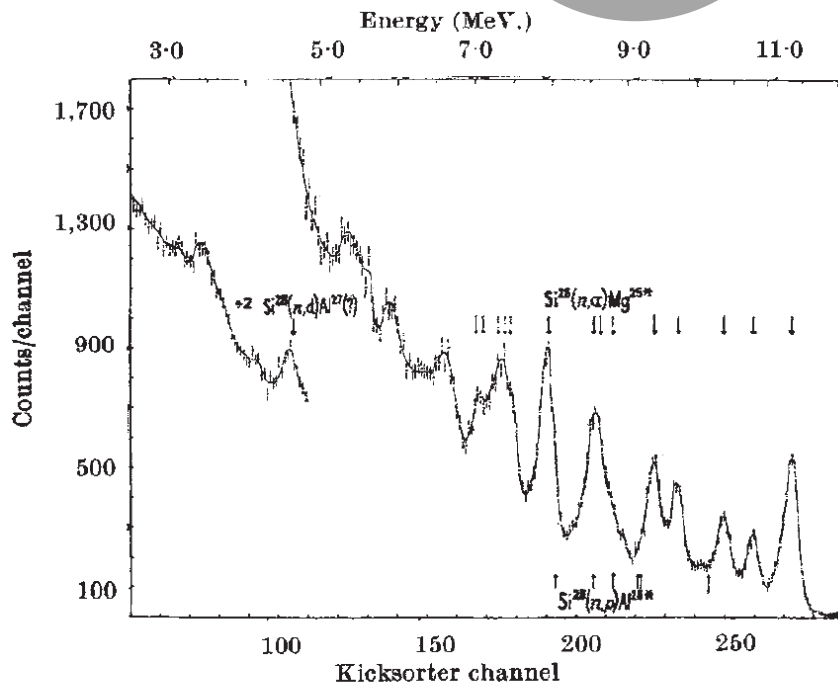


Fig. 1. Energy spectrum observed from interaction of 14.03 MeV. neutrons with a silicon surface barrier detector



Excited states of nuclear reaction channels



Neutron energy: 13.64 MeV

^{25}Mg (NuDAT 2.8)

$Q = -2.654$ MeV (CATKIN)

E_{exc} [MeV]	E_{peak} [MeV]
-----------------	------------------

0.00	10.99
------	--------------

0.59	10.40
------	--------------

0.97	10.01
------	--------------

1.61	9.38
------	-------------

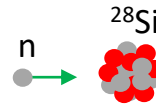
1.96	9.02
------	-------------

2.56	8.43
------	-------------

2.74	8.25
------	-------------

2.80	8.19
------	-------------

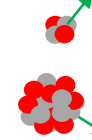
3.41	7.58
------	-------------



compound nucleus

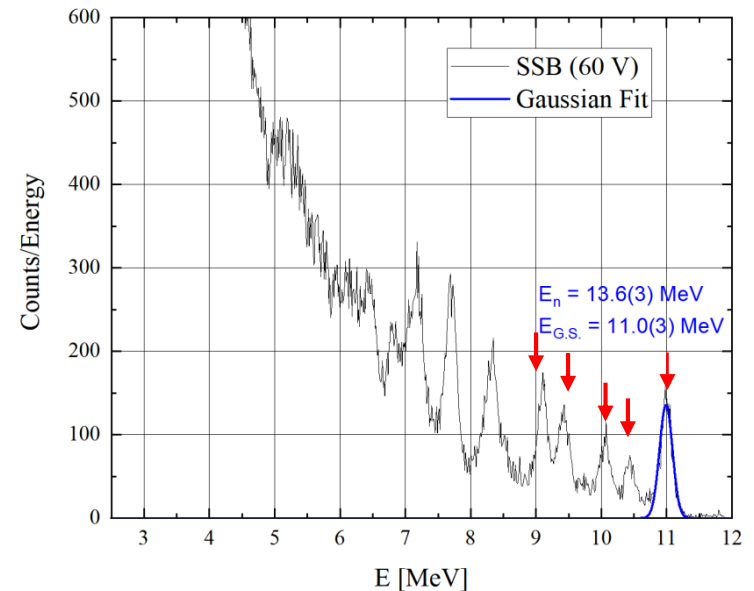
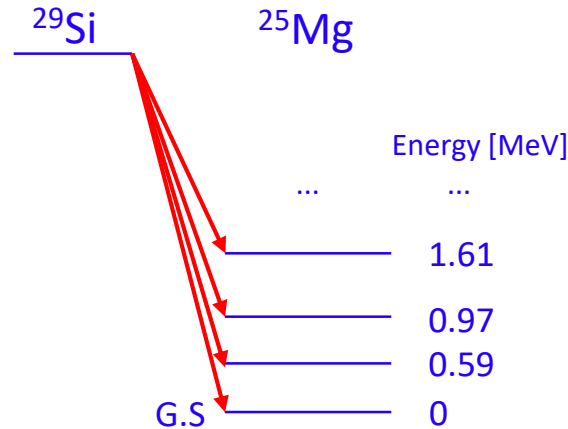


ground state/
excited state



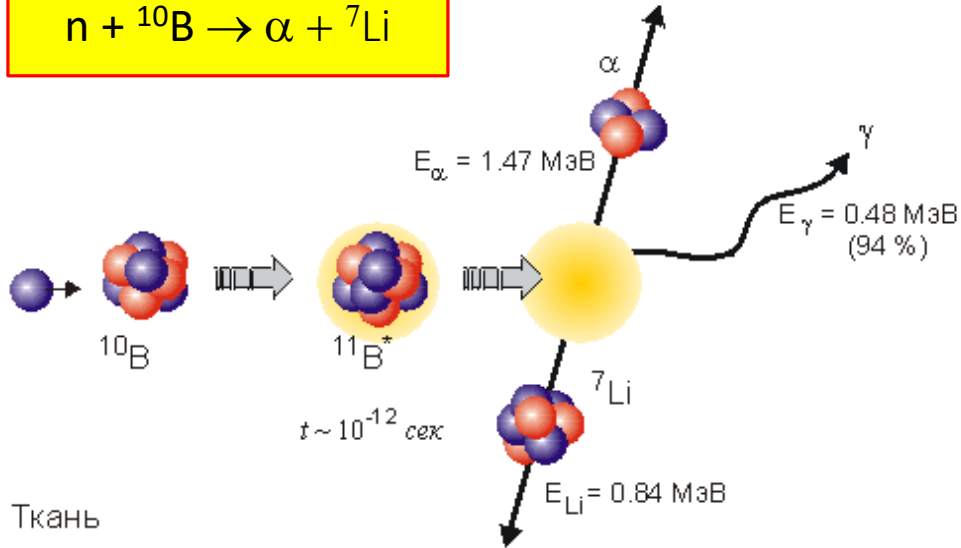
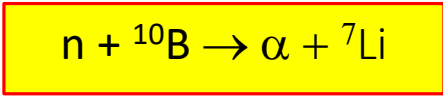
^4He

$^{25}\text{Mg} / ^{25}\text{Mg}^*$





H



Ткань

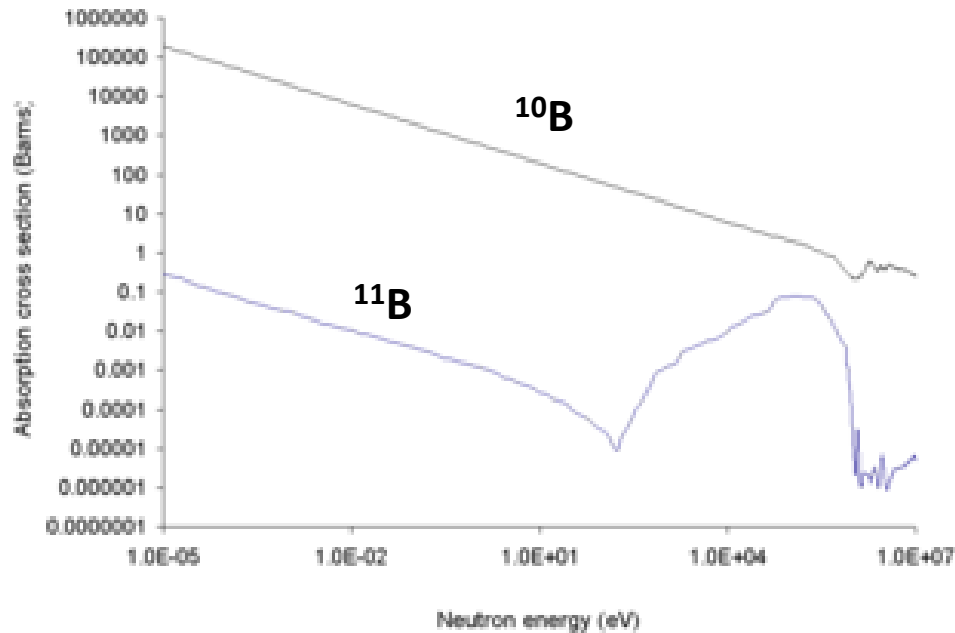
S



$E \sim \frac{3}{2}kT$

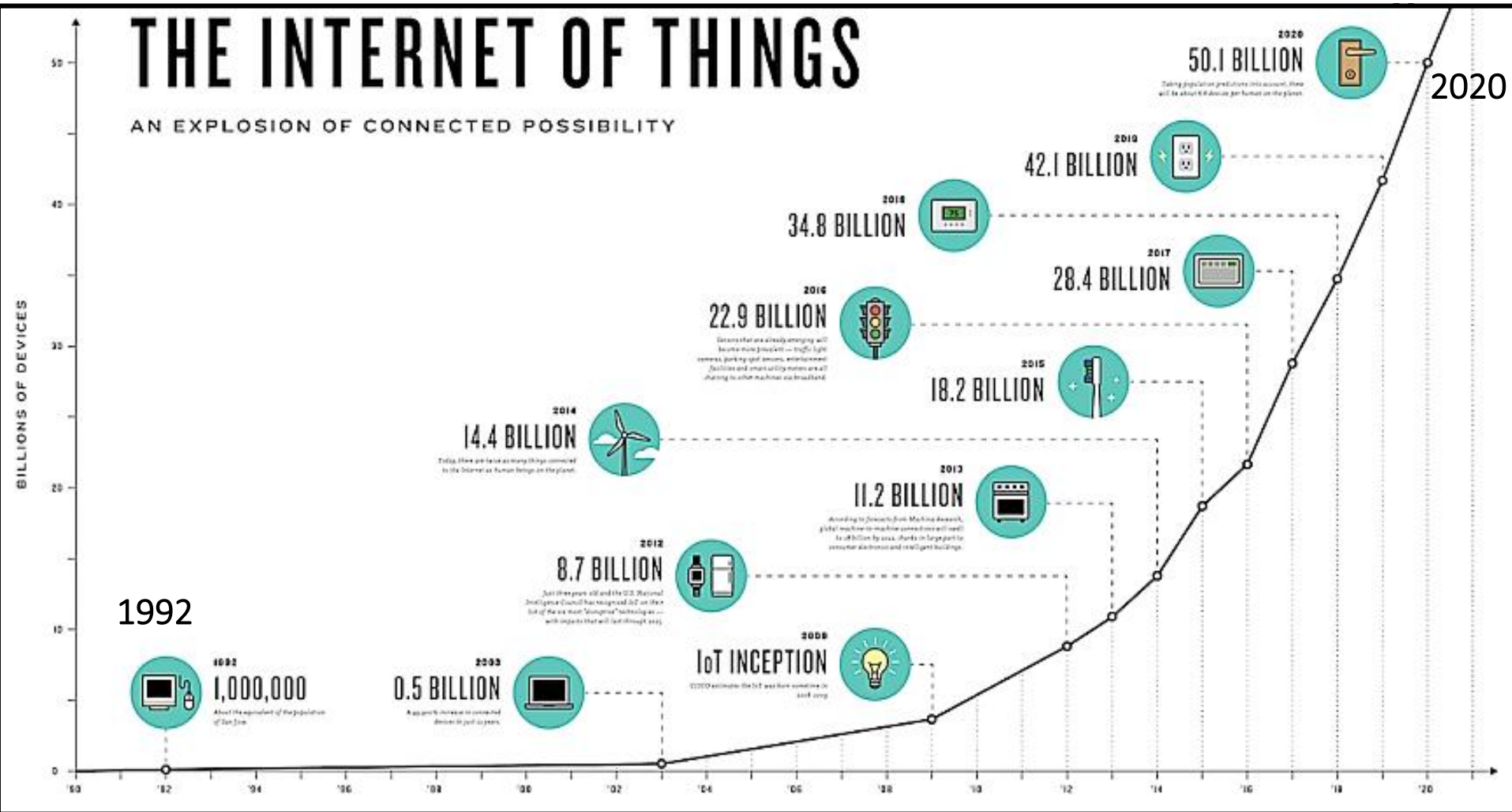
Other enviro

- Ma
- Syn
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- sen



THE INTERNET OF THINGS

AN EXPLOSION OF CONNECTED POSSIBILITY



The number of transistors per chip increases exponentially thanks to the exponential decrease of the transistor size.

Intel's Stratix-10 has the largest transistor count, containing over 30 billion transistors.



All the Electronic Devices May Suffer from Radiation Effects



Accelerator experimental hall

Space Environment

Ground High Radiation Environment

α -particle emission from radioactive contaminants

**Particle and electromagnetic radiation
Ionizing and non-ionizing dose**

Degradation of:

**Micro-electronics, micro-processors, optical components,
semiconductor detectors, front-end electronics, cabling, etc**

Causing:

System shutdowns

Circuit damage

Data corruption, etc



Radiation effects in electronic devices

TID, DD, and SEE



Electromagnetic radiation, electrons, protons, neutrons and heavy ions

Total Ionizing Dose is a cumulative effect caused by trapped charges in the oxide. These trapped charges modify the transistor characteristics such as threshold voltage (V_{th}), mobility, leakage current, power dissipation, etc.

Atom Displacement Damage is provoked by protons, heavy ions, electron with high energy and neutrons, which change the arrangement of atoms in the lattice, modifying electrical properties of a device.

Single Event Effects are caused by particles of high LET (Linear Energy Transfer) due to, for example, the **strike of a single ion**. They can be non-destructive, causing current or voltage peaks, changing the state of a bit, or destructive, burning the device or destroying the gate oxide in a MOSFET.



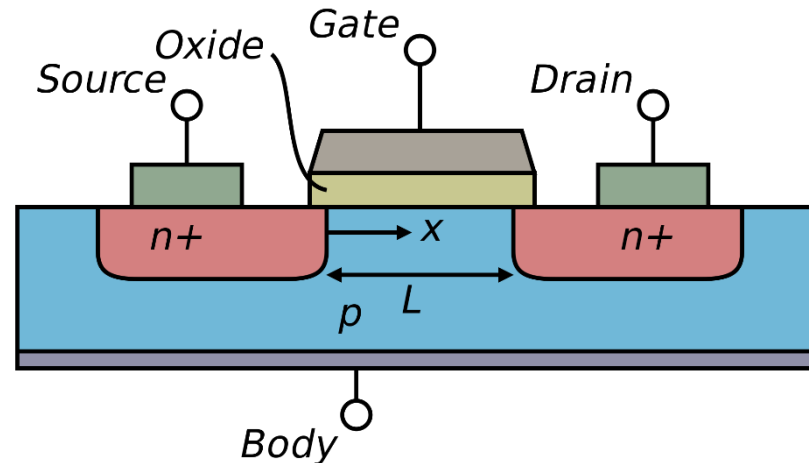
Radiation Effects

Total Ionizing Dose



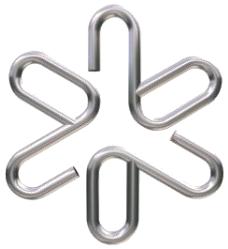
Cumulative effect due to the ionization in the SiO_2 due to neutrons, protons, gamma rays, X rays, heavy ions and electrons.

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)



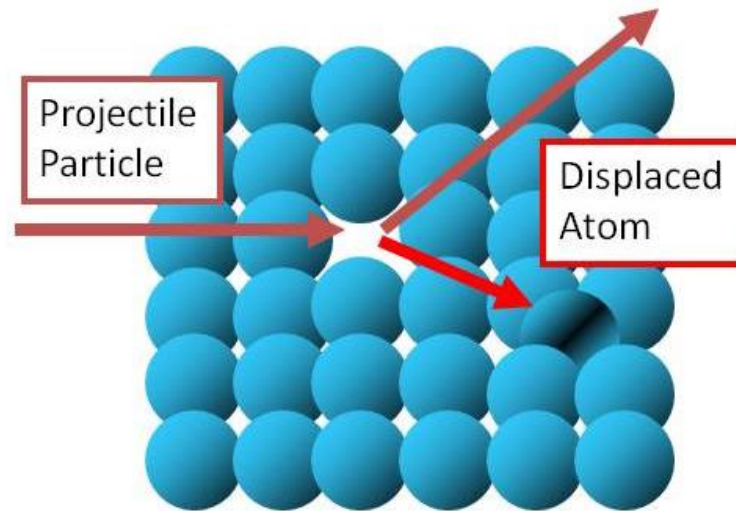
Applied voltage through the gate allows current to flow from source to drain.

Ionization in SiO_2 creates electron-hole pairs which induces defects in transistors. These **trapped charges modify the transistor characteristics** such as threshold voltage (V_{th}), mobility, leakage current, power dissipation, etc.



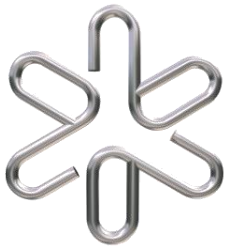
Displacement Damage

Non-Ionizing Energy Loss



Originated from nuclear interactions, typically scattering, which cause lattice defects. Displacement damage is due to a cumulative long-term non-ionizing damage from **neutrons**, protons, and electrons. The collision between an incoming particle and a lattice atom subsequently displaces the atom from its original lattice position

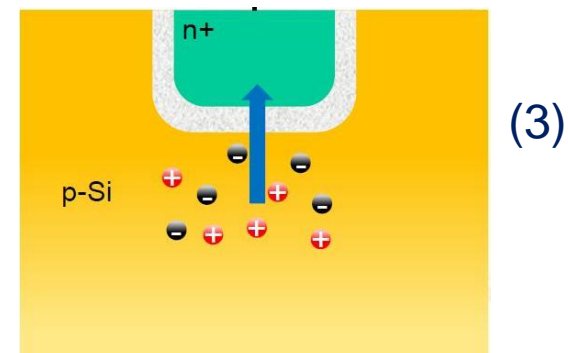
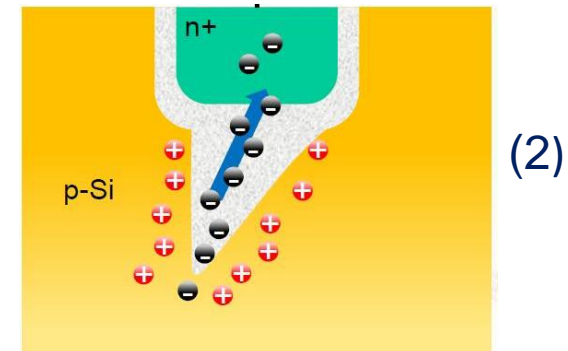
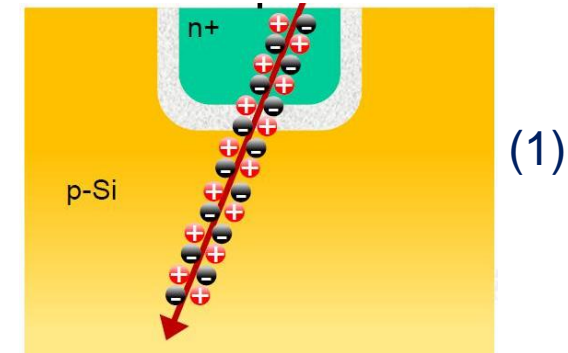
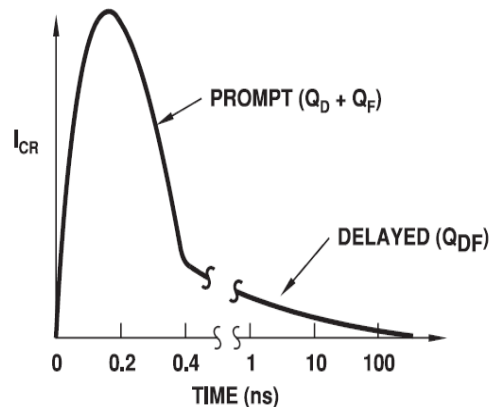
Stable defects in crystalline lattice (vacancies and interstices) modify electrical properties of electronic devices.



Single Event Effects



- Charge deposition induced by a heavy ion interaction within a sensitive volume, followed by the charge collection at the output node of the circuit.
- High-LET particles generates a track of electron-hole pairs in semiconductor (Si) and dielectric (SiO_2).
- 1 MeV deposited \longrightarrow $2.8 \cdot 10^5$ pairs
 \longrightarrow 44.5 fC
- Charge collection occurs in three steps: drift (1), funnel (2) and diffusion (3)



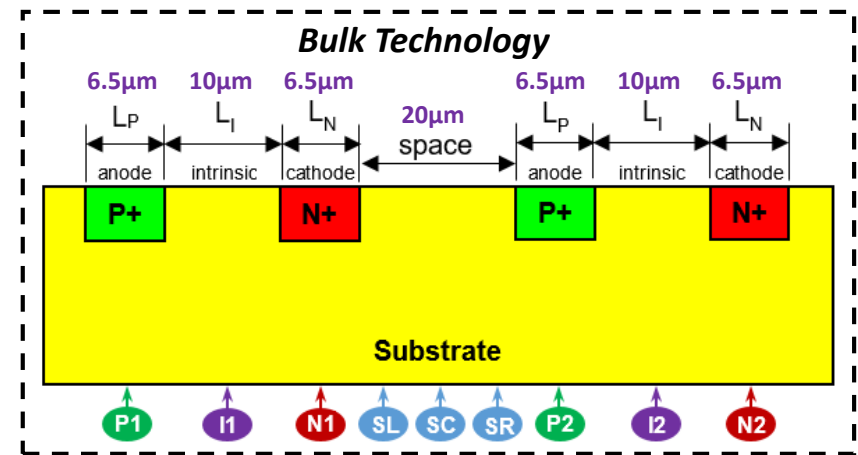
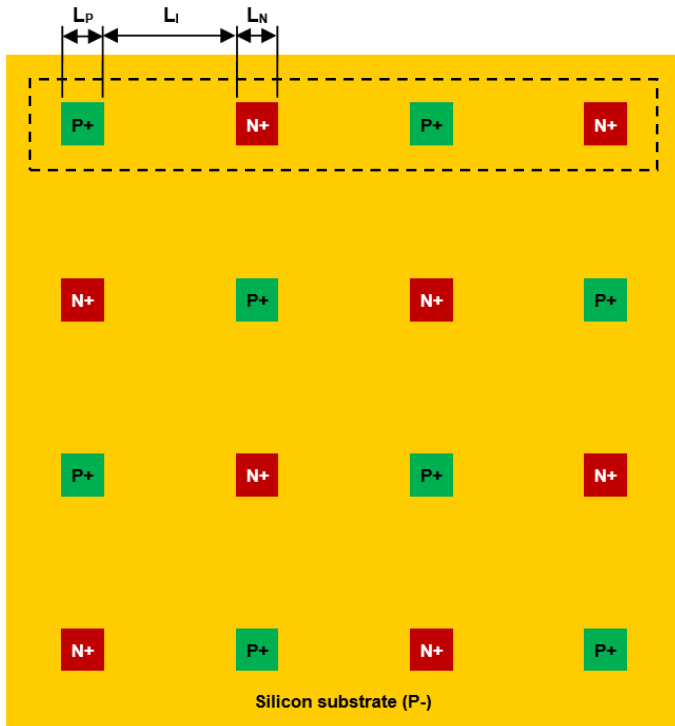


PIN DIODE SIMULATION

GF BiCMOS 8HP 130 nm technology



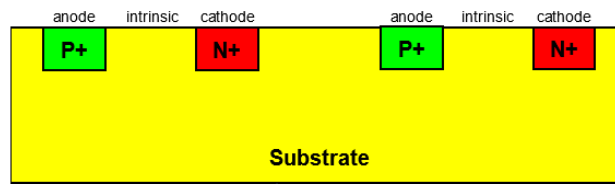
Proposed Array



SEE Parameters:

- Heavy-Ion LET = 10 MeV/mg/cm²
- Particles Strike vertically at specified positions

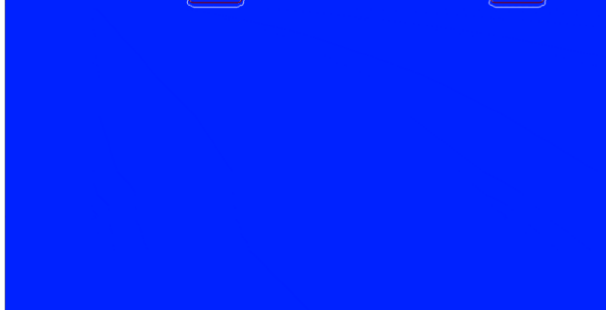
Incident Particle – 10 MeV/mg/cm² Calculations by Rudolf R. Bühler (FEI)



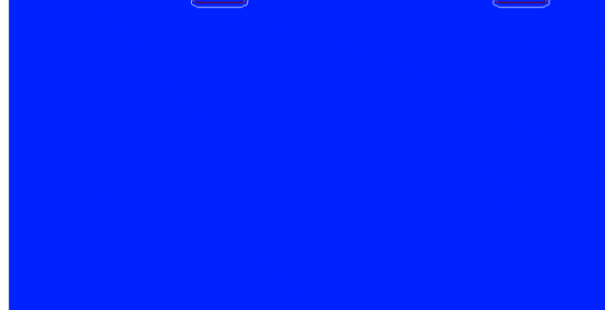
Abs Total
Current Density
[A/cm²]



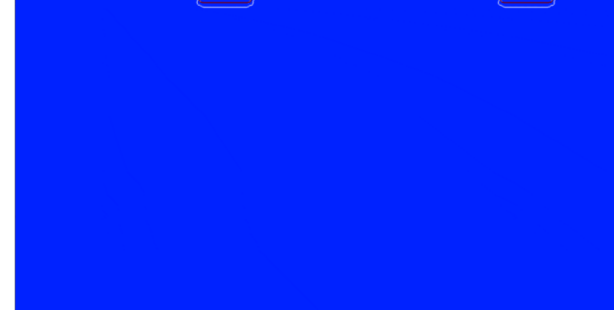
↓
P1 I1 N1 SL SC SR P2 I2 N2



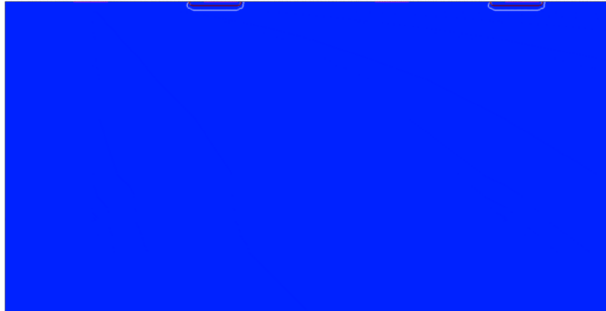
↓
P1 I1 N1 SL SC SR P2 I2 N2



↓
P1 I1 N1 SL SC SR P2 I2 N2



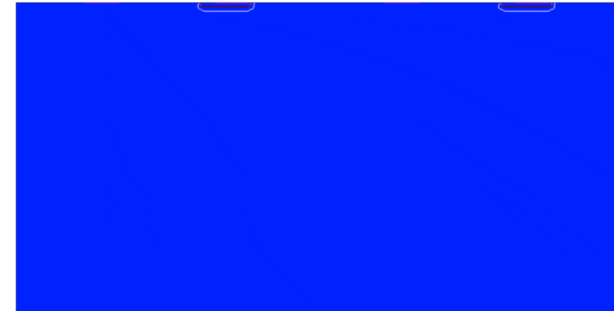
↓
P1 I1 N1 SL SC SR P2 I2 N2



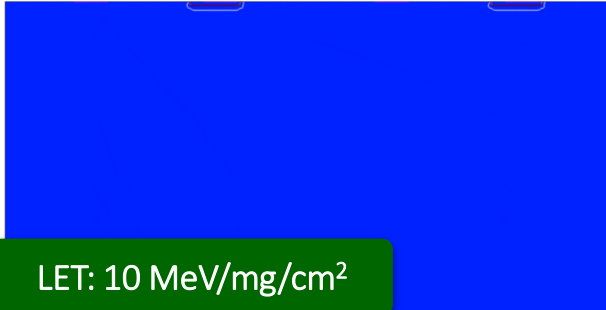
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P1 I1 N1 SL SC SR P2 I2 N2



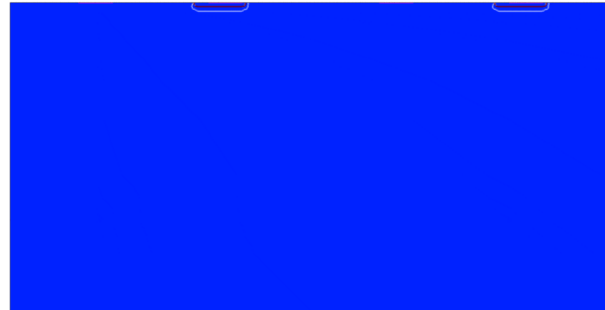
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P1 I1 N1 SL SC SR P2 I2 N2



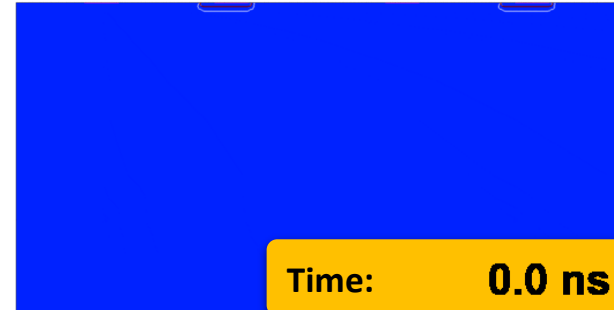
↓
P1 I1 N1 SL SC SR P2 I2 N2



↓
P1 I1 N1 SL SC SR P2 I2 N2



↓
P1 I1 N1 SL SC SR P2 I2 N2



LET: 10 MeV/mg/cm²

Time: 0.0 ns



Single Event Effects



Non-destructive Effects

Single event upset (SEU)

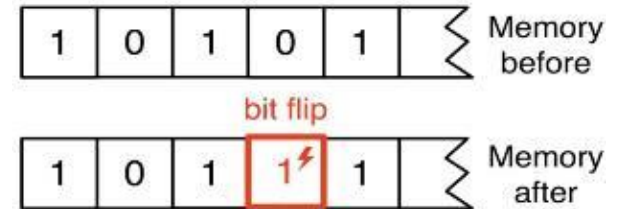
e.g. memory bit-flip (logic error)

Single event transient (SET)

A transient effect (voltage/current pulses) which may provoke a SEU

Single event functional interrupt (SEFI)

Logical malfunction in programmable devices



Destructive Effects

Single event latch-up (SEL)

high current flux overheated power transistors,
affecting e.g. CMOS devices

Single event gate rupture (SEGR)

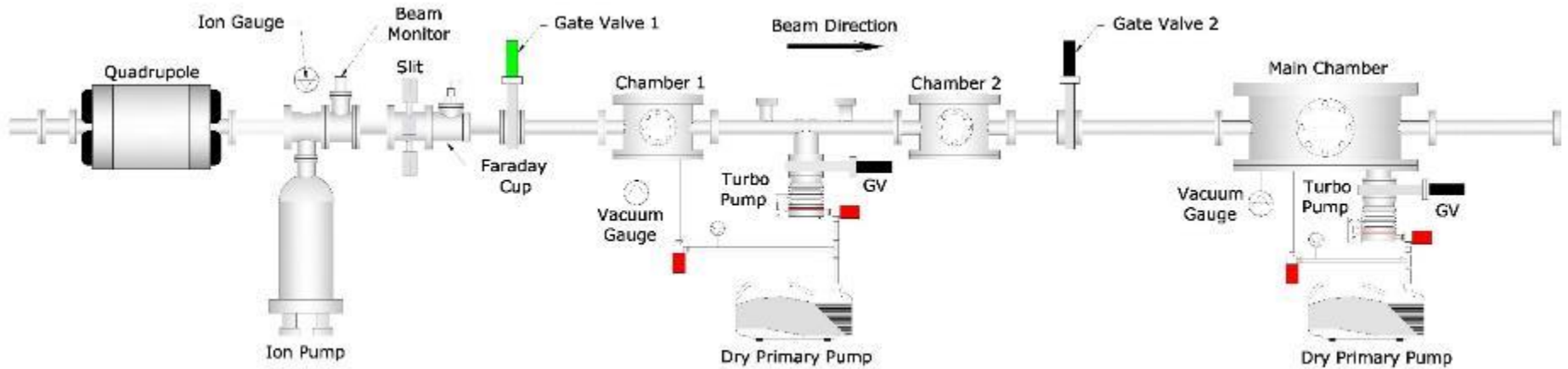
dielectric breakdown of the oxide layer of a MOSFET

Single event burnout (SEB)

Similar to SEL. The high current damage irreversibly,
e.g. power MOSFET



New beamline for SEE tests



Beam optics simulation

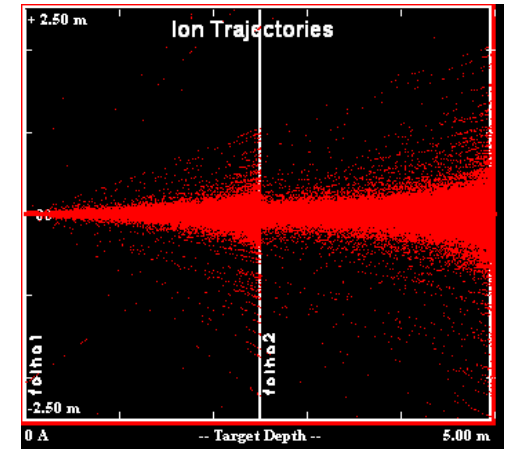
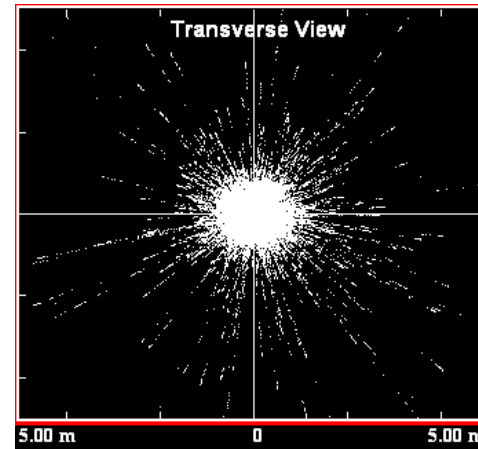
ESA requirements:

Flux 100 to 100,000 part/cm²s

Fluence 10⁶ to 10⁷ part/cm²

< 10% uniformity variation

30 μm depth

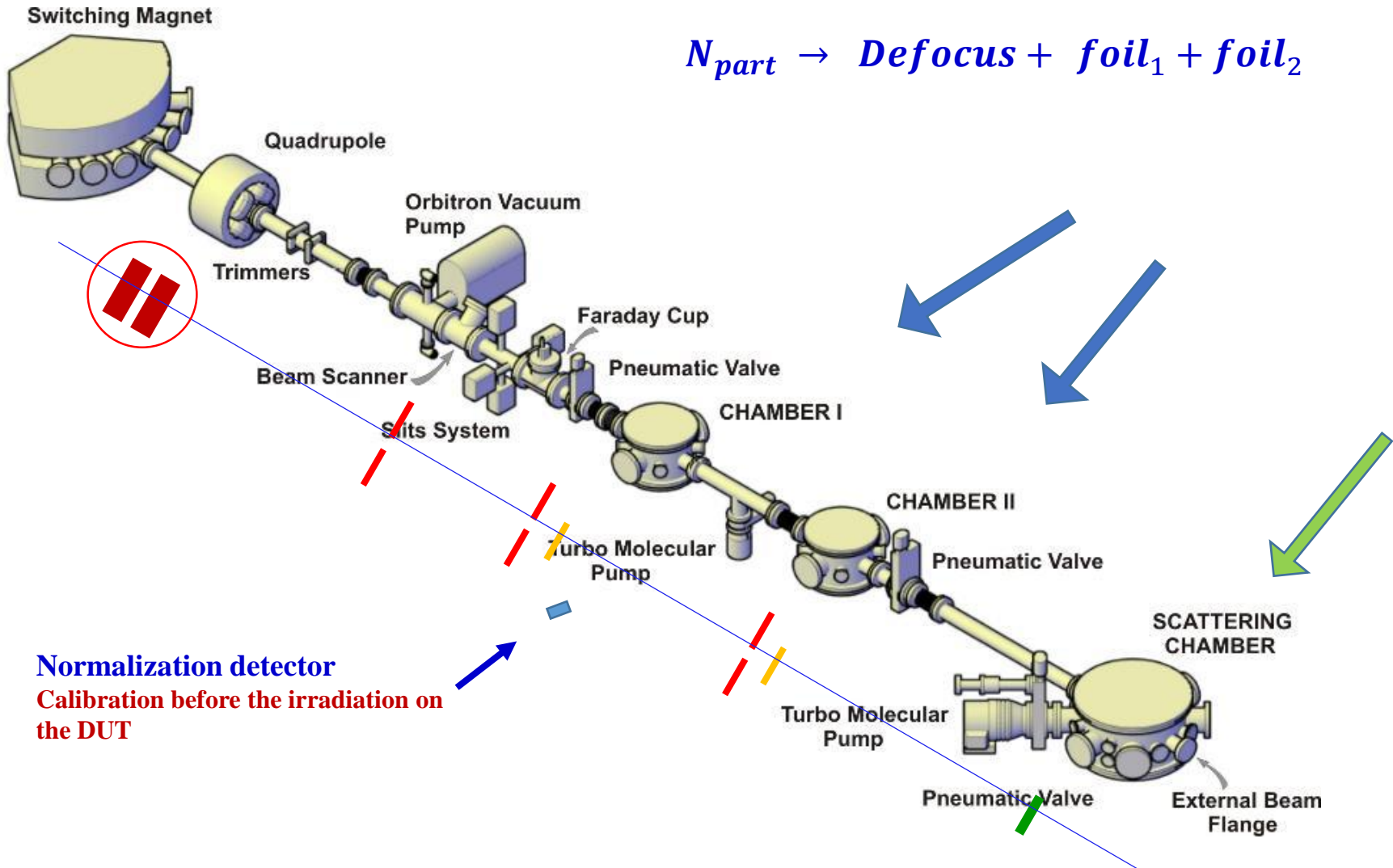




Beam Line Project

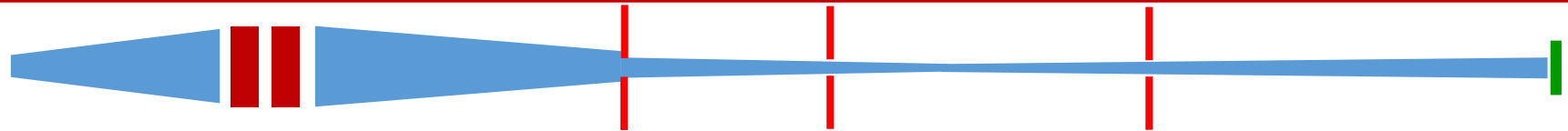


$$N_{part} \rightarrow Defocus + foil_1 + foil_2$$





Particle flux control



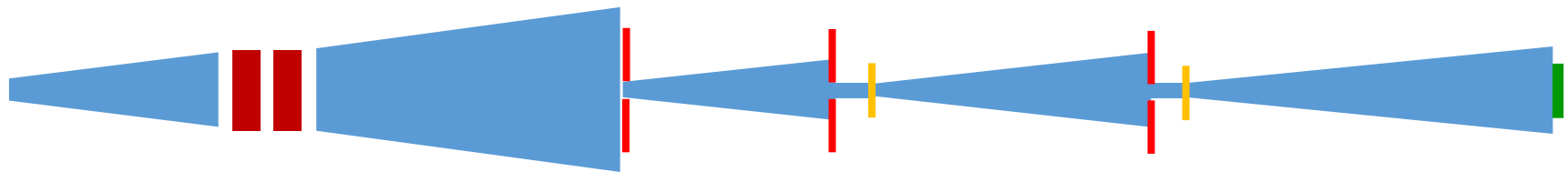
Focalization – no foils

$10^9 - 10^{11}$



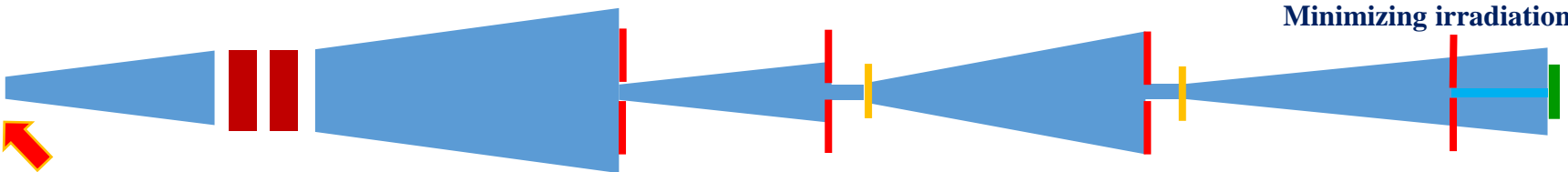
Focalization – with gold foils

$10^5 - 10^7$



Defocalization – with gold foils

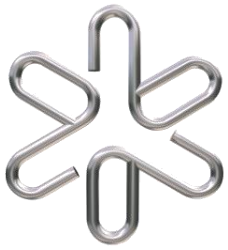
$10^3 - 10^4$



Minimizing irradiation area

$10^2 - 10^3$

Reducing the beam before the beam line



Performed Measurements



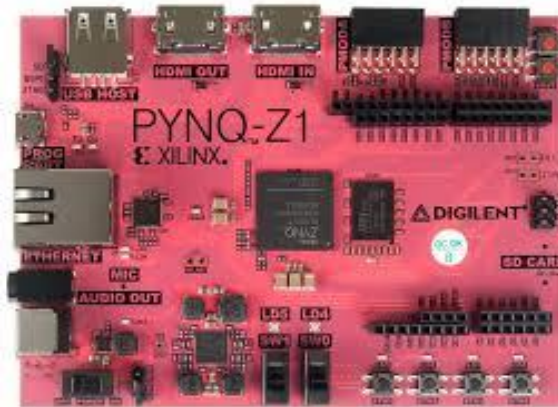
Analogic devices

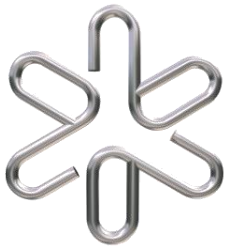
- 3N163 transistors
- Power Transistors
- Pin diode
- Solar cells



Digital devices – Hardware and Software

- System On Module (SOM)
- Field Programmable Gate Array (FPGA)
- Processors
- Memories



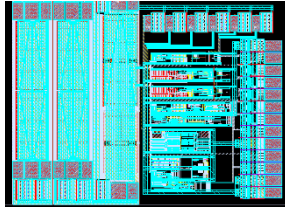


CITAR Project

Radiation Tolerant ICs & Test Facilities



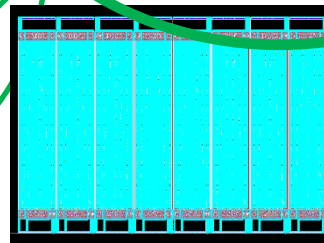
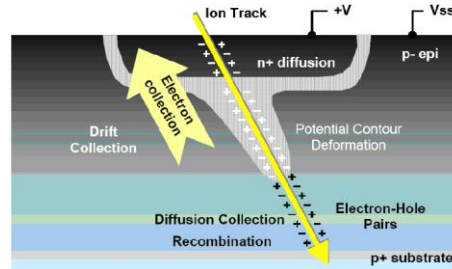
End user - Satellites



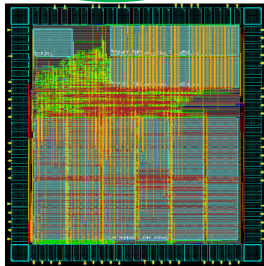
Telecommand
ASIC



System & IC design



Power Switch
ASIC



SpaceWire
IP & ASIC



SEE

TID



Radiation Testing



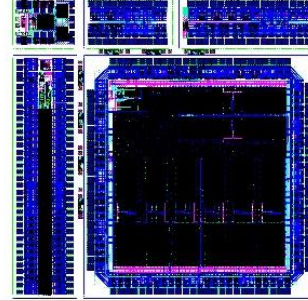
ASIC – Application Specific Integrated Circuit



SEU in SpaceWire ASIC chip

CTI-USP-FEI Collaboration

- CITAR
MPW
- 5 x 5 mm
 - SpaceWire
 - LVDS
 - MultiGates
 - 1V8 Reg
 - Test structs



Radiation tolerant chip developed to the Brazilian Space Agency (AEB) and INPE
180 nm technology

SpaceWire is a standard for high-speed links and networks for use onboard spacecrafts
Interconnection of: sensors, memories, processing units, and telemetry sub-systems

- Bit-flip tests in flip flop registers (SEU)
- Memory tests (mitigation techniques)
- SpaceWire communication

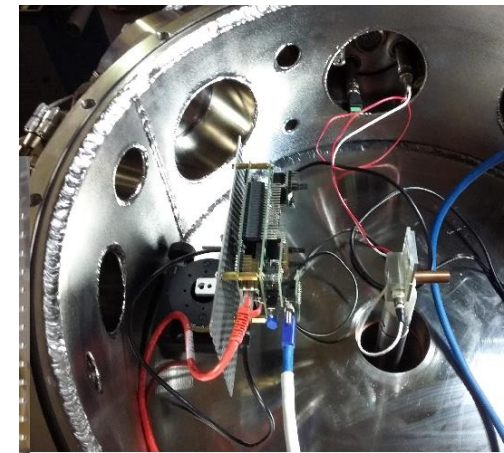
Results

No failures in the flip-flop registers with heavy-ion beams.
Mitigation procedures worked properly for the SRAM memories.
SpaceWire communication is tolerant to radiation.



The SpaceWire chip was aged with X-rays up to 500 krad
with no significant modification

Next steps – other tests with heavy ion beams
ASIC tele command
ASIC Power switch

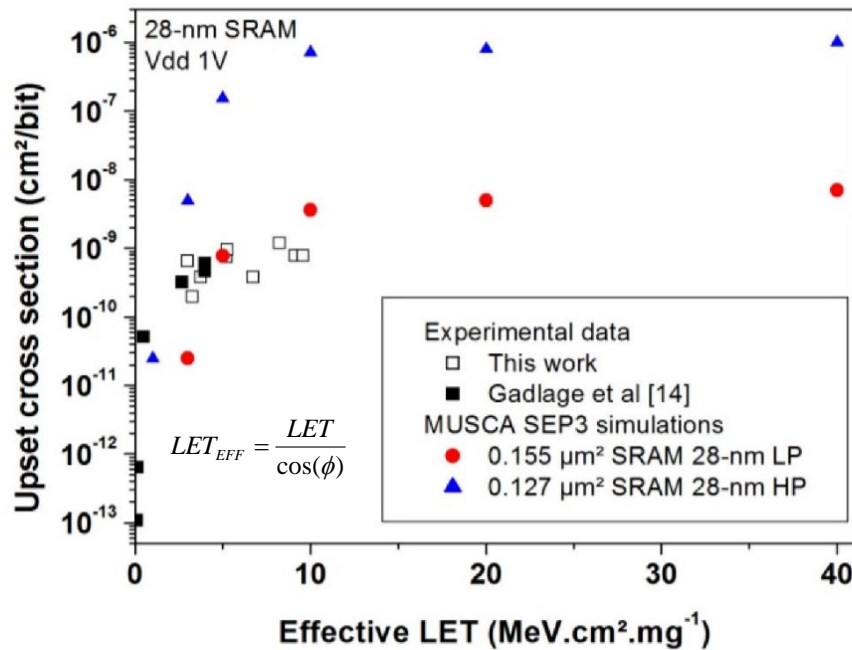


Scattering
chamber



Collaboration with UFRGS

Algorithm Tests



Analyzing the Influence of the Angles of Incidence and Rotation on MBU Events Induced by Low LET Heavy Ions in a 28-nm SRAM-based FPGA

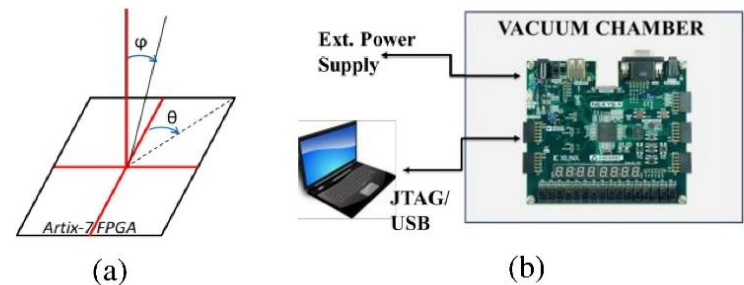


Fig. 1. In (a) Beam incident angle (ϕ) and rotation angle (θ) of the board in the vacuum chamber. In (b) the test setup for heavy ion testing.

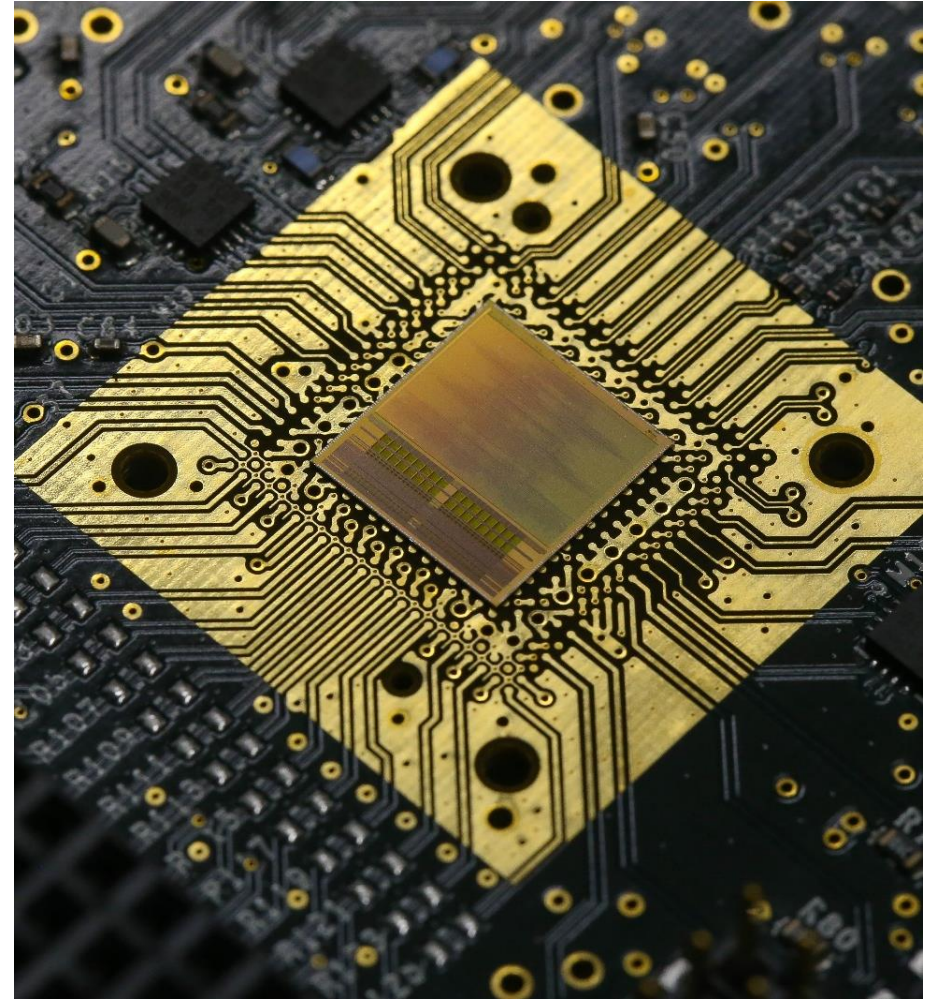
- **Reliability on ARM Processors Against Soft Errors Through SIHFT Techniques.**
- **Analyzing Reliability and Performance Trade-Offs of HLS-Based Designs in SRAM-Based FPGAs Under Soft Errors**
- **Heavy Ions Induced Single Event Upsets Testing of the 28 nm Xilinx Zynq-7000 All Programmable SoC.**



SAMPA CHIP

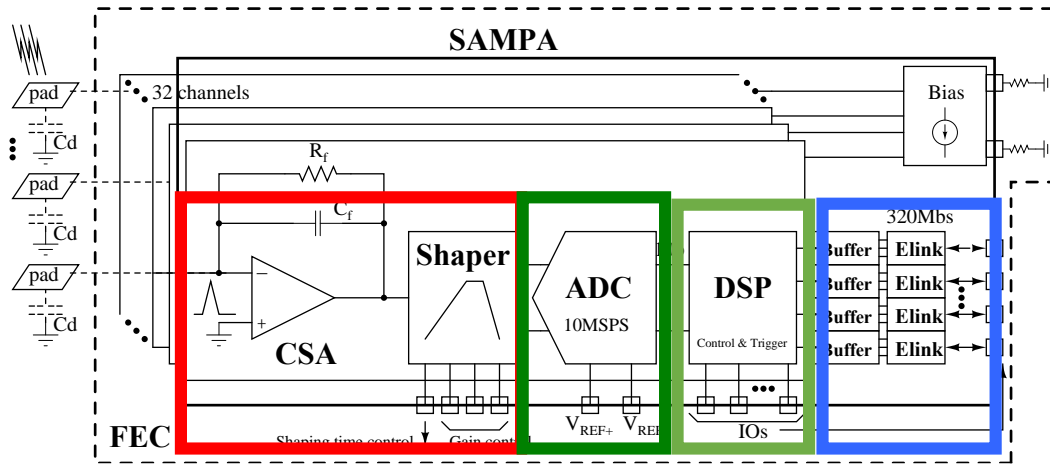


- Upgrade of the Detection System of the ALICE experiment (LHC)
- Increase of about 100 times the Data Acquisition Rate.
- Brazilian Project:
IFUSP (HEPIC), POLI (LSI)
and UNICAMP





SAMPA CHIP



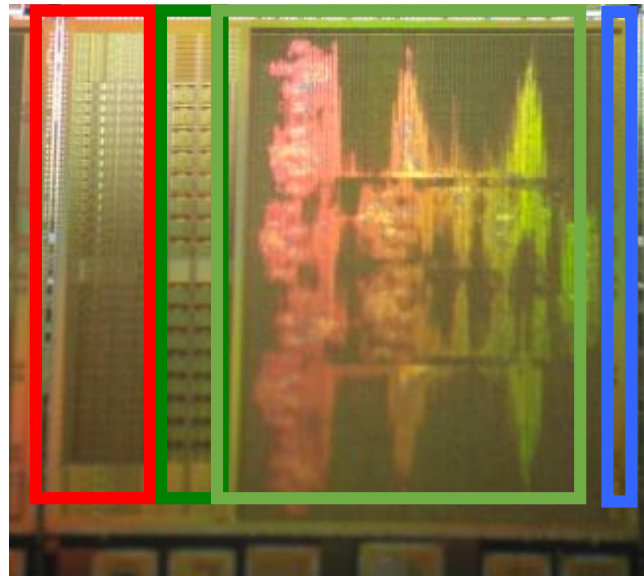
DSP: Digital Signal Processor
FEC: Front-End Card
CSA: Charge Sensitive Amplifier

32 FEs (CSAs + Shapers)

32 ADCs

Output Drivers

DSP



32 channel ASIC (Application Specific Integrated Circuits), CMOS 130 nm technology

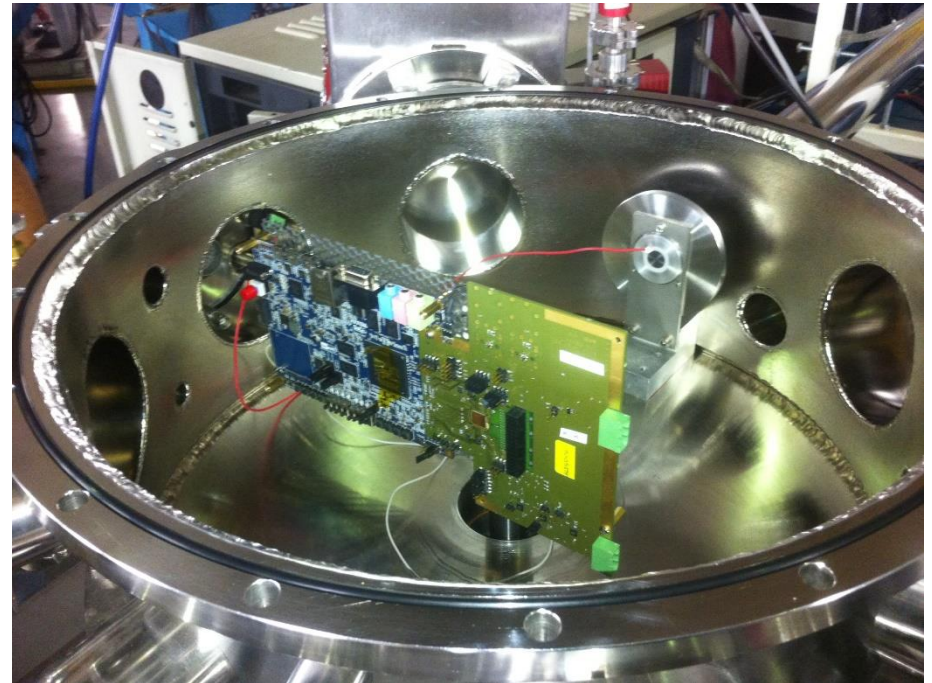


Radiation Tests Proton and ^{16}O Beams



- The component will be subject to very high radiation doses in the ALICE experiment.
- Some complementary tests with proton beams were performed in the new beam line of the 8 MV Pelletron accelerator.
- Analogic systems (*e.g.* amplifier) were tested with ^{16}O beams to scan specific regions of the chip.

Scattering chamber

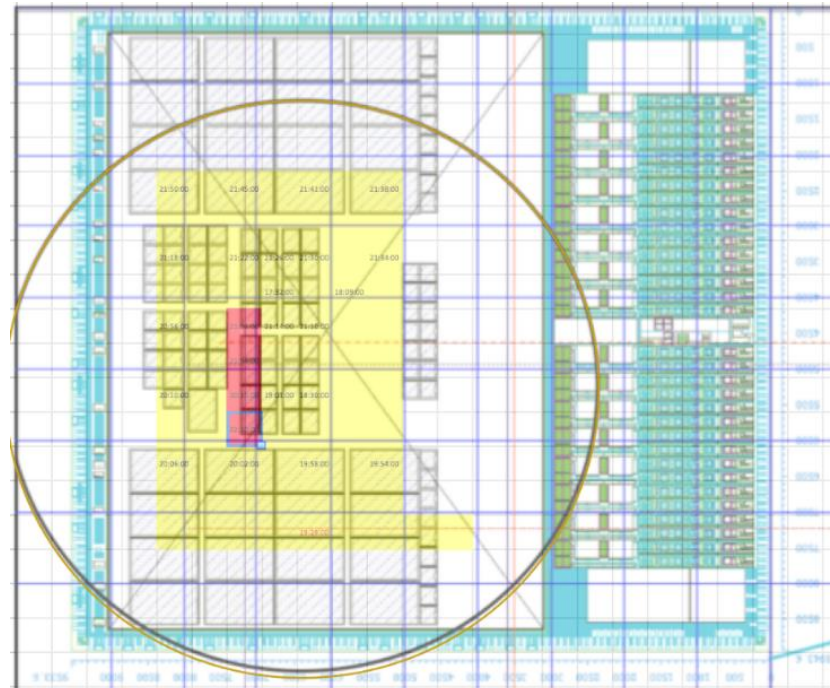


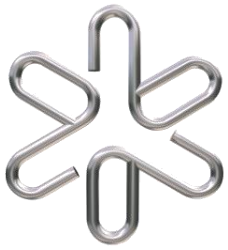


Radiation Tolerant Tests



- The results indicate that one of the memories chosen in the initial project was too sensitive to radiation. These memories were changed to another version in the final chip project.
- These tests were crucial for the final chip design.





Instrumentation with the LHC-CERN



Ultra-Fast silicon detectors

The state of the art in the development of Ultra-Fast Semiconductor Detectors (UFSD) devices, that are capable of timing resolutions of few picoseconds, came with the introduction of **Low Gain Avalanche Detectors (LGAD)**, a novel structure pioneered by the RD50 collaboration that incorporates a very thin intrinsic charge multiplication layer in order to fulfill the performance requirements for the High Luminosity-LHC (and beyond) experiments.

Based on the simulation results, the group will design and fabricate prototypes of LGAD and AC-LGAD sensors (and the equivalent PIN diode as a non-multiplication device reference), **characterize and perform the irradiation of the sensors using the facilities available in Sao Paulo (Laboratorio de Sistemas Integraveis (LSI) from EPUSP, IFUSP and FEI).**

The goal in this part of the project is to fully characterize the SAMPA chip and LGAD semiconductor sensors tolerance for radiation using different probes, from gamma and X rays to protons, neutrons and heavy ions.

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SAFIIRA SYSTEM



*Thank you for
your attention*



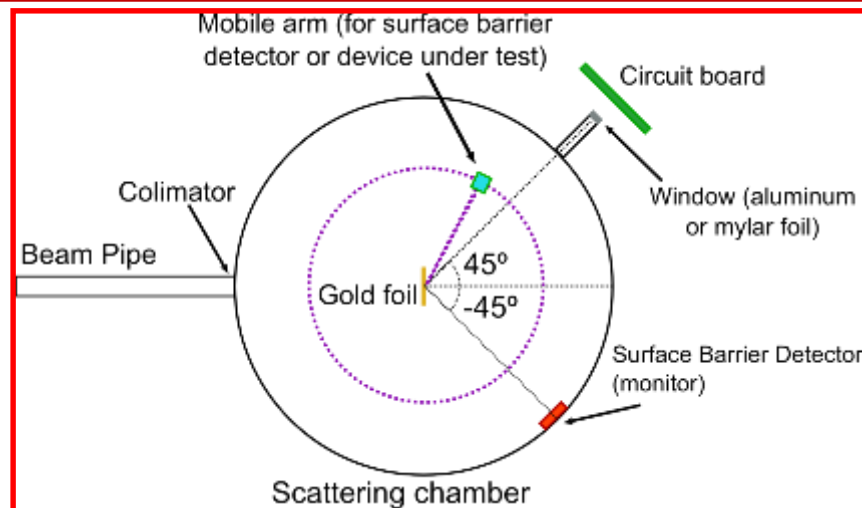


Pelletron Accelerator 30B Beam Line



Rutherford Scattering

ESA beam requirements:
Flux 10^2 to 10^5 part/cm²s
< 10% uniformity variation



30B beam line



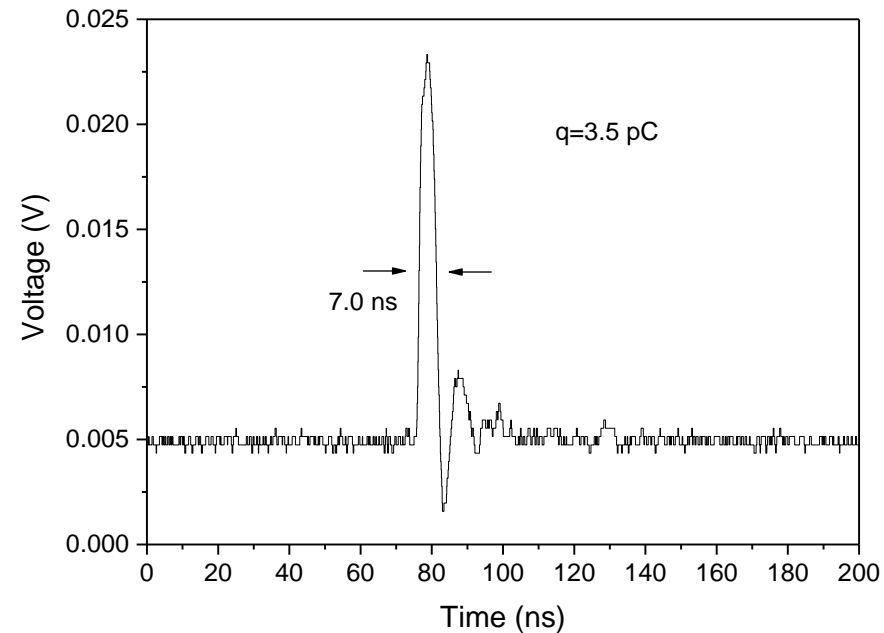
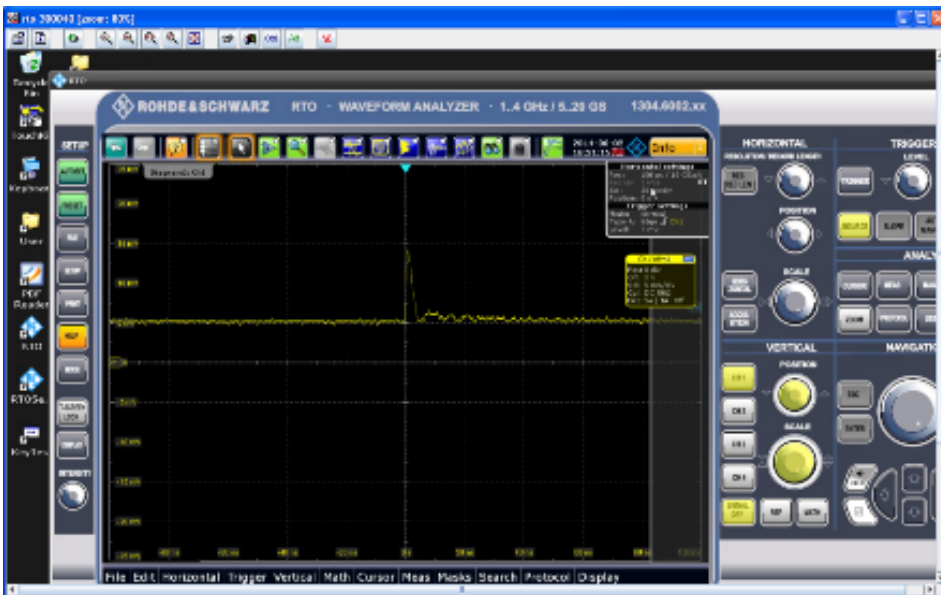
External beam setup



SEU measurements in a p-channel MOSFET transistor (3N163) USP-FEI Collaboration



SEU signal observed with an oscilloscope due to ^{35}Cl heavy ion beam at 75 MeV.



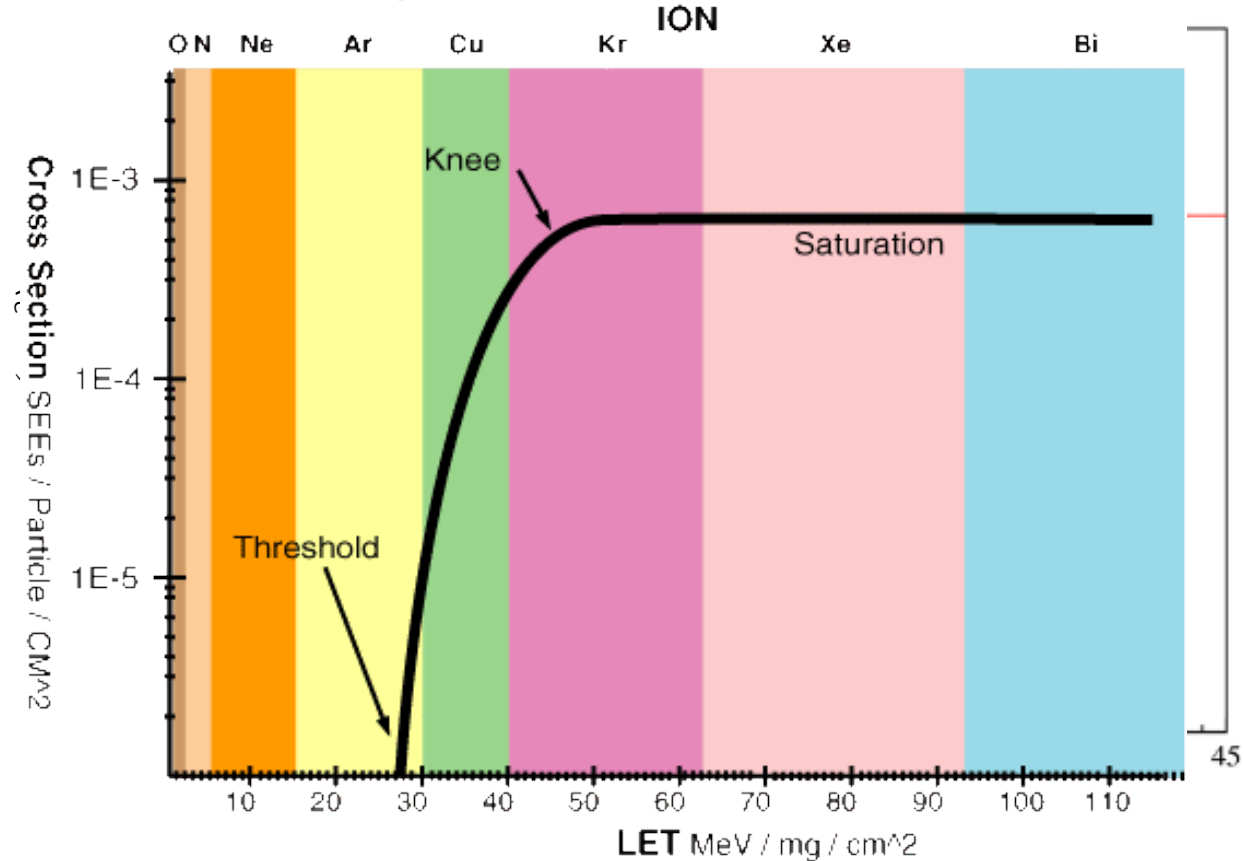


SEU Cross Section

p-channel MOSFET transistor (3N163)



A Sample Cross Section VS. LET Curve



$$\sigma_{SEE} = \frac{\text{events}}{\Phi}$$

$$\Phi = \frac{\text{particles}}{\text{cm}^2}$$

Weibull Function

$$\sigma = \sigma_{sat} \left[1 - e^{-\left(\frac{LET - LET_{th}}{W}\right)^s} \right]$$

$$\sigma_{sat} = 294(10)10^{-5} \text{ cm}^2$$

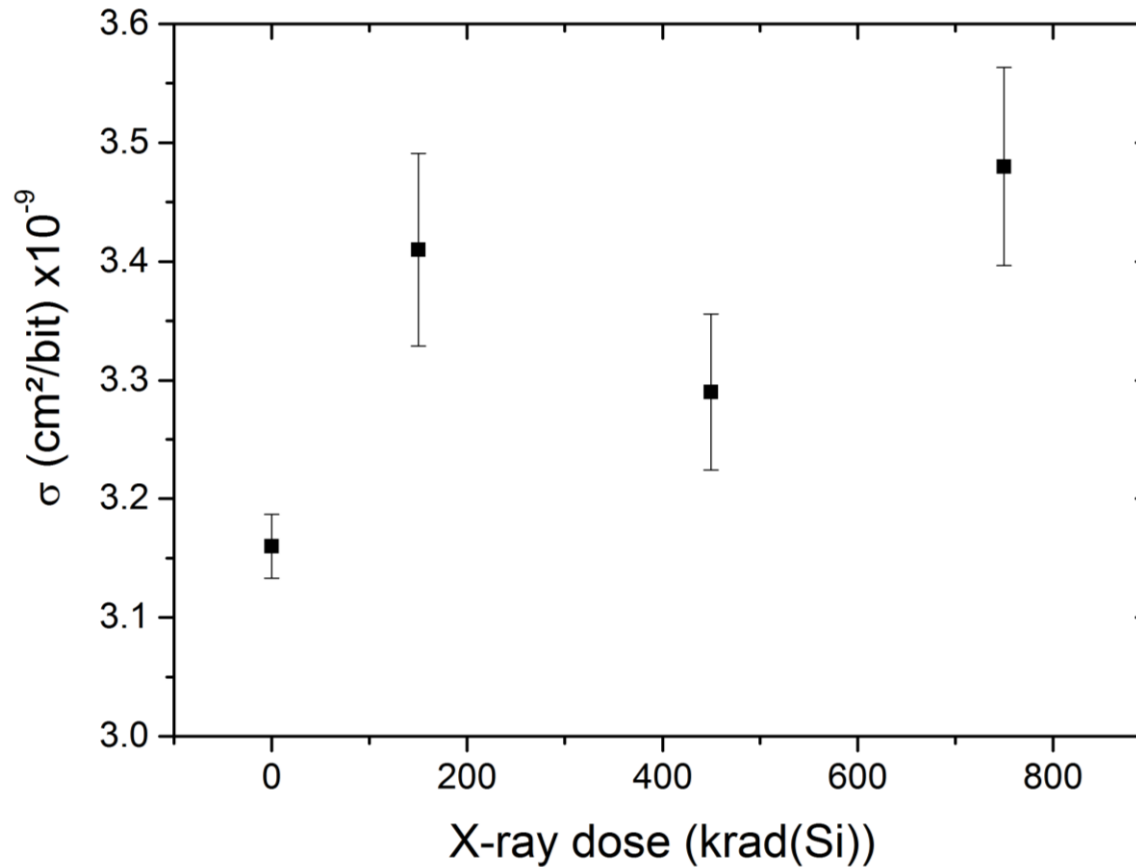
$$LET_{th} = 2.35(36) \text{ MeV/mg/cm}^2$$

$$W = 1.06(11) \text{ MeV/mg/cm}^2$$

$$S = 0.62(10)$$



SEU + X-ray TID in Xilinx FPGA Spartan 3



**^{16}O beam; $E_b = 50$ MeV LET = 5.0 MeV/mg/cm²
10-keV effective energy (X-ray)**



Collaboration with PUC-RS and FEI



- **Analysis of SRAM-Based FPGA SEU Sensitivity to Combined EMI and TID-Imprinted Effects**
- **Analysis of Single-Event Upsets in a Microsemi ProAsic3E FPGA**

Industrial, communications and medical applications with commercial and industrial temperature devices. ProASIC3 FPGAs can be delivered with specialized screening for automotive and military systems.

SRAM – Static Random Access Memory

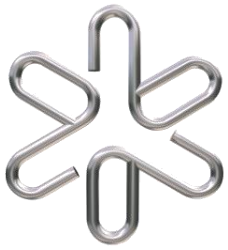
COTS – Commercial Off-The-Shelf

ARM - microcontroller Advanced RISC Machine

Used in cellphones, calculators, computers, industrial applications

RISC - Reduced Instruction Set Computer

FPGA – Field-Programable Gate Array



SEU in FPGA Microsemi ProAsic3 CTI-USP-FEI Collaboration



To study the basic characteristics when chips are submitted to heavy ion beam
130 nm technology

- Mitigation techniques
- FLASH and SRAM memories
- Flip-flop registers

Ion Beam	LET (MeV/mg/cm ²)
¹² C	3
¹⁶ O	5
³⁵ Cl	17
¹⁰⁷ Ag	40

**8UD Pelletron accelerator
low flux**



Results

Validation of error detection, correction algorithms
and redundancy techniques

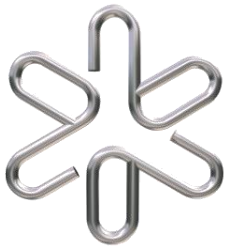
Flash memory is radiation tolerant

Failures in SRAM memories and flip flops

Necessity to implement new circuits to become more tolerant

Validation of the techniques to be used in the SpaceWire chip.





SAFIIRA SYSTEM

Sistema de Feixes Iônicos para IRradiações e Aplicações
Ion Beam System for Irradiations and Applications





Experimental Beam Uniformity



^{16}O beam $E= 42$ MeV



ZnS fluorescence

(2,0 x 2,0) cm² beam area
Fluxes from 10^2 to 10^5 part/s/cm²
Observed uniformity around 93%

