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A 2.56 Gbps or 10.24 Gbps 1:16 Deserializer in 55 nm for High-Energy Physics Experiments

Deserializer is used to convert the high-speed serial data into a low-speed parallel data in the downlink direction of data transmission system in high-energy physics experiments. This paper presents the design and test results of a 2.56 Gbps or 10.24 Gbps 1:16 deserializer fabricated in a 55 nm CMOS process.

In order to meet the demand of current data volume and adapt to upgrade of the equipment in the future, the deserializer compatible with 2.56 Gbps and 10.24 Gbps data rates is proposed. The 2.56 Gbps or 10.24 Gbps 1:16 deserializer ASIC mainly consists of an equalizer, 1:4 DEMUX module, 4:16 DEMUX module, clock divider by 4, LVDS drivers and an automatic frequency comparator. The 1:4 DEMUX module and 4:16 DEMUX module are implemented by one and four 1:4 DEMUX units, respectively. According to the different data dates, there are two different 1:4 DEMUX units and clock divider by 4 have been designed. In order to improve the bandwidth, the high-speed 1:4 DEMUX unit and the high-frequency clock divider by 4 adopt the latches with an optimized compressed CML structure. And the low-speed 1:4 DEMUX unit and the low-frequency clock divider by 4 adopt CMOS latches to save power consumption.

The 2.56 Gbps or 10.24 Gbps 1:16 deserializer ASIC has been designed in 55 nm CMOS process with core area of 1120 μm × 600 μm. The simulation results show that the logic of output data at 2.56 Gbps and 10.24 Gbps are correct in different process corners. And the clean and open output eye diagrams can be obtained at the input data rate of 2.56 Gbps and 10 .24 Gbps, respectively. The chip has been taped out and is being tested, the test results including logic and eye diagram test will be displayed in the poster.

Submission declaration

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Authors: CHEN, Qiangjun; Prof. GUO, Di (Central China Normal University); ZHAO, Cong; Mr LI, Juncheng; Mr SHI, Qunqi; Mr YAN, Shiwei

Presenters: CHEN, Qiangjun; Prof. GUO, Di (Central China Normal University)

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