Characterization of a baseline vertex detector prototype for the CEPC

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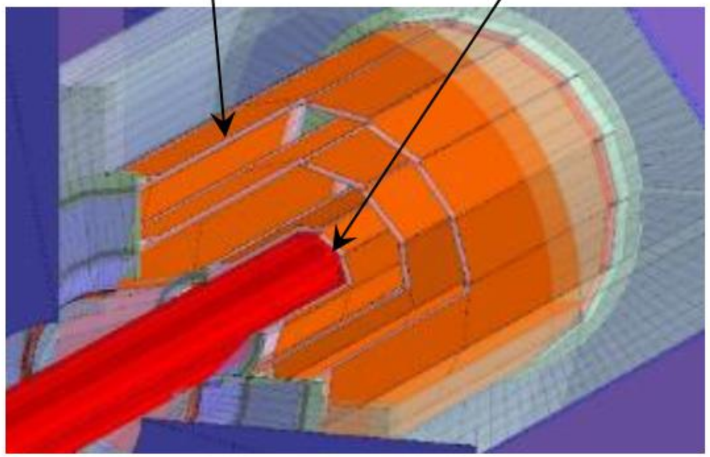
Circular Electron Positron Collider

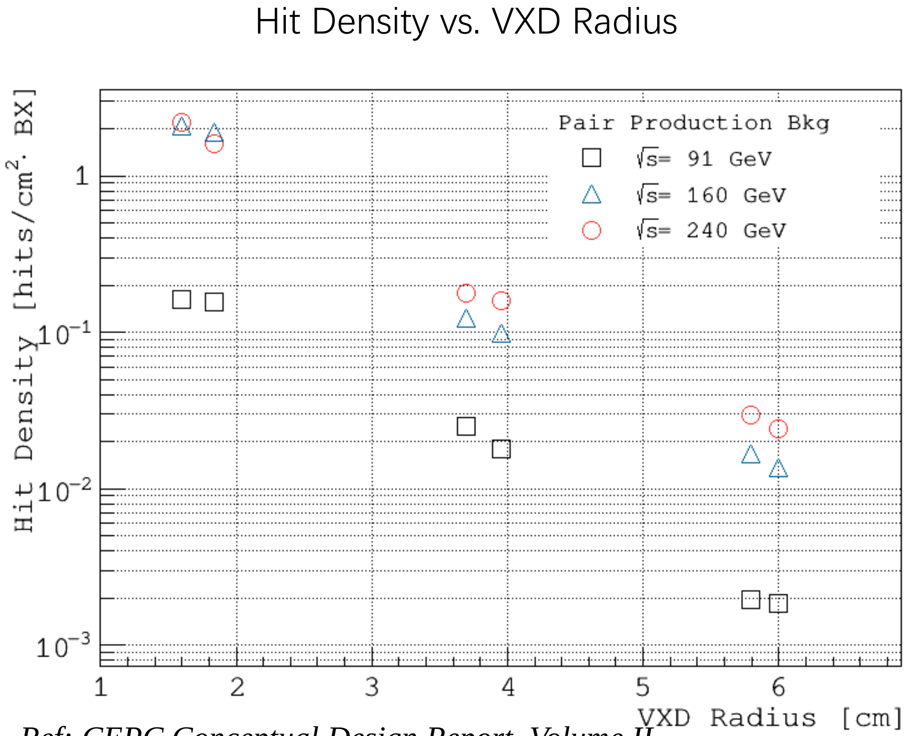
OUTLINE

- Development of the pixel sensors
- Overview of the baseline vertex detector
- Beam test of the prototype
- Summary

CEPC vertex detector Requirement



CDR: critical to provide excellent impact parameter resolution



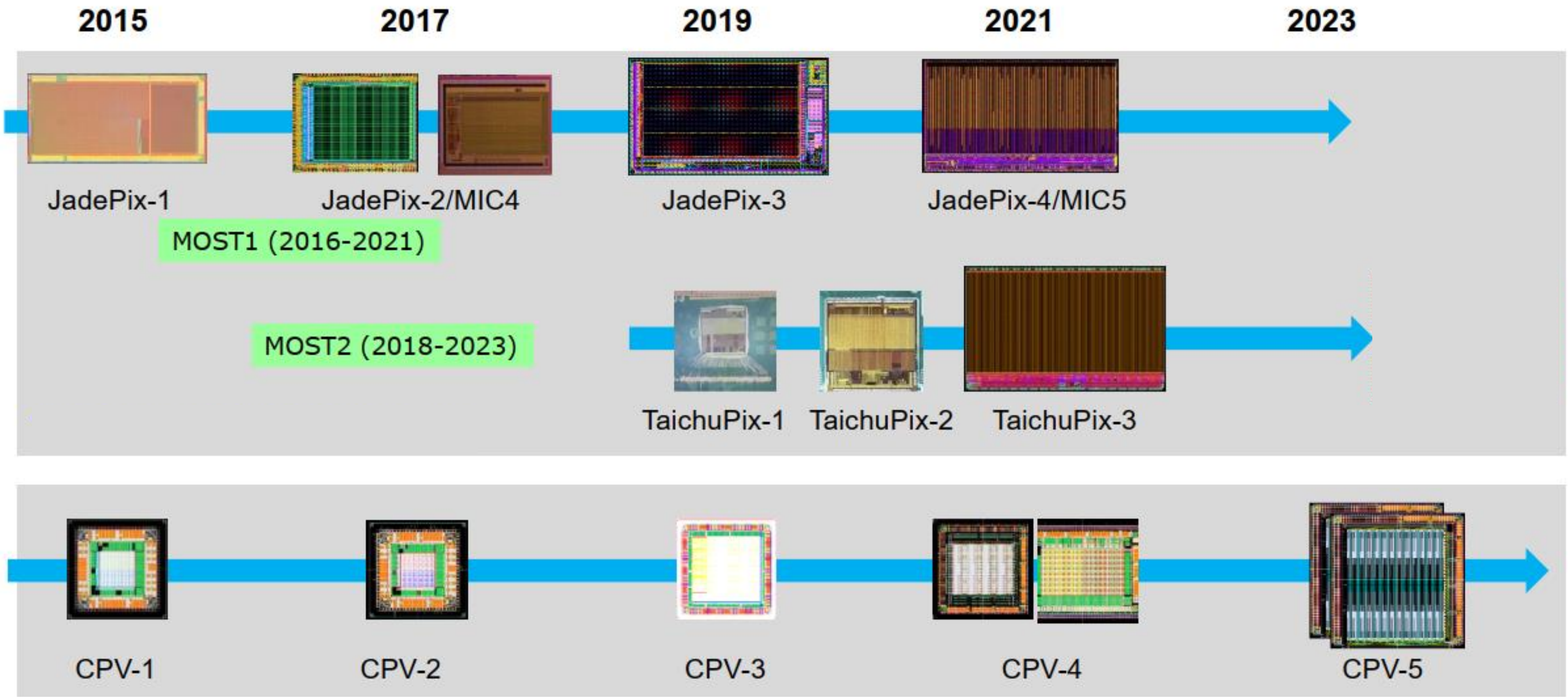
Ref: CEPC Conceptual Design Report, Volume II

Main requirement:

- First layer located at a radius: ~1.6 cm.
- Single-point resolution : <3 µm. *~16 µm pixel pitch*
- Material budget :<0.15% X0/layer.
- Power consumption： *<50 mW/cm^2,if air cooling used*

Target: *small pitch, low power, light structure and high data rate.*

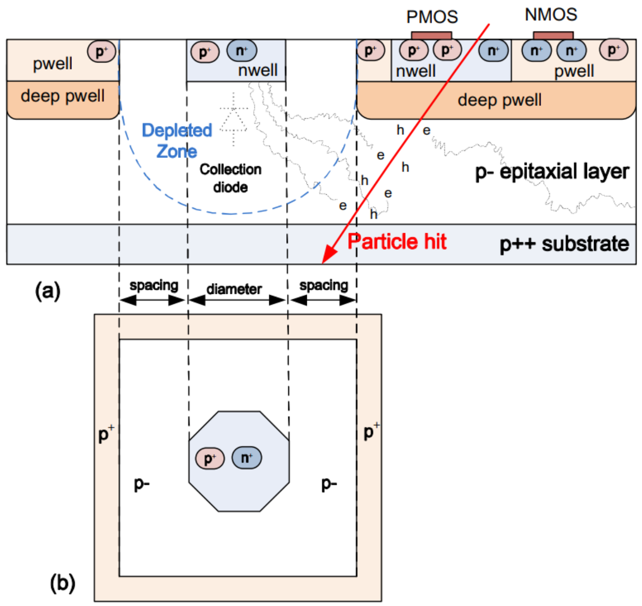
Timeline of Silicon Pixel sensor R&D



MOST2 aims to study the design of a fully functional chip to realize a baseline vertex detector

Ref: Jianchun Wang, Status of The CEPC Detector R&D, on CEPC workshop 2023 .

Monolithic Active Pixel Sensor

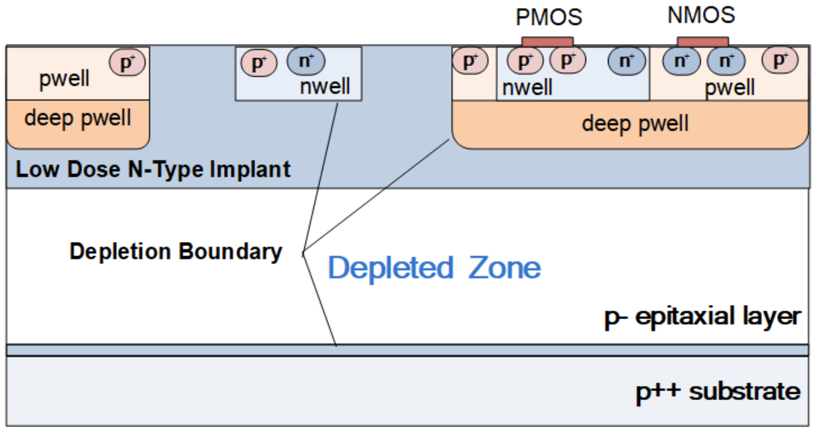


Standard MAPS (ALPIDE, TaichuPix-1)

MAPS is a promising candidate to meet the high speed, high granularity, small pitch and adequate radiation tolerance.

Small electrode of the 0.18 μm technology

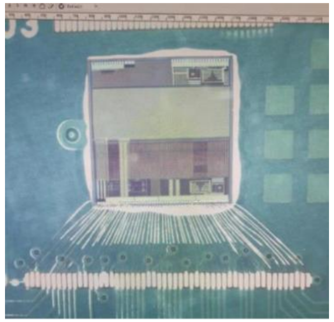
- Small sensor capacitance (<5 fF)
- A quadruple well technology
- Speed is limited by the depleted zone, a modified technology can be used to have a full depleted zone.
- Epitaxial layer with 25 μm and high resistivity of 1 kΩ·cm, improving the radiation hardness



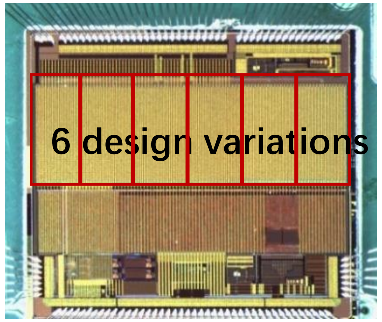
Depleted MAPS (TaichuPix-3)

TaichuPix sensor prototyping

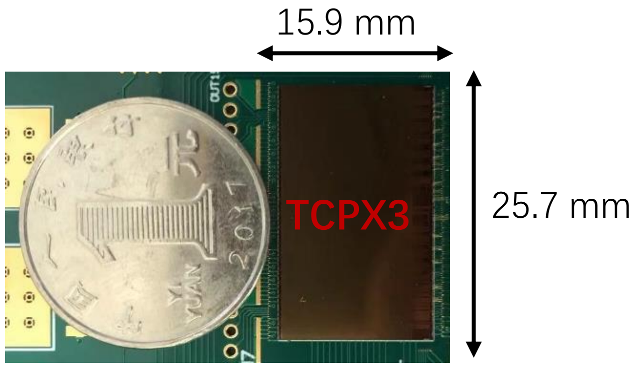
- Major challenges for the CMOS sensor
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance : 1 Mrad TID
- Completed 3 round of sensor prototyping in CIS 180 nm process
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019.06 – 2019.11
    - TaichuPix-2: 2020.02 – 2020.06
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022



TaichuPix1

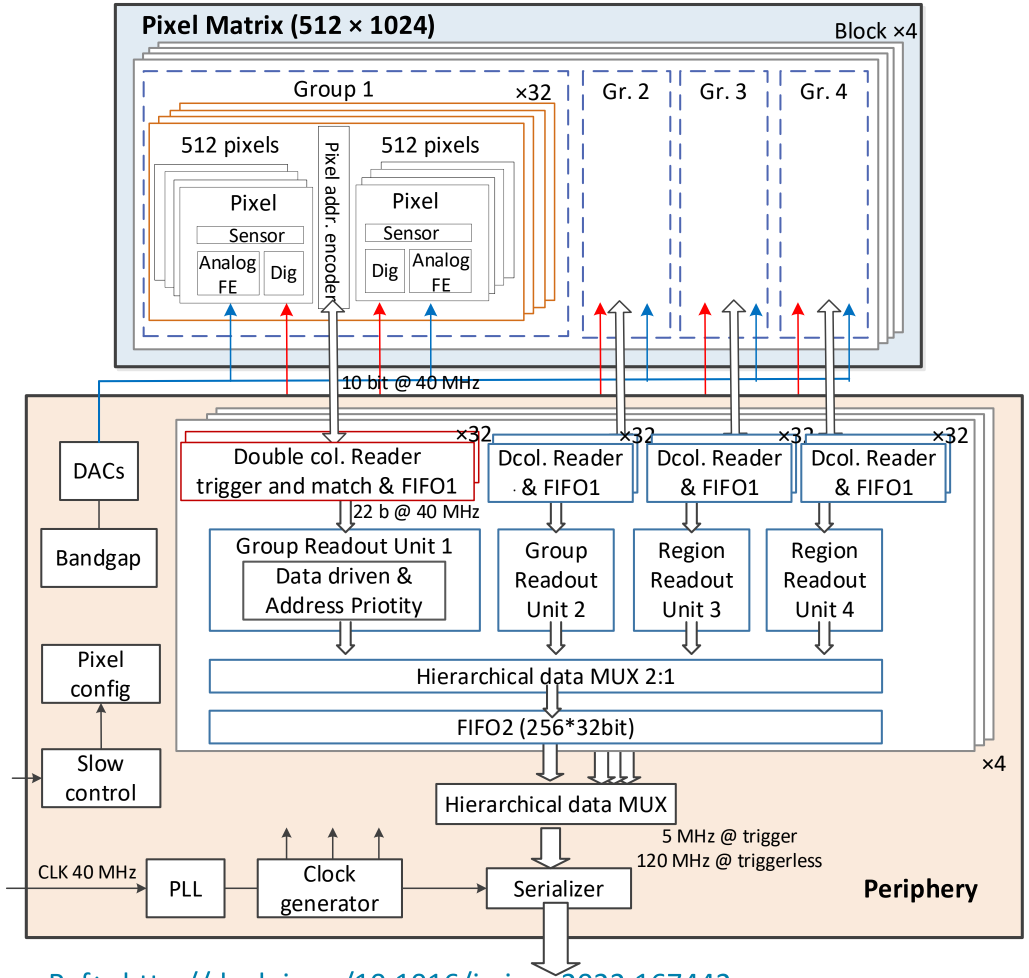


TaichuPix2



TaichuPix3
Pixel size：25 μm × 25 μm

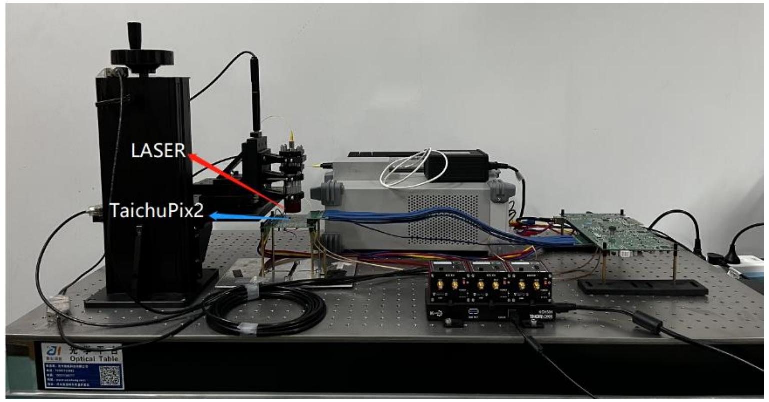
TaichuPix chip architecture



Ref：http://dx.doi.org/10.1016/j.nima.2022.167442.

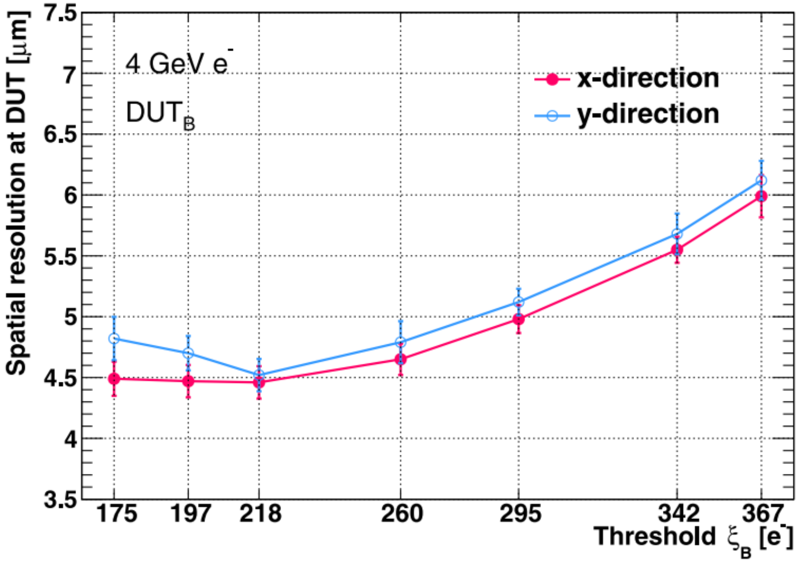
- **Pixel 25 μm × 25 μm, Pixel matrix: 512x1024**
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at the end of column
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

Characterization for the TaichuPix chip

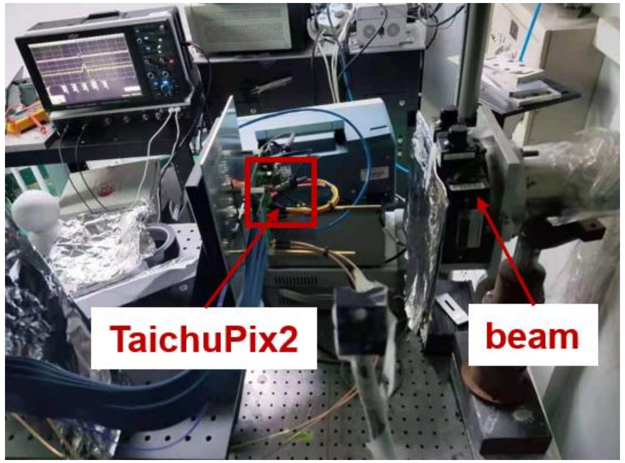


Laser test setup

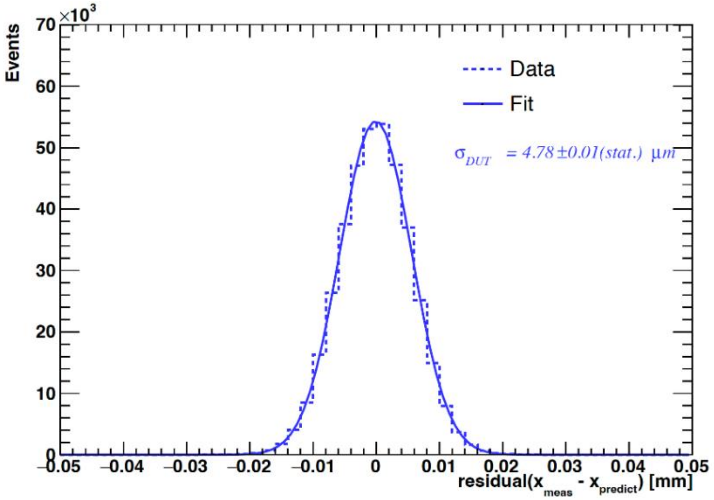
Telescope made by TaichuPix3



Spatial resolution vs. threshold



Radiation test setup

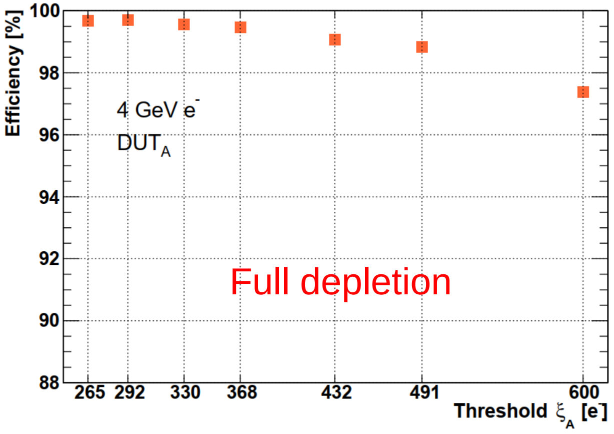


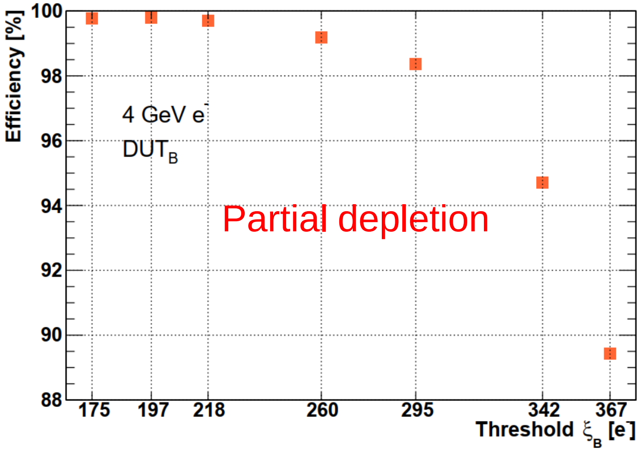
Spatial resolution on X direction

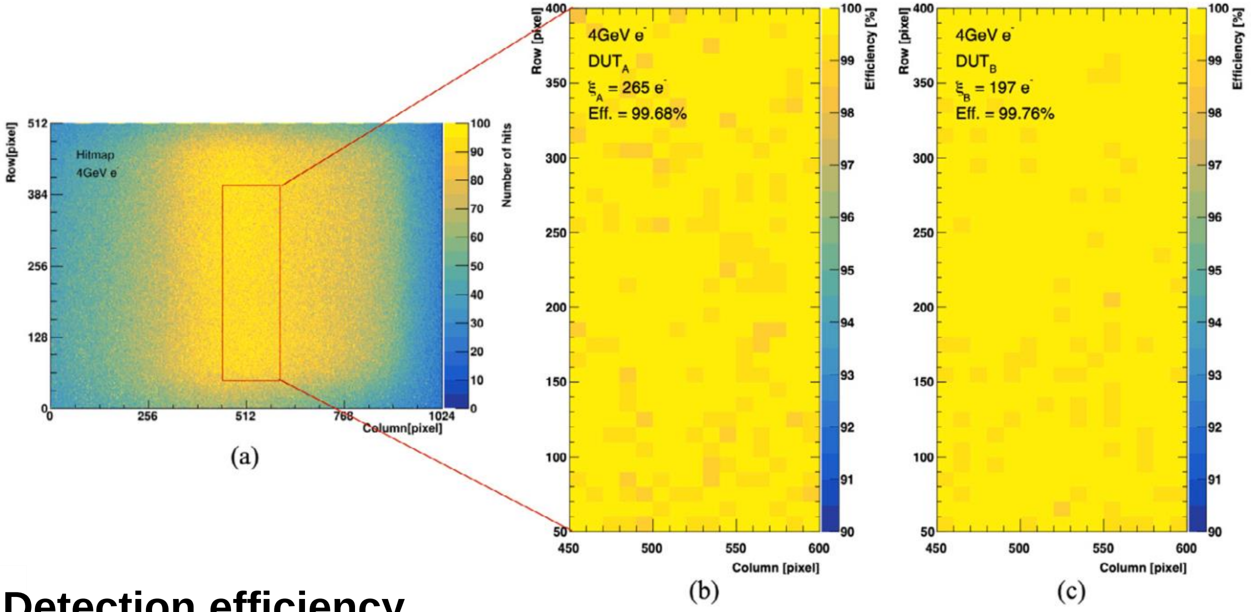
Spatial resolution	Laser	Testbeam
X	*3.98±0.23*	*4.48±0.12*
Y	*4.12±0.25*	*4.52±0.10*

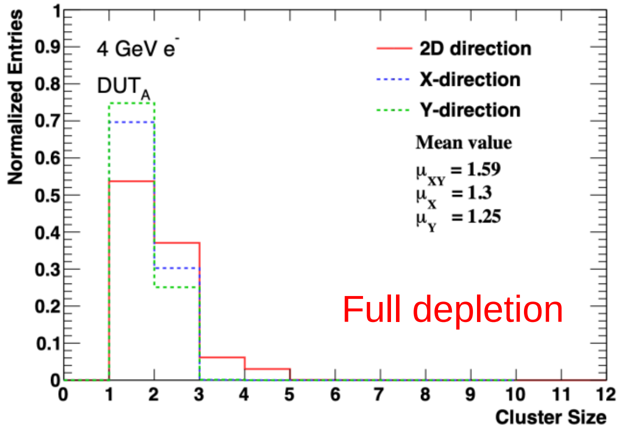
https://doi.org/10.1016/j.nima.2023.168601

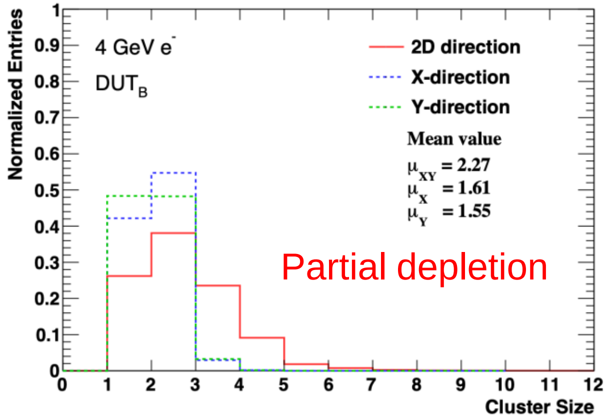
Detection efficiency and cluster size











Detection efficiency

- With increasing threshold, the efficiency decrease
- Maximum eff. for DUTA is 99.68%, maximum eff. for DUTB is 99.76%

Cluster

- The peak value for DUTA is 1 pixel,around 2 pixels for DUTB
- Less charge sharing effects in modified process with full depletion

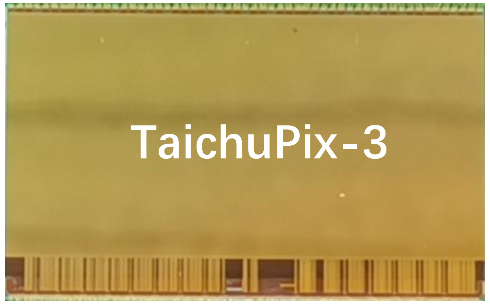
REF： https://doi.org/10.1016/j.nima.2023.168945

Figures are made by Shuqi Li

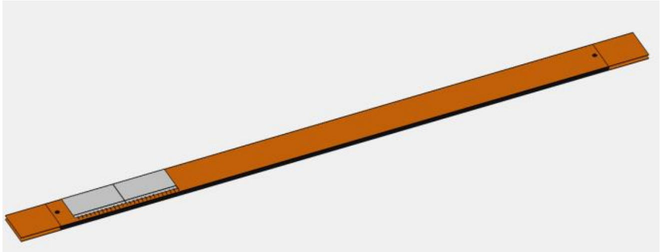
Overview of a baseline vertex detector R&D

- Can break down into sub-tasks
  - CMOS Pixel Sensor chip R&D
  - Detector Module prototyping
  - Detector assembly

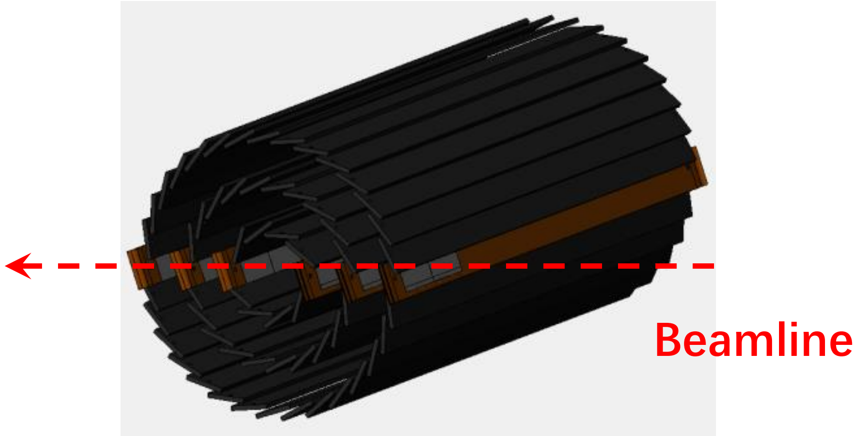
CMOS pixel sensor prototyping



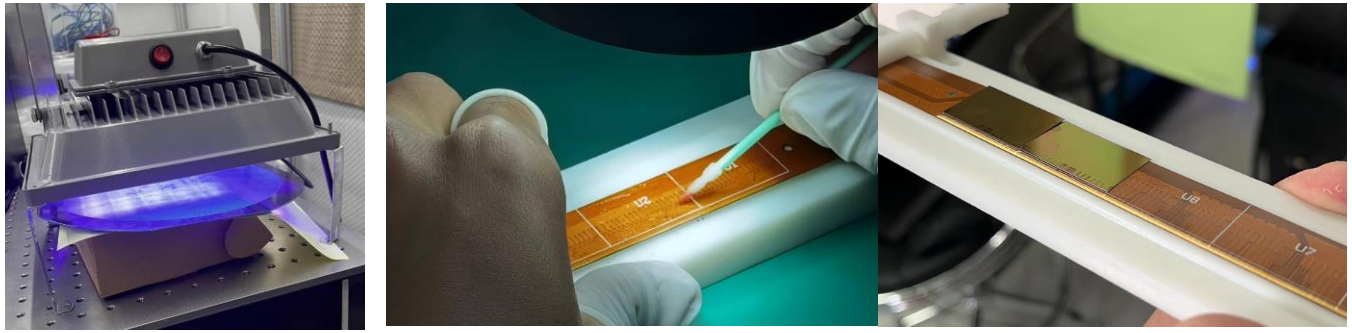
Detector module (ladder) prototyping



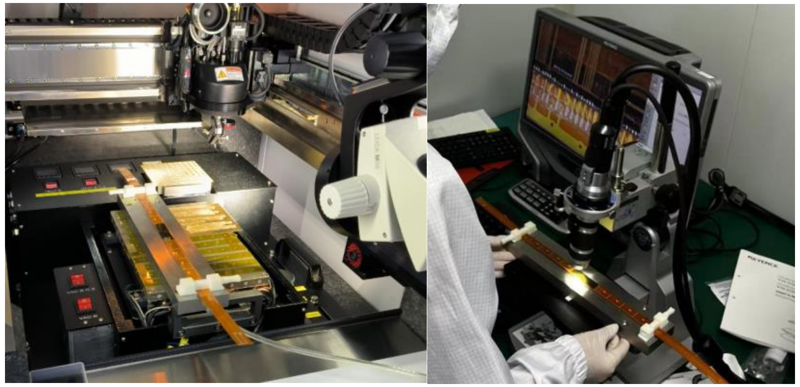
Full size vertex detector prototype



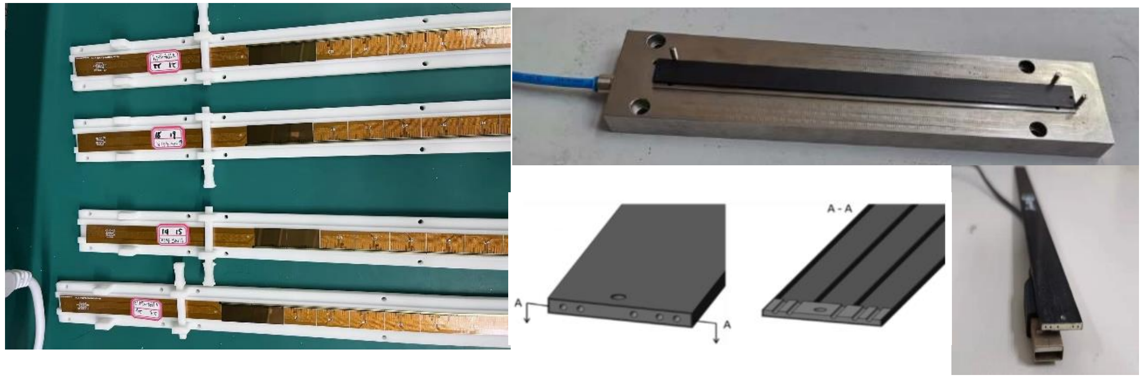
Detector module assembly



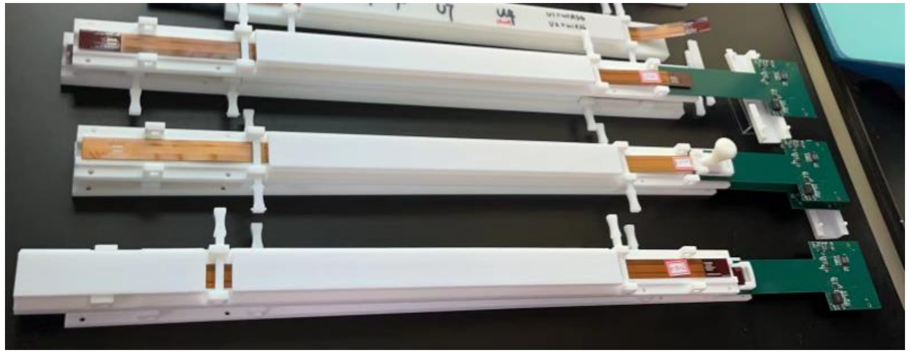
Step 1: Chip fixation - After exposing the chip to UV light, detach it from the blue film and then adhere it to the flexible board using glue.



Step 2: Wire bonding - Utilize a vacuumed plate tool to wire bond the TaichuPix-3 chip.



Step 3: Ladder assembly - Affix two flexible boards on both sides of the carbon fiber-reinforced plastic using adhesive.



Step 4: Ladder production - Following the electronics test, place the ladders on a protective support.

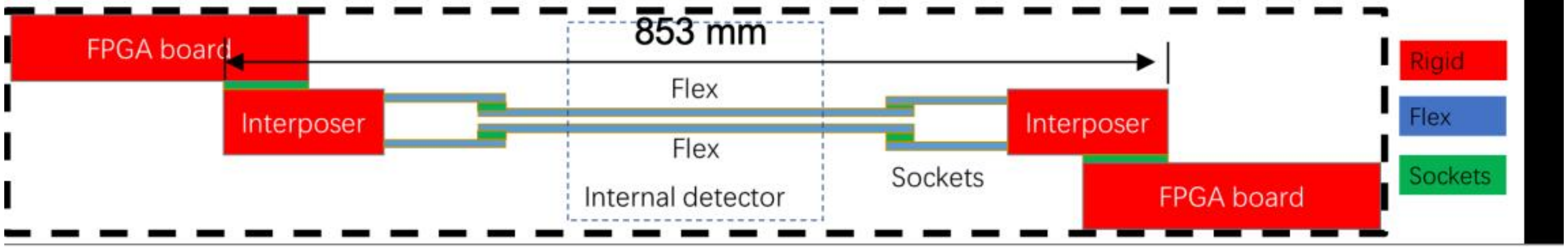
- Tooling for the specific process has been designed.
- Wire bonding for 10 chips on a flex board can be carried out in the IHEP lab.

All mechanical tools are designed by Jinyu Fu,
Ref : https://doi.org/10.1007/s41605-021-00310-4

Detector module prototyping

Detector Module (Ladder) Components:
- 10 sensors
- Readout board
- Support structure
- Control board

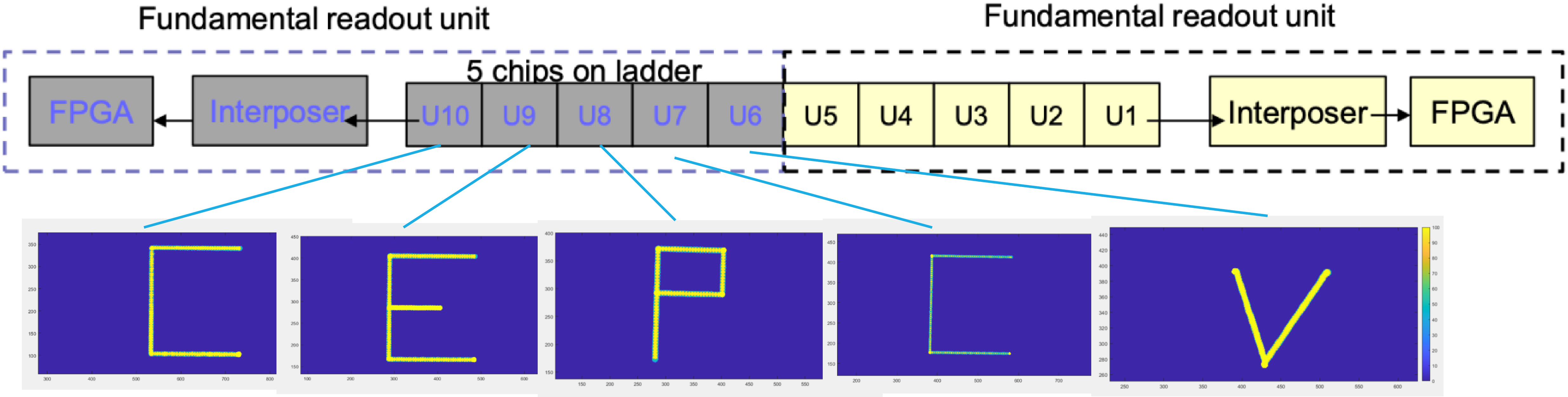
Signal & Power Distribution:
- Signal, clock, control, power, and ground are managed by the control board through the flexible PCB.



Challenge:
- Long flex cable complicates assembly and poses issues with power distribution and delays.
- Limited space for power and ground placement.

Solution:
- ✓ Implement a dual-ended readout strategy.
- ✓ The readout comprises three parts.
- ✓ Carefully design power placement to address challenges related to the long flex cable.
- ✓ Consider strategic power and ground placement within the constrained space.

Laser test for a detector module



"CEPCV" pattern by scanning laser on different chips on ladder

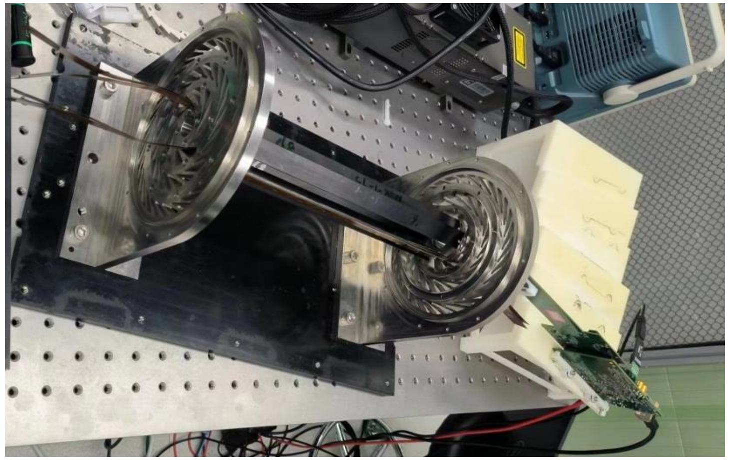
A complete ladder consists of four identical fundamental readout units, each comprising:

- 5 TaichuPix-3 chips
- An interposer board
- An FPGA readout board

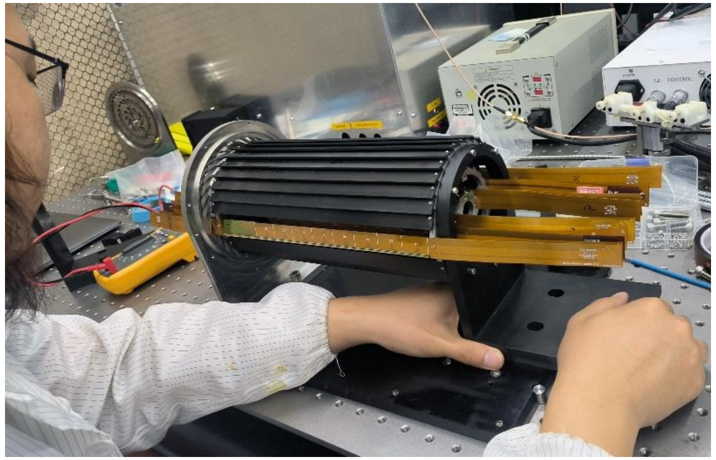
A full ladder fundamental readout unit was verified in following steps:

a) Configuring 5 chips in the same unit.
b) Scanning a laser spot on different chips with a step of 50 μm.
c) Clear and correct letter imaging was observed during the scanning process.
d) Demonstrating the coordinated operation of 5 chips, confirming the successful functioning of one ladder readout unit.

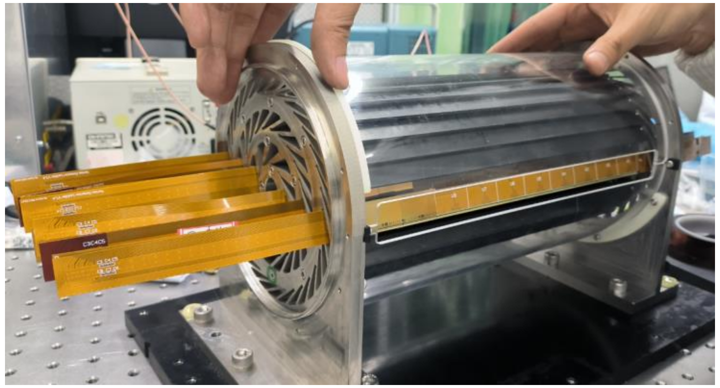
Preparation for the VXD prototype



After installation, flex boards were tested one by one



The outer barrel is under installation

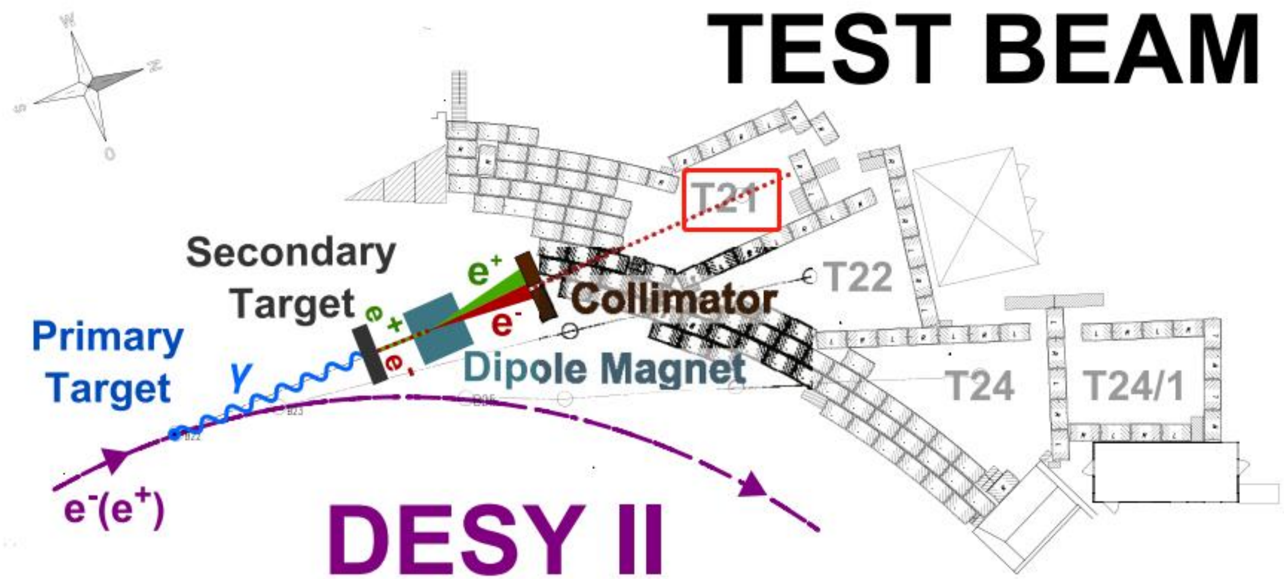


The transparent cover serves as a ventilation duct

The full VXD setup was measured at lab

For DESY beam test， a special flight ticket was bought for VXD（Vertex Detector） prototype.

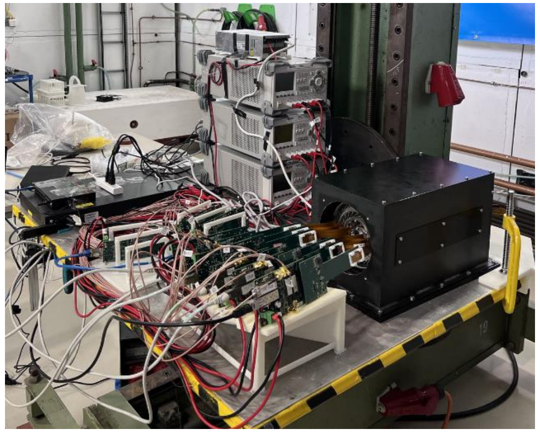
Introduction of DESY TB21



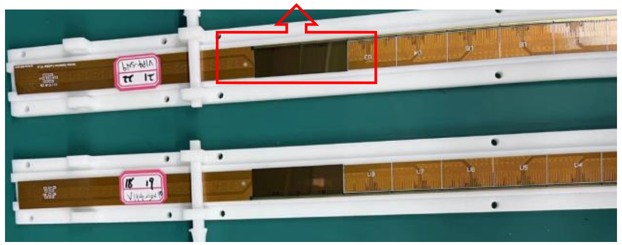
Ref: Test Beams at DESY
https://doi.org/10.1016/j.nima.2018.11.133

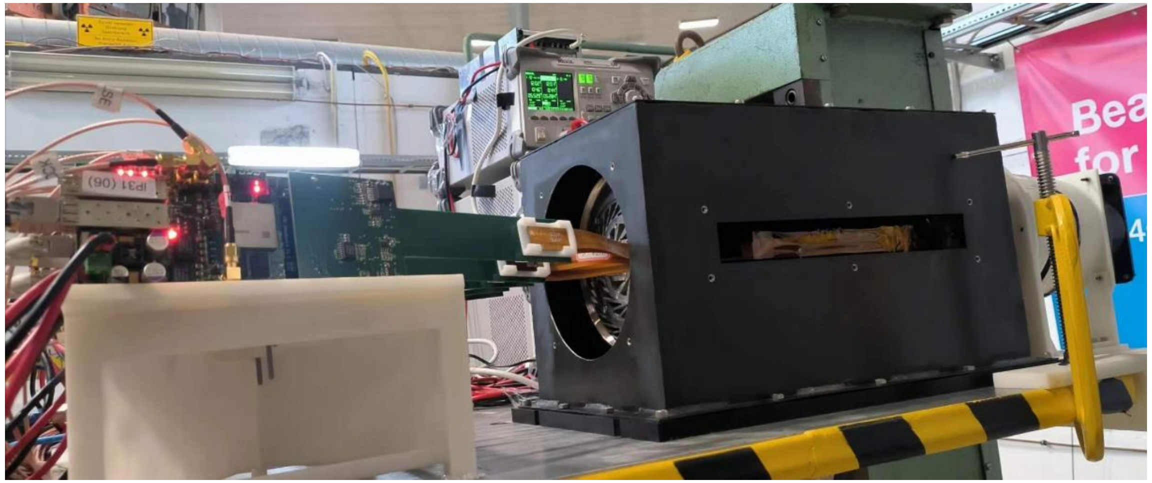
- Electron-positron synchrotron DESY II
- Beams are converted bremsstrahlung beams from carbon fibre targets
- Up to 1000 particles per cm^2
- Energies from 1 to 6 GeV,
- Energy spread of ~5% and a divergence of ~1mrad.

SETUP at DESY TB21



Only two chips were assembly on one flex board



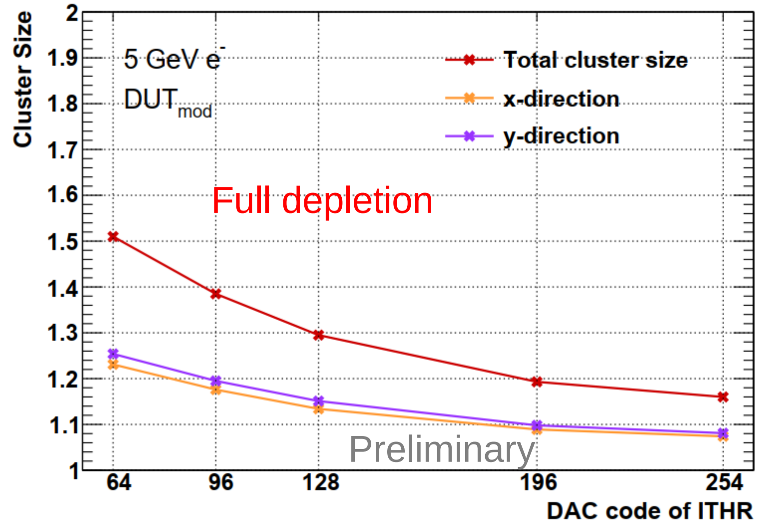


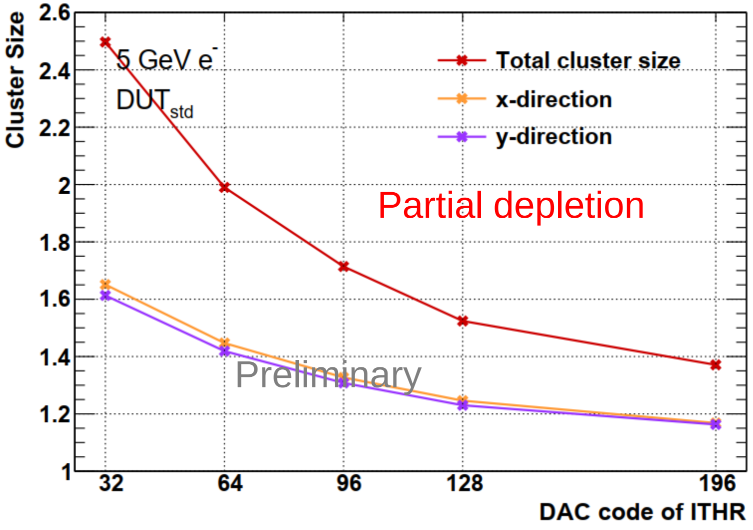
Size of 2.5cmx2.5cm

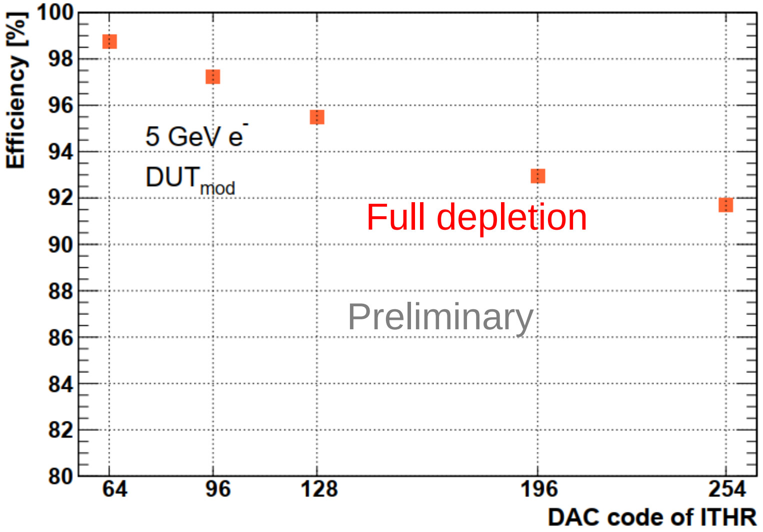
Beam spot Collimator

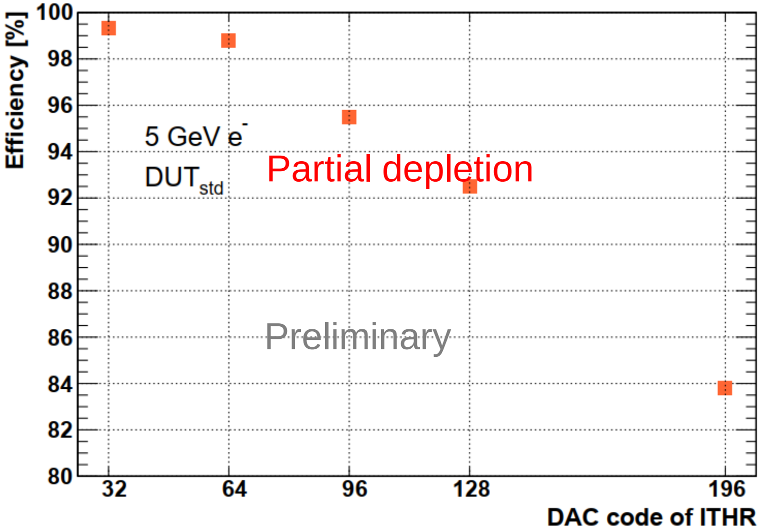
- All equipment fits within the 3D stage at DESY TB21 hut.
- A larger collimator (2.5x2.5cm²) was employed to concentrate on the center of two TaichuPix3 chips.
- The temperature of the outermost layer was decreased to 28℃ from 40℃ using either a fan or dry ice.

Detection efficiency and cluster size









Cluster

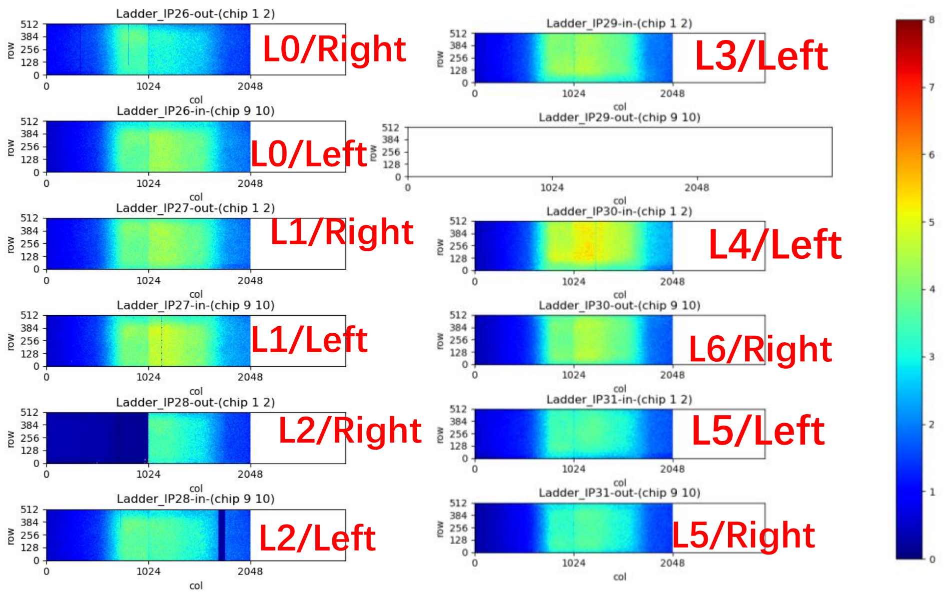
- Cluster size decreases with rising threshold.
- Overall cluster size of full depletion is smaller.

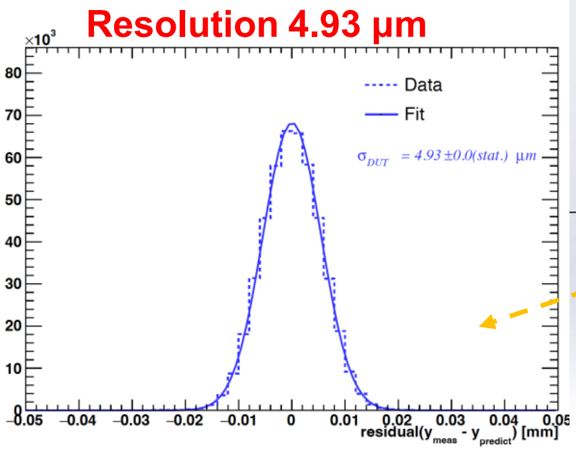
Detection efficiency

- With increasing threshold, the efficiency decrease
- Maximum eff. for DUT_{mod} is 99.1%, maximum eff. for DUT_{std} is 99.2%.

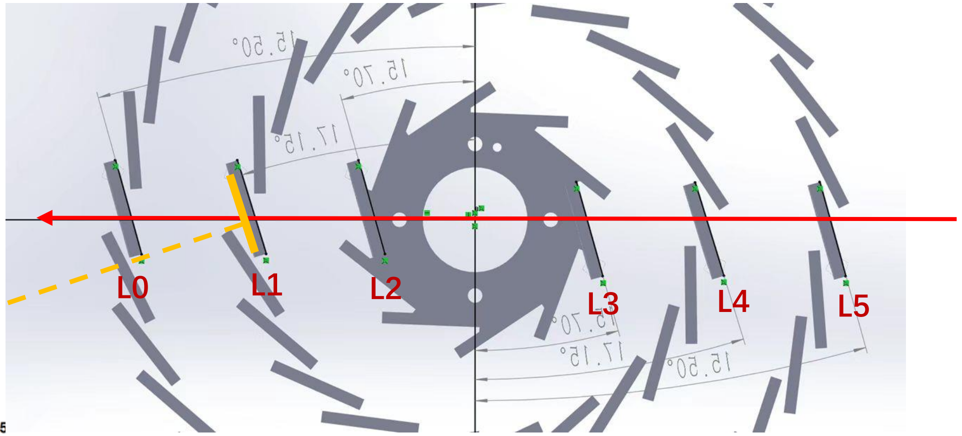
- Further offline analysis is currently underway.

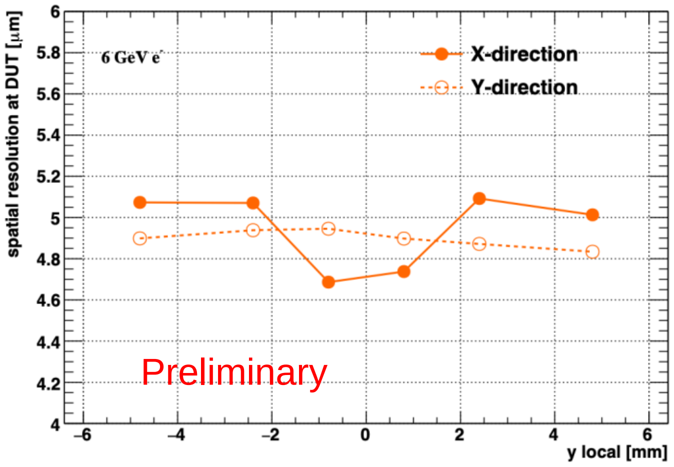
Preliminary spatial resolution





Made by Shuqi Li





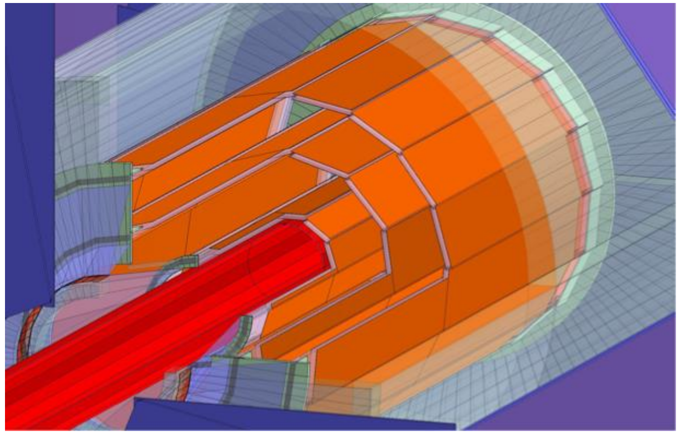
- 21 chips are working on the prototype.
- Beamline spot was recorded correctly.
- One flex is set as DUT, the rest chips are set as a telescope.
- Spatial resolution is around 5 µm

	L0-L1	L1-L2	L2-L3	L3-L4	L4-L5
L(mm)	21.2	20.6	37.46	20.6	21.2

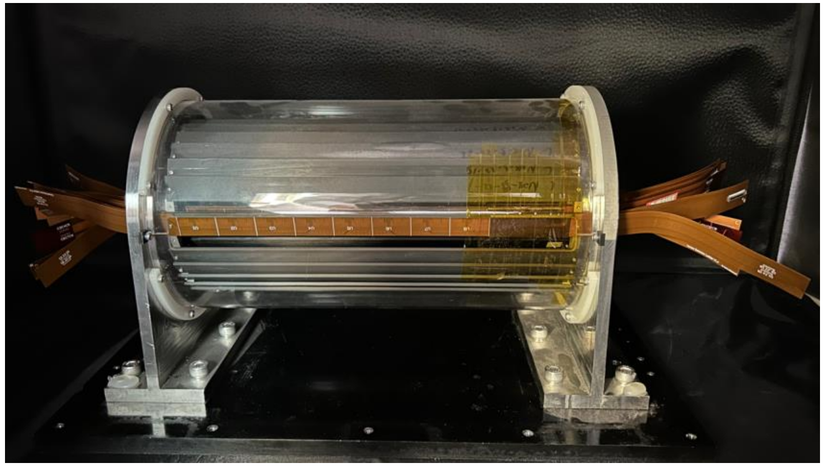
Preliminary offline results indicate a good performance for the vertex detector prototype.

Summary

- ✓ A full-size TaichuPix prototype has been developed and tested, demonstrating the spatial resolution (< 5 µm) and radiation hardness.
- ✓ The prototype marks the realization of the first CEPC silicon vertex detector prototype.
- ✓ Two setups were evaluated at the DESY II TB21 beamline, each revealing spatial resolutions less than 5 µm and detection efficiencies over 99%. This highlights the promising performance of the baseline vertex detector prototype for the CEPC.



Concept (2016)



Vertex detector prototype(2023)

Contribution list

- IHEP, CAS, China: João Guimarães da Costa, Wei Wei, Zhijun Liang, Ying Zhang, Tianya Wu, Shuqi Li, Wei Wang, Jia Zhou, Ziyue Yan, Xinhui Huang, Hao Zeng, Xuewei Jia, Jun Hu, Jinyu Fu, Hongyu Zhang, Gang Li, Linghui Wu, Mingyi Dong, Xiaoting Li, Weiguo Lu, etc.
- Nanjing University: Ming Qi, Lei Zhang, Xiaoxu Zhang, Yiming Hu , etc.
- Northwestern Polytechnical University: Xiaomin Wei, Jia Wang, Ran Zheng, etc.
- Shandong University: Liang Zhang, Jianing Dong , etc.
- IFAE, Barcelona, Spain: Sebastian Grinstein, Raimon Casanova , etc.
- …

Looking forward to more cooperation on CEPC

Thanks for your attention!

Introduction

- Motivation
  - Building a standalone offline analysis framework for CEPC vertex detector TaiChu pixel chip test beam
  - Track reconstruction

    no magnetic

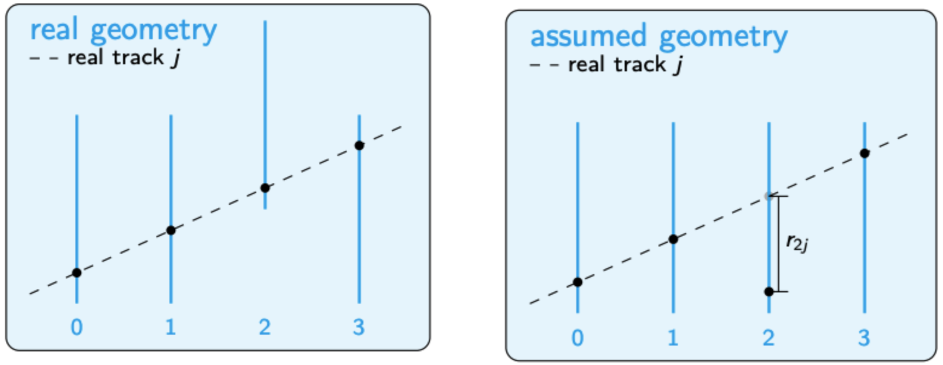
    straight line fit

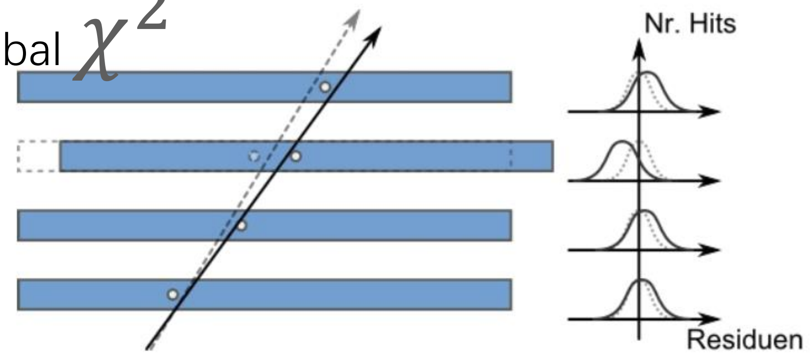
    no considering multi-scattering currently
  - Track alignment

    correction for the misalign chip position

    misalignment effects the resolution of detector

    find the solution of real geometry for global tracks based on global χ^2

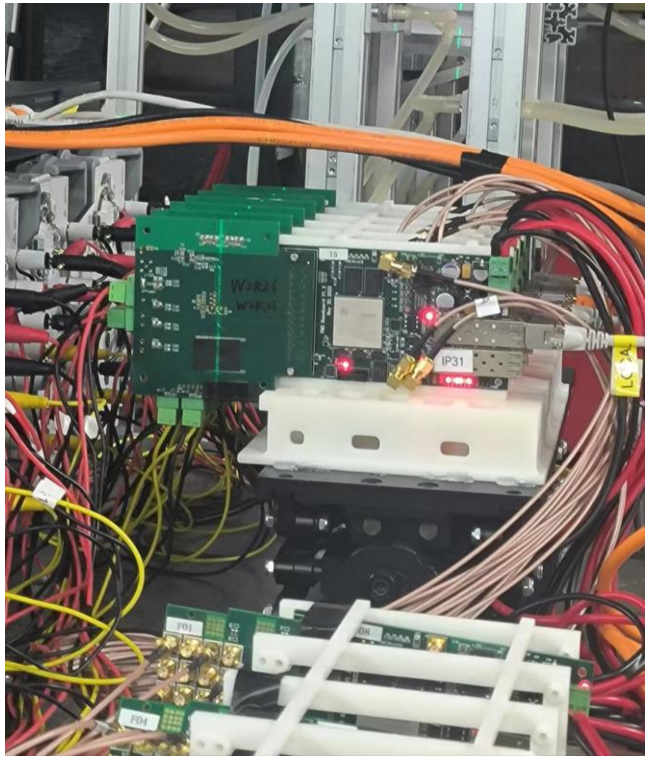




Residual: distance of measured hit with the intersection point of track in the measured chip

- TaiChu silicon pixel detector
  - Pixel size: 25 um
  - Theoretical resolution: 25um/sqrt(12) ~ 7.22 um
  - The experimental resolution should be better than theoretical resolution due to charge sharing

Track reconstruction

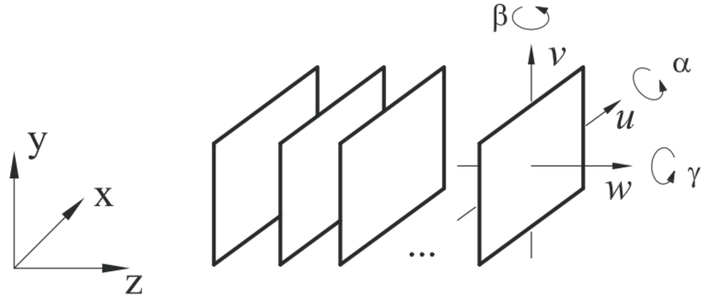


- Setup
  - 6 layer chips
  - 4cm between each other
  - electron beam energy 3-6 GeV
  - One of the chips is the detector under test (dut), the others are the telescope
- Steps for track finding and reconstruction
  - Finding hits in every chip with same time stamp of FPGA (+/- 1)
  - Forming adjacent hits into a cluster
  - No considering multiple clusters on one chip for one track currently
- Track fitting
  - least squares line fitting

x = a1z + b1;

y = a2z + b2;

Chi2 definition: $\chi^2(\alpha) = \sum_{i=1}^{n} \frac{f(x_i, \alpha) - e_i)^2}{\sigma_i^2}$, sigmax = sigmay = 25um/sqrt(12)



Track alignment

- Method - millepede matrix method

p: alignment parameters, q: track parameters

  - minimize: $\chi^2 = \sum_{i \in tracks} \vec{r}_i^{\,T} V_i^{-1} \vec{r}_i$ r is residual $\vec{r}_i(\vec{p}, \vec{q}_i)$, V is the covariance matrix

$$\frac{d\chi^2(\vec{p})}{d\vec{p}} = 0 \longrightarrow \chi^2(\vec{p}) = \chi^2(\vec{p}_0) + \left.\frac{d\chi^2(\vec{p})}{d\vec{p}}\right|_{\vec{p}=\vec{p}_0} (\vec{p} - \vec{p}_0) \longrightarrow \underbrace{(J^T V_i^{-1} J)}_{C} \Delta\vec{p} = \underbrace{J^T V_i^{-1} \vec{r}_i(\vec{p}_0)}_{b}$$

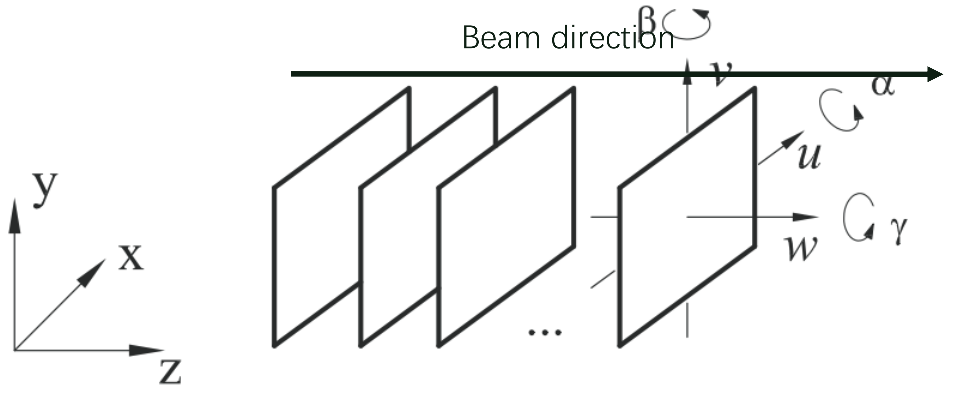
$$C \, \Delta\vec{p} = \vec{b}$$

  - invert the Matrix C to find alignment correction Δp
  - reduce matrix C for alignment only

$$S = C_{11} - C_{12} C_{22}^{-1} C_{21}$$

$$\begin{pmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{pmatrix} \begin{pmatrix} \Delta\vec{p}_1 \\ \Delta\vec{p}_2 \end{pmatrix} = \begin{pmatrix} \vec{b}_1 \\ \vec{b}_2 \end{pmatrix} \longrightarrow \begin{pmatrix} \Delta\vec{p}_1 \\ \Delta\vec{p}_2 \end{pmatrix} = \begin{pmatrix} S^{-1} & -S^{-1} C_{21}^T C_{22}^{-1} \\ -C_{22}^{-1} C_{21} S^{-1} & C_{22}^{-1} - C_{22}^{-1} C_{21} S^{-1} C_{21}^T C_{22}^{-1} \end{pmatrix} \begin{pmatrix} \vec{b}_1 \\ \vec{b}_2 \end{pmatrix} \longrightarrow \Delta\vec{p}_1 = S^{-1} \left(\vec{b}_1 - C_{21}^T C_{22}^{-1} \vec{b}_2\right)$$

  - Matrix S with smaller size than C, and C_{22} is easy to invert

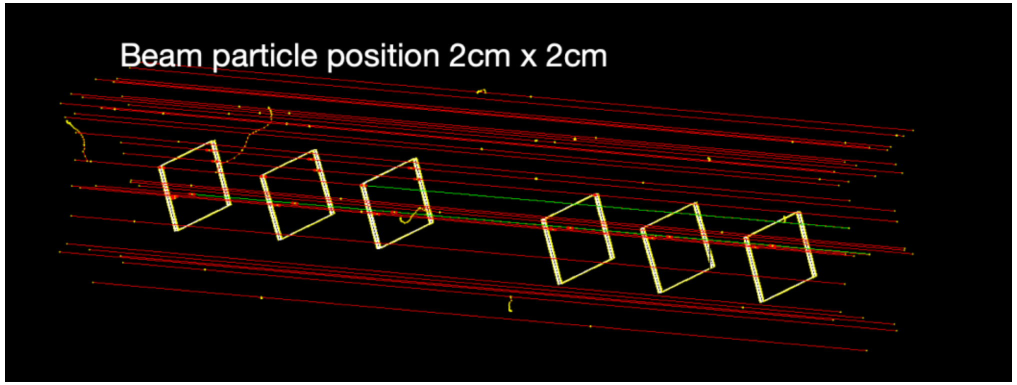


- Six alignment parameters considered
  - Translation along X, Y, Z direction
  - Rotation around X, Y, Z axis

Offline reconstruction and alignment

Track Reconstruction

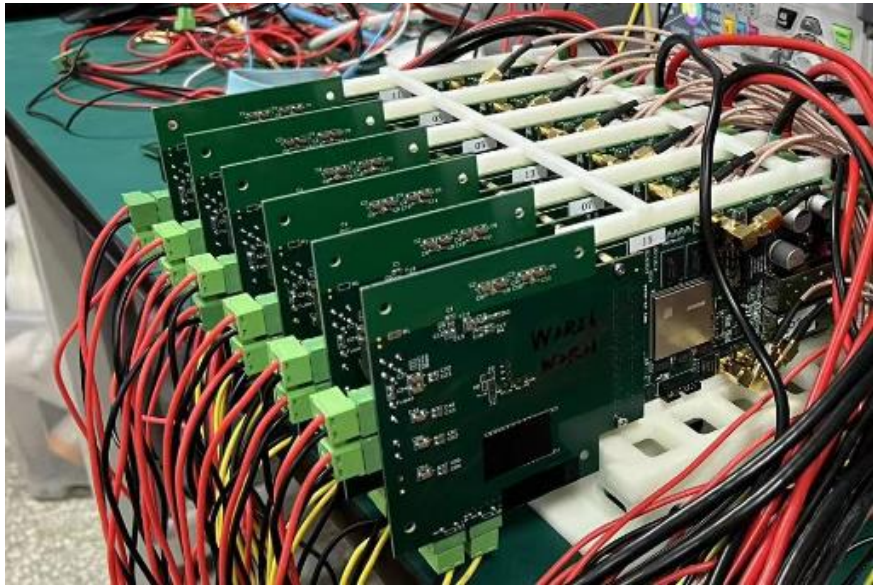
- No magnetic field
- Least squares fitting (Straight line fit)
- No considering multi-scattering now



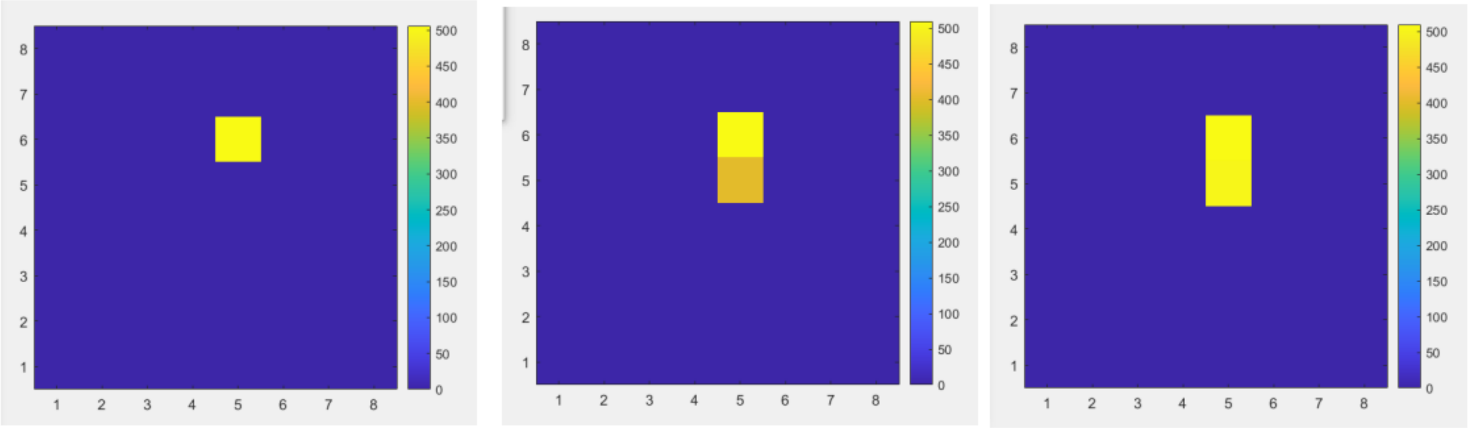
Alignment

- Using Millepede (c++ version) matrix method
- Correct for the misalignment chip position
- Evaluate the influence of different alignment parameters on spatial resolution

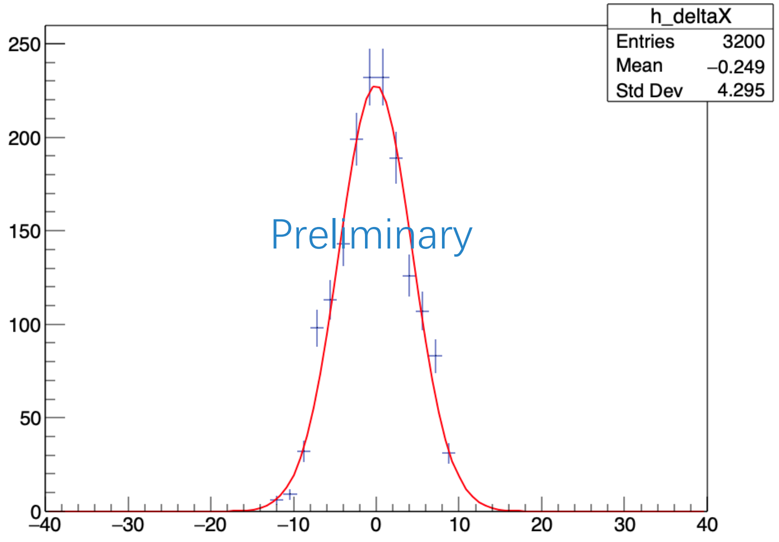
Designed by Shuqi Li



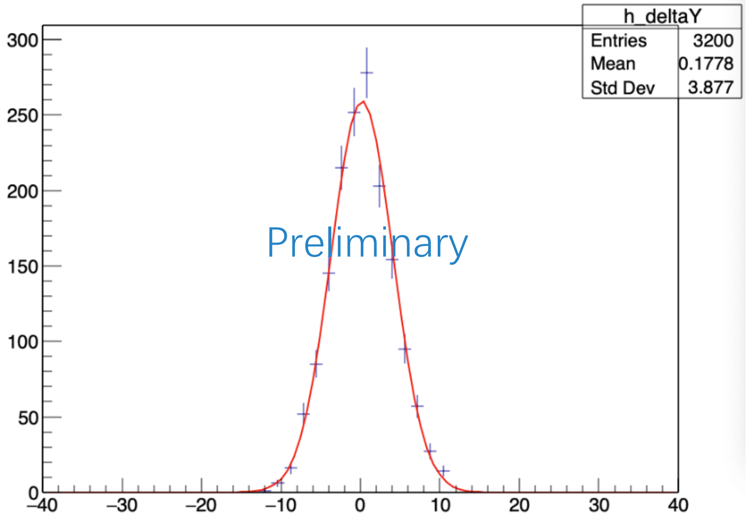
Preliminary spatial resolution with laser



- Laser was scanning with a step of 1 μm on the back of the TaichuPix2.
- Trace of two pixels' response can be figured out clearly on the hit map.
- Preliminary analysis of the data shows a spatial resolution less than 4.5 μm.



Sigma_residual_x =4.43 μm



Sigma_residual_y =3.93 μm

Made by
Wei Wang

Detection efficiency

- Efficiency definition:

$$\epsilon = \frac{N^{matched\ Tracks}_{|x_{meas},y_{meas}-x_{pre},y_{pre}|<d}}{N^{Tracks}_{tel}}$$

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- with increasing threshold, the efficiency decrease
- minimum eff. for DUT_A is 97%, minimum eff. for DUT_B is 89%