Development of Silicon Interposers with Embedded Microchannels and Metal Re-distribution Layer for the Integration of Hybrid Detector Systems

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Scope

- Introduction and Framework
  - Microchannel Cooling
- Embedded Microchannel Technology
  - Technological process
  - Microchannels
  - Wafer bonding
  - Initial Prototypes
- Current Objectives
  - Technological process
  - Metal with microchannels
  - Results
- Summary and Future Work

Framework

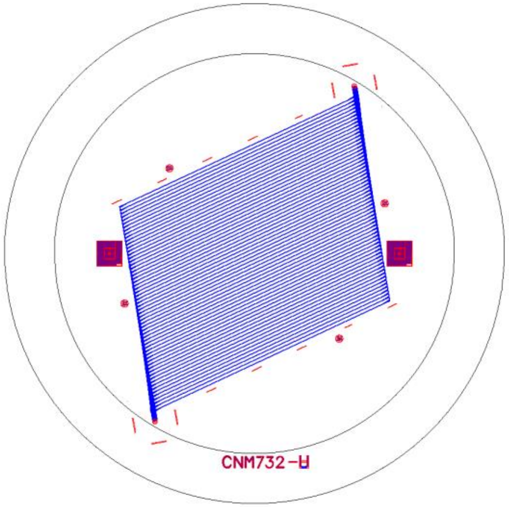
- In current HEP and other Physics experiments there is a need to keep the silicon detectors at low temperature (-10 ºC to -40 ºC)
  - ➢ Leakage current increase with temperature and irradiation
    - ⇒ Power needs → partial depletion → inefficiency
    - ⇒ Thermal runaway
- Different solutions
  - ➢ Air cooling
  - ➢ Liquid cooling
  - ➢ Bi-phase cooling
- Complex system integration (sensors, electronics, services)
  - ➢ Larger heat densities
  - ➢ Technology limits for pipe reduction and coverage
  - ➢ Thermal connection with sensors and electronics
  - ➢ Complex hybrid detector assemblies

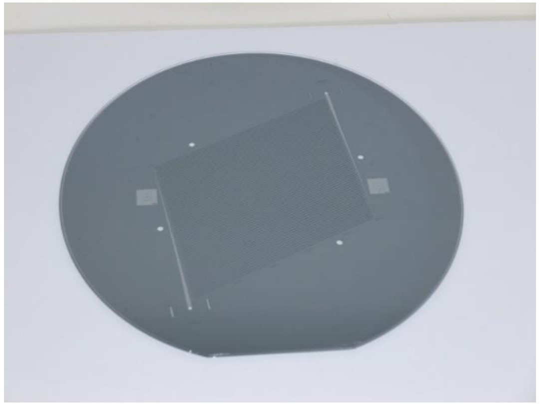
Enter Microchannel Cooling

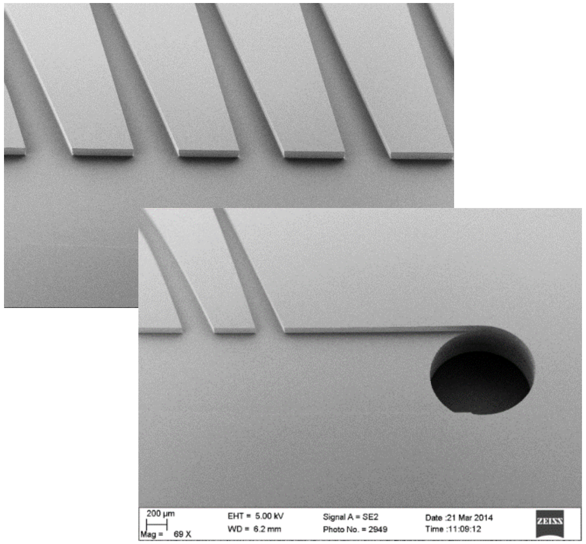
- In Electronics:
  - Scaling
  - High power (heat) densities
  - Heat transfer efficiency
- In HEP and other Physics facilities:
  - Reduce material (radiation length)
  - Many thermal cicles + position resolution → small (no) CTE mismatch
  - Large areas to refrigerate (lower heat density)
  - Thermal Uniformity → Non-uniform heat removal – “capilars”
  - Assembly and integration needs
- Our work:
  - Embedded microchannels basic technology development and prototyping
  - Using the IMB-CNM technological capabilities (DRIE, wafer bonding, CMOS processing)
  - DESY (Hamburg) in fluidic and thermal tests and system integration
  - X-FEL in simulations and design assessment

Past Work

- In the past, we developed the technology of embedded microchannel cooling for High Energy Physics detectors
  - N. Flaschel, et al. ”Thermal and hydrodynamic studies for micro-channel cooling for large area silicon sensors in high energy physics experiments”, NIMA, vol. 863, pp. 26-34, 2017. http://dx.doi.org/10.1016/j.nima.2017.05.003
  - Ph.D Thesis: Micro-channel Cooling For Silicon Detectors. Nils Flaschel. Hamburg University. 2017

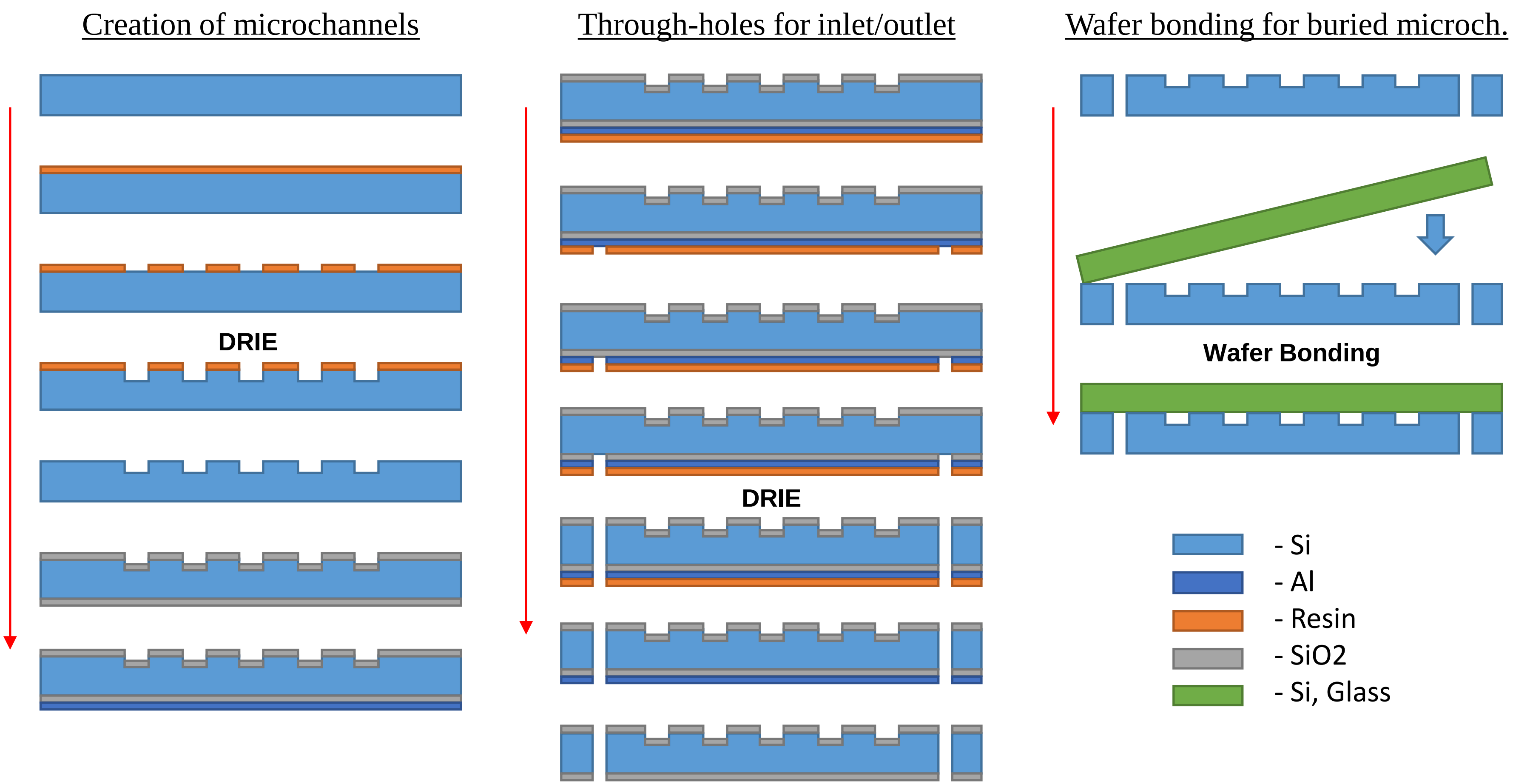




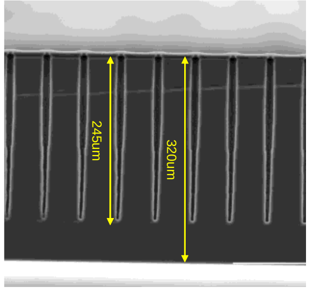


Technological Process

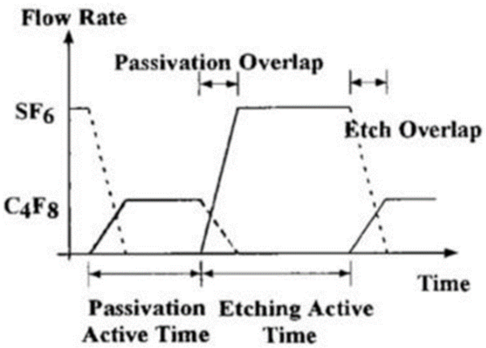
- Technological steps for buried micro-channels at CNM

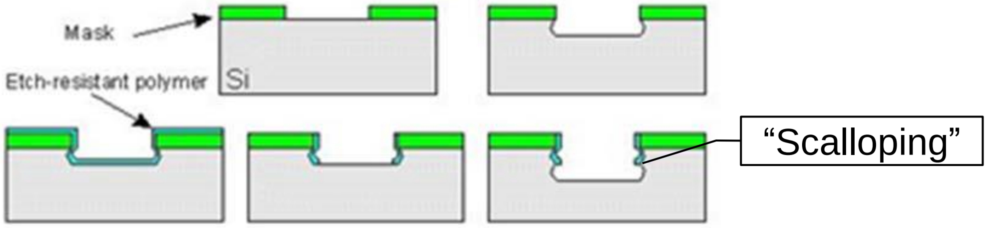


Creation of microchannels

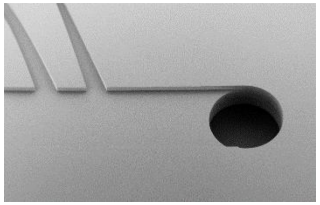


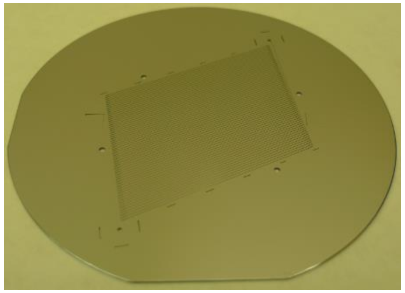
- Deep Reactive-Ion Etching (DRIE) (Alcatel 601 E)
  - Chemical-Physical etch of silicon
  - Very anisotropic → high aspect ratio (deep and vertical holes)
  - Bosch process: alternating between etching (SF_6) and passivation (C_4F_8)





- Two Si-etching processes
  - 1st to create the channels (100 um deep)
  - 2nd to form the inlet and outlet:
    - ✓ Through hole
    - ✓ "double-side" alignment

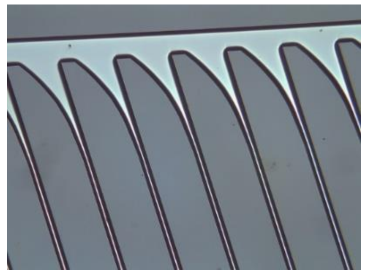
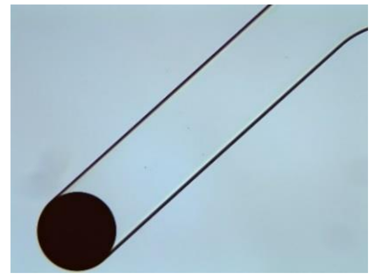




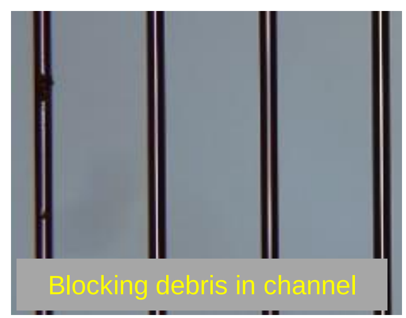
Microchannels – Test Methods

Microchannels evaluation

- Microscope – defect/yield analysis

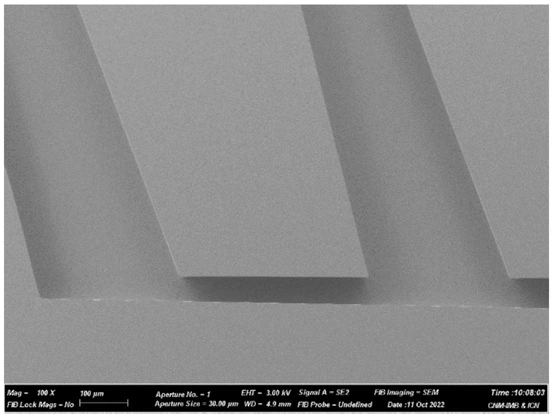
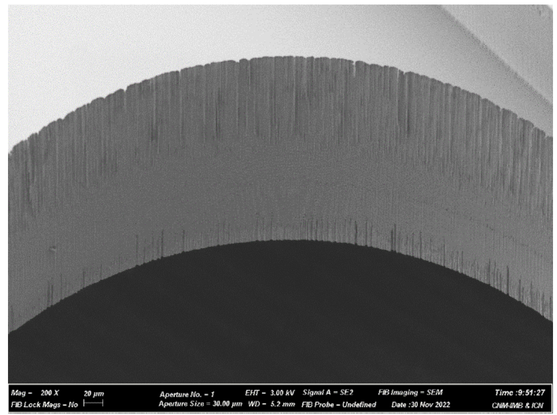
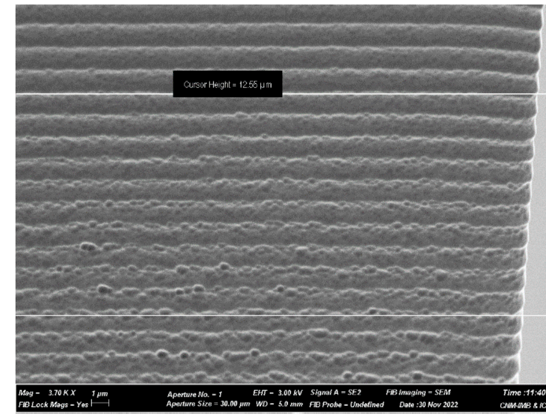
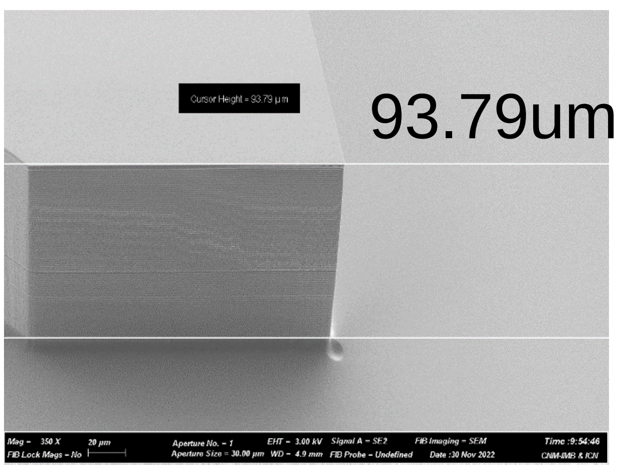
- Yield analysis made on 10 wafers (49 channels/wafer = 490 ch)
  - Several channels: Non-critical minor defects and dust
  - Three channels: Blocking debris (can be cleaned)
  - Seven channels: “Columnar” channel etch defect (not blocking)

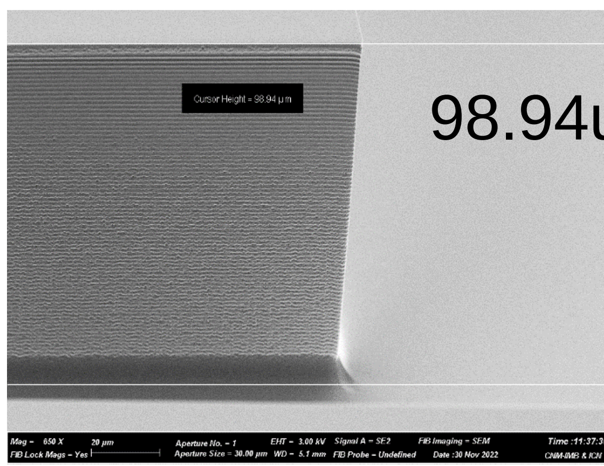


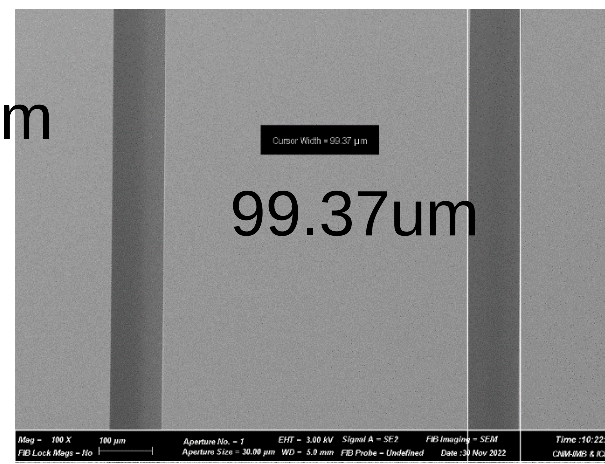
Microchannels – Test Methods

Micro-channels evaluation

- SEM (Scanning Electron Microscopy) (Zeiss Auriga 40)

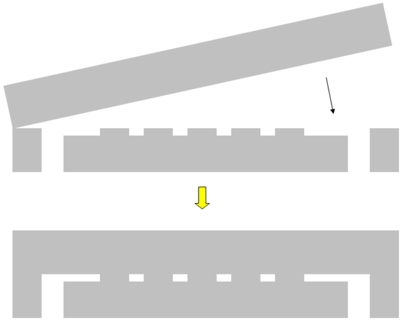


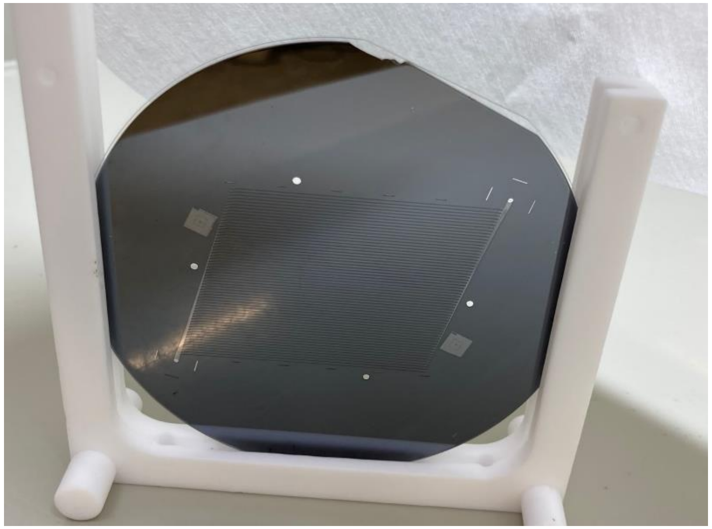


Basic Technology: Wafer Bonding

Wafer bonding (Süss Microtech Sb6e)

- Anodic: Borosilicate Glass – Si
  - High V (1000 V), Low T (~**350 ºC**),
  - PYREX®, MEMpax®
  - ☞ Micro-machining in the glass wafer
- Eutectic: Metal-Si
  - Low T (~400 ºC), Au
  - ☞ Al?
- Fussion/Direct: Si-Si
  - High pressure (2-8 Bar), Low T (~450 ºC),
  - ☞ Surface preparation is critical



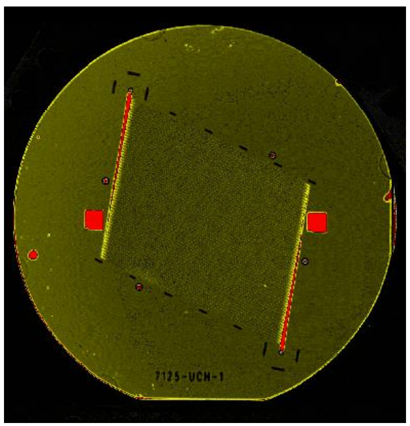


Wafer Bonding – Test methods

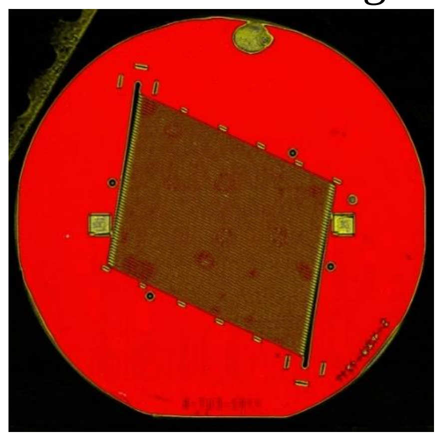
Wafer bonding evaluation

- SAM (Scanning Acoustic Microscopy) (Sonoscan-Gen5)

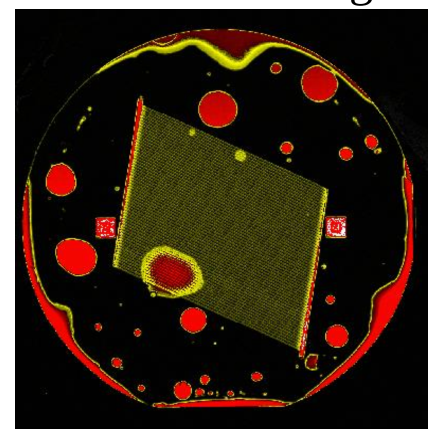
Anodic bonding:



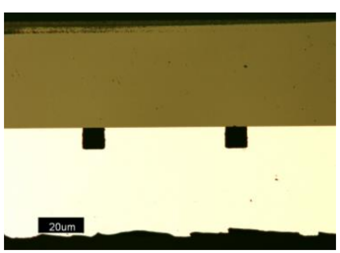
Eutectic bonding:

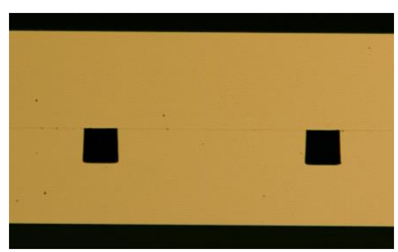


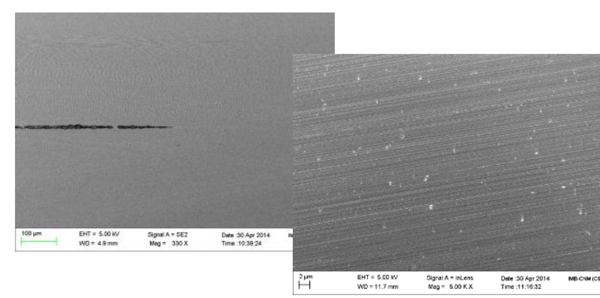
Fusion bonding:



- Cross sections (Reverse engineering)



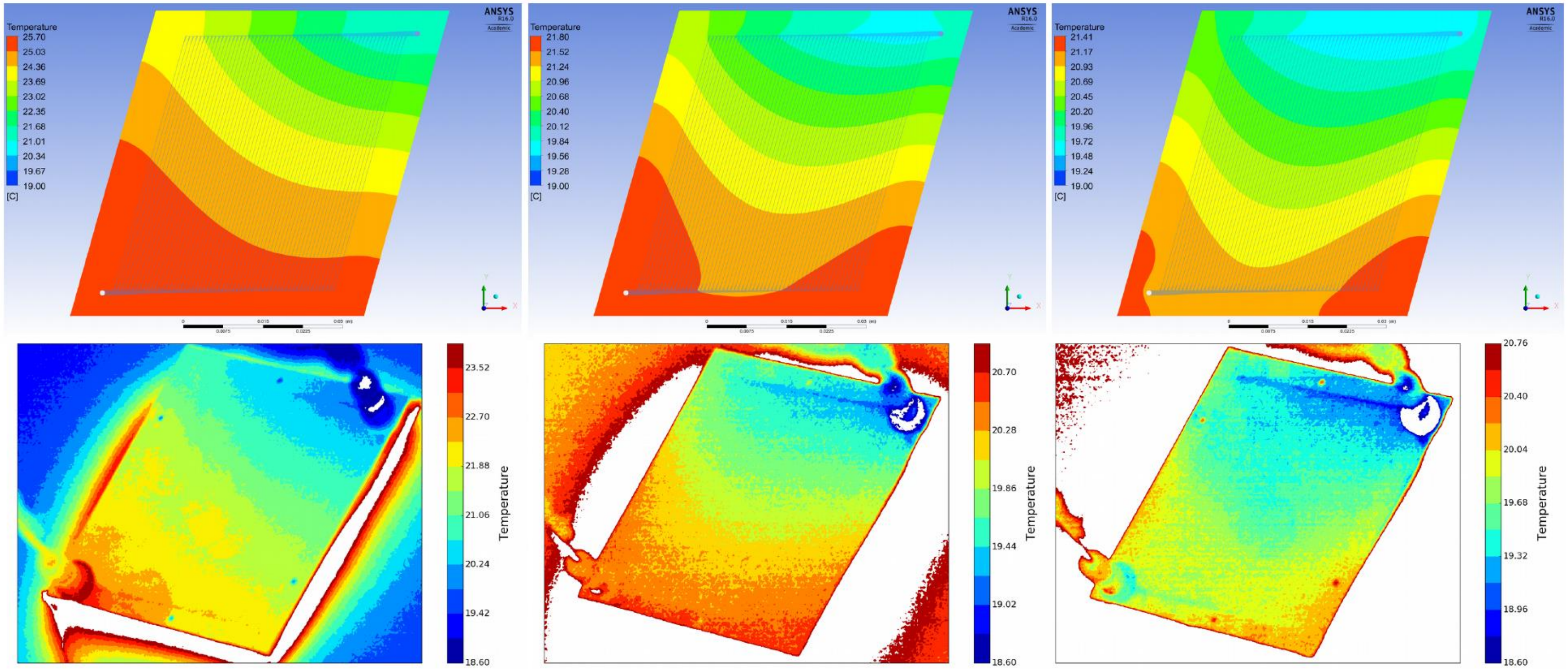




Initial Prototypes

- Fluidic and thermal tests
  - Laminar flow
  - Good agreement with simulation
  - Thermal homogeneity across the sample, < ±1 ºC (for lowest flow rate)

10 ml/min | 30 ml/min | 50 ml/min

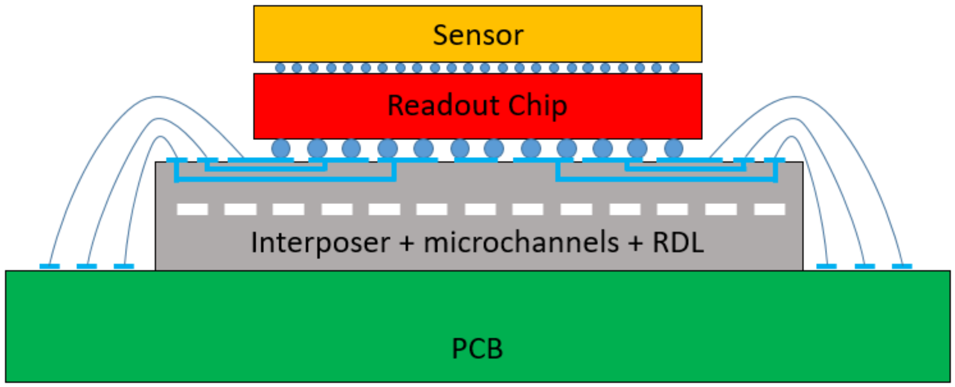


Current Objective

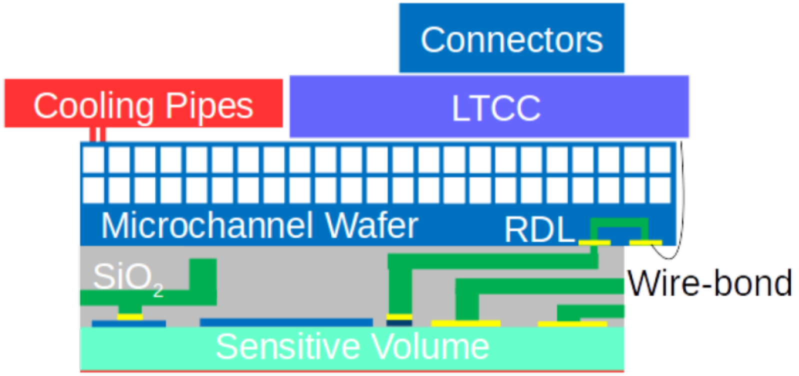
Integration of embedded micro-channels with metal Re-distribution Layer (RDL) in silicon interposers

- Combining the cooling capabilities with the electrical connection of the detector hybrid assembly – or monolitic detector – with the backend electronics and outside world
  - Both for signal and power routing

Hybrid assembly

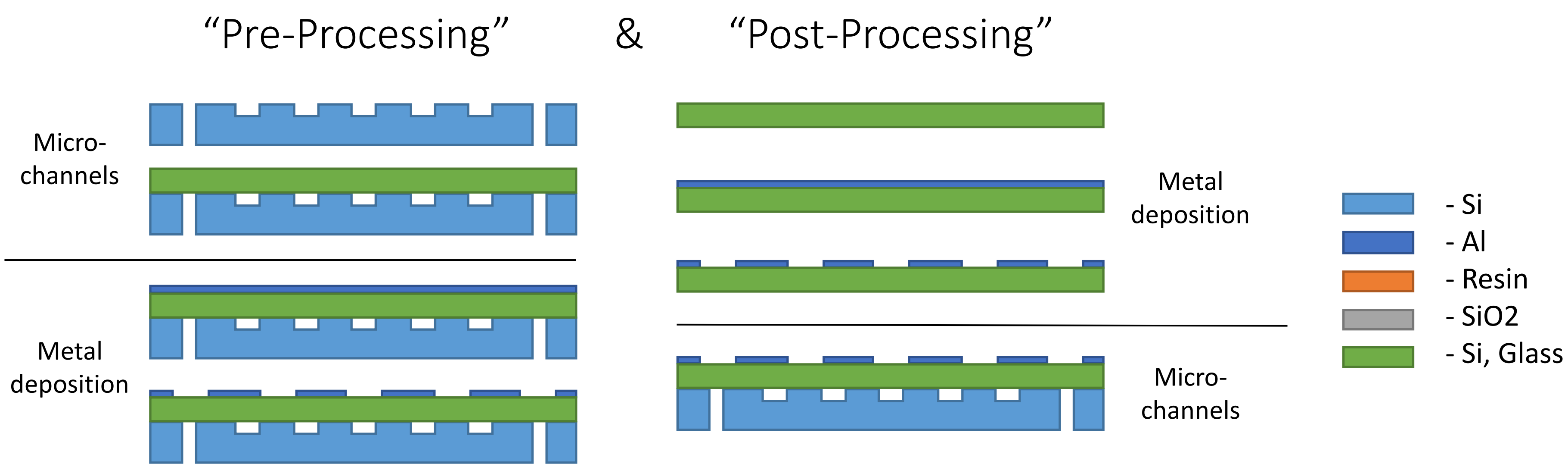


Monolithic integration



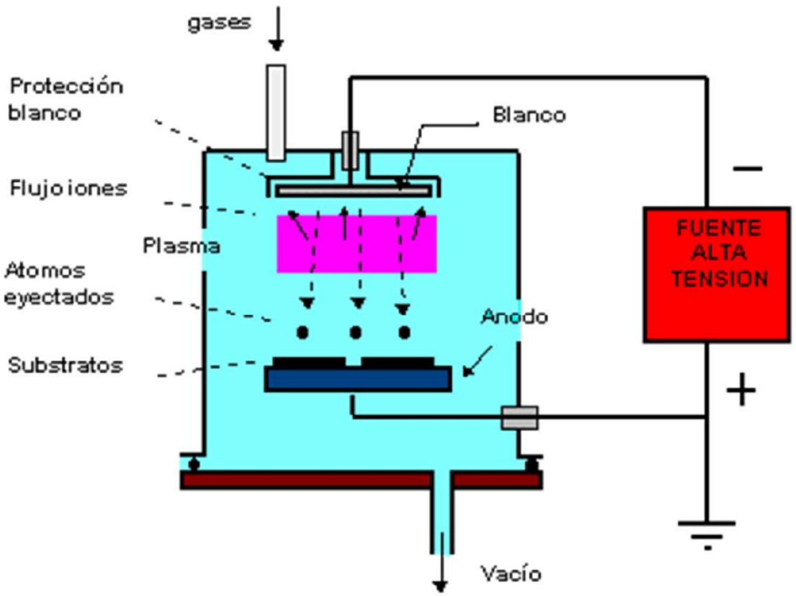
Technological process

- Technological options
  - **Pre-processing**: The microchannels are created first and then the metal is deposited on the assembly and structured with a photolithographic process
  - **Post-processing**: The metal is deposited and structured first on a single wafer, then the buried microchannels are created by wafer bonding



Metal deposition

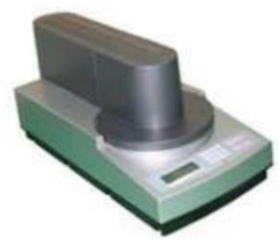
- Sputtering process (Kenosistec KS800H)
  - Sputtering system to deposit metallic layers
  - Target used: Al (99.5%) / Cu (0.5%)
  - Other targets available: Au, W, Ti, …
  - Better adherence than evaporation



Metal w/ µ-channels – Test methods

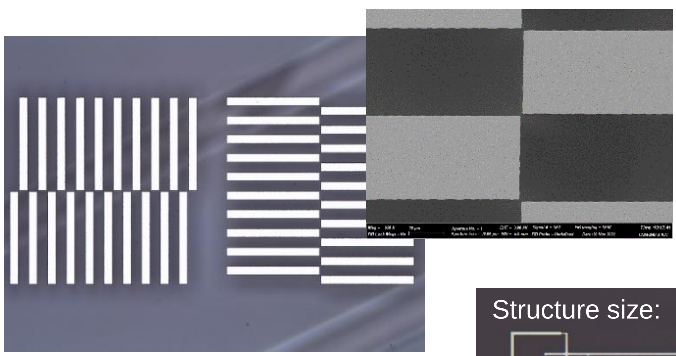
Metal evaluation (in assembly with micro-channels)

- Four point probe Resistivity Measurement (Chang Min Four)
  - ➢ Metal sheet resistance

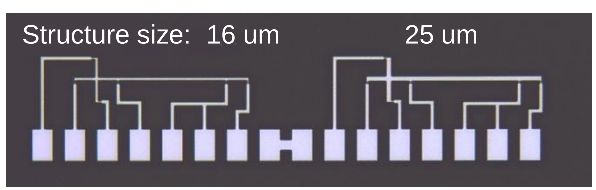


Al 1 um	Rs (Ω/□)	Rs St. deviation (Ω/□)
A-11	33.1E-3	1.3E-3
A-13	42.3E-3	4.4E-3
A-14	42.3E-3	4.9E-3

- Test structures (optical, CBR)

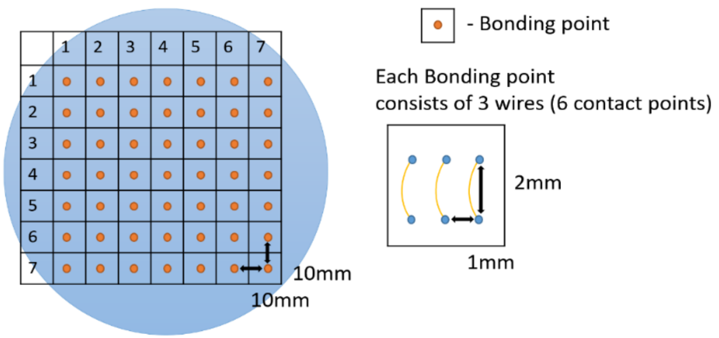


A-20, Al 0.5um	Small (avg.)	Wide (avg.)
Rs (Ω/□)	62.74E-3	63.18E-3
Rs St. deviation (Ω/□)	3.44E-3	3.48E-3
Weff (um)	15.02E+0	24.32E+0
Weff St. deviation (um)	236.31E-3	321.04E-3

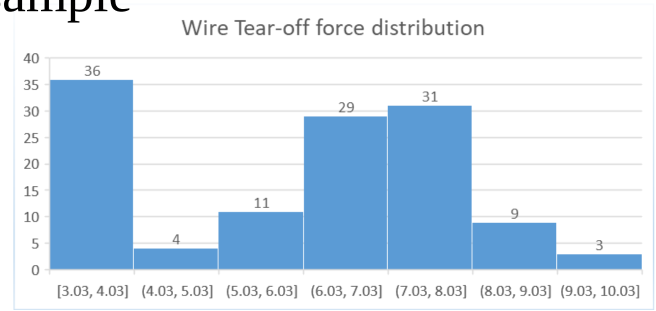


Metal evaluation (in assembly)

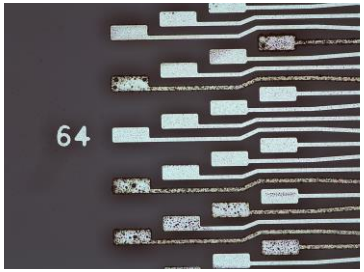
- Wire-bonding – pull tests
  - ➢ 7x7 array, 3 wires in each point. 25 um Al wire.



  - ➢ Test performed on **Pre-processing** blanket sample
    - – No parameter optimization
    - – Bonding on full wafer
    - – Final results on-going

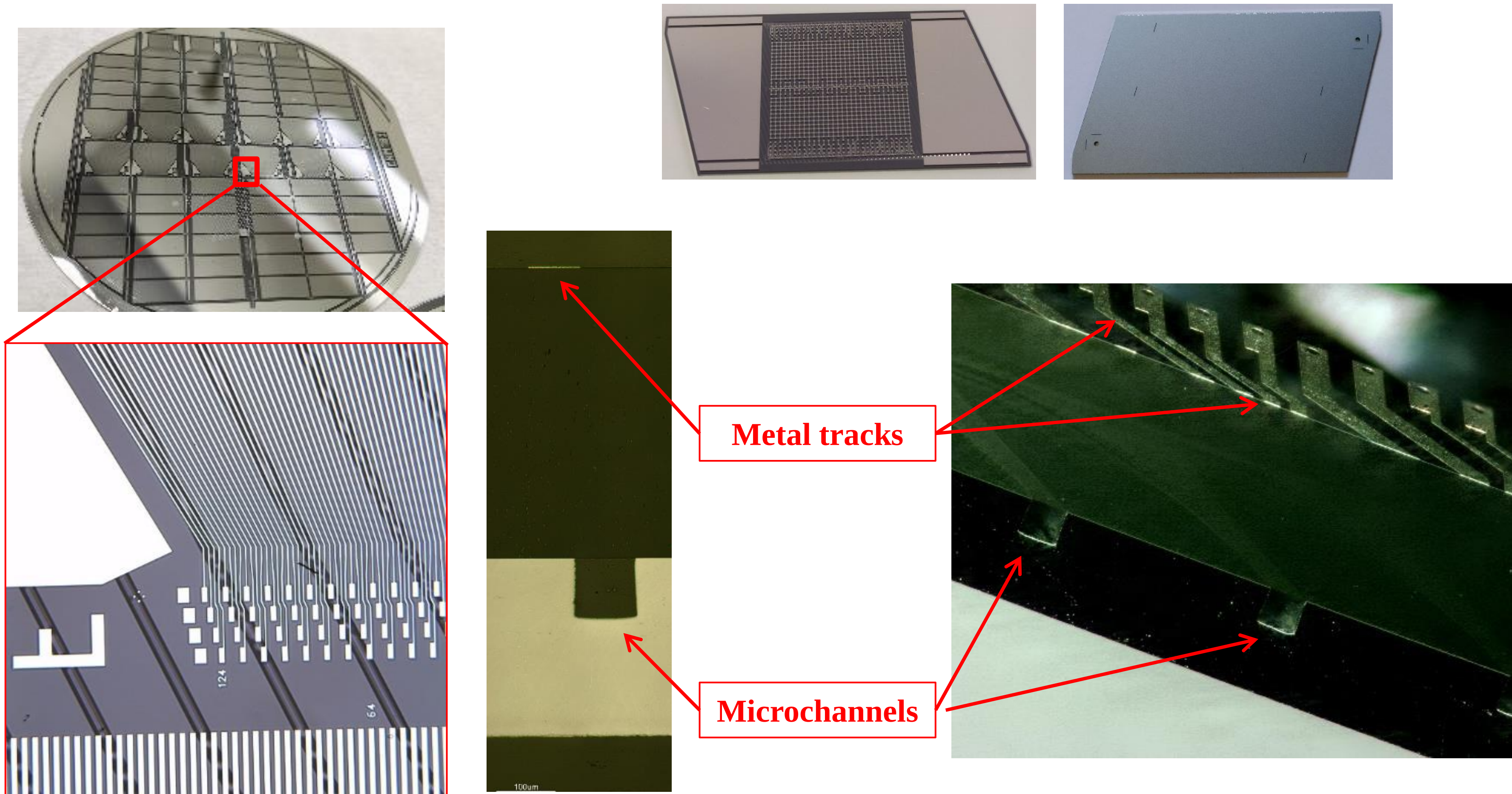


  - ➢ Test performed on **Post-processing** blanket sample
    - ☞ Bad adherence of Al layer on Silicon.
    - ☞ Problematic wire-bonding & pull tests
    - ☞ See optimization below



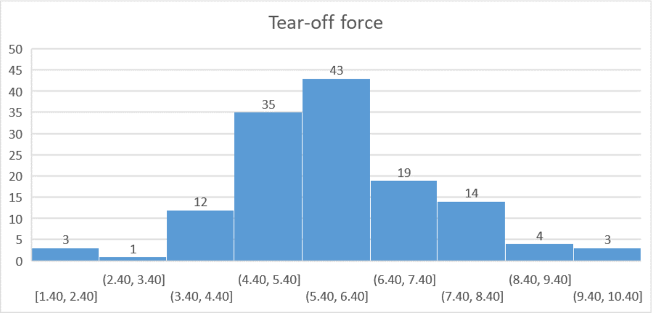
Current Status - Results

- Successful integration of micro-channels in silicon interposers with integrated signal (RDL) – **Pre-processing**

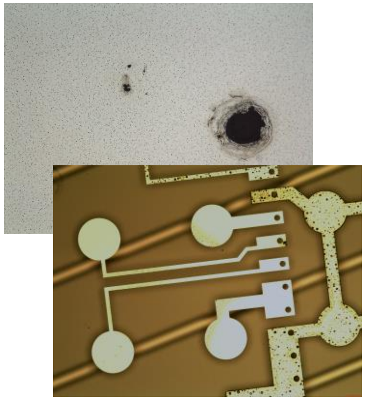


Current Status - Results

Post-processing



- Optimization of metal deposition process
  - ➢ Better metal test results on blanket wafers



- Still some localized problems observed in the metal layer
  - ➢ Could be derived from the ion displacement within the glass wafer, inherent to the anodic bonding process
  - ➢ Also some defects produced by the wafer electrode
  - ➢ Investigating
- Process modification to place the metal on the Silicon side.
  - ➢ Good metal results in blanket wafers
  - ➢ Final assemblies and tests on-going

Summary and Future Work

- Technology for embedded microchannel fabrication demonstrated
- Fluidic and thermal simulations and tests of the initial prototypes
  - Good hydrodynamic and thermal behavior
  - In good agreement with simulations
- Successful integration of micro-channels in silicon interposers with integrated signal (RDL)
  - Good tests results at the different technological steps
- Optimization needed for some technological alternatives
  - Metal on Silicon
  - Eutectic and fusion bonding
- Thermal and fluidic tests with new prototypes have started
- Working on further integration of microchannel cooling for a full system
  - Exploring other technological options (microchannels on glass, TSV, …)
  - Full monolithic integration with CMOS processing

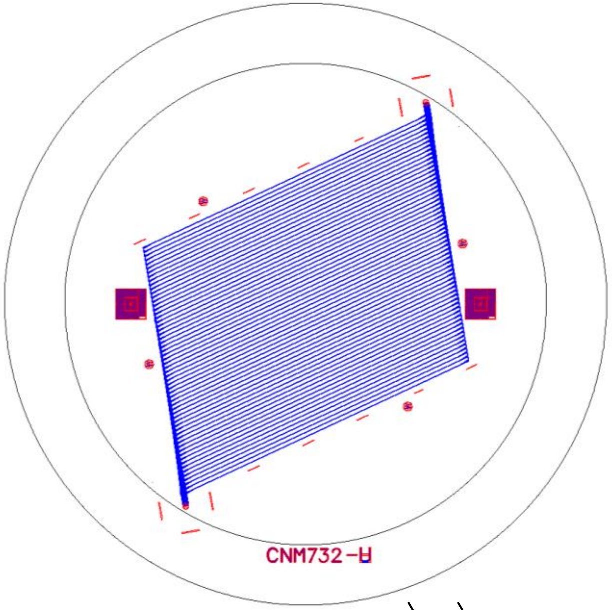
Thank you for your attention

Backup

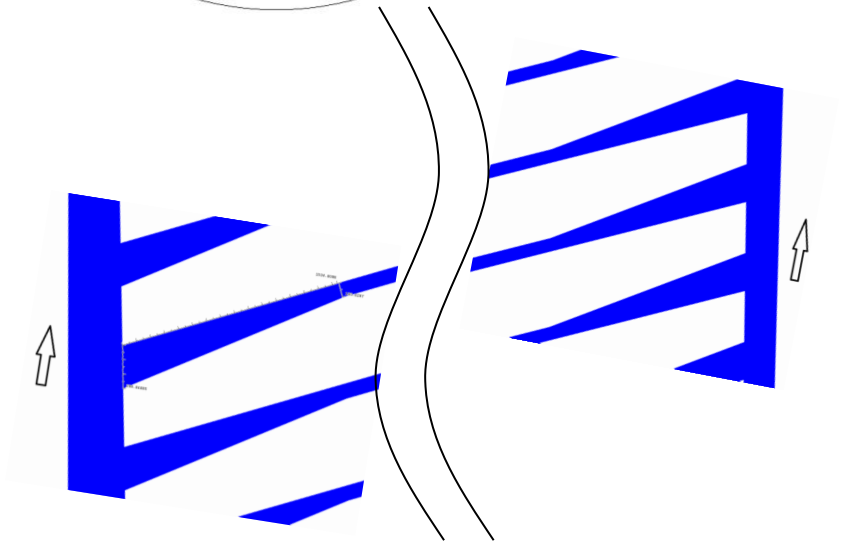
Design

Design Features:

- Full 4'' wafer ATLAS-prototype design
- Parallel flux
- Uniform heat removal
- 60 channels
- Width & depth 100 um,
  pitch 675 um, separation 575 um
- 15º inclination with respect to manifolds to facilitate flux
- Gradual channel inlet and outlet with 250 um initial width, and 2000 um length to facilitate flux
- Special manifold design developed by simulation to assure uniform flux
- 10º rotation to mis-align channels with respect silicon crystal lattice for mechanical stability



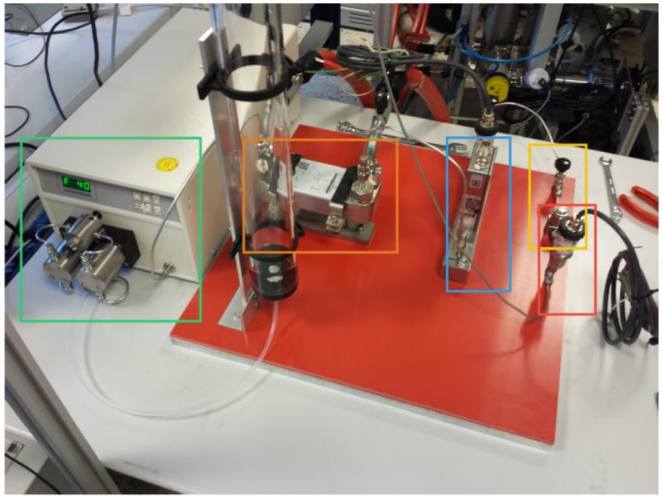
ATLAS-Itk-Strips prototype cooling



Hydrodynamic tests

Setup

- Green: Pump
- Orange: Heat Exchanger
- Blue: Flow Meter
- Yellow: Valve & Filter
- Red: Pressure Sensor
- Transparent column: Fluid Reservoir



Pressure vs. flow tests

- Simulation with laminar flow model
- Good simulation agreement with prototype A, B and D
- Most likely prototype C has some flow problems
- Critical pressure around 31 bar