# The ATLAS ITk Pixel Detector Status and Roadmap



Stefano Passaggio (INFN Genova) on behalf of the ATLAS ITk Collaboration



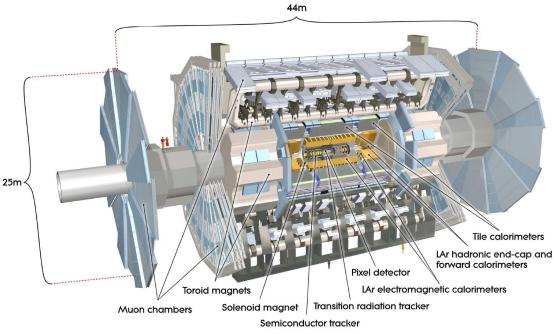
13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors HSTD13, Vancouver, Canada, 3-8 Dec 2023

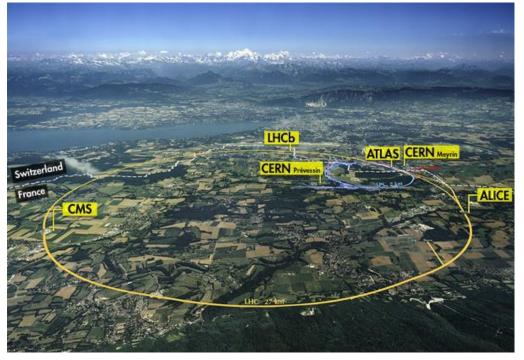
### LHC and ATLAS



### Large Hadron Collider at CERN

- 27km circumference
- Protons and heavy ions
- 4 experiments





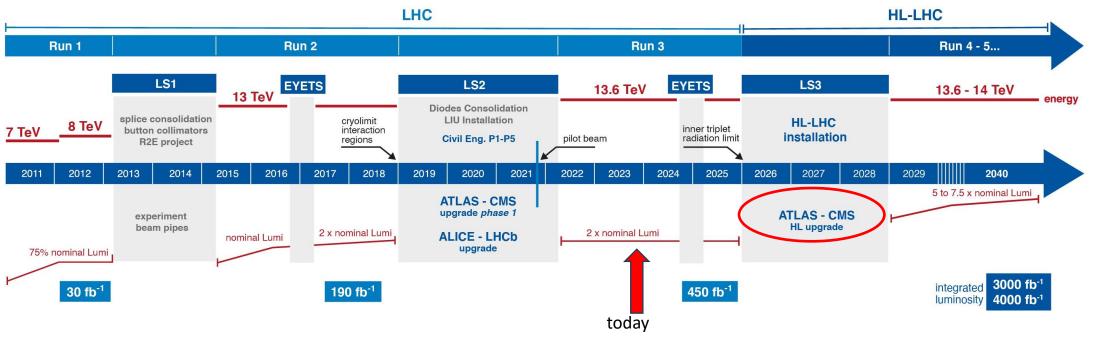
### ATLAS

### Layered multi-purpose detector

- Tracking
- Calorimetry
- Muon Spectrometry

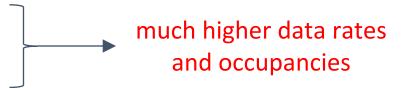
# High Luminosity LHC Upgrade





Phase-II upgrade of ATLAS in progress in parallel with ongoing Run3 Data Taking HL-LHC data taking planned to start in 2029 and to accumulate 4000 fb<sup>-1</sup> (x10 of Run3) The upgraded tracker will need to <u>cope with</u>

- 200 interactions per bunch crossing on average
  - Currently: ~50
- x5 pileup
- x10 integrated luminosity  $\rightarrow$  x10 radiation damage



### ITk – The new Inner Tracker



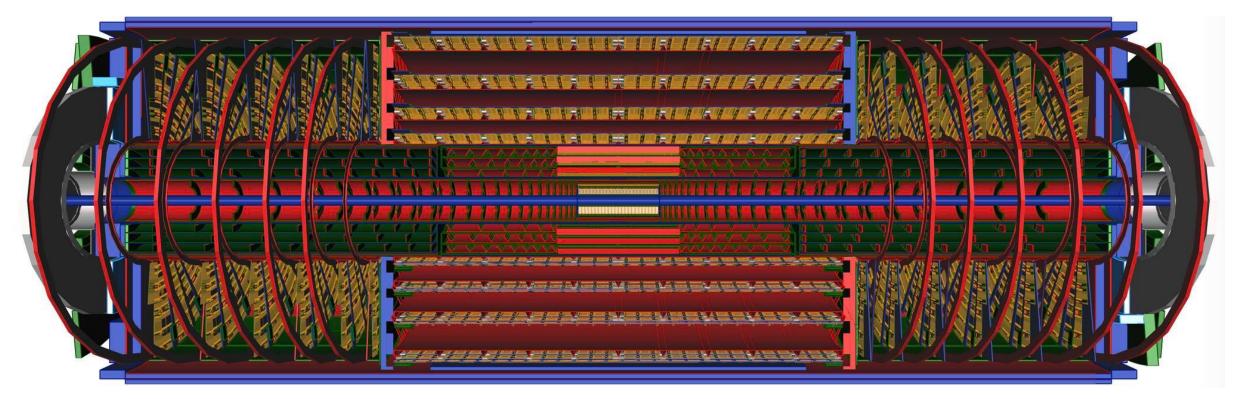
#### All-silicon

Coverage up to  $|\eta| < 4$ 

- $\geq$  13 hits / track (barrel)
- ≥ 9 hits / track (forward)

The ITk tracker consists of **outer strip tracker** and **inner pixel tracker** to replace current ATLAS "Inner Detector"

- 168 m<sup>2</sup> of silicon strip and 13 m<sup>2</sup> of silicon pixel
- Designed to withstand up to  $10^{16} n_{eq}/cm^2$  on the innermost pixel layer



#### ATL-PHYS-PUB-2021-024

# ITk – The new Inner Tracker

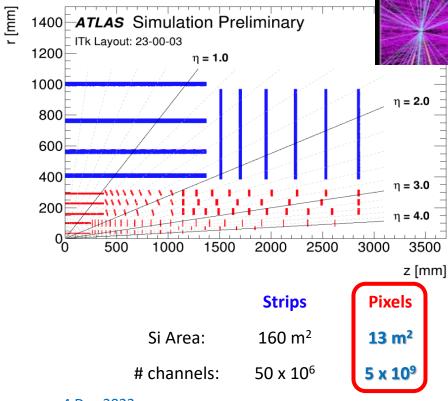


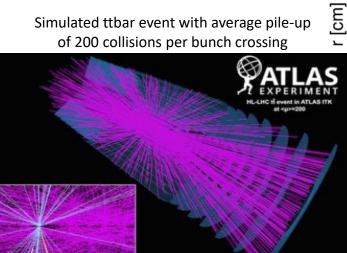
#### All-silicon

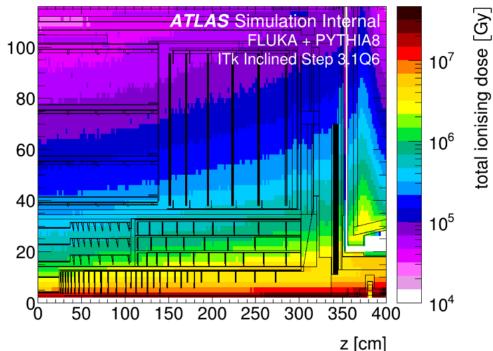
Coverage up to  $|\eta| < 4$ 

- ≥ 13 hits / track (barrel)
- ≥ 9 hits / track (forward)

#### ATL-PHYS-PUB-2021-024







#### **Requirements for ITk pixel detector**

- <u>Radiation hardness</u> up to
  - 10 MGy (TID)
  - 2x10<sup>16</sup> n<sub>eq</sub>/cm<sup>2</sup>
- <u>Track reconstruction efficiency</u>
  - > 99% for muons
  - > 85% for electrons and pions
- <u>Fake rate < 10<sup>-5</sup></u>

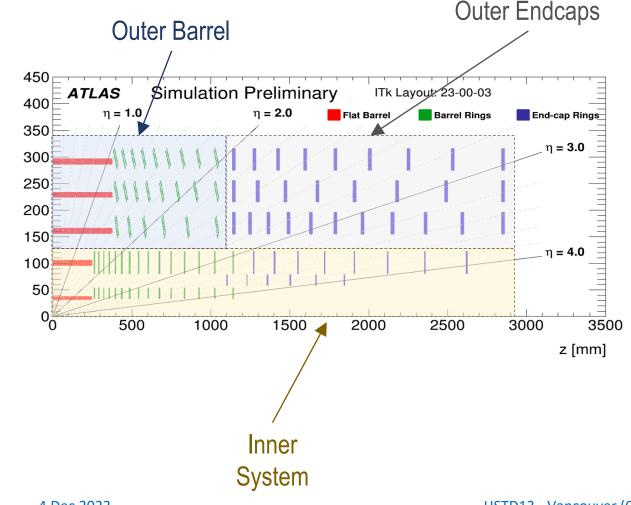
- Occupancy < 1%</li>
- <u>Robust</u> against loss of 15% of channels
- Readout rate 1 MHz
- <u>Output bandwidth up to</u>
  5.12 Gb/s per front-end chip
- <u>Material budget</u> ~ 2.0% X<sub>0</sub>
  per layer 5

4 Dec 2023

### **The ITk Pixel Detector**



#### Three distinct sub-systems with complementary designs



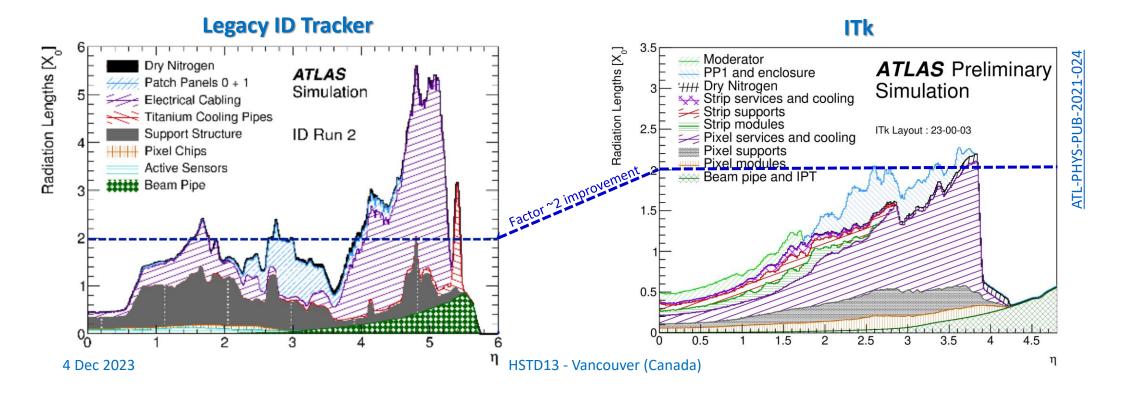
- Aimed at keeping the silicon ~normal to high-p tracks from the interaction point
- Work on mechanics and on-detector services is organized in geographical clusters
  - Outer Barrel: CERN, Switzerland, France, Germany, Japan
  - Outer Endcaps: Italy, UK
  - Inner System: USA
  - Facilitates detailed collaboration
  - Minimises parts flow across borders
  - Some exchanges e.g. UK/Italy, Japan/Europe require careful handling
    - $\rightarrow$  special logistics group based at CERN
  - Provides local redundancy
    - we can help each other through temporary problems
      - equipment failure
      - personnel problems

### **Material Budget**



#### **Material reduction strategies**

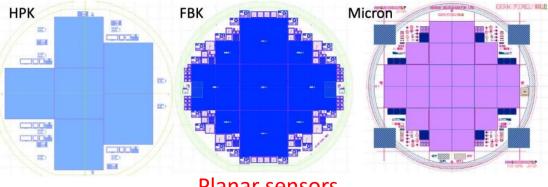
- CO<sub>2</sub> cooling with <u>thin-walled titanium pipes</u>
- Minimize material in modules using thin sensors and FE-chips
- Serial powering  $\rightarrow$  fewer cables
- Low-mass carbon structures for mechanical stability and mounting
- Optimize number of readout cables using data link sharing



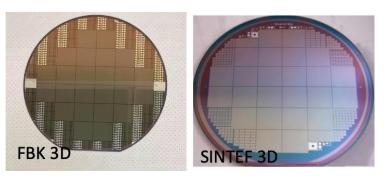
### **Silicon Sensors**

### Sensor production is in progress

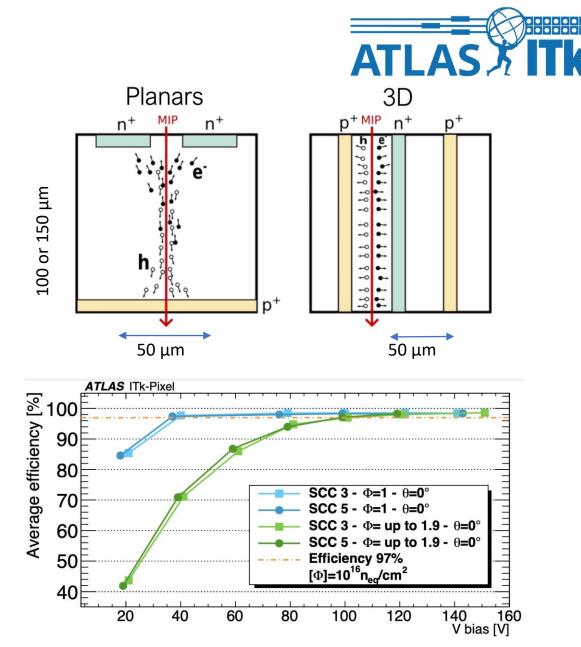
- Following successful pre-production (10% of total)
- Including qualification in beam tests and with irradiated samples



Planar sensors



3D sensors



#### FBK sensor performance after irradiation to 1.0 and 1.9 10<sup>16</sup>n<sub>eq</sub>/cm<sup>2</sup>

HSTD13 - Vancouver (Canada) @HSTD13, see: 8 Christopher Krause "TB perf. of pixel detectors for the ITk Upgrade of the ATLAS exp"

# **FE chips and Hybrid Modules**

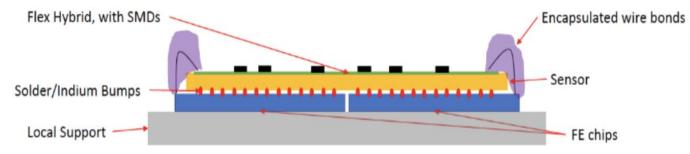
Abhishek Sharma "Module development for the ATLAS ITk Pixel Detector"

ATLAS

### The Hybrid Module

### **The Front-End Chip**

- Developed by RD53 collaboration
- Joint effort for ATLAS and CMS
  - common chip design
  - slight difference in FE and matrix size
- Rad-hard chip design, 65nm technology
- Chip size
  - 400 x 384 (153,600) 50x50 μm<sup>2</sup> pixels
  - $2.0 \times 2.1 \text{ cm}^2$
- Shunt-LDO regulator for serial powering
- Production design completed and submitted in March 2023
  - Prototyping: RD53A, ITkPixV1
- First 100 ITkPixV2 production wafers now in hand and being tested
- Main focus of tests:
  - verify fixes implemented from previous version

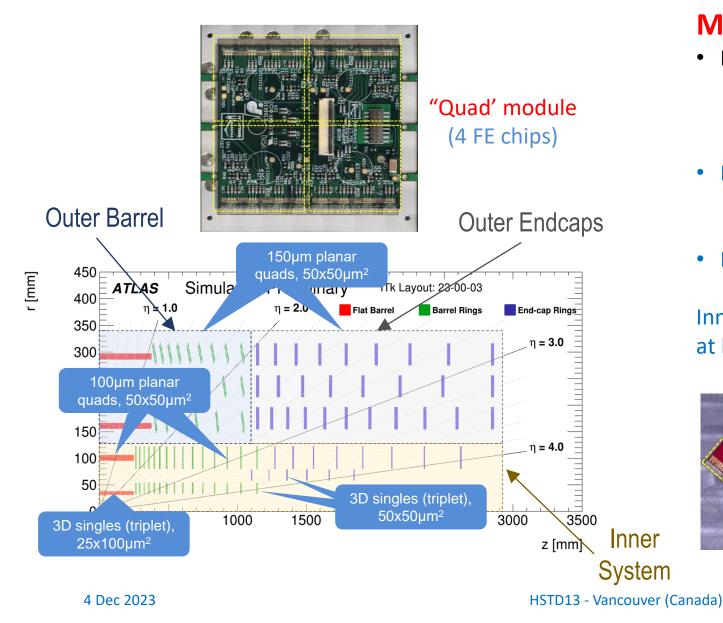


#### • 1 or 4 FE chips bump-bonded to sensor

- 4 industrial vendors
- Cu-Kapton flex hybrid glued to sensor
- Common flex design for quads  $\rightarrow$  modularity for production
- Flex provides connection to power, slow controls and data distribution
  - Wire bonds connect the flex to the FE chip(s)
  - "Pigtails" connecting modules to power / monitoring are subsystem-specific
- Serially-powered to reduce cable mass
- Up to 14 modules in a single power chain
- Up to 7A per module

### **Module Placement**

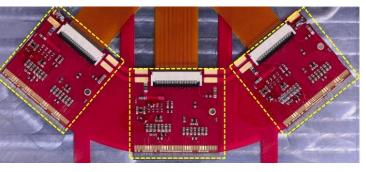




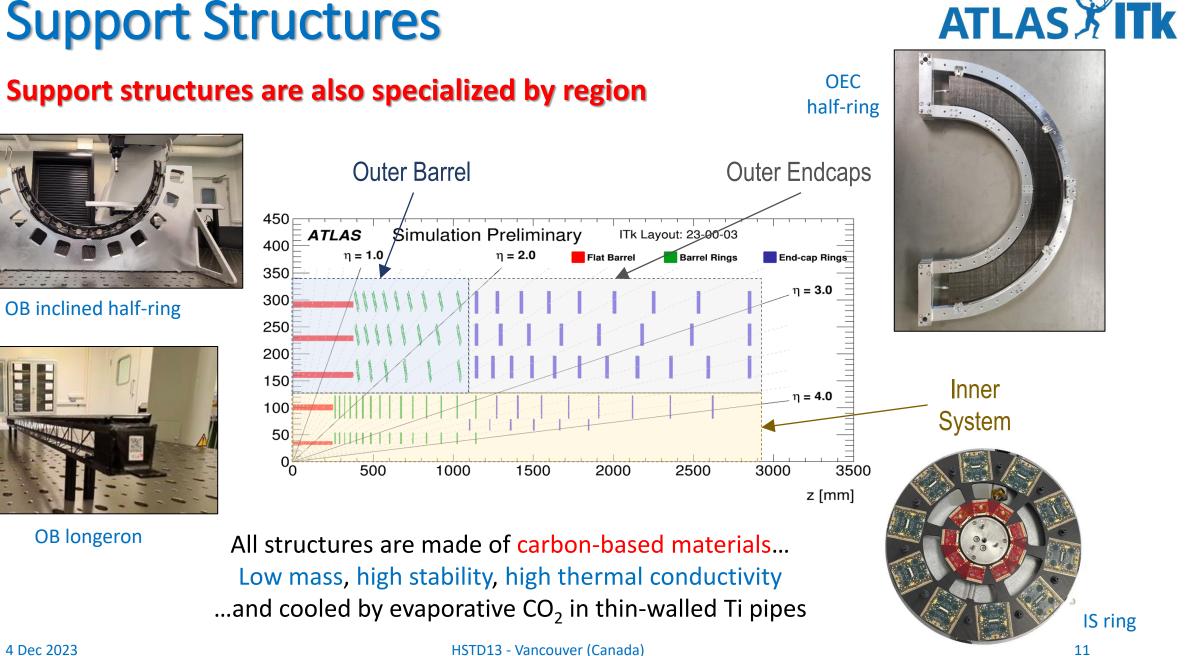
#### **Module type is region-dependent**

- Innermost layer ("Layer 0"): 3D sensors
  - Higher radiation tolerance
  - Lower power consumption  $\rightarrow$  easier servicing
  - Pixel size 50x50 μm<sup>2</sup> or 25x100 μm<sup>2</sup>
- Layer 1
  - 100µm thick planar Si
  - Pixel size  $50x50 \ \mu m^2$
- Layers 2-4

150μm thick planar Si, 50x50 μm<sup>2</sup> pixels
 Innermost two layers will be replaced
 at half-lifetime (~2000 fb<sup>-1</sup>)



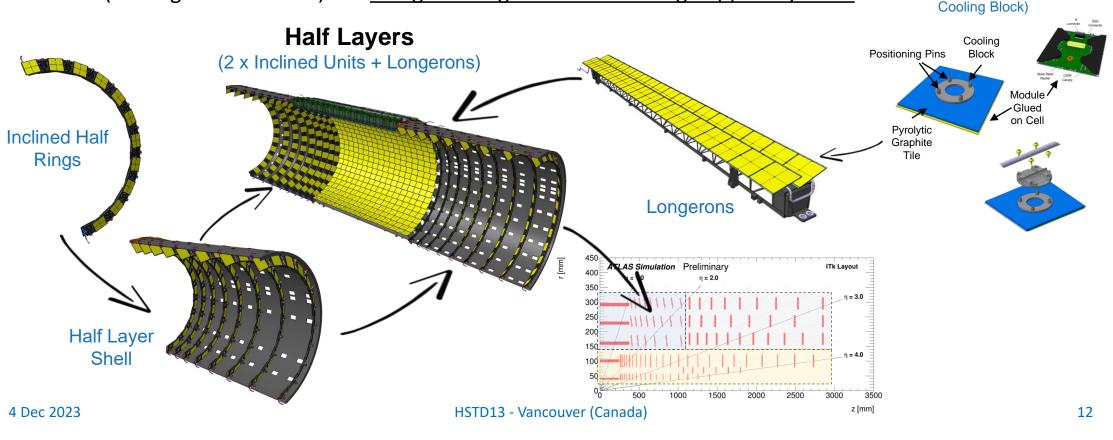
3 Single-chip modules in a "triplet"



# Outer Barrel Supports

Modules are glued to pyrolytic graphite tiles, which are then attached to <u>supporting structures</u> with integrated cooling pipes:

- In the central (low-η) region modules are "flat", on lightweight open structures called "longerons" Adjacent rows of modules overlap in φ
- In the mid-η region, inclined-module layout keeps modules ~normal to high-p<sub>t</sub> tracks
- Services (cooling and electrical) run along the longerons and the ring-support cylinder



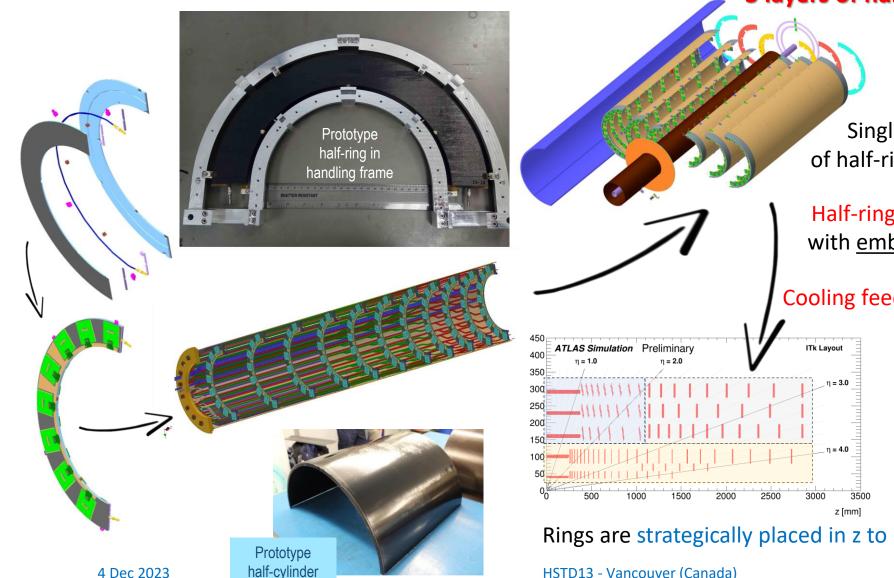


Module Cells

(Module + PG Tile +

### **Outer Endcap Supports**





**3** layers of half-rings loaded into half-cylinders

Single rows of modules on both sides of half-rings  $\perp$  to beampipe  $\rightarrow \Phi$  hermeticity

Half-rings are C-foam / C-fibre "sandwiches" with embedded cooling pipe and fixation lugs

Cooling feed, exhaust lines and electrical cables run between outer rims of rings and inner surface of cylinder

Rings are strategically placed in z to provide hermeticity in  $\eta$ 

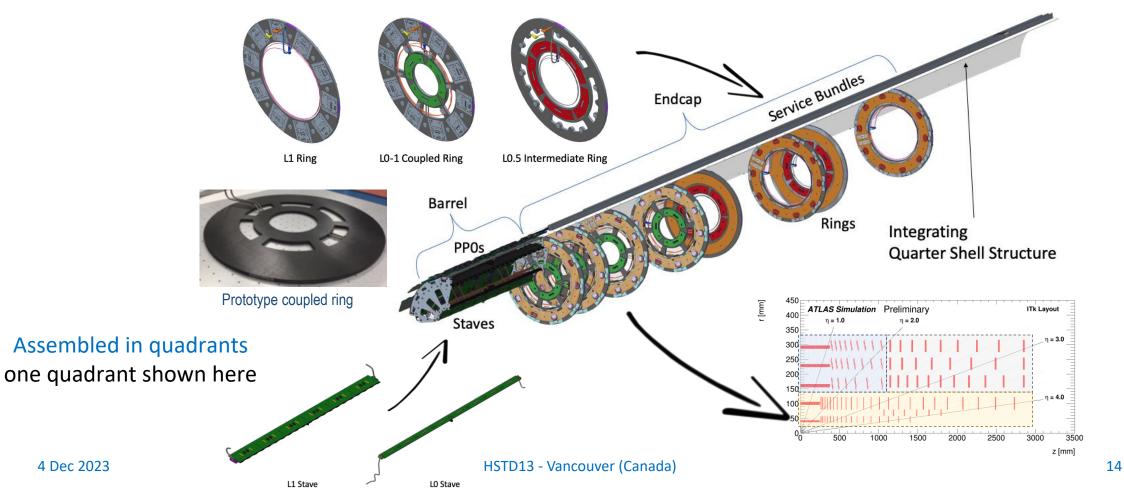
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### **Inner System Supports**



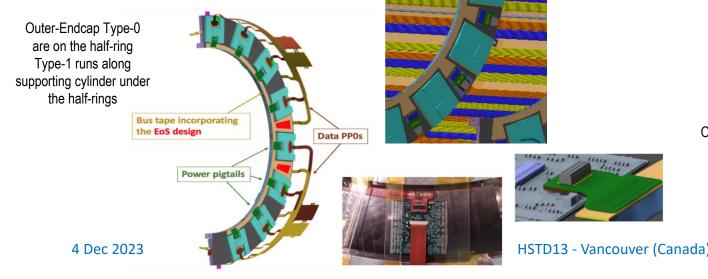
#### The inner system will be contained inside an Inner Support Tube and will be replaced once (at ~2000 fb<sup>-1</sup>)

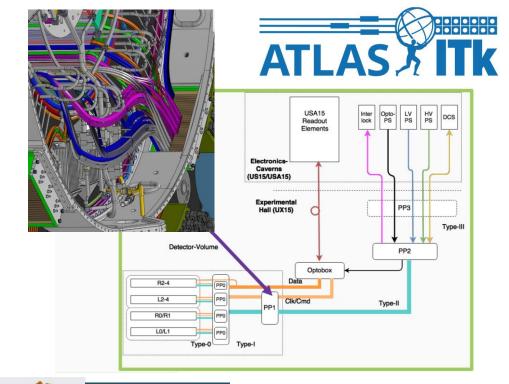
Short 2-layer flat barrel + long section of rings (3 types) Cooling feed/exhaust and cables <u>run along the quarter shell</u>

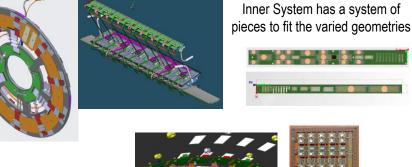


## Electrical Services (power, data, monitoring)

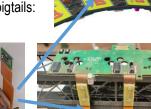
- Local supports hold "PPOs" with connections to modules
- "Type-I" cables carry services into / out of the detector
  - Twisted pairs for HV and monitoring/interlocks
  - Co-ax for LV
  - Data is on twin-ax cables inside the detector with electrical-to-optical conversion outside at "opto-boxes"
    - Accessible, lower radiation
- Successive steps of patch panels, thicker cables
  - ... up to services caverns

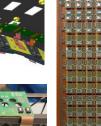






Outer Barrel PP0s and pigtails: Inclined and flat





#### 4 Dec 2023

### **Data Transmission**

Twinax cables for high-speed data transmission from local supports to opto-boxes r

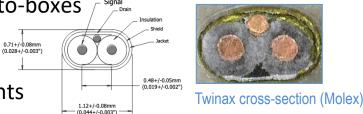
- Two vendors with slightly different characteristics
- Very thin (~1.1 x 0.7 mm<sup>2</sup>): extremely limited space
  and material considerations are balanced with impedance requirements
- Cables can be ribbonized for easier handling
  - Detector end termination
    - Via Samtec FireFly<sup>™</sup> for outer system
    - Direct soldering to PPO for inner system (not shown)
  - Opto-box end termination: bespoke PCBs

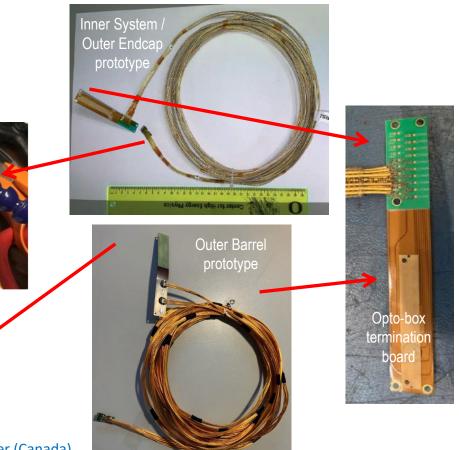
Qualified vendor for ribbonized & terminated cable: Tekdata (UK)

> Samtec <u>Fi</u>reFtv™



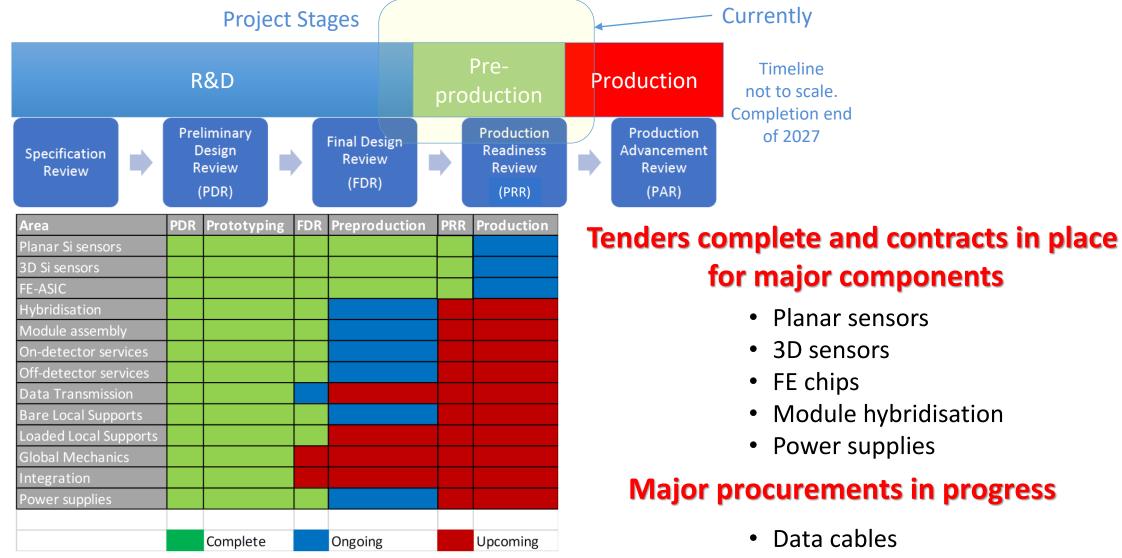






### **Current Status**





HSTD13 - Vancouver (Canada)

### Summary



- The LHC → HL-LHC upgrade requires a new tracker (ITk) for ATLAS, with tough requirements
- Features of the ITk pixel detector
  - 5-layer coverage to  $|\eta| < 4$
  - New FE chip (RD53) and sensor (3D, planar) developments
  - Serially-powered
  - CO<sub>2</sub> cooled
- Individual components have been verified in prototype runs during last two years and most have passed final design reviews
  - Sensors, FE-chips, Outer Barrel local supports in production
  - Module hybridization and assembly, most services in pre-production
  - Remaining activities planning final design reviews in next few months
- Completion scheduled for 2027