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A 10-Gb/s Serial Link Transmitter With 4-Tap FFE Function in 55-nm CMOS

The serial data rate has reached the 10 Gb/s level nowadays in the data acquisition system (DAQ) in high-energy physics experiments. Due to various wireline transmission scenarios in different detector front-end readout environments, the high-speed chip-to-chip or board-to-board serial data transmission is encountering severe and various signal quality degredations. A general-purpose, low-power, area-saving and high-speed transmitter (Tx) technique with tunable pre-emphasis function is crucial and in great demand. This paper presents the design and test results of a 10 Gb/s high-speed serial link transmitter (Tx) with the adjustable 4-tap feedforward (FFE) function fabricated in a 55 nm CMOS technology. The half-rate topology is adopted in this FFE transmitter design with full CMOS logic cells working at 5 Gbps data rate.

The proposed FFE transmitter consists of a demultiplexer (DMUX), two latch-chains, four high-speed MUXes and an output combiner. With this half-rate topology, the needed maximum clock rate is 5 GHz, and thus the full CMOS logic cells can be safely used in the whole design to save power consumption. Besides, a custom-designed high-speed TSPC latch is designed to gain better performance in 5 Gb/s data rate. A high-speed CML-based 2:1 MUX is proposed to achieve the highest data combination in the system. The clock distribution tree is also deliberately designed between each sub-module to ensure suffice timing margins for latches, DMUX and MUXes over different PVT combinations.

The proposed 10 Gb/s 4-tap FFE transmitter features an area of 120 μm x 290 μm, and the power consumption is around 50 mW including the CML output driver when working at the date rate of 10 Gbps. The chip has been designed and taped out in the end of 2022, and will be tested in September 2023. The test results will be presented and discussed in the meeting.

Submission declaration

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