

## Feasibility study of implementing CMOS sensor in 55nm process for tracking

High-Voltage CMOS (HVCMOS) sensors, featuring a deep n well separating the transistors and the depletion region, is intrinsically radiation hard and a good candidate for tracking systems in future high energy experiments, such as LHCb upgrade II or future electron-positron colliders. In hope of reducing the power density and incorporating more functionality in the same area, we are looking for foundries where HVCMOS sensors can be implemented in smaller feature size. In the talk we report the feasibility study using 55nm processes. Sensor diodes are designed with deep n well serving as electrode in a low-resistivity substrate, and the test results are reported. New design for MPW in 55nm high voltage process on a high-resistivity substrate will also be described.

### Submission declaration

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