

## A High-Counting-Rate Readout ASIC for CZT Detectors

Photon-counting detector computed tomography (PCD-CT) is a promising new technique for CT imaging. Compared to traditional energy-integrating detector CT (EID-CT), PCD-CT allows for more refined image reconstruction and lower radiation doses because it has higher energy resolution. CdZnTe hybrid pixel detectors are usually used for PCD-CT. To avoid the stacking of signals, the application-specific integrated circuit (ASIC) used in CdZnTe hybrid pixel detectors is needed to feature a high counting rate.

An ASIC named Topmetal-PCD for CdZnTe hybrid pixel detectors have been designed in TSMC 180 BCD process, and consists of a three-side buttable matrix of  $20 \times 100$  pixels with a pitch of  $150 \mu\text{m}$ . Each pixel is composed of an exposed top-most metal, a charge sensitive preamplifier (CSA), a peak detecting and holding circuit, two source followers (SFs), three comparators and three 12-bit counters. The CSA is used to amplify the signal. A two-stage SF is connected after the charge-sensitive preamplifier to reduce the load, improve shaping time, and increase driving capability. The signal of the SF is split into the peak detecting and holding circuit and comparators. The threshold of each comparator can be adjusted by off chip. The output of each comparator is detected and counted by 12-bit counter. The pixel array is read out through a rolling shutter technique with a maximum frame rate of up to 10kfps. The analog front-end has a gain of  $\sim 11 \text{ mV/ke}^-$  and the chip can deal with a maximum flux of  $\sim 200 \text{ MHz mm}^{-2}\text{s}^{-1}$ , while single pixel power consumption is as low as  $80 \mu\text{W}$ . In addition, the ASIC has also an analog readout channel that can directly transmit the signal waveform off chip. The ASIC can be used the flip-chip bonding technique to directly connect to the detector for charge collection.

### Submission declaration

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