Contribution ID: **81**   Type: **Poster**

A 4.4-Gbps Serializer ASIC in 180 nm for NICA-MPD Detecter

The inner tracker of the Multi-Purpose Detector (MPD) at Nuclotron-based Ion Collider fAcility (NICA) is responsible for detecting charmed particles with average decay lengths (λ) of several hundred micrometers. Monolithic active pixel sensors are adopted in the inner tracker. A high speed serializer presented in this paper is used to convert the parallel data from the front-end of the pixel sensor chip into serial data and transmit off chip.

The serializer consists of a multiphase clock generator, ten Low-Voltage Differential Signaling (LVDS) data receivers (RXs) , two multi-phase structure 5:1 multiplexers, a tree-structure 2:1 multiplexer, a high-speed clock receiver, a clock divider by 5, a duty cycle correction (DCC) circuit , a Current Mode Logic (CML) driver, and a PRBS self-test source. The 5:1 multiplexer adopts the multiphase structure to reduce the power consumption. To ensure the synchronization between the external data inputs and the internal clock, ten D flip-flops (DFFs) are used to latch the external input data. A multiphase clock generator is designed to provide high phase accuracy clocks for the 5:1 multiplexers. In 2:1 multiplexers, the tree structure is adopted to reduce the power consumption. Additionally, the DCC circuit is employed in the clock paths of the 2:1 multiplexers to ensure the correct duty cycle.

A test chip of the serializer has been manufactured and the chip has been fully tested. During the test, 10-channel parallel data with a data rate of 425Mbps is injected into the chip. The test results show that the output data rate is 4.25Gbps. The measured power consumption is 31 mA with 1.8 V power supply including the RX and CML driver. The measured total jitter is 49.37ps at a bit error rate BER of $< 1 \times 10{-}12$, and the output amplitude is differential peak to peak of 600mV.

Submission declaration

Original and unplublished

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Track Classification: ASICs