Development of high-time-resolution ASICs in CMOS 28-nm technology, dedicated to precision 4D-tracking

Adriano Lai
INFN Cagliari

HSTD13 Symposium, Dec 5th 2023

On behalf of

IGNITE$_{\mu d}$
INFN Ground-up iNITiative for µElectronics developments
INFN Istituto Nazionale di Fisica Nucleare

Talk outline

1. Scope of this talk: High-intensity 4D-tracking (some specs)
2. Previous achievements (and limits) in HI-4D-tracking (*TimeSPOT*, 2018-2022)
3. Strategy for further steps (modularity, vertical integration)
4. First (and preliminary) results from **IGNITE** (started 2023)

4D-tracking: in what sense?

- The term 4D-tracking can be and is used in a broad sense, to indicate tracking with time-sensitive pixels or pads
- In this talk we refer to 4D-tracking when this technique is necessary at the level of the **inner tracking detector** and in each pixel (no timing layers)
- Such kind of 4D-tracking start to be necessary in some setups of the **next generation of collider experiments**: in particular, LHCb-U2, HIKE (NA62 Upgrade), CMS Endcap (less stringently) and other possible envisaged detectors. The trend is foreseen to be kept and enforced in future circular colliders (if ever any)

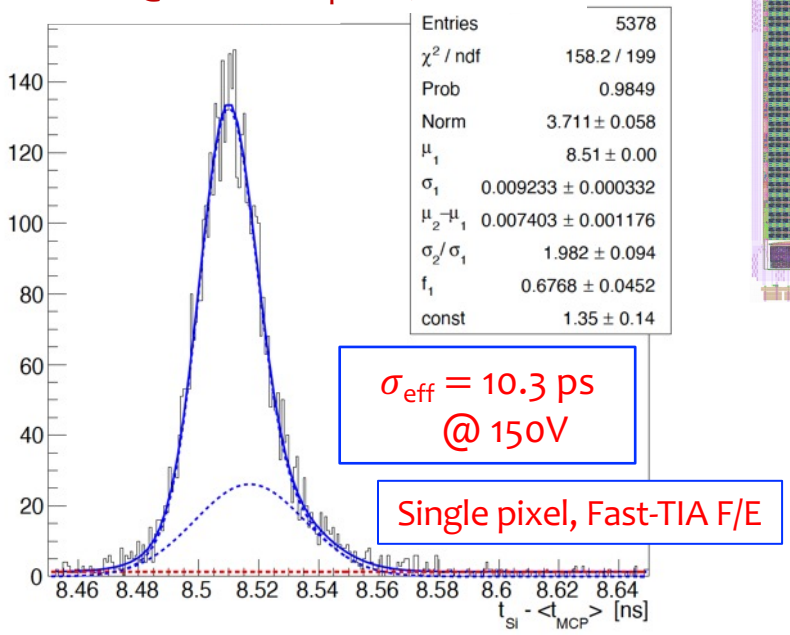
- In this case, it is important to identify a set of key specific requirements, to be met **all at the same time**:
  1. Pixel pitch: ~ 50 µm with 99% fill factor
  2. Time resolution: < 50 ps rms per hit on the full chain, even after irradiation
  3. Radiation resistance: fluence > 10^{16} 1 MeV n_{eq}/cm^2 (limited by electronics, CMOS 28-nm)
  4. Sustainable rate per pixel: order (10^2) kHz (low multiplicity of pixels per single TDC)
  5. High output data bandwidth: order (10^2) Gbps per 1 cm^2 ASIC
  6. High performance at limited power budget: 20–30 µW per channel

… We can call it High-Intensity 4D-Tracking

Results on Sensors and Electronics for (HI)4D-tracking

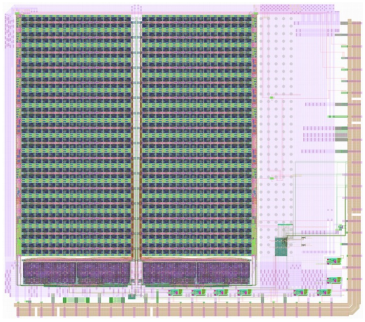
2018 – 2022

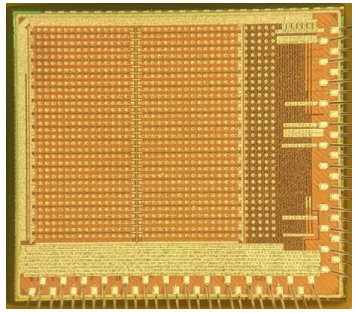
Irradiated @ 2.5 10^{16} n_{eq}/cm^2 , $\alpha_{tilt} = 0°$

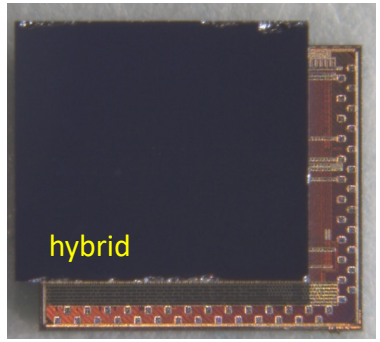


σ_{eff} = 10.3 ps @ 150V

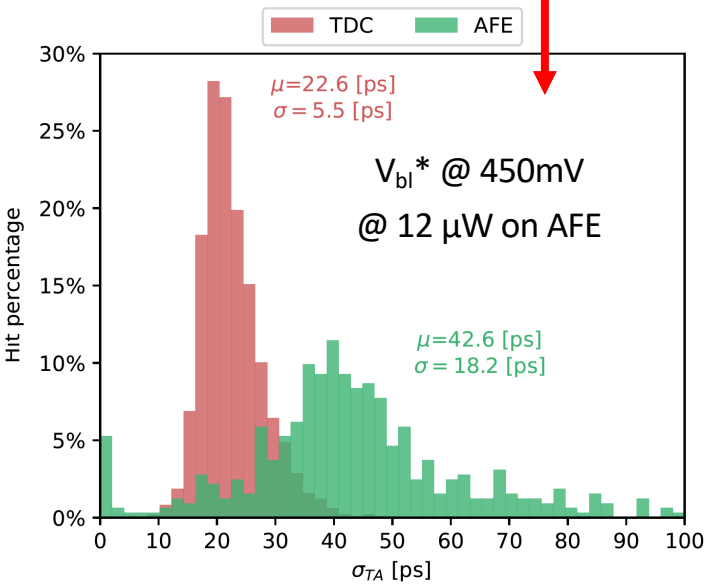
Single pixel, Fast-TIA F/E



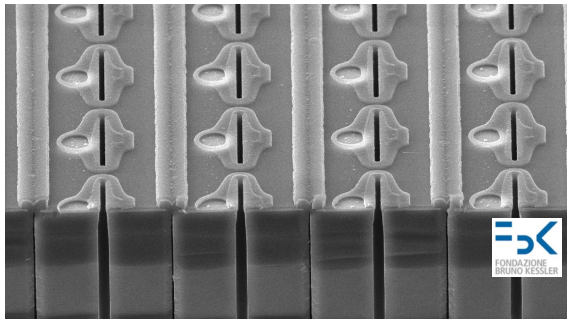




CMOS 28–nm Timespot1 ASIC – 32x32 pixel matrix, 55 µm pitch



Distribution of the TA standard deviation across 1024 channels and 7 clock phases. Each point is computed from **100** repeated measurements.



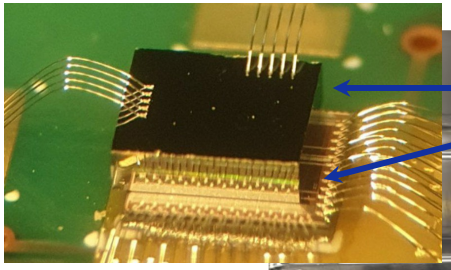
3D-trench Silicon sensors

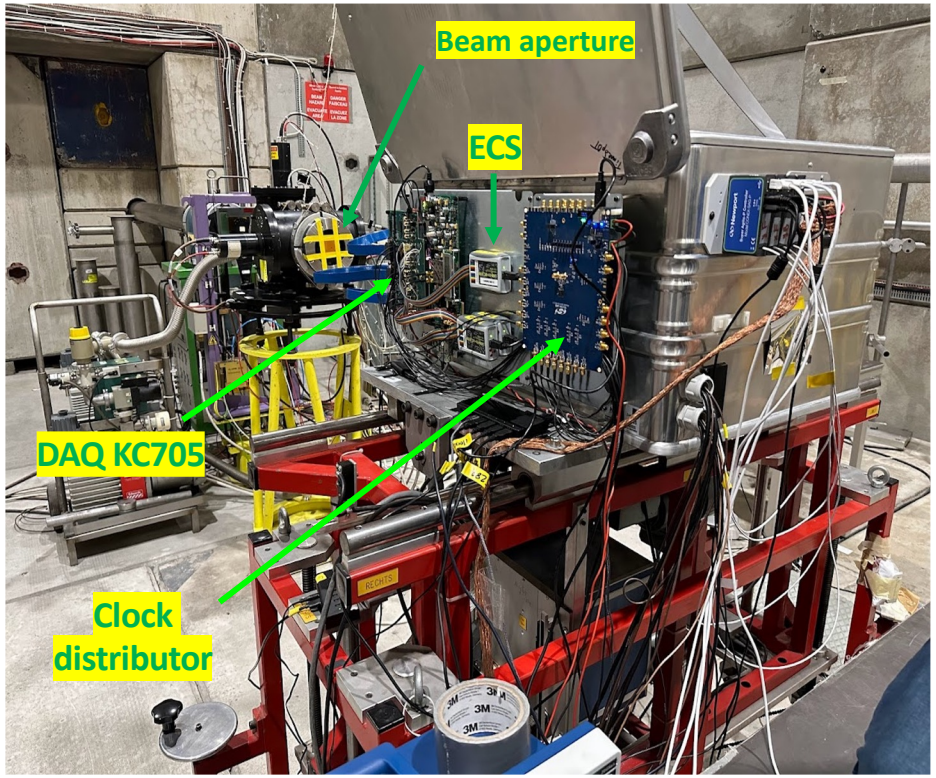
Tests @ 10^{17} n_{eq}/cm^2 are ongoing just these days

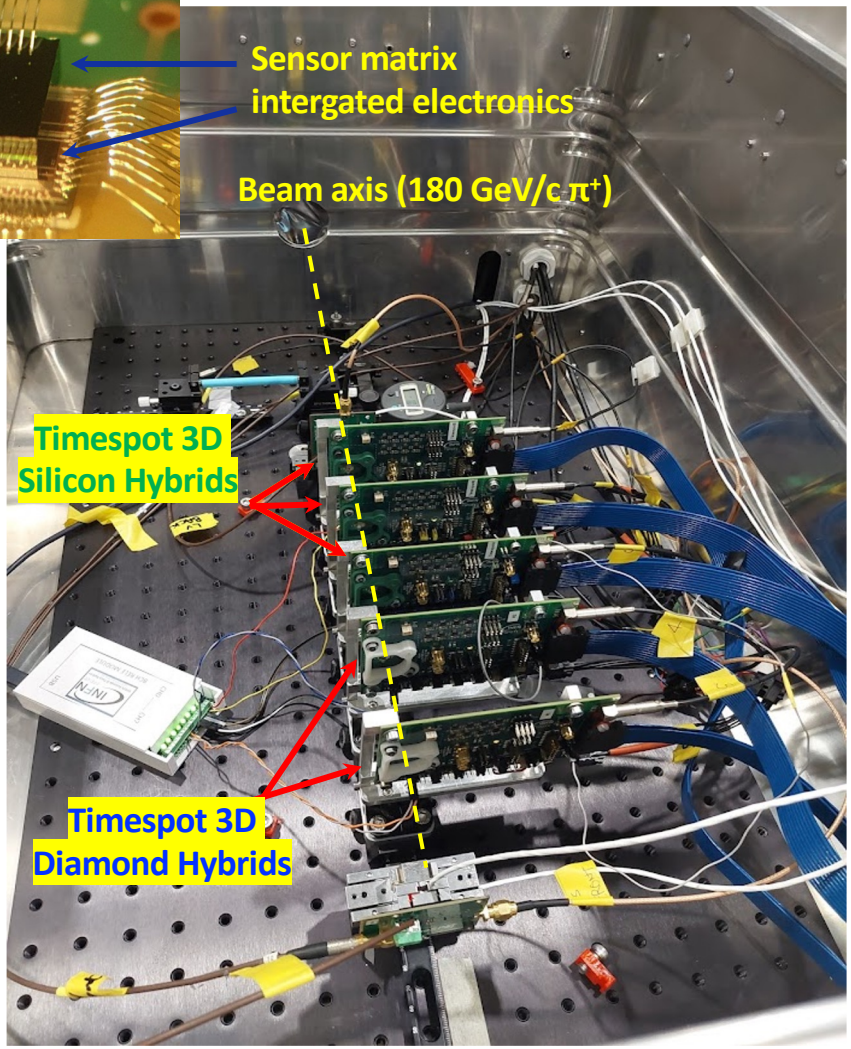
TEST beam @SPS, May 2023

A mini-tracker demonstrator (5 stations)

More questions than answers, but extremely instructive experience







M. Addison et al., ***A Prototype 4D Tracker Demonstrator For Future Vertex Detectors***, paper in preparation.

Pixel electronics at high rates and high resolution:

A major technical challenge!

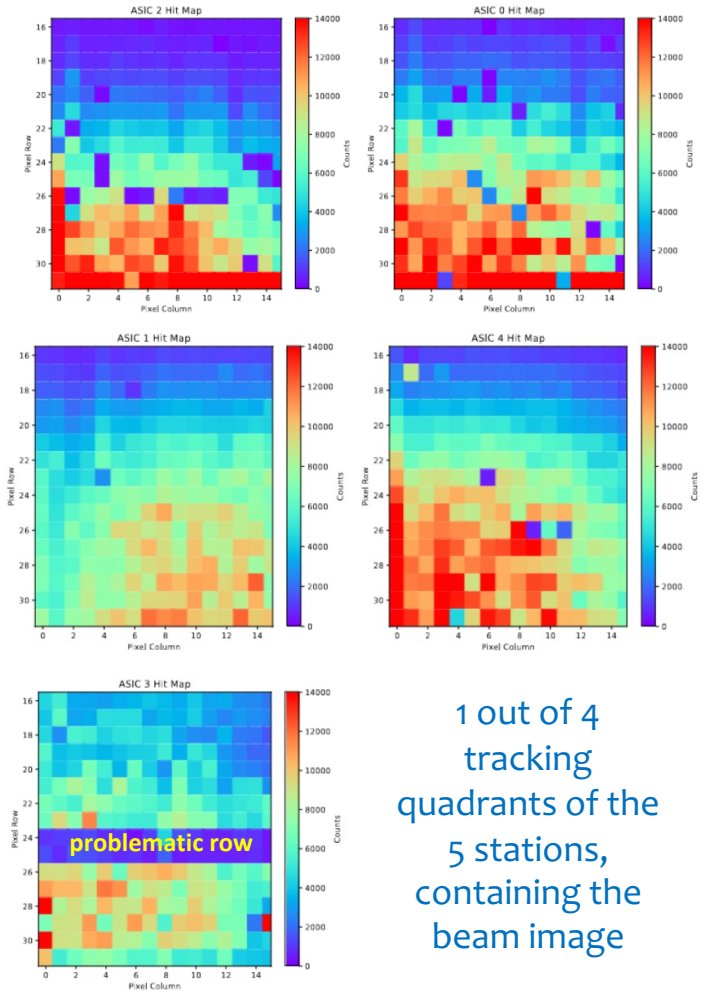
Issues with our Timespot1 ASIC (small 32x32 device!) and 5 tracking stations:

Power distribution is critical (high voltage drop across the matrix, rate dependent)
Clock distribution is critical
→ **Both have impact on pixel time resolution at first order !**

Relevant lack of uniformity in performance across the matrix
→ **Difficult to have high and uniform performance at system level!**

During the design phase, the full matrix simulation was heavy, difficult and time consuming
→ **Critical system verification during the design phase**

How to face the design and implementation of a large tracking matrix (about and more than 2 cm², 16 times larger) ?
Furthermore: how to have it ready in the next 3-4 years ?



1 out of 4 tracking quadrants of the 5 stations, containing the beam image

M. Addison et al., ***A Prototype 4D Tracker Demonstrator For Future Vertex Detectors***, paper in preparation.

Modular (fractal) design

Arrive to the result by single, simpler, consistent steps

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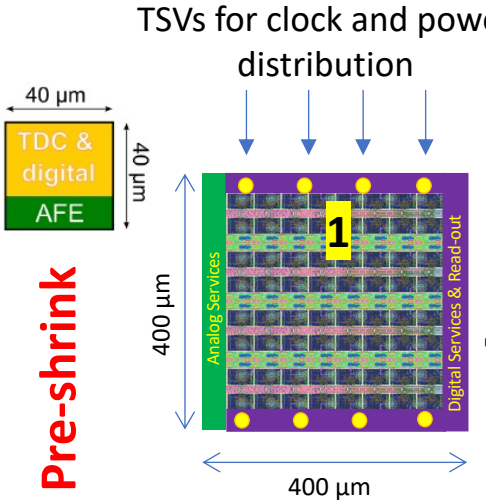
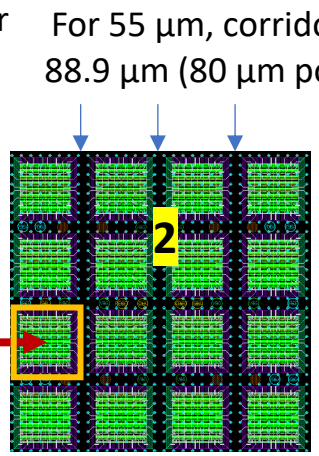
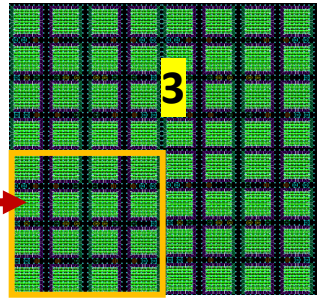


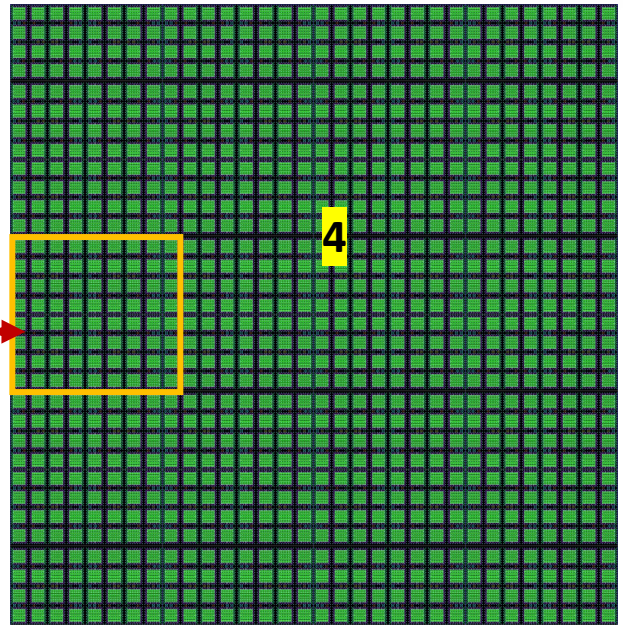
Elementary Square
8x8 pixels,
(400 x 400 μm²).
Each pixel integrates an Analog Front-End and a TDC



4x4 Squares form a **32x32 Matrix** (Timespot1 ASIC size, 55 μm pixel pitch and 1.76 x 1.76 mm² area).
Corridors are partially "elastic" to allow different pitches



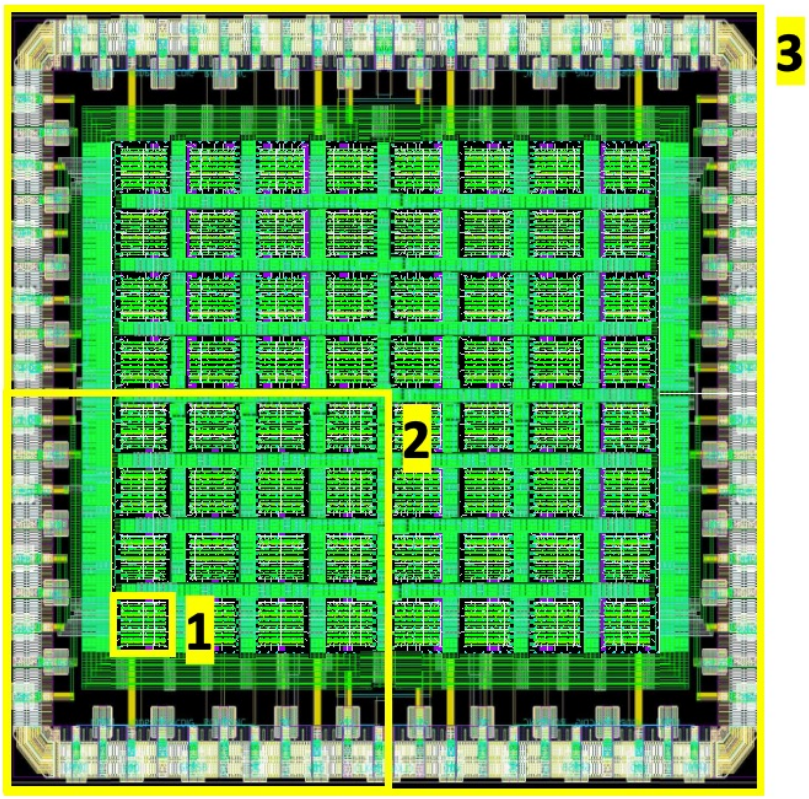
4x4 matrices form a **super-Matrix (64x64 pixels** ≈ 3.5 x 3.5 mm² for 55μm pitch).
Next ASIC.
Now under design



Full size ASIC. Different aspect ratios are possible by implementing different arrangements of the sub-structures (here a 256x256 pixels, 1.4x1.4 cm² ≈ 2 cm²).
Global routing distribution remains structurally local by exploiting vertical connectivity.

Modular (fractal) design

Step 1, 2, and 3



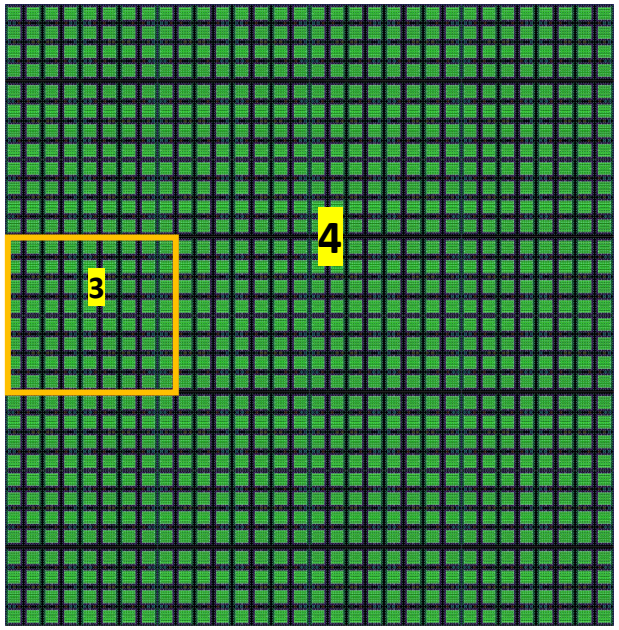
4x4 matrices form a **super-Matrix (64x64 pixels** ≈ 3.5 x 3.5 mm^2). This can reasonably be the size of a **prototype MPW**, to be tested also under particle beam after hybridization

- The large structure is based on the elementary Square (8x8), the Step-1
- Step-1 is a self-contained structure, exception made for the final stage of readout
- Step-3 is relatively easy by double-mirroring the Step-2 (32x32) structure
- Verification in Step-3 should imply only marginal additional efforts w.r.t. Step-2

- The Step 3 ASIC is conceived also for use in test beams to test prototypes of timing sensors having pitch of 55 µm or its multiples.
- **Target time resolution: < 30 ps after full chain**
- Submission Q3 2024

Modular (fractal) design

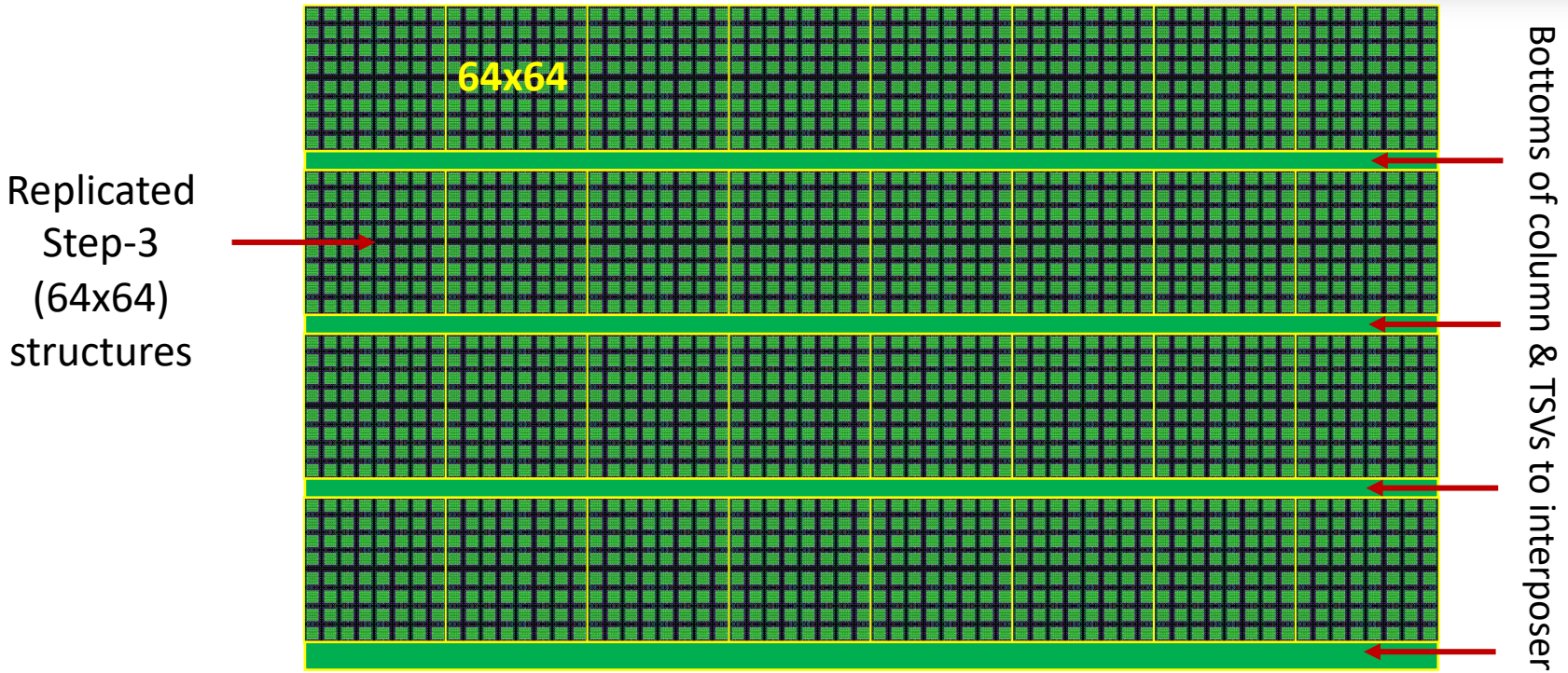
Step 4 (final)



Full size ASIC (some cm²)
Global routing distribution remains structurally local by exploiting vertical connectivity.

- Such assembly is conceivable only by abutment. The corridors, if any, are empty. Large use of TSVs is mandatory
- It requires a 3D-connected **companion digital ASIC**, which takes the place of the bottom-of-column services and is used to:
  1. Distribute global lines in optimal way (autoroutes not mountain trails)
  2. Integrate services (output buffers, power management circuits, HF serializers and drivers, possible additional fuctionalities for data reduction (e.g. clustering)
- In the absence of massive use of 3D interconnections, a more traditional architecture with periphery/end-of-column can still be used here. It is however evident the disadvantage in terms of:
  a. Routing congestion
  b. Locality breaking and severe hardening of verification operation
  c. Limitation in adding possible functionalities and programmability
  d. Integration of output stages (Serializers, Drivers)

A back-up solution…

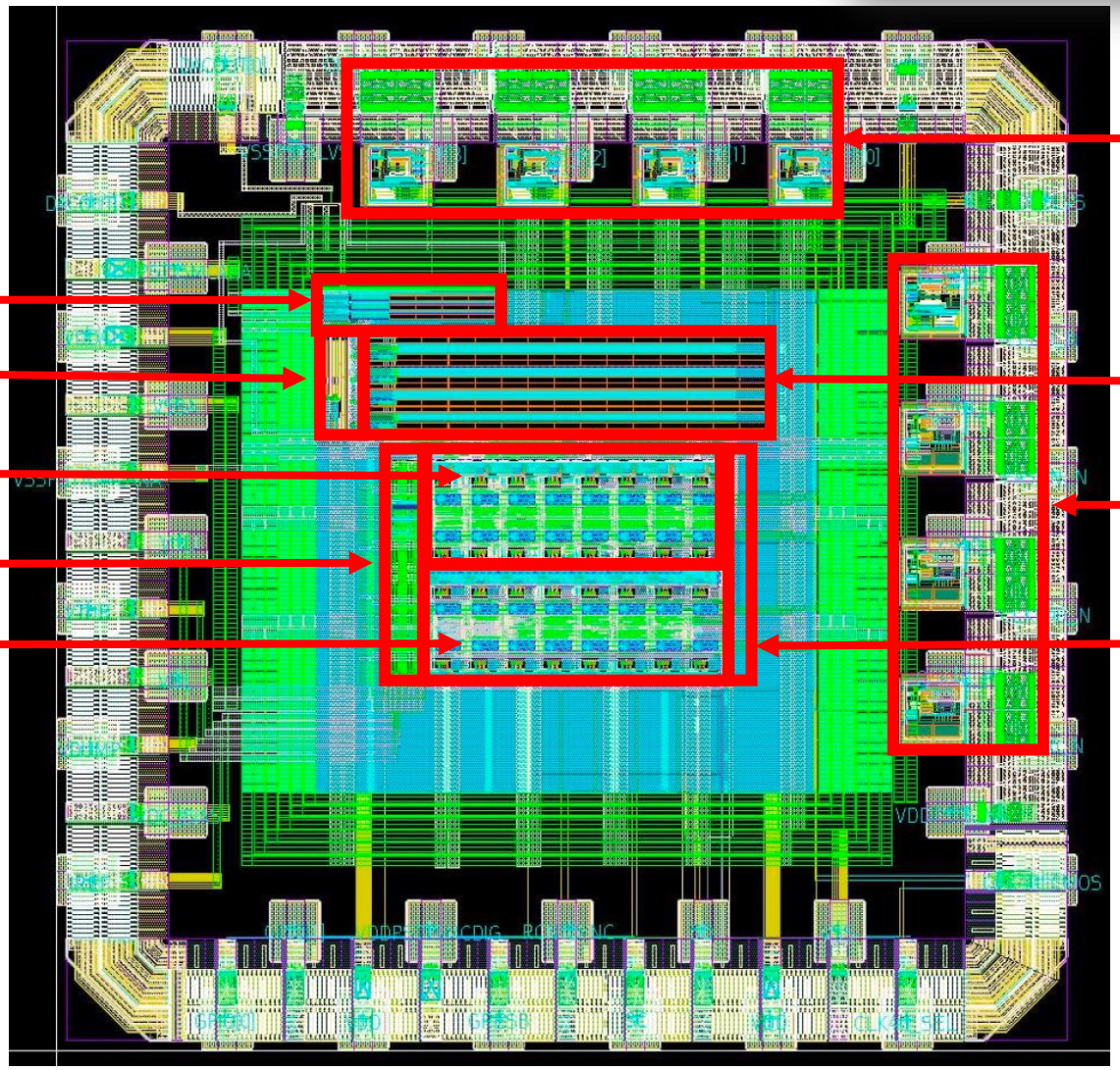


Example: 512x256 pixels ≈ 2.8 x 1.4 cm² (active area).

The BoC areas are gained by implementing a pixel pitch on the electronics side which is smaller than that on the sensor side. A RDL (re-distribution layer) on top metals re-aligns the two pitches. **TSVs are here necessar as well, but in a much less aggressive approach**

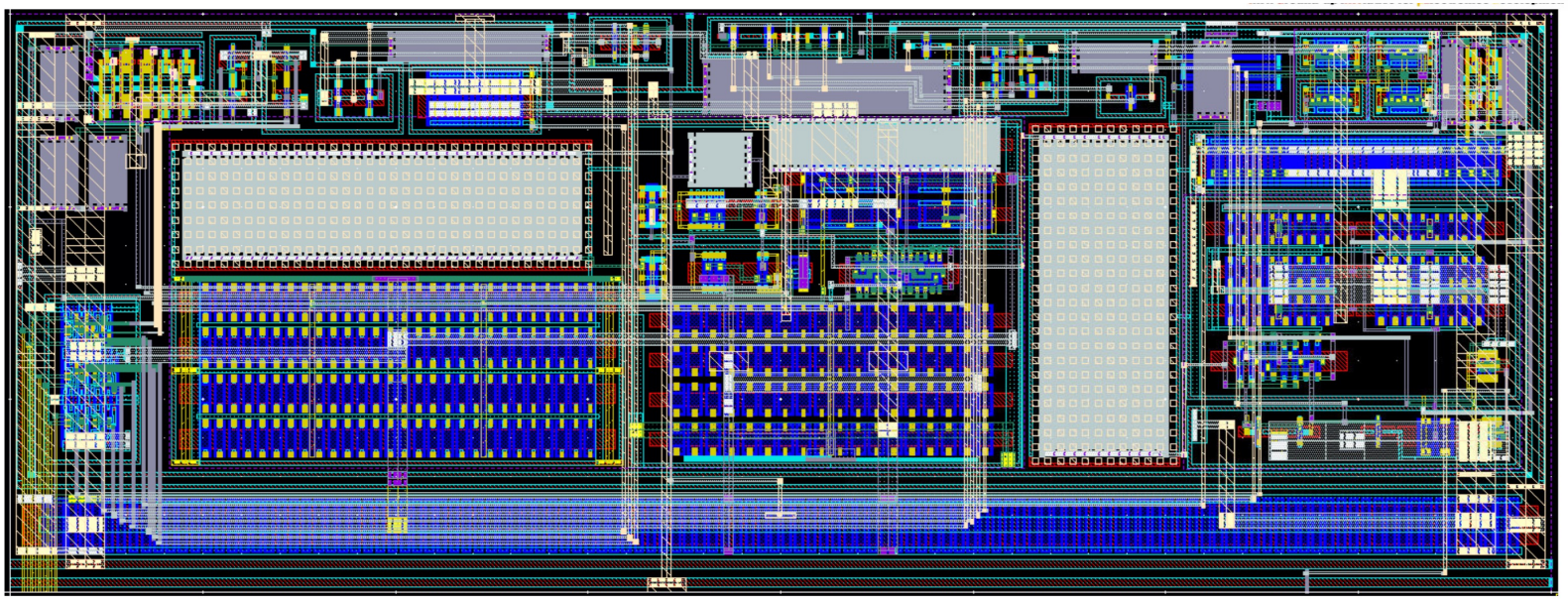
Modular (fractal) design: *Step-0*

Ignite-0 ASIC
Submitted August '23
Dies received 1 week ago
Test in preparation



32 channels per ASIC
8 different AFE flavors

Ignite-0: Analog Front End (AFE) Layout



- **Area: 36µm×13.5µm** (in figure: Offset Compensated version)
- Bias and power transmission: top metals (M7→M9), horizontally, decoupled and filtered.
- Digital IO: bottom side in M3,M5, with digital buffers in analog domain.
- Sensor connection: AP, middle-bottom side.
- Encapsulated inside a 3-Nwell for substrate-noise insulation.
- **Nominal power consumption: 10.8 µW per channel** – adjustable

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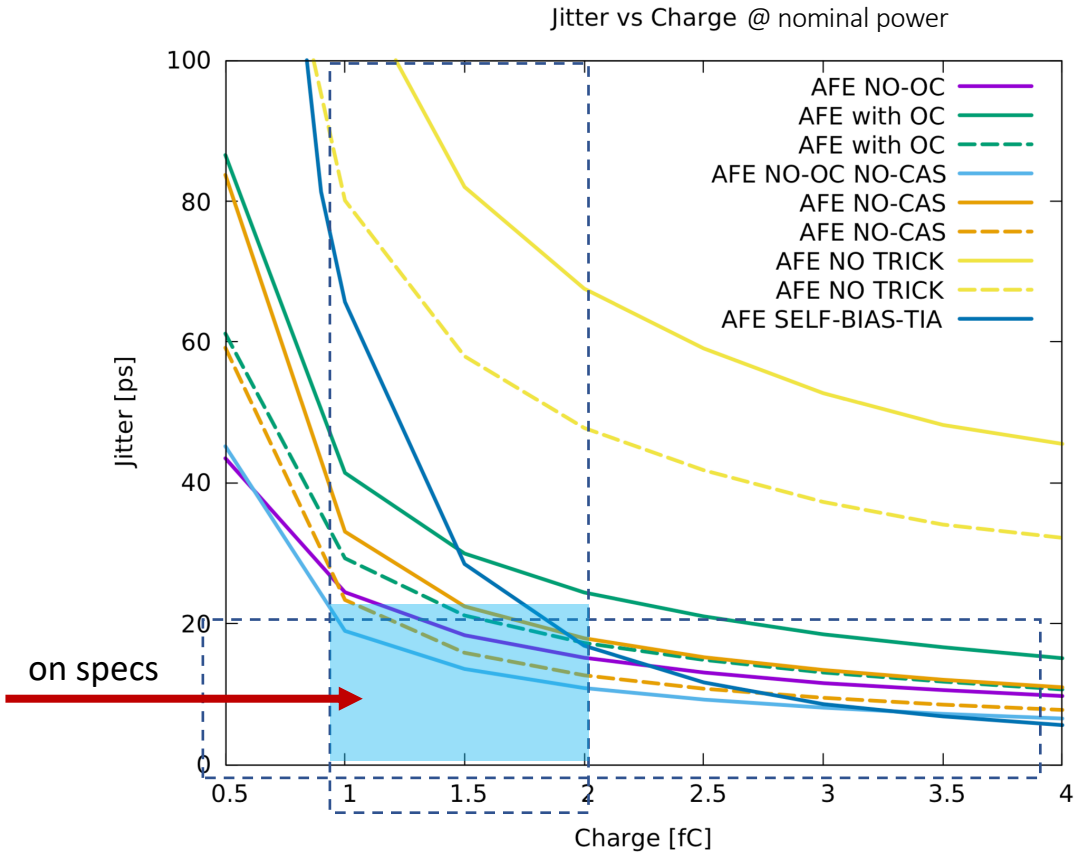
AFE performance (1)

Post-layout simulations

- **Power = 10.8 µW, C_{in} = 100 fF**
- MIP MPV 2 fC, but value considered is 1 fC. Indeed:
  - → charge sharing can decrease the effective MPV
  - → also, it can vary with sensor geometry.
- The OC has a cost on power and resolution.
- The CAS (cascoded) core is sensitive to output loading.
- SELF-BIAS TIA: poor performance at low-charge*, due to uneven threshold crossing.



*(no discriminator was integrated for the self-bias in this version).

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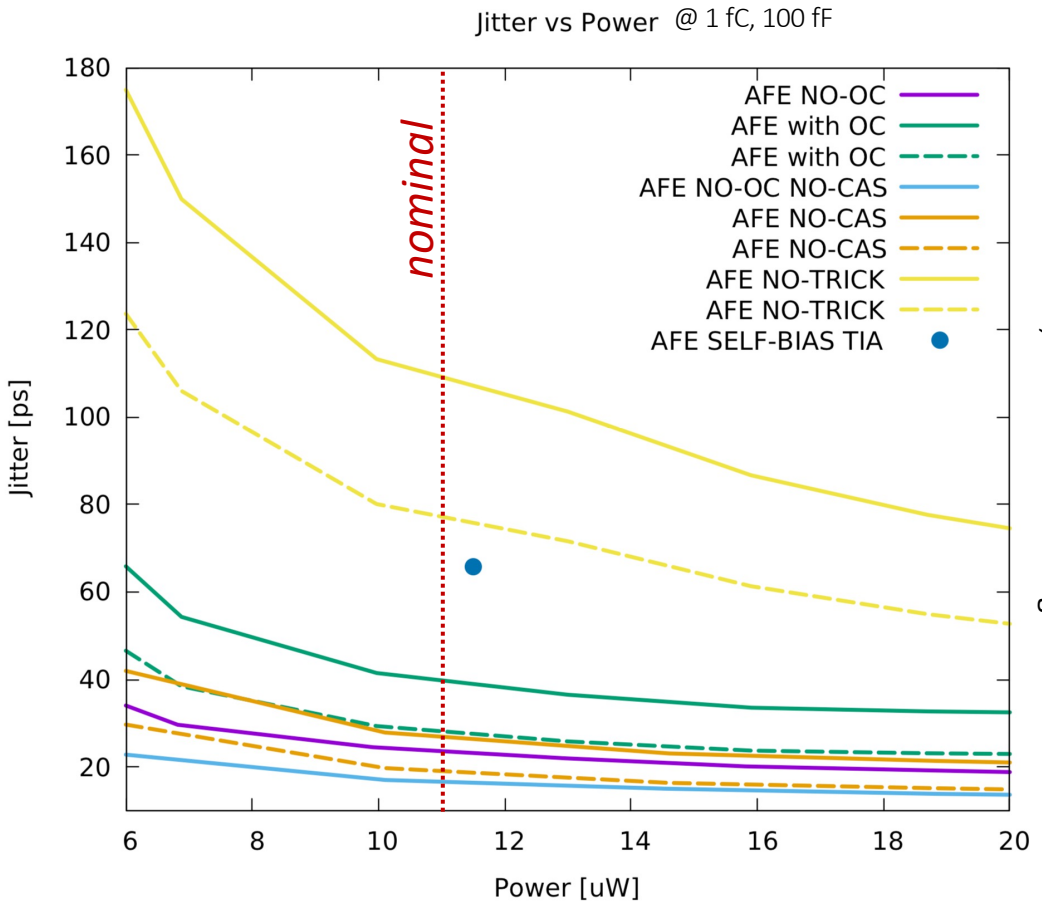
AFE performance (2)

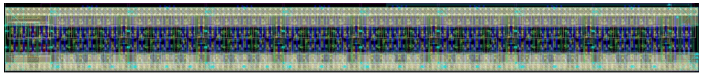
Post-layout simulations

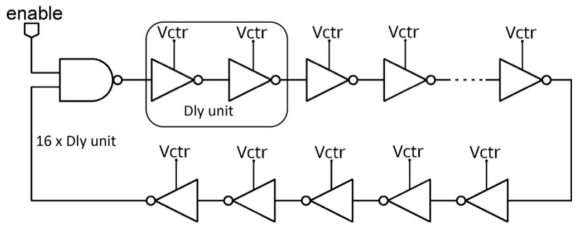
- **Q_{in} = 1 fC, C_{in} = 100 fF.**
- SELF-BIAS TIA has fixed power (≈ 11 µW). The modest performance is due to the lack of a discriminator in this specific solution
- Pre-Amp and Discriminator power are varied to maintain performance.
- Nominal performance close to saturation → can still be tuned-up.
- Some CSA options exhibits good performance at sub-nominal power.
- Power increase above nominal value does not help much in this specific (optimized) design

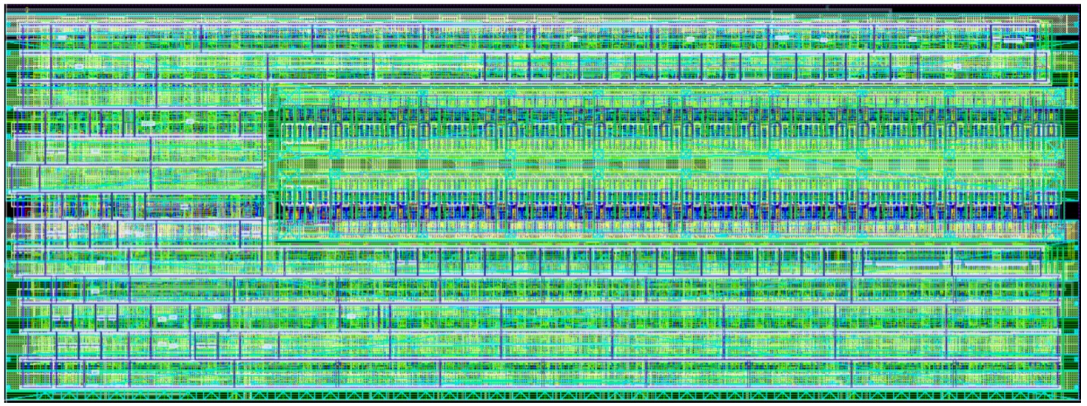


DCO & TDC: Layout and Performance

Vernier architecture







DCO

- **Size**: **19.78 x 1.94 µm²**.
- **Number of Steps**: 16 Delay Units
  - Single delay cell with starved architecture
  - Power on/off configuration
  - fine tuning – coarse tuning
  - Decoupling capacitors
- **Step controls**: Fine ≈ 3ps & Coarse ≈ 50ps
- **Period Range**: ~ 900ps – 780ps (Typical)
- **Power Cons.**: ~ 45 µA – 55 µA (Typical)
- **Jitter**: ~ 750 fs – 600 fs (Typical)

TDC

- **Size: 27 x 9.9 µm²**
- **Resolution** from post-layout simulation: ~ 12 ps (rms)
- Full custom design
- Particular care for **power distribution** as well as 40 MHz master clock distribution → important improvement in power w.r.t. the TimeSPOT version (> factor 10 !)

Power vs Event rate

TDC status	Current
OFF	0.5 µA
IDLE	1.3 µA
Calib. DCO {Istant. @1.12 GHz}	98 µA
RUN (4.5 MHz)	28.3 µA
RUN (1.0 MHz)	7.5 µA
RUN (500 kHz)	3.9 µA
RUN (333 kHz)	3.0 µA
RUN (200 kHz)	2.3 µA

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Conclusions

and next steps in preparation

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- Pixel size is 40x40 µm² (pre-shrink, 36x36 µm² on silicon). **Compatible with sensor pitch from ≈ 40 µm to ≈ 100 µm**

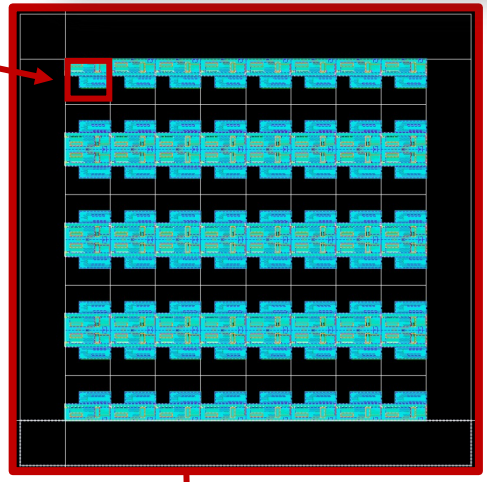
- Preparation **of Step-1 (elementary Square) has started** , by assembly of the elementary rows of Step-0 (after de-bugging). To be added:
  1. **Optimization of configuration registers**
  2. **Triple voting strategy**
  3. **Definition of services for the Analog (biasing and config) and Digital part (Read-Out Manager)**
  4. **Definition and set-up number and position of TSV connections in the Square periphery (temporarily without implementing them)**

- The **64x64 pixel matrix (2D) is planned for the 2nd half of 2024** as composition of 8x8 elementary Squares (total area ≈ 4x4 mm²)

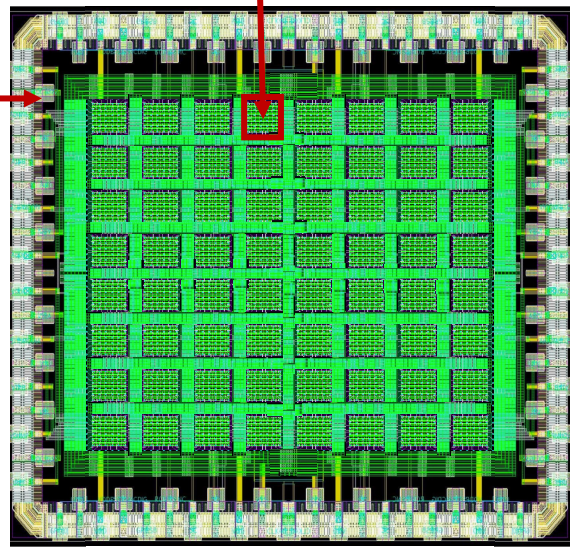
- This ASIC should be usable as readout matrix for 4D-high-resolution sensors at test beams

- We aim at a **full size ASIC (≈ 2 cm²) for 2026-27,** by exploiting 3D vertical interconnections

- **Will the «fractal» strategy of IGNITE solve the challenge for HI-4D-Tracking? We hope so!**



First draft of the Elementary Square



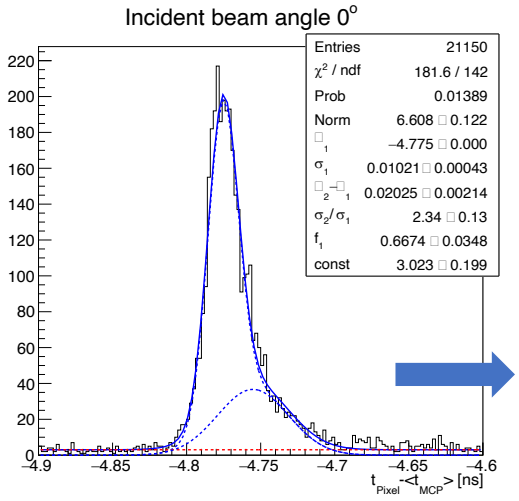
First draft of the 64x64 matrix (16 mm²)

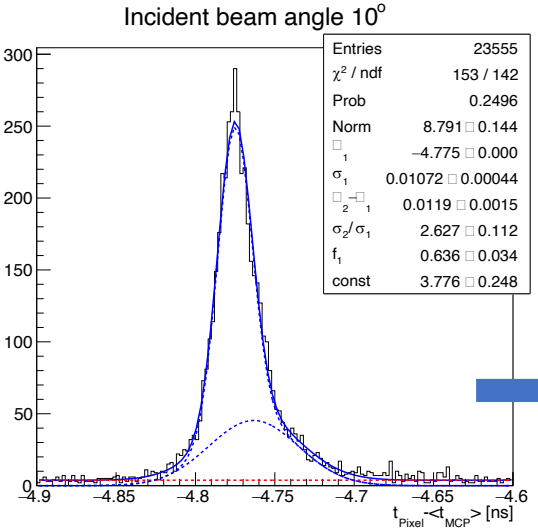
Insights/Spares

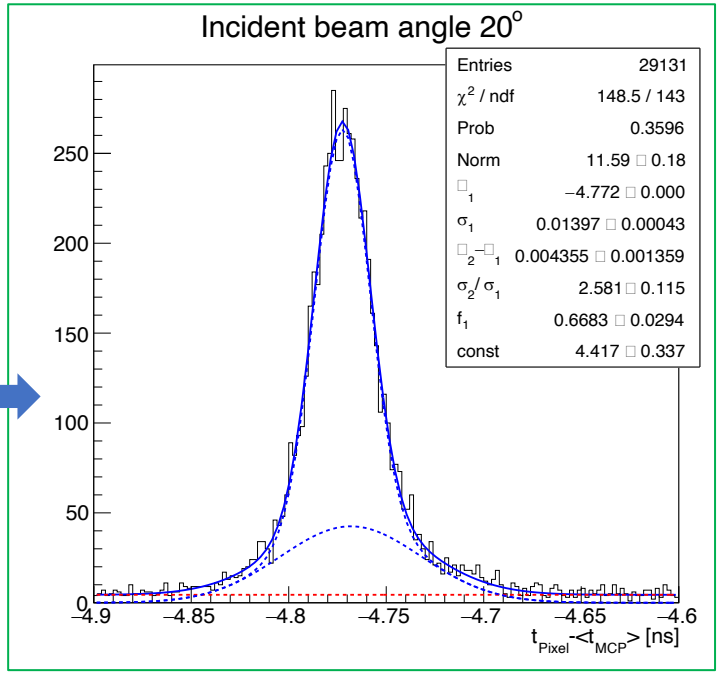
Effect of tilting on distribution shapes

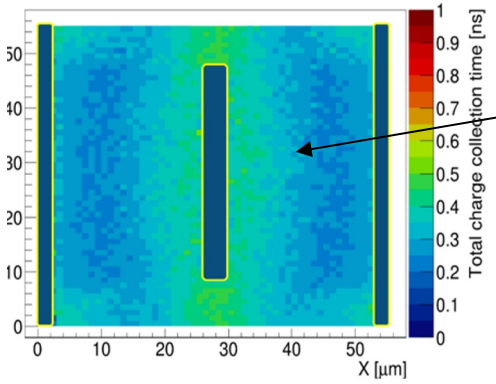
Spline method, SPS/H8 (Nov'21)

Single Pixel @ 50V









Simulated CCT map of a single 3D-trench sensor pixel scan (α_{tilt} = 0°)

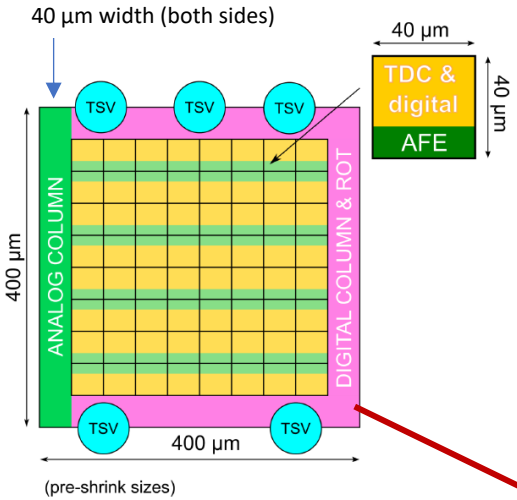
Tilting has the effect of «mixing up» the fast and less-fast regions of the pixels, thus uniforming the timing response

As a result, the shapes are more Gaussian at increasing α_{tilt}

Notice that, due to detection efficiency, α_{tilt} = 20° is the normal working condition of a 3D in a detecting system

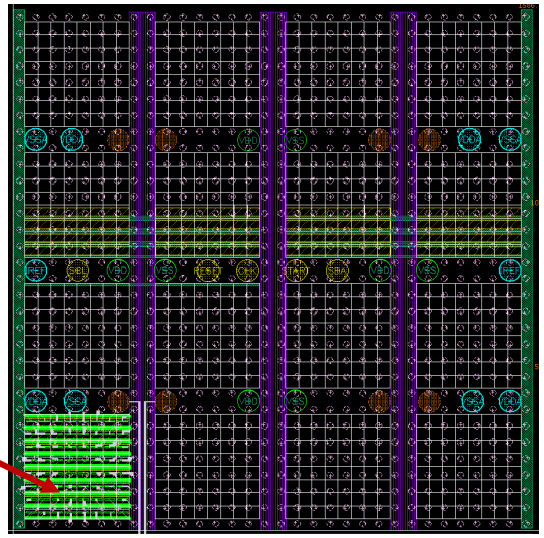
IGNITE Fractal IC(s): tiles, 45 µm pitch and 55 µm pitch

NB: Pixel sizes with higher modularity (e.g. 110 µm) can be obtained by channel masking



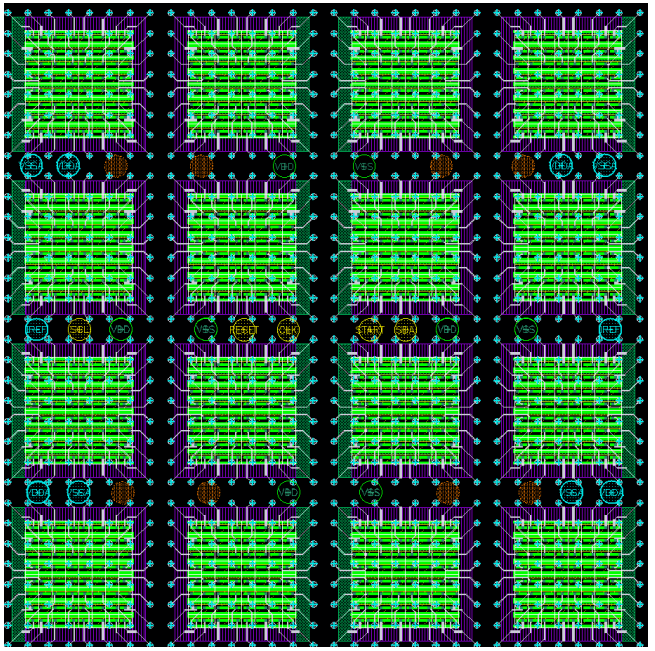
Elementary Square
8x8 40 µm (36µm) pixels

- Digital and Analog columns are abutted
- PLLs for Local clock distribution are placed in the digital spaces between tiles. They serve a group of 8x8 tiles
- Digital spaces are also used to route output data towards periphery



45 µm pitch sensor

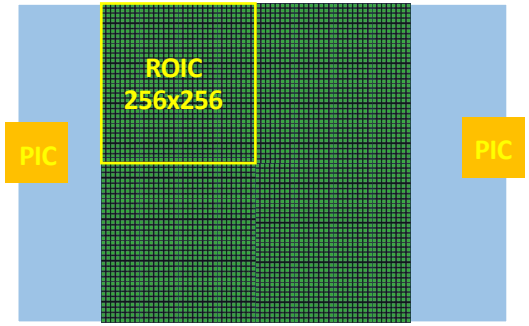
- The 8x8 tiles fill the whole the chip Area. 40µ x 2 columns are left on the 2 sides for service circuits and TSVs
- 1024 channels area: ~ 2,5 mm^2.
- 4k channels area: ~ 9 mm^2 + periphery



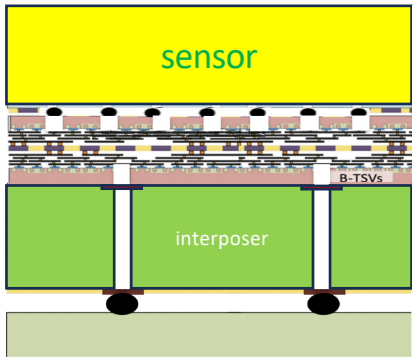
55 µm pitch sensor

- The 8x8 tiles don't fill the whole chip area
- Some "blockage" are needed to "stretch" the area.
- 1024 channels area: ~ 3.7 mm^2.
- 4k channels area: ~ 16 mm^2 + periphery

Final step(s) in development



A 4x4 cm^2 2.5D-3D integrated module



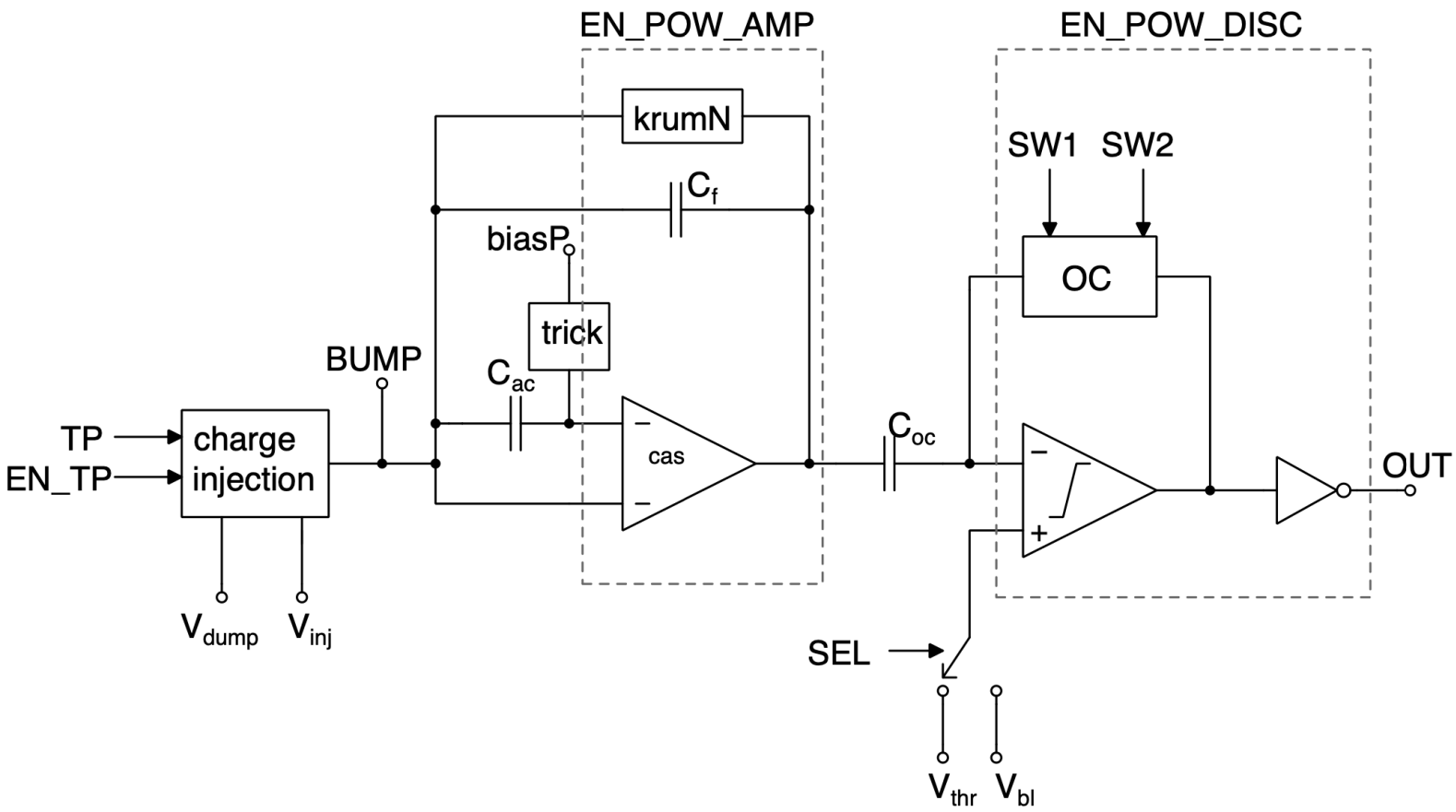
ROIC
(A+D)

Such module can be conceived as:

- A demonstrator for 4D-Tracking (LHCb, HIKE, CMS-Endcap + others)
- A perfect demonstrator following Falaphel developments
- A device for extensive characterization of timing sensors under development
- A module for a timing tracker

- In case of no need for timing, the analog layer can be different, but the companion digital layer could be made the same, by adding programmable/configurable facilities.

- Otherwise, the same 3D-integrated approach can be exploited even in a different ROIC, with great simplification in design and verification procedures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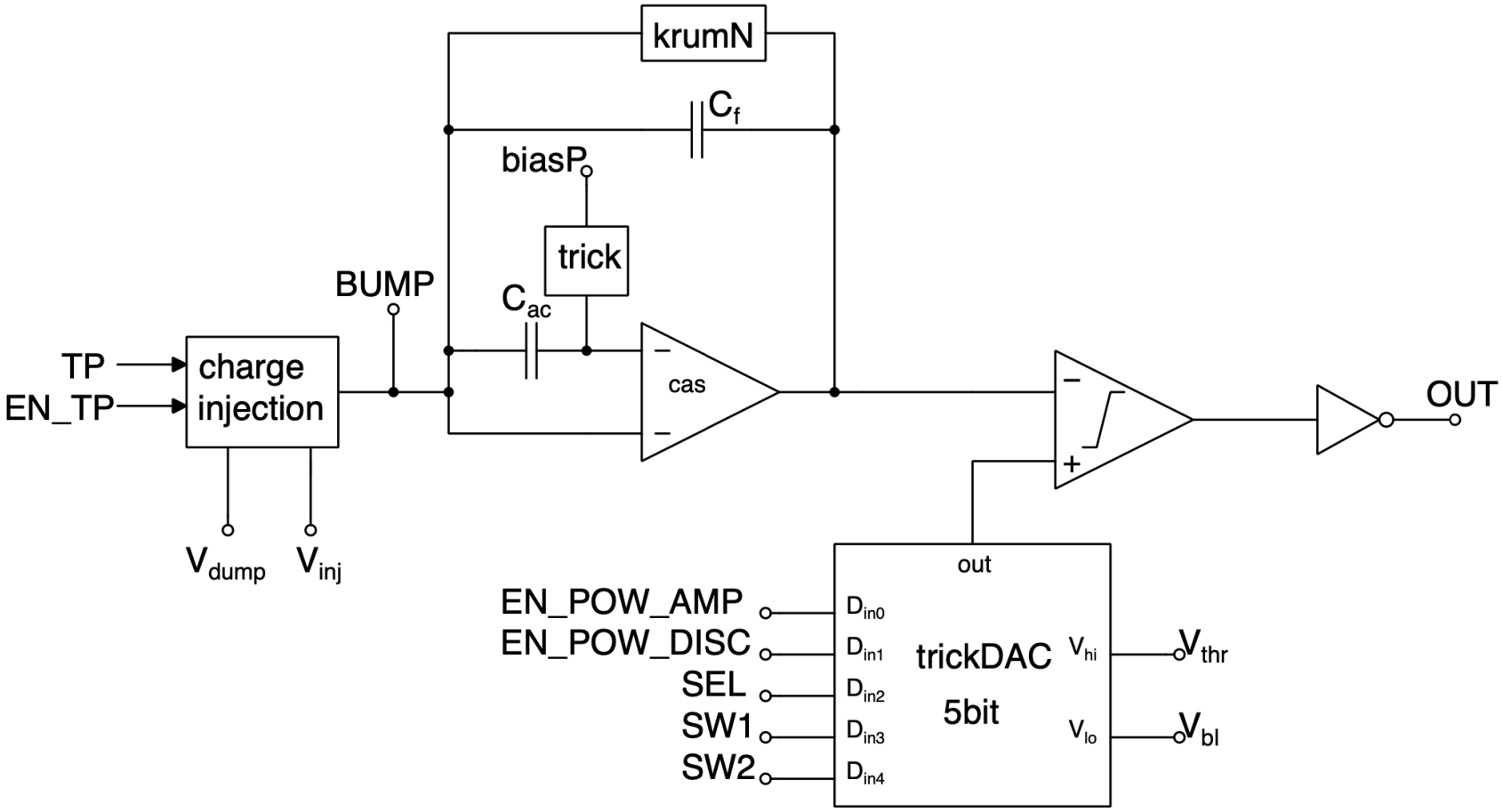
EN_POW_DISC
krumN
C_f
biasP
trick
C_{ac}
BUMP
TP
EN_TP
charge injection
cas
C_{oc}
SW1
SW2
OC
OUT
SEL
V_{dump}
V_{inj}
V_{thr}
V_{bl}


krumN
C_f
biasP
trick
BUMP
C_{ac}
TP
EN_TP
charge
injection
cas
OUT
V_{dump}
V_{inj}
out
EN_POW_AMP
EN_POW_DISC
SEL
SW1
SW2
D_{in0}
D_{in1}
D_{in2}
D_{in3}
D_{in4}
trickDAC
5bit
V_{hi}
V_{lo}
V_{thr}
V_{bl}