13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13), Vancouver, Canada

Contribution ID: **102** Type: **Poster**

# Design of a Pixel Detector Readout Scheme with Controllable Delay Chain for Enhanced Positioning Accuracy

Pixel detectors play a crucial role in various fields such as optical imaging and particle physics experiments. However, traditional pixel detectors face limitations in their electronic readout systems, including resolution and response speed. To address these challenges, we propose a novel readout scheme incorporating a controllable delay chain within each individual pixel. This scheme allows for simultaneous transmission of the pulse generated by particle impact to both the top and bottom of the pixel array, by propagating the particle signal in multiple directions. The differences in transmission path length are then exploited to accurately determine the particle's position.

By controlling the delay time of the delay unit within each pixel, our design accommodates variations in delay magnitude. This flexibility enables the extraction of precise position information based on the differences in delay among multiple transmission directions. The circuitry within each pixel primarily comprises a low-noise charge-sensitive amplifier, comparator unit, and controllable delay unit for establishing energy reconstruction signals. Our proposed scheme incorporates two readout configurations. The first configuration employs two transmission delay chains, enabling signal transmission in both forward and backward directions after a particle hit. The second configuration utilizes four transmission delay chains, facilitating signal transmission in four directions: up, down, left, and right.

For evaluation, we designed a prototype chip using TSMC 180-nanometer technology, featuring a pixel array size of 10 rows by 20 columns, with a chip area of 2.83mm x 3.81cm. Test results demonstrate that the delay unit accuracy of a single pixel is 3.12ps, with a controllable delay range of 4.976ns to 29.76ns distributed among six levels. The achieved pixel timing resolution is 44.12ps. Moreover, we verified the robustness of the input delay chain circuit under various PVT (process, voltage, and temperature) conditions, highlighting the stable performance of our design.

## Submission declaration

Original and unplublished

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**Track Classification:** ASICs