

Analysis of MOS capacitor with p layer with TCAD simulation

The ATLAS18 strip sensors of the ATLAS inner tracker upgrade (ITk) are under production since 2021. Along with the large-format n^+ -in-p strip sensor in the center of the wafer, test structures are laid out in the open space for monitoring the performance of the strip sensor and its fabrication process. One of the structures is a $1.2 \times 1.0 \text{ mm}^2$ test chip that includes representative structures of the strips, and metal-on-silicon (MOS) capacitors. In addition to the standard MOS capacitor, a MOS capacitor is designed with a p implantation representative of the p-stop doping for isolating the n^+ strips on the surface of silicon, the MOS-p capacitor. The C-V curve of the MOS capacitor shows characteristic behavior in the accumulation, depletion, and inversion regions as a function of bias voltage, from which one can deduce the amount of the interface charge. The MOS-p capacitor shows the C-V curve modulated by the properties of the p layer.

With over 50% of the full production complement delivered, we have observed consistent characteristics in the MOS-p capacitors. Rarely and currently only in two batches, we have observed abnormalities. To further study them, we have simulated the MOS-p capacitor with TCAD software, which successfully reproduces the normal behavior, including a feature caused by a geometrical offset of the area of the metal and the p implantation, with the p doping and the interface charge within the expected range. By contrast, the overall shape of the two abnormal cases is only reproduced when introducing 1/10 of the doping of the p implantation and charge traps in the p implanted area. A smaller but distinctive feature in the behavior is reproduced with a non-uniform distribution of the interface charge or other equivalent component. These simulations help to take final decisions for the batches in production.

Submission declaration

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