ALICE ITS3: a truly cylindrical vertex detector based on bent, wafer-scale stitched CMOS sensors

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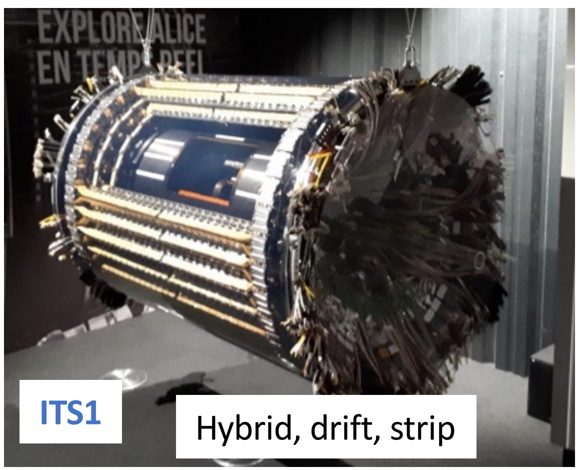
on behalf of the ALICE Collaboration

13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors

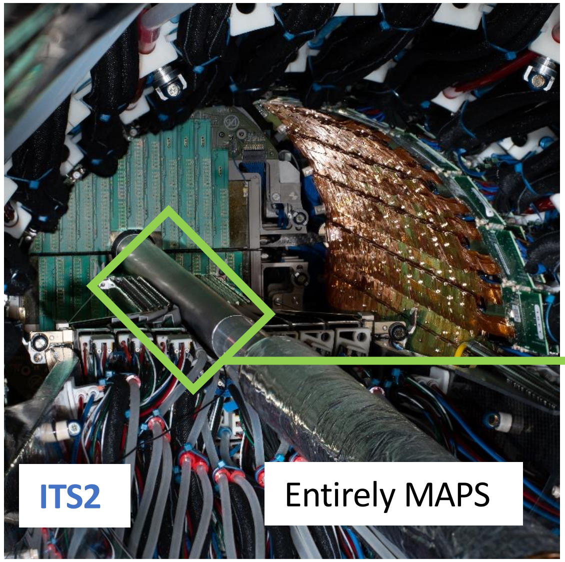
3-8 December 2023, Vancouver, Canada

ITS upgrade timeline

Shutdown/Technical stop
Protons physics
Ions
Commissioning with beam
Hardware commissioning/magnet training

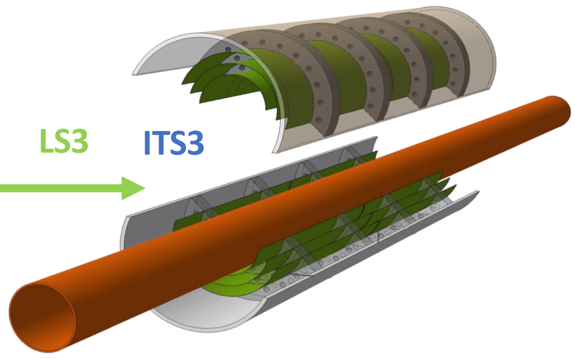


LS2



LS3

ITS3



Wafer-scale bent sensors

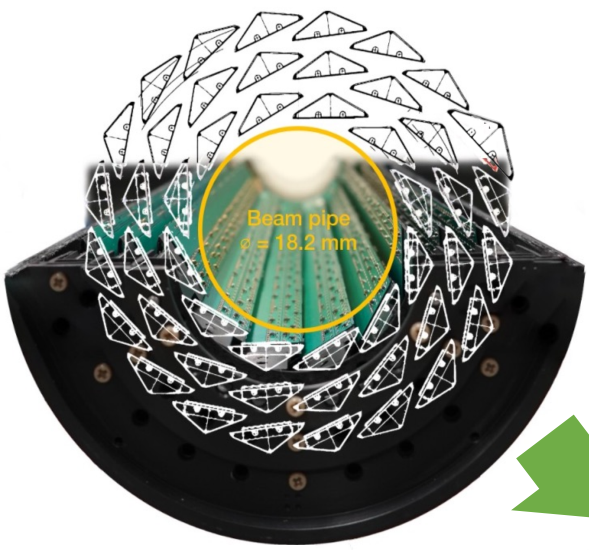
ITS3 LoI: CERN-LHCC-2019-018

ITS3

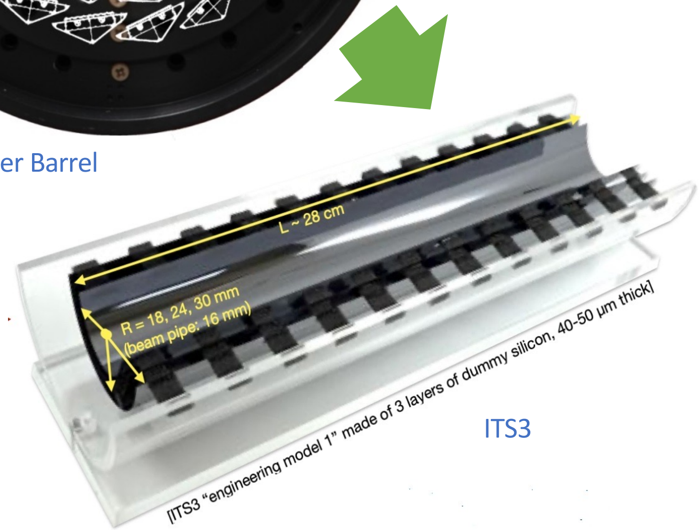
Replacing the 3 innermost layers with new ultra-light, truly cylindrical layers

- Reduced material budget (from 0.36% to 0.05% X_0 per layer) with a very homogenous material distribution by removing water cooling, circuit boards and mechanical support
- Closer to the interaction point (from 23 to 19 mm)

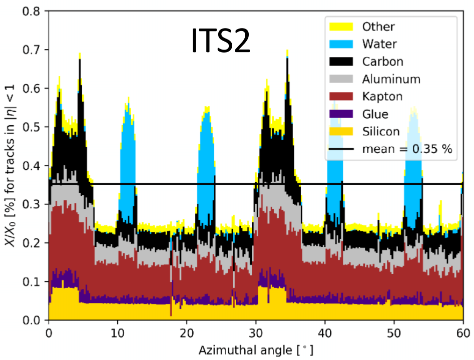
Improved vertexing performance and reduced backgrounds for heavy-flavour signals and for low-mass dielectrons

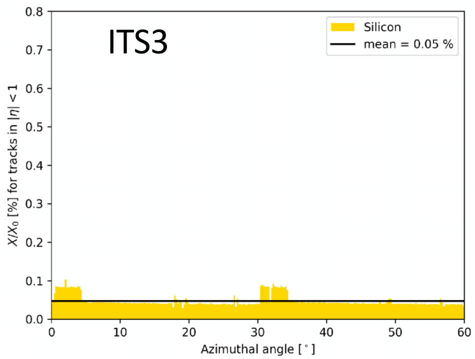


ITS2 Inner Barrel



ITS3

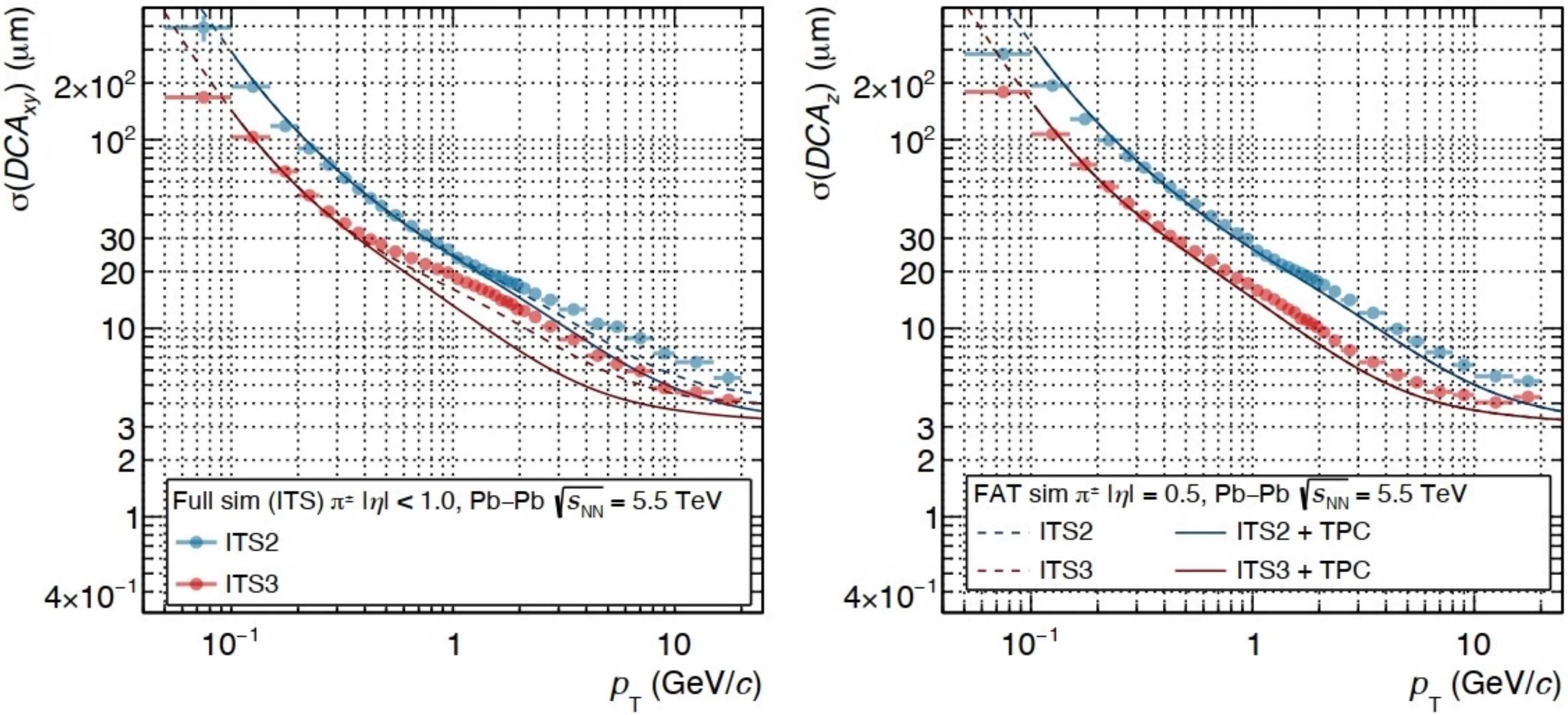




IB Layer Parameters	Layer 0	Layer 1	Layer 2
Sensor length [mm]		265.992	
Sensitive length [mm]		259.992	
Sensor azimuthal width [mm]	58.692	78.256	97.820
Radial position [mm]	19.0	25.2	31.5
Equatorial gap [mm]		1.0	
Max thickness [µm]		50	

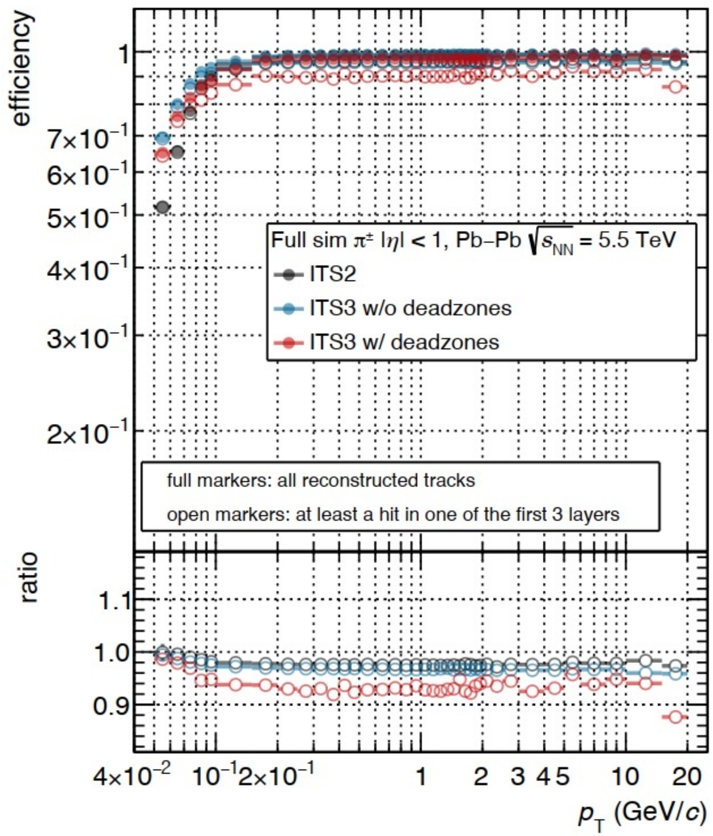
Table 3.3: Design dimensions of the sensor dies and radial position.

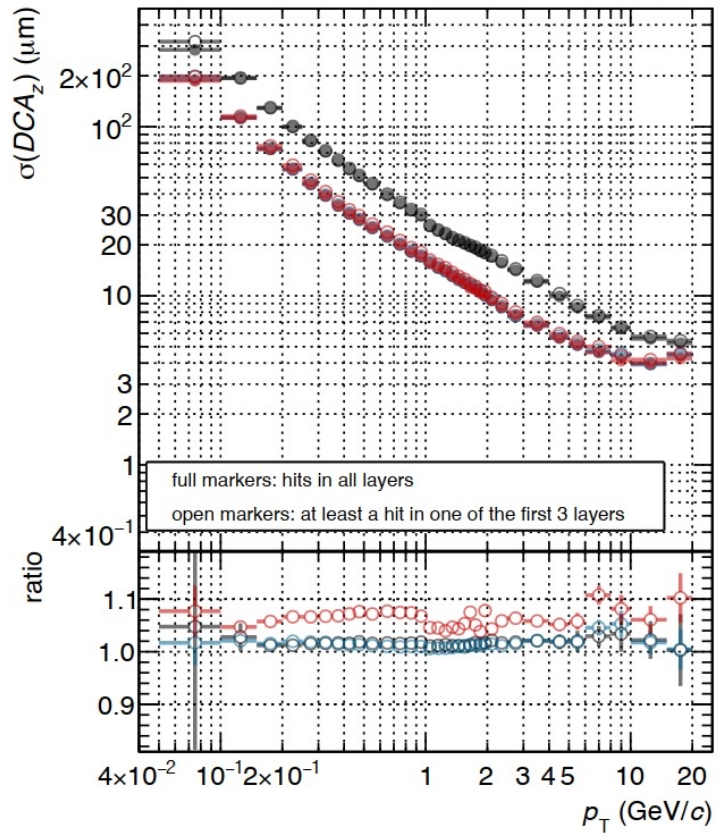
Pointing resolution



- Improvement in pointing resolution by a factor of 2 over all momenta

Impact of dead zones



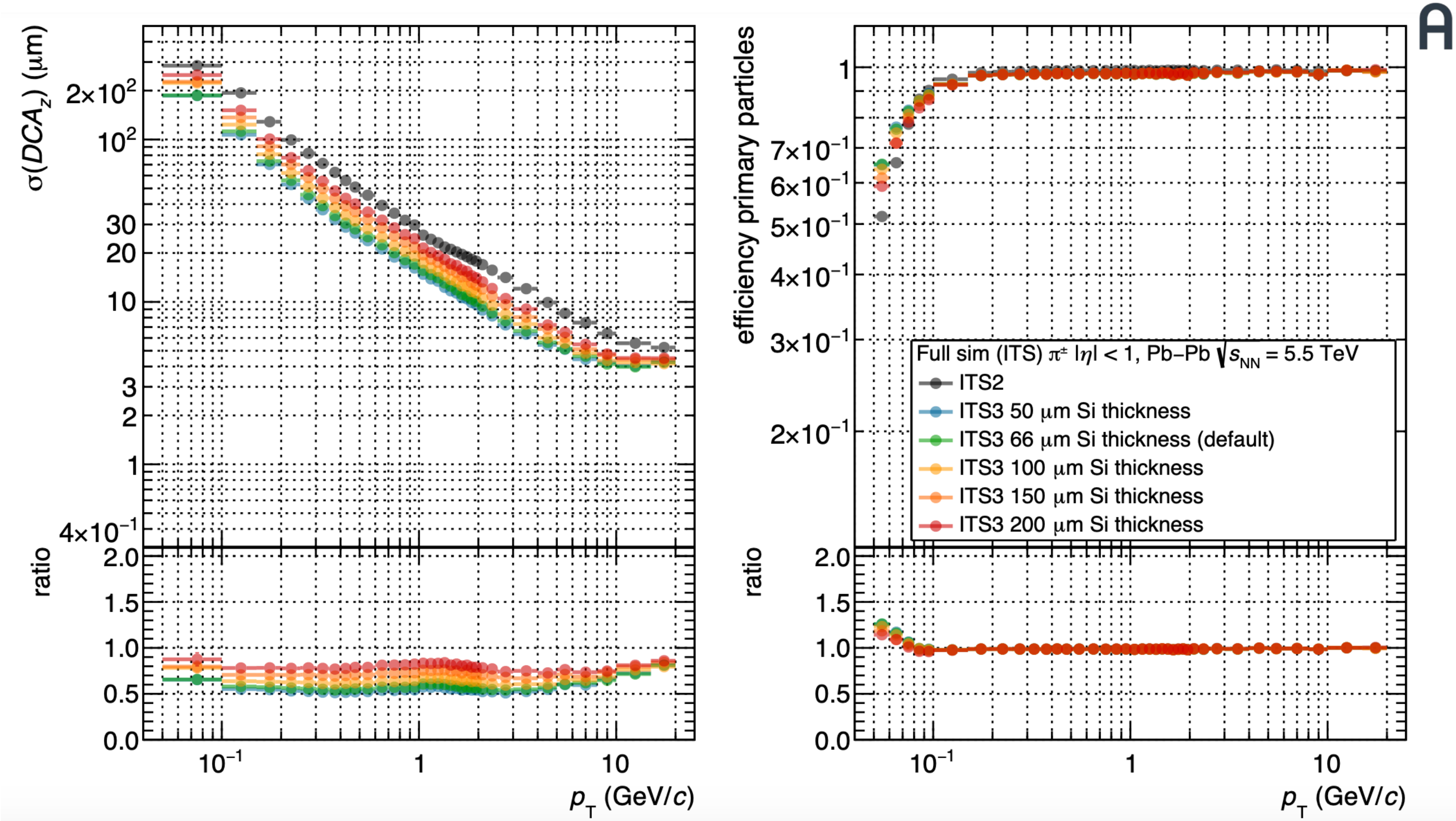


Current assumptions on dead areas:

- 1 mm gap between top and bottom barrels + dead areas on sensor
- Total: 8-9% dead zone

- Increase of tracking efficiency for low-p_T particles and extension of the low-p_T reach
- Dead zones have direct impact on efficiency and pointing resolution → important to optimise mechanics and chip design in this parameter

Impact of material budget



- Physical sensor thickness is assumed to be 50 µm → radiation length equivalent to 66 µm of silicon, taking into account Cu-based metal stack
- No significant degradation observed from 50 to 66 µm Si-equivalent

Sensor development roadmap

2021

2022

2023

2024

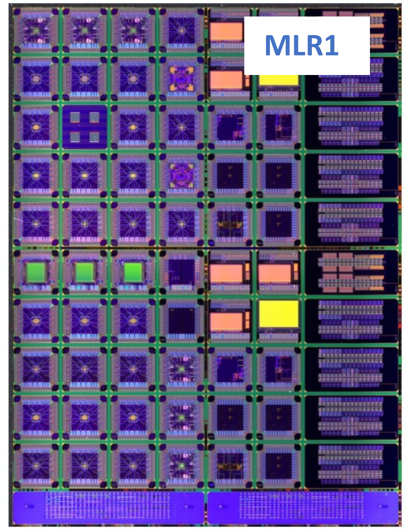
2025

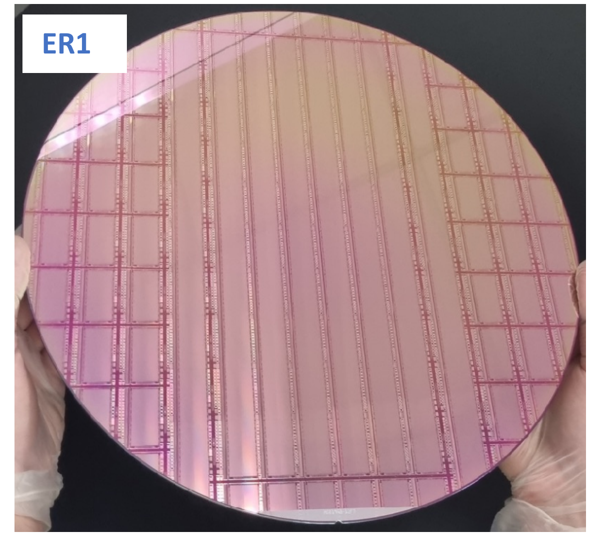
MLR1 (Multi-Layer Reticle 1): first MAPS in TPSCo 65 nm
- Successfully qualified the 65 nm process for ITS3 (and much beyond)

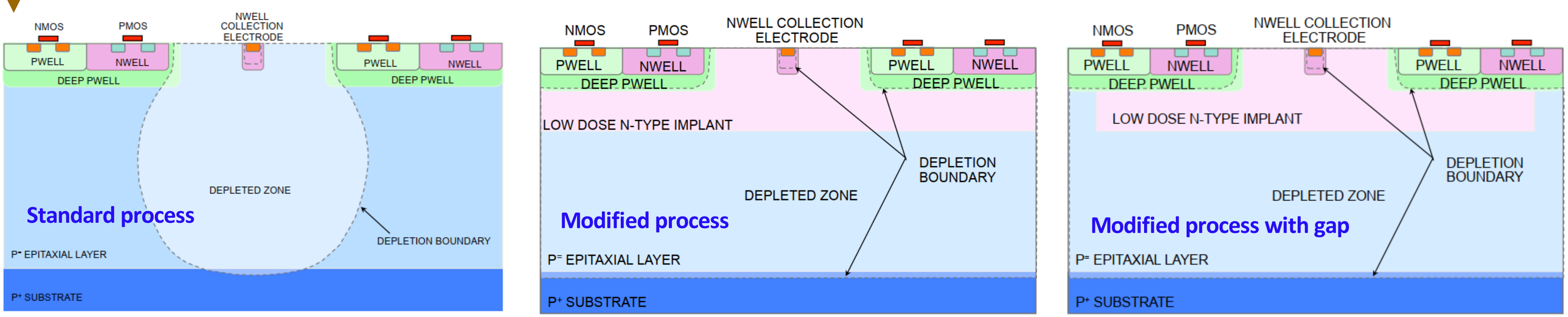
ER1 (Engineering run 1): first stitched MAPS
- Large design "exercise", stitching was new
- Tests ongoing

ER2: first ITS3 sensor prototype
- Specifications frozen
- Design ongoing

ER3: ITS3 sensor production





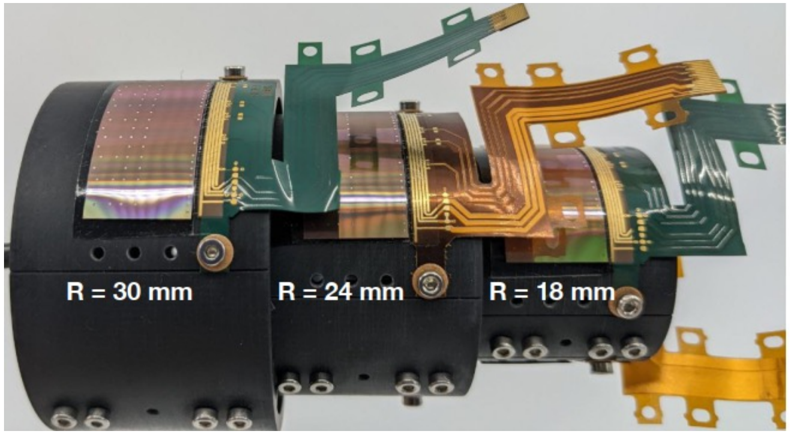


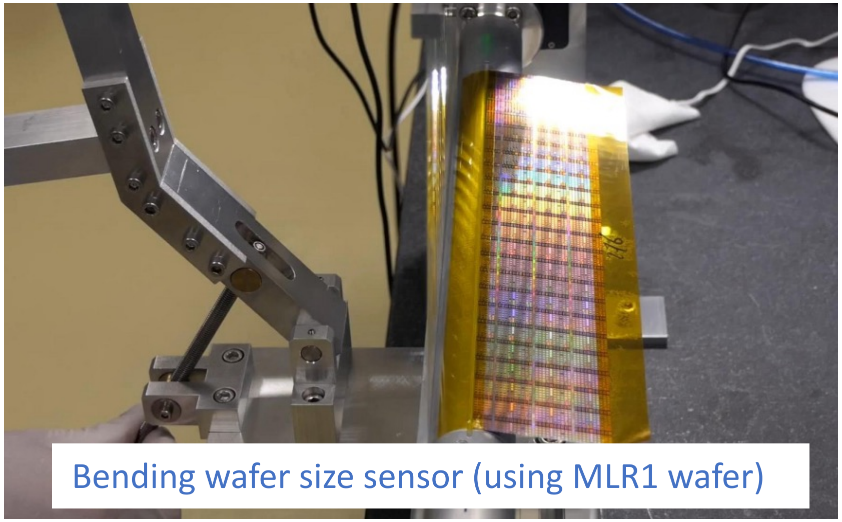
See more details on sensor design and stitching from Magnus Mager's talk on Thursday

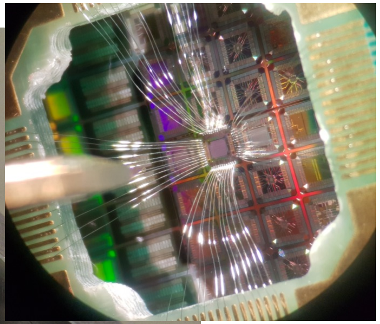
Sensor bending

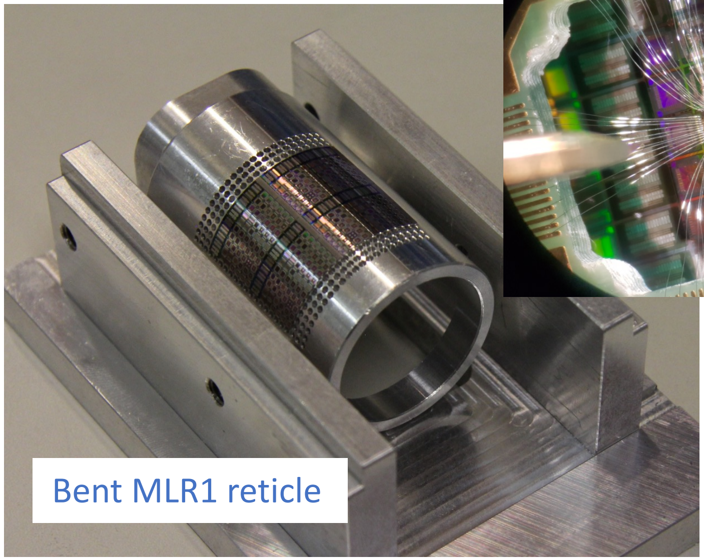
- Functional chips (ALPIDEs) and MLR1 sensors are bent routinely at different labs)
- Full mock-up of the final ITS3, called “μITS3”
  - 6 ALPIDE chips, bent to the target radii of ITS3 tested
- The sensors continue to work after bending (see next slide)
- Bent MLR1 prototypes are being tested

μITS3: 6 ALPIDEs bent at 18 mm, 24 mm, 30 mm




Bending wafer size sensor (using MLR1 wafer)

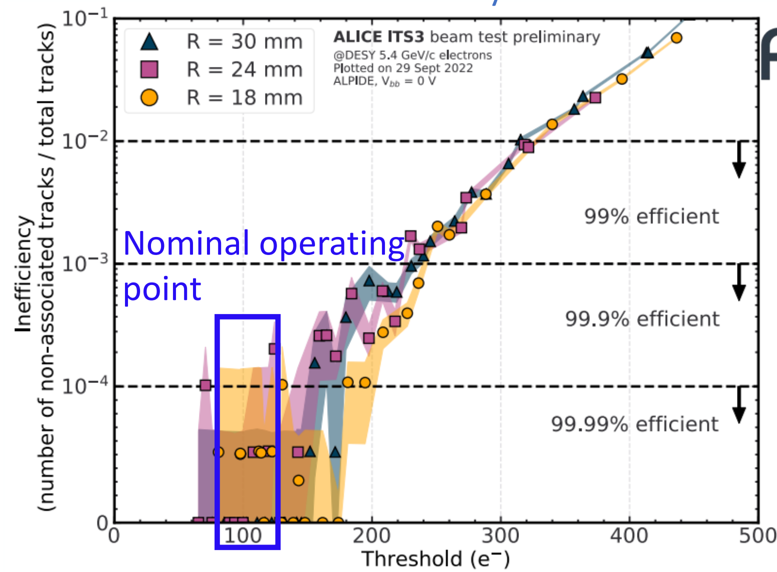


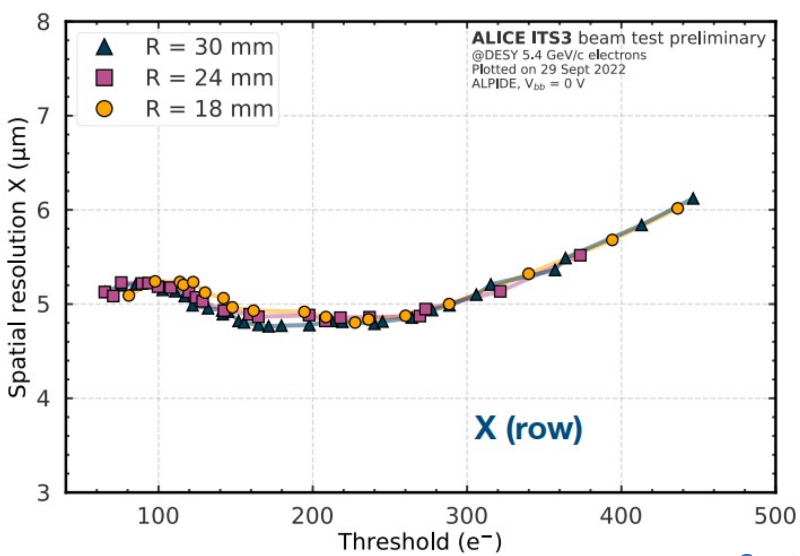

Bent MLR1 reticle

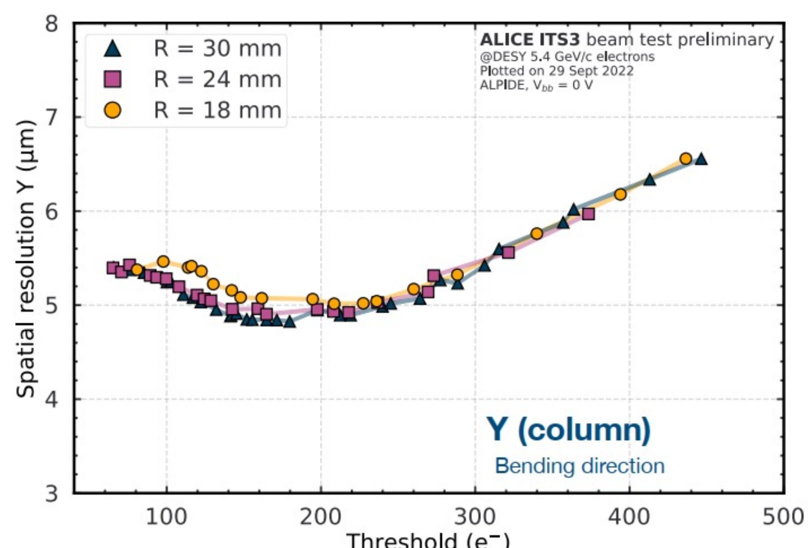
Bent ALPIDE test beams

- No effects on bending radius observed
- Spatial resolution of 5 µm consistent with flat ALPIDEs
- Efficiency > 99.99 % for nominal operating conditions
- Inefficiency compatible with flat ALPIDEs

Inefficiency





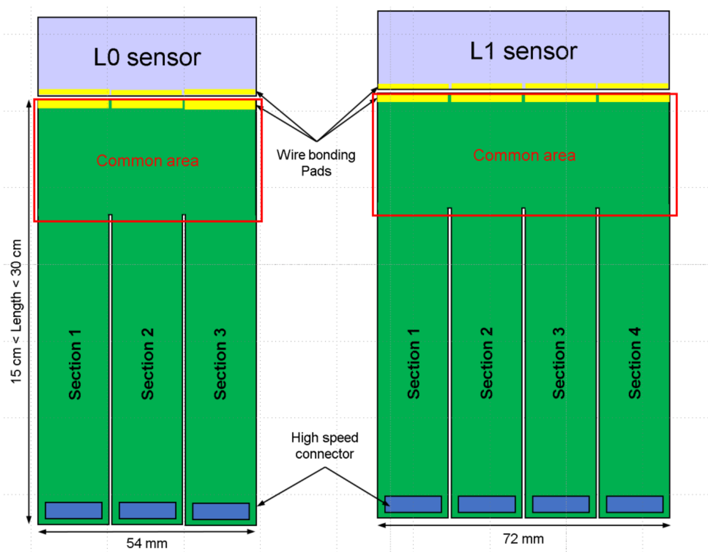


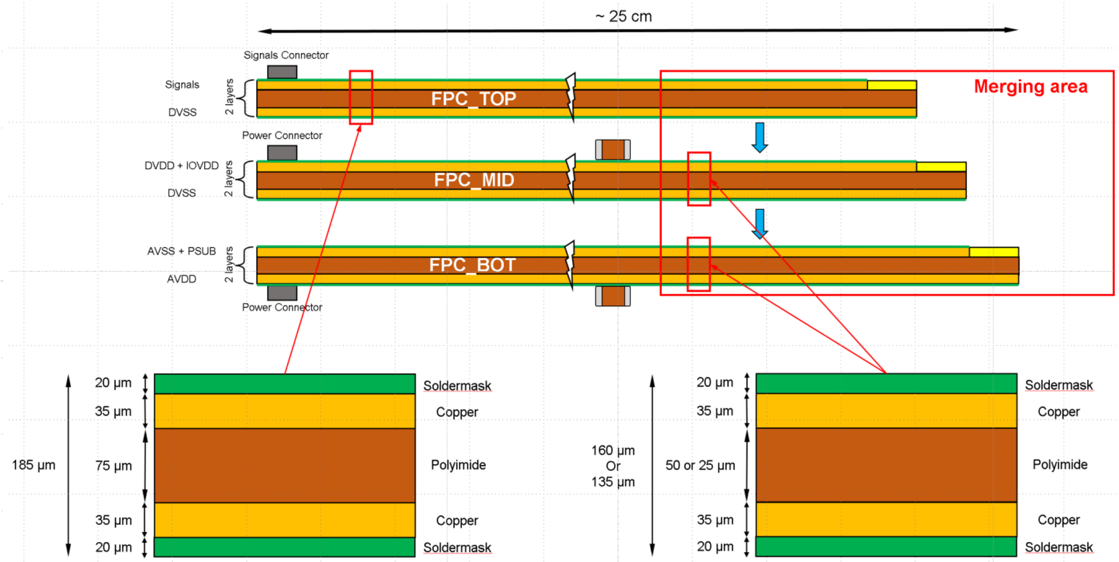
Spatial Resolution

Interconnection (1/2)

Flexible printed circuits (FPC) for communication and powering

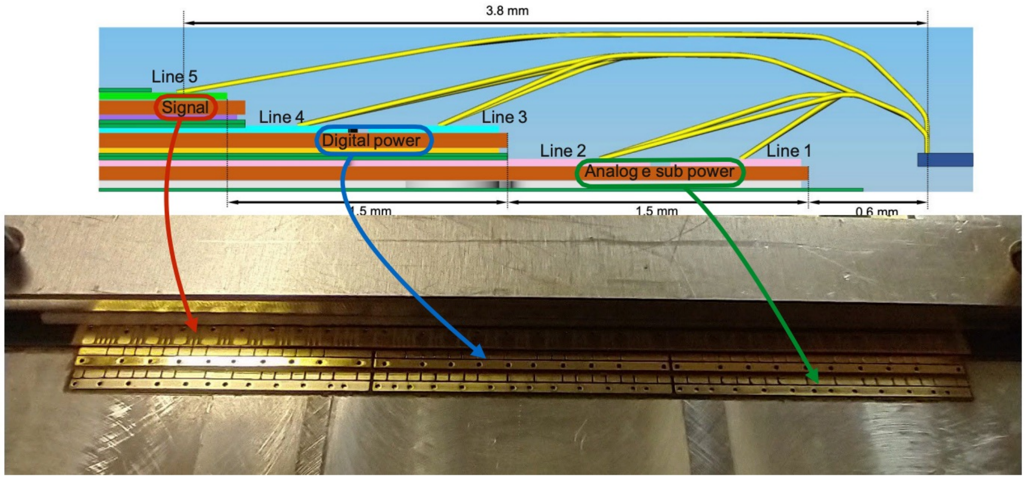
- Placed outside the sensible area
- 3,4 or 5 sections corresponding to the number of detector chip segments of the half-layer
- Three double copper layers flex, multi-strip shaped (15-30 cm long), connected in a concentrated merging area

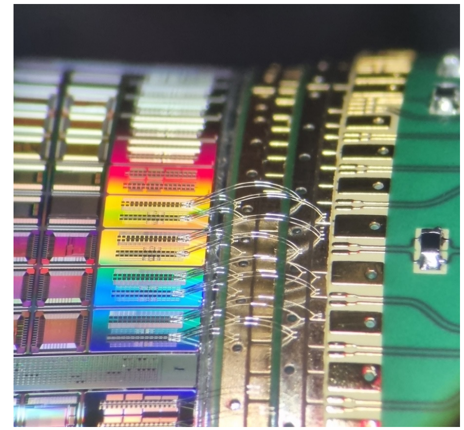




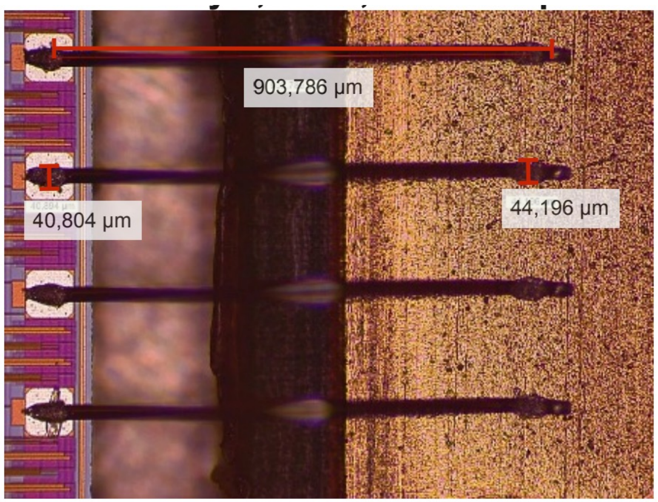
Interconnection (1/2)

- Interconnection through wire-bonding at the edge of the sensor verified
- Wire-bonds loops optimized based on pull-force measurements with ALPIDE sensors

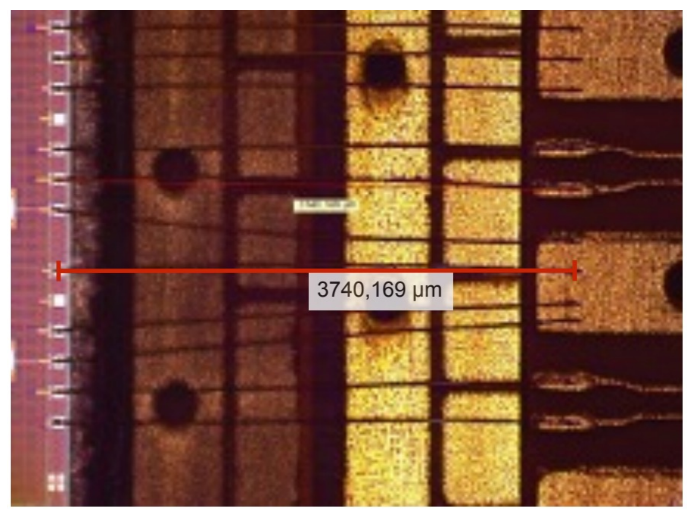




Wire-bonding to MLR1 prototypes



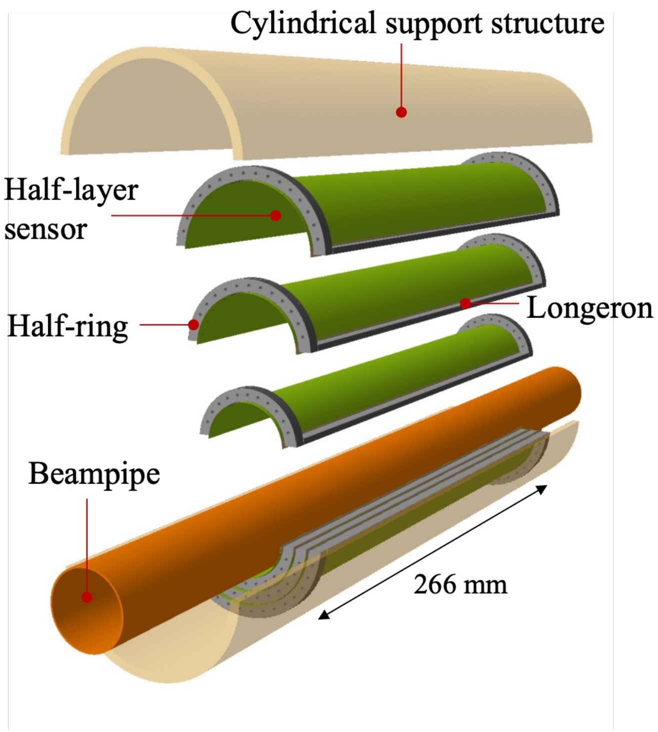
Bottom layer, line 1

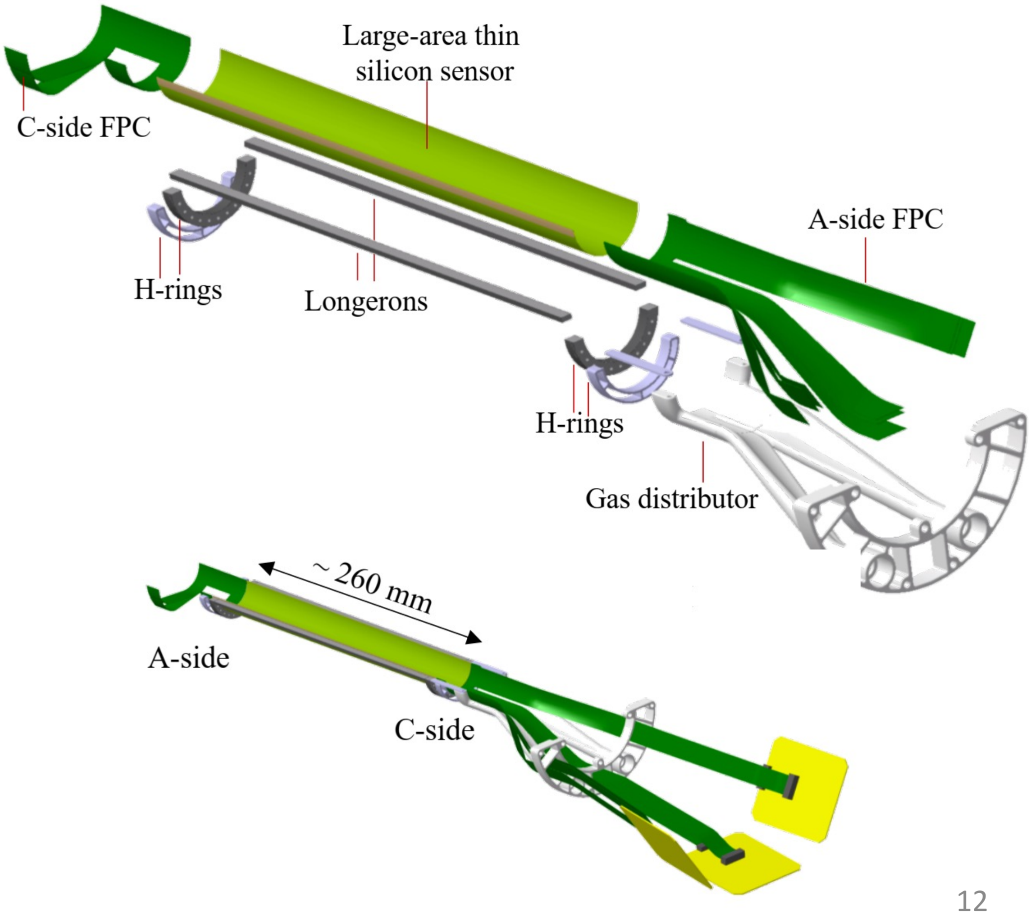


Upper layer, line 5

Detector concept

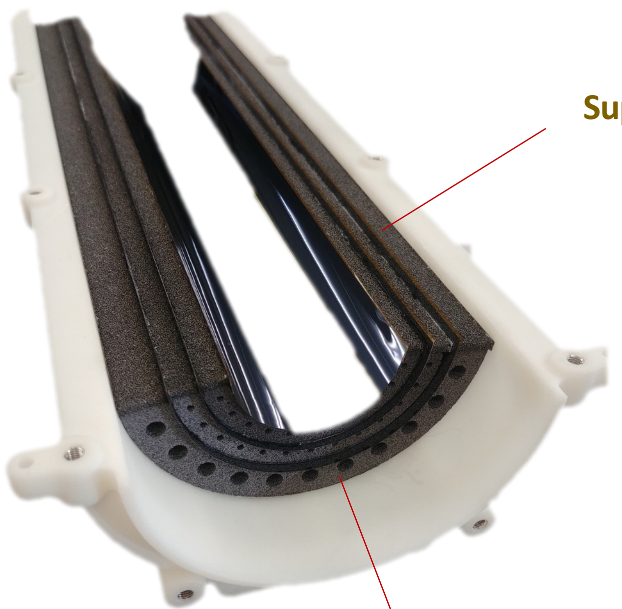
- Three detector layers and each layer is divided into two half-layers
- Each half-layer includes: wafer-scale silicon sensor, FPCs, lightweight support structures, radiator half-ring and gas distributor





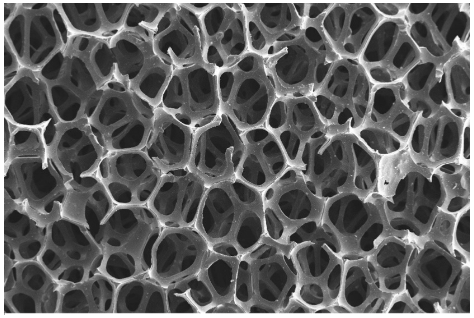
Mechanics and cooling

- The limited dissipated power allows for the use of air cooling at ambient temperature (colder gas are also being considered as back up)
- The material budget requirement call for a unpalpable support structure, i.e., carbon foam used as support and radiator (carbon fiber truss support being considered as backup)

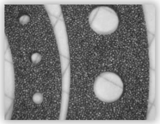


Support

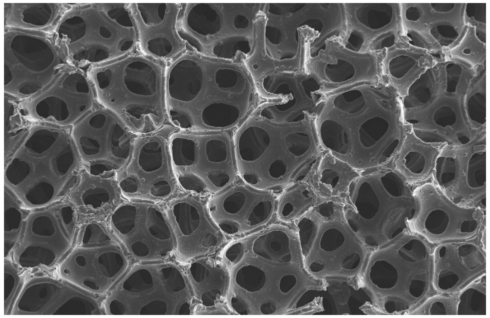
ERG Carbon
@Duocel
ρ = 0.045 kg/dm³
k = 0.033 W/m·K



Support & cooling

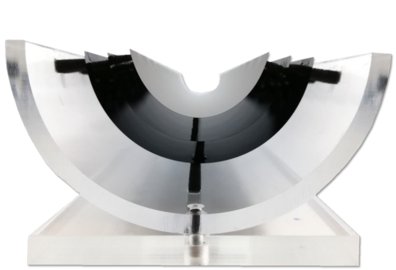


K9
Standard Density
ρ = 0.2-0.26 kg/dm3
k = >17 W/m·K



Mechanical prototypes

- Engineering models (EMs): used for design development, a mixture of final-grade components and commercial components




EM1

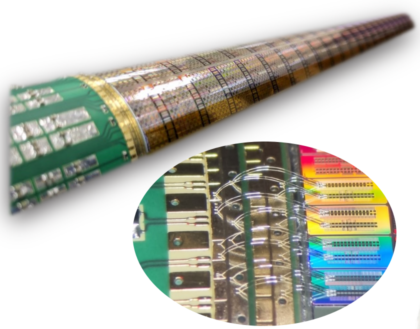
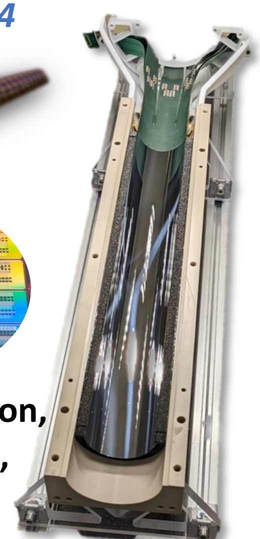

EM2

- Breadboard models (BBMs): test samples and initial prototypes, partially representative of some of the final model features

BBM3

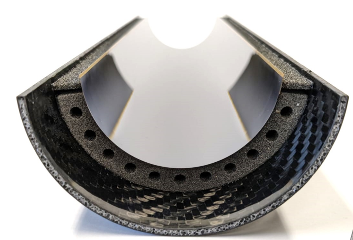
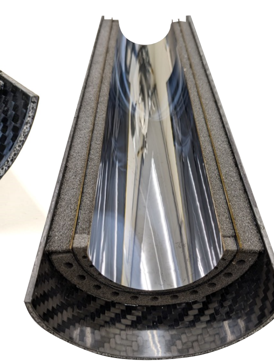
Thermal test, Aeroelastic test

BBM4

Wafer-size sensor integration, FPC-sensor wire bonding, Aeroelastic test

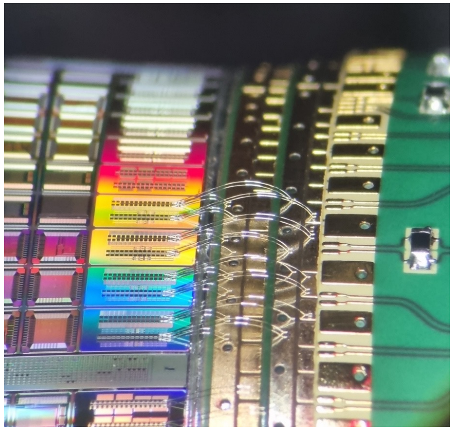
BBM5

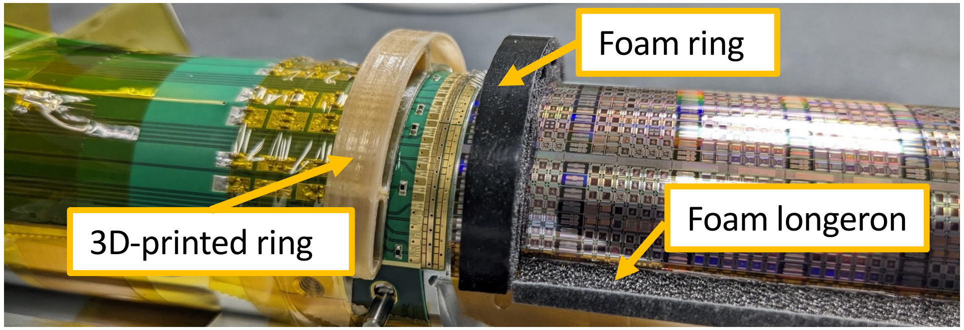
Thermoelastic test

Layer assembly

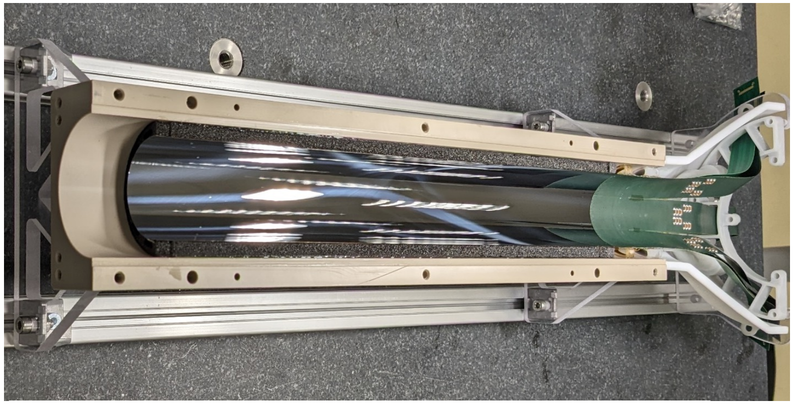
Aligning FPC and the sensor



Wire-bonding for the curved sensor

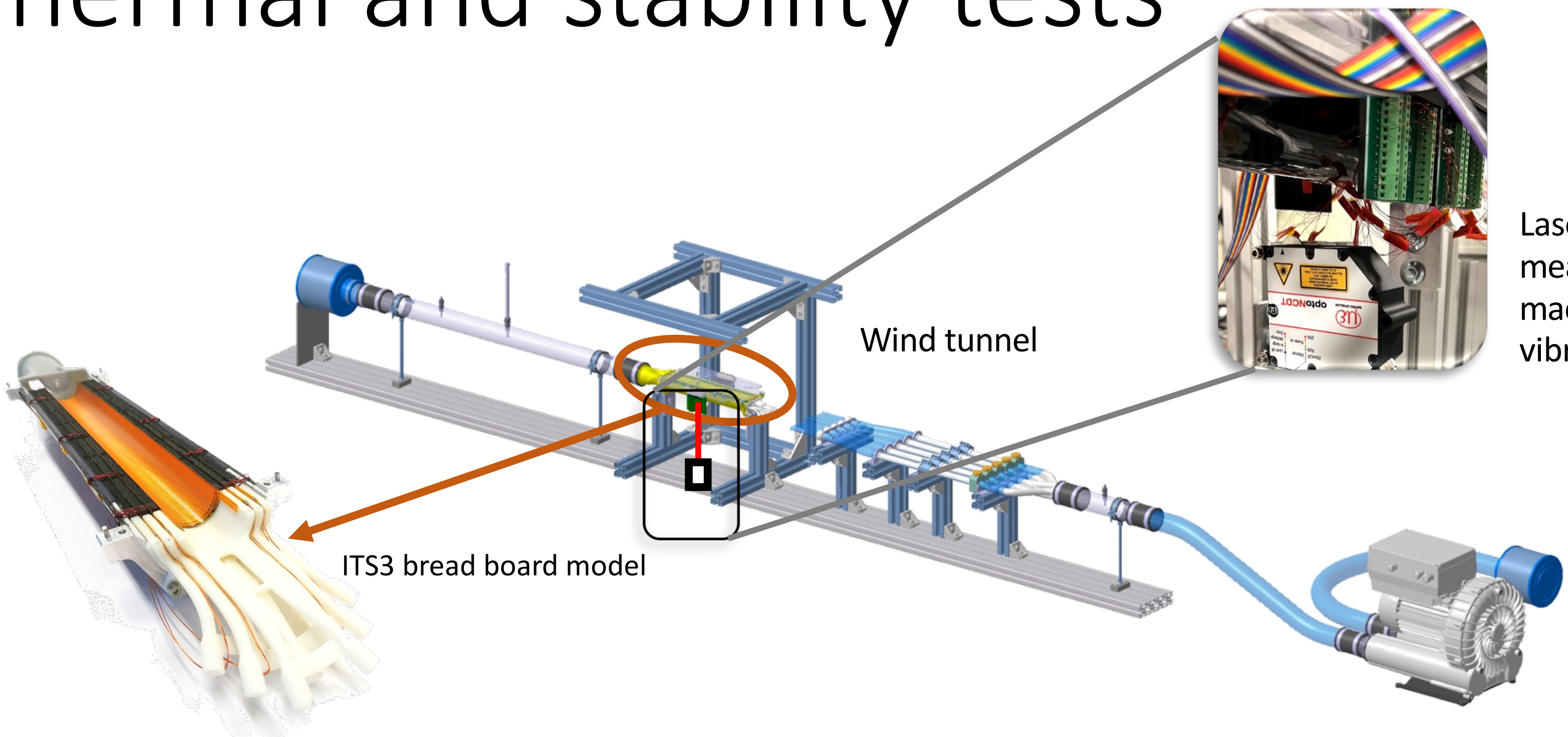


Gluing of foams and additional supports

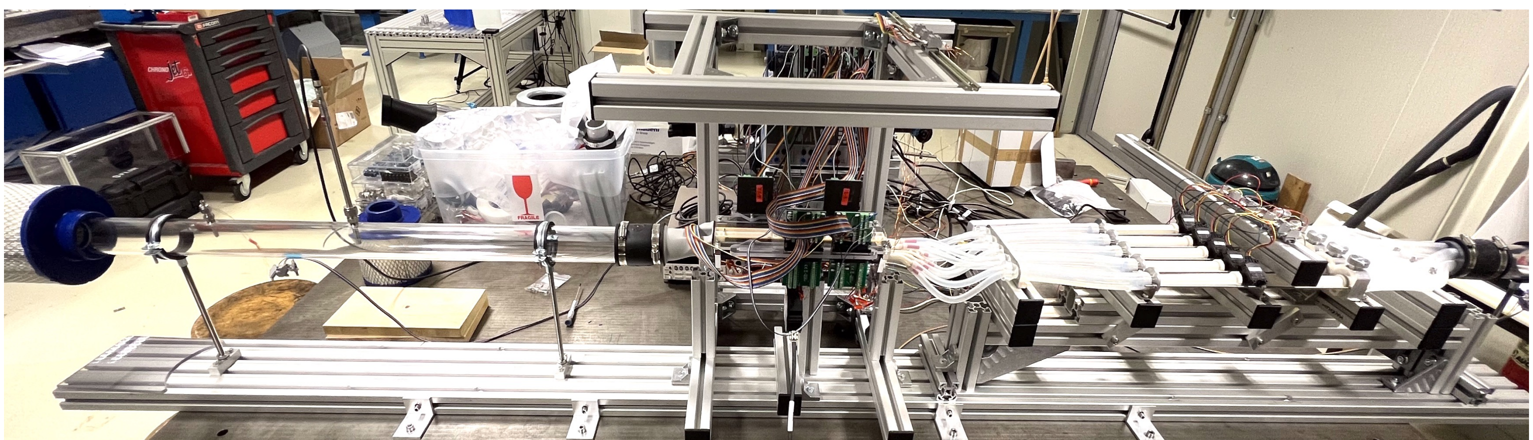


Assembled first demonstrator half-layer 0

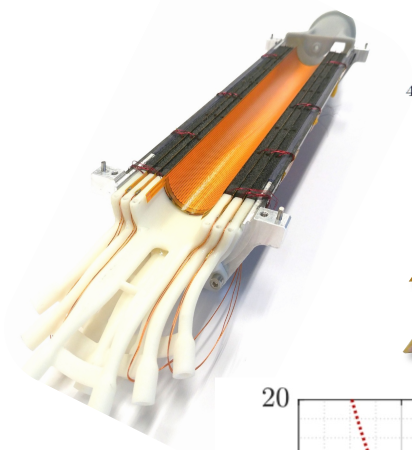
Thermal and stability tests

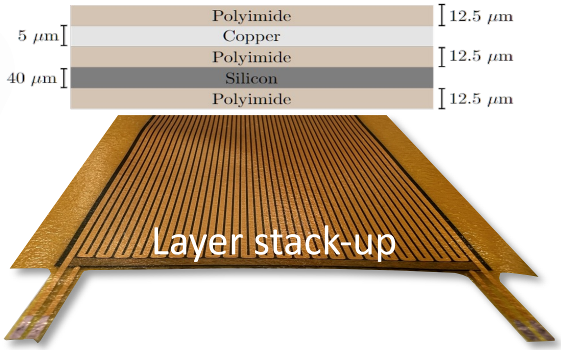


Laser measurement machine for vibration analysis



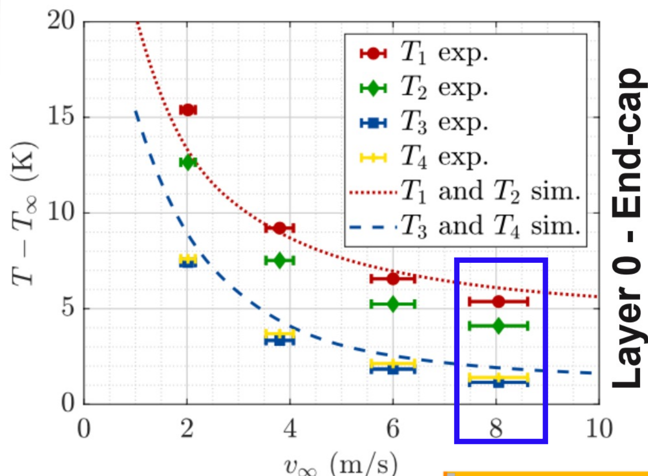
Thermal analysis

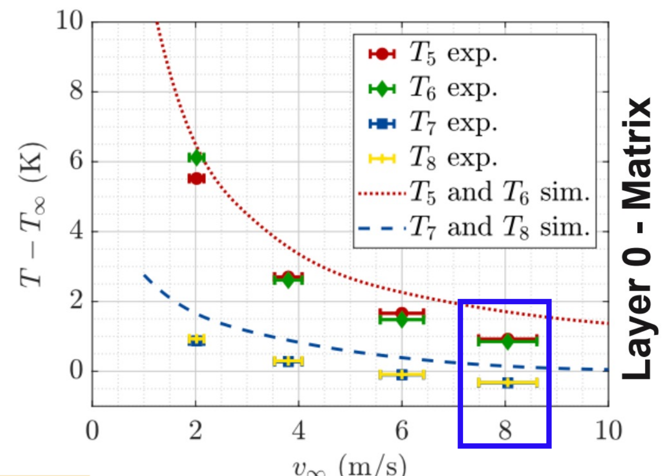




Thermal characterization setup

- Dummy silicon equipped with copper serpentine simulating heat dissipation in matrix (25 mW/cm²) and end-cap (1000 mW/cm²) regions
- 8 PT100 temperature sensors distributed over the surface of each half-layer



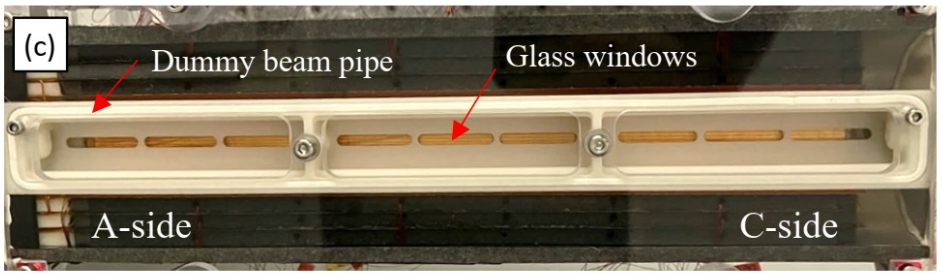


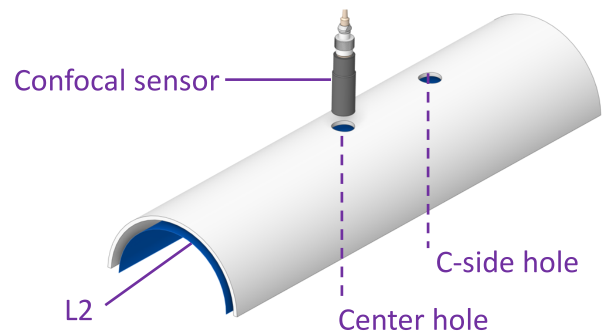
Temperature sensor position and nomenclature

- With an average airflow free-stream velocity between the layers of about 8 m/s, the detector can be operated at a temperature of 5 degrees above the inlet air temperature
- Temperature uniformity along the sensor can be also kept within 5 degrees
- Preserved performance when increasing the matrix heat dissipation to 50 mW/cm² → further studies to be done with a new BBM

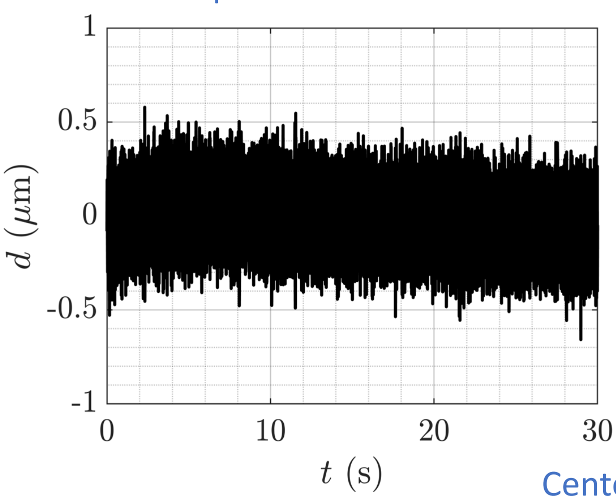
Vibrational study

- Non-contact displacement sensors for vibration measurements → avoid perturbation of the airflow approaching the half-layers
- Glass windows implemented on the dummy beampipe and CYSS → allow displacements on the half-layer 0 and 2 to be measured

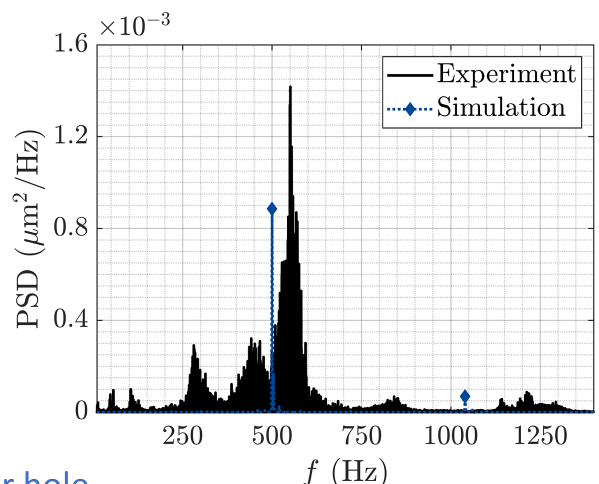




Displacement vs. time



Power spectral density of the displacements



- Peak-to-peak ~ 1.1 µm
- rms of the displacement < 0.4 µm

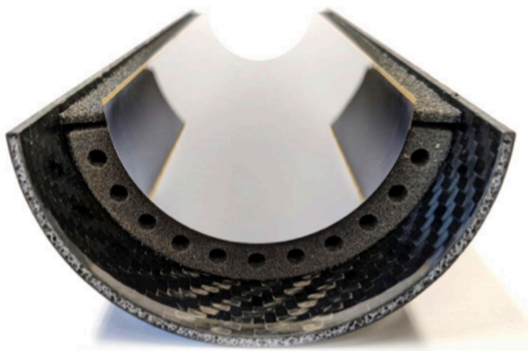
Center hole

half-layer 2, v_∞ = 8 m/s

Thermoelastic tests

Thermoelastic expansion setup

- Differential thermoplastic expansion caused by short-term temperature fluctuation among different components could introduce failures
- Final grade material half-layer assembly in climate chamber (up to 40 °C by steps of 2 °C)



Materials

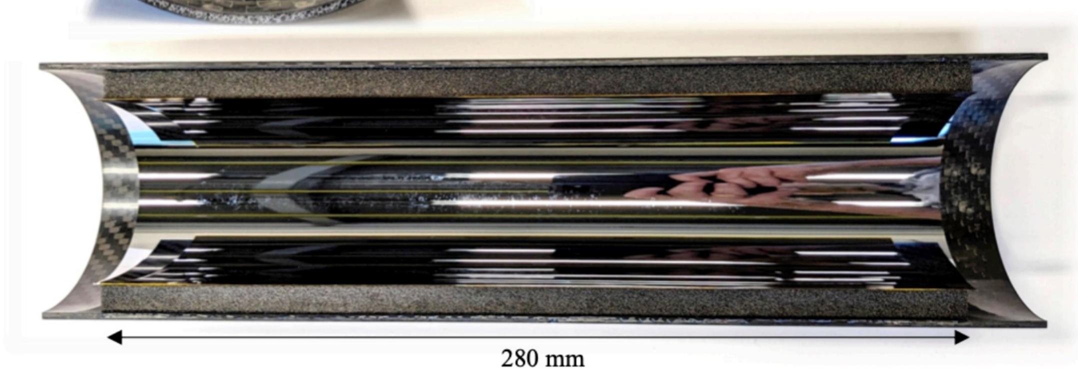
C-side H-ring: carbon foam, ERG (RVC) Duocel®

Longerons: carbon foam, ERG (RVC) Duocel®

Half-layer 2: Blank silicon 40 µm

CYSS: carbon sandwich

A-side H-ring: carbon foam, Allcomp k9 SD



- Several thermal cycles for a total of 50 hours → assembly unaffected
- Further tests will be performed to investigate rapid increase of the temperature and maximum failure temperature

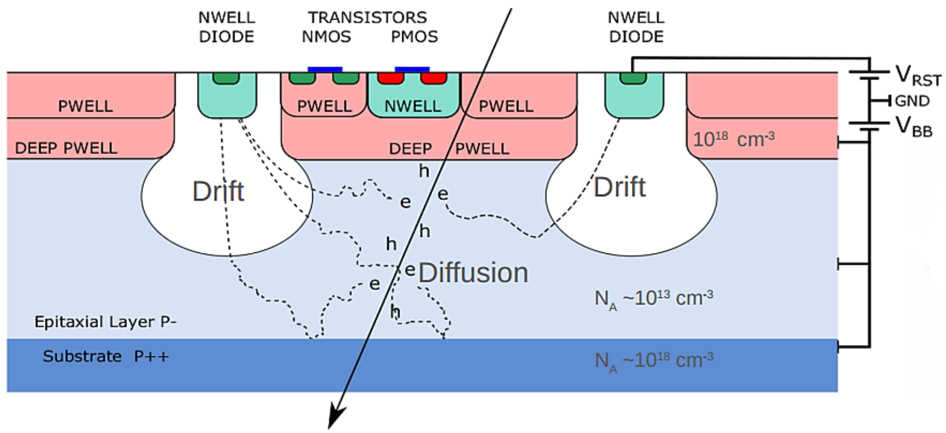
Summary

- ITS3: replacement of inner barrel of ITS2 with stitched wafer-scale 65 nm CMOS sensors to improve pointing resolution and tracking efficiency
- 65 nm sensor technology validated for ITS3
- Characterization of stitched sensors ongoing
- Silicon flexibility and bending proved with routine bending tests; observed compatible performance between bent and flat sensors
- Optimization of air cooling and mechanics ongoing
- TDR is ready for December 2023

ITS3 is on track for installation in LHC LS3

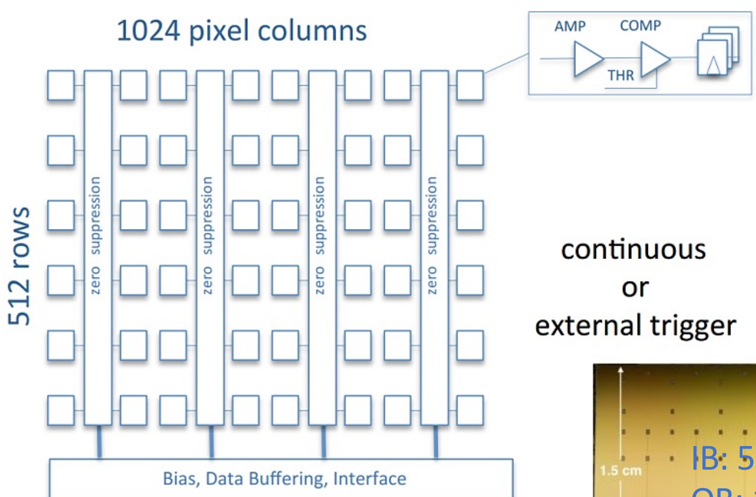
Backup

ALPIDE: ALICE PIxel DEtector

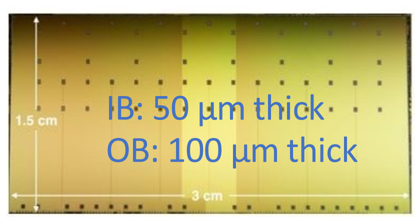


ALPIDE technology features:

- TowerJazz 180 nm CiS Process, full CMOS
- Deep P-well implementation available
- High resistivity epi-layer (>1 kΩ·cm) p-type, thickness 25 µm
- Smaller charge collection diode → lower capacitance → higher S/N
- Possibility of reverse biasing
- Substrate can be thinned down



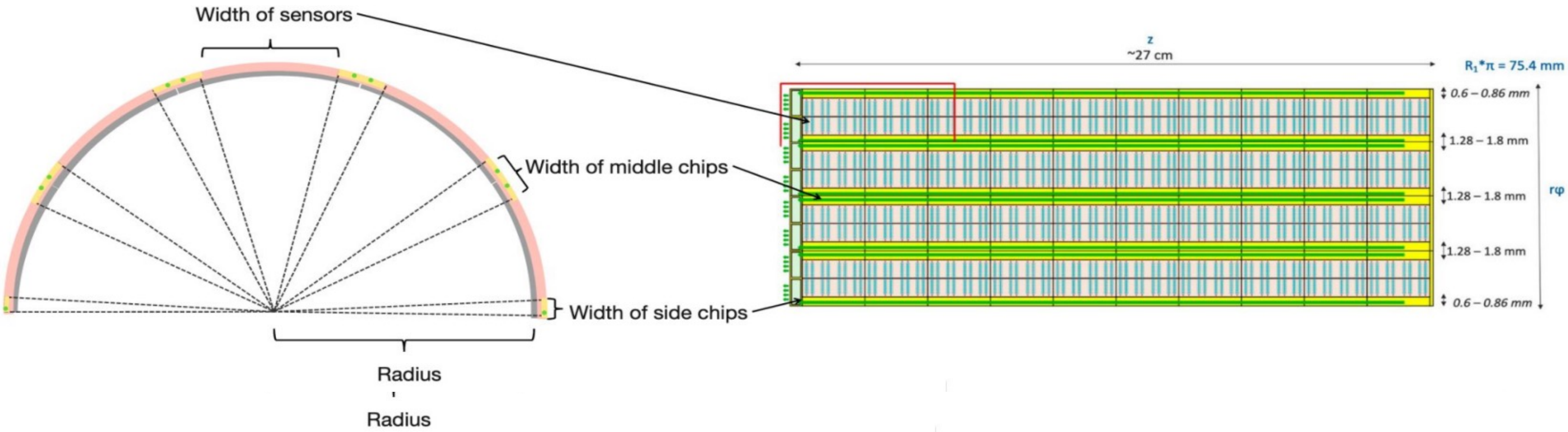
continuous
or
external trigger

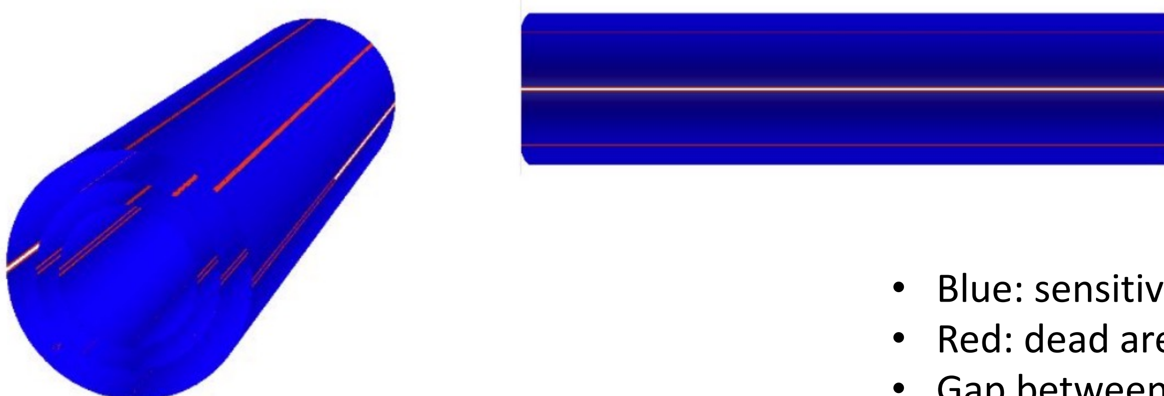


Sensor specification:

- Pixel pitch 27 µm x 29 µm → spatial resolution 5 µm x 5 µm
- Priority Encoder Readout
- Power: 40 mW/cm^2
- Trigger rate: 100 kHz
- Integration time: < 10 µs
- Read out up to 1.2 Gbit/s
- Continuous or triggered read-out

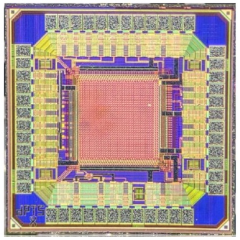
ITS3 geometry - dead zones



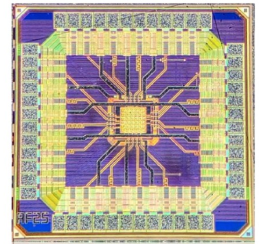


- Blue: sensitive areas
- Red: dead areas
- Gap between the two hemicylinders

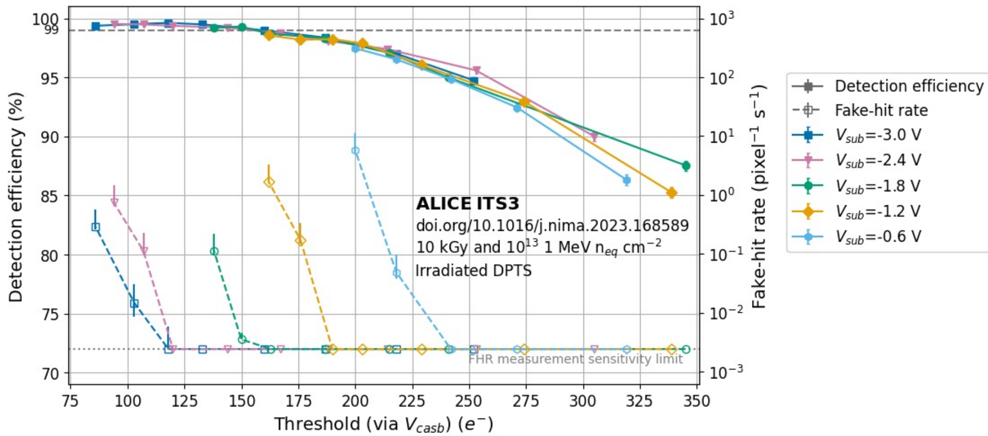
MLR1 characterization

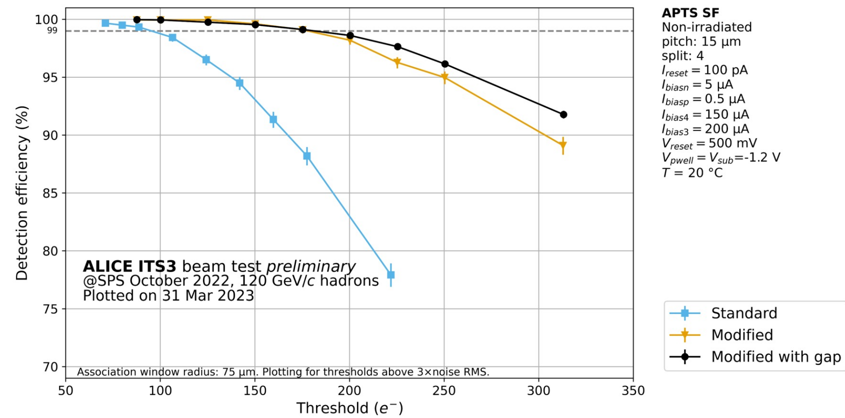


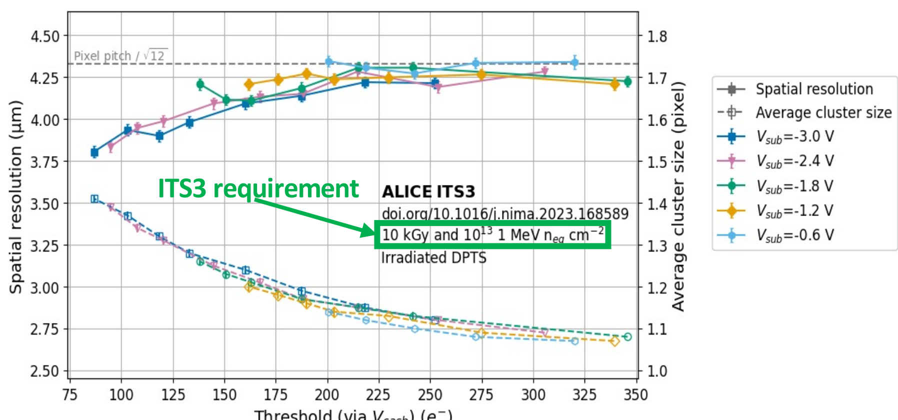
Digital Pixel Test Structure (DPTS)
- 32x32 pixel matrix
- Asynchronous digital readout with Time-over-Threshold information
- Pitch: 15 µm
- Only "modified with gap" process



Analogue Pixel Test Structure (APTS)
- 6x6 pixel matrix
- Direct analog readout of central 4x4 pixels
- Two types of output drivers
  - Source follower (APTS-SF)
  - Fast OpAmp (APTS-OA)
- Pitch: 10, 15, 20 and 25 µm







- Validated in terms of charge collection efficiency, detection efficiency and radiation hardness
- Several pixel variants (pitch 10 - 25 µm) were tested both in laboratory and in beam tests
- Excellent detection efficiency over large threshold range for the ITS3 radiation hardness requirement (10 kGy + 10^{13} 1MeV n_{eq} /cm^2)

ER1 design

First MAPS for HEP using stitching

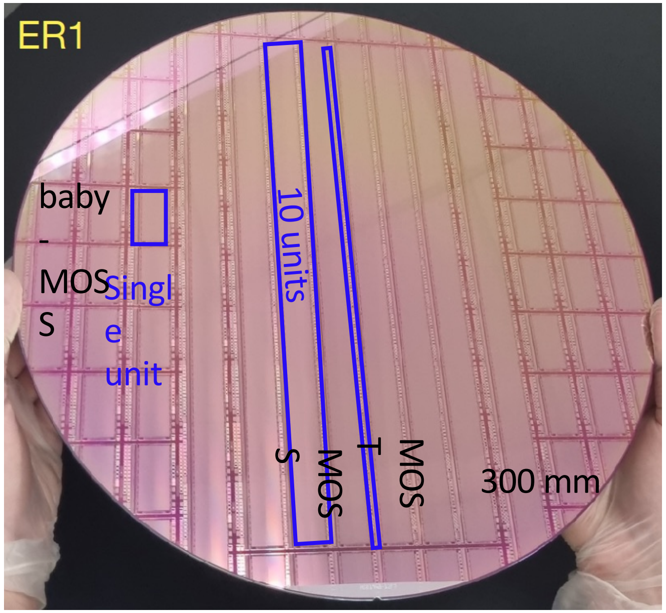
- One order of magnitude larger than previous chips

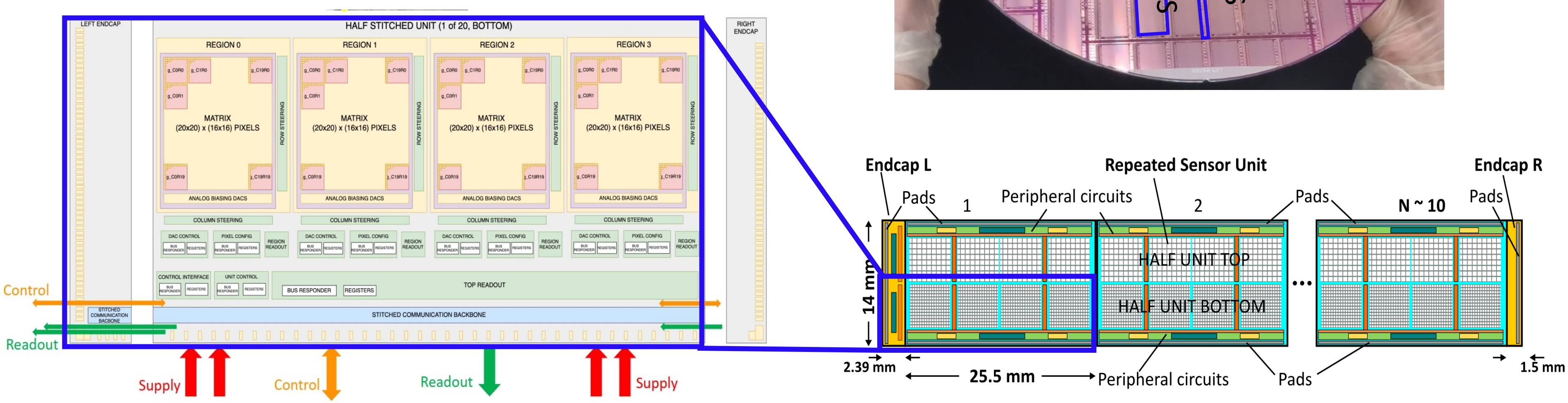
"MOSS": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm^2)

- Conservative design, different pitches

"MOST": 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm^2)

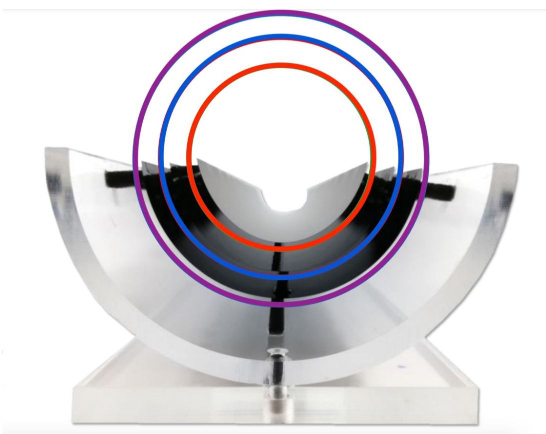
- More dense design



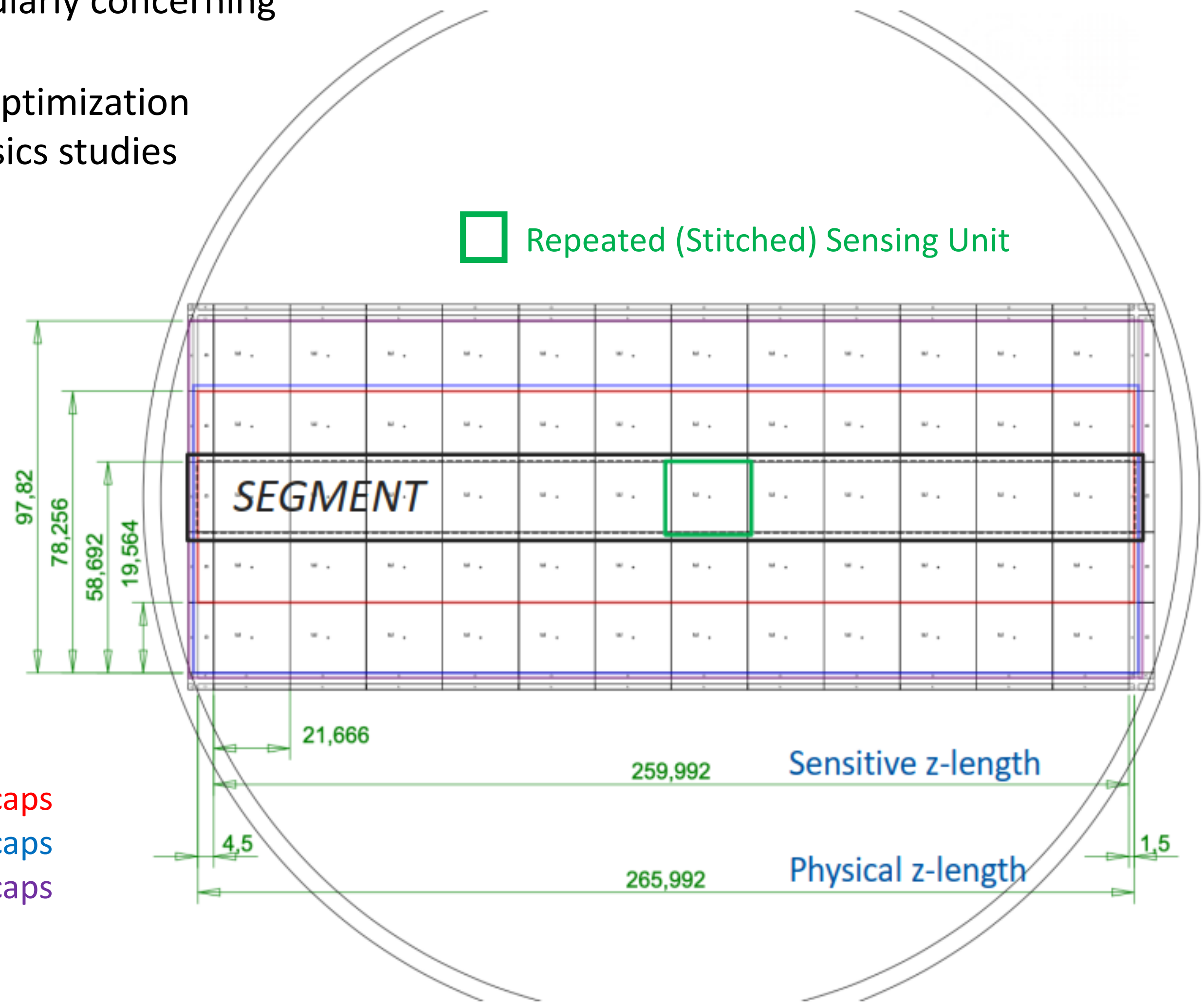


ER2 sensor (MOSAIX) geometry

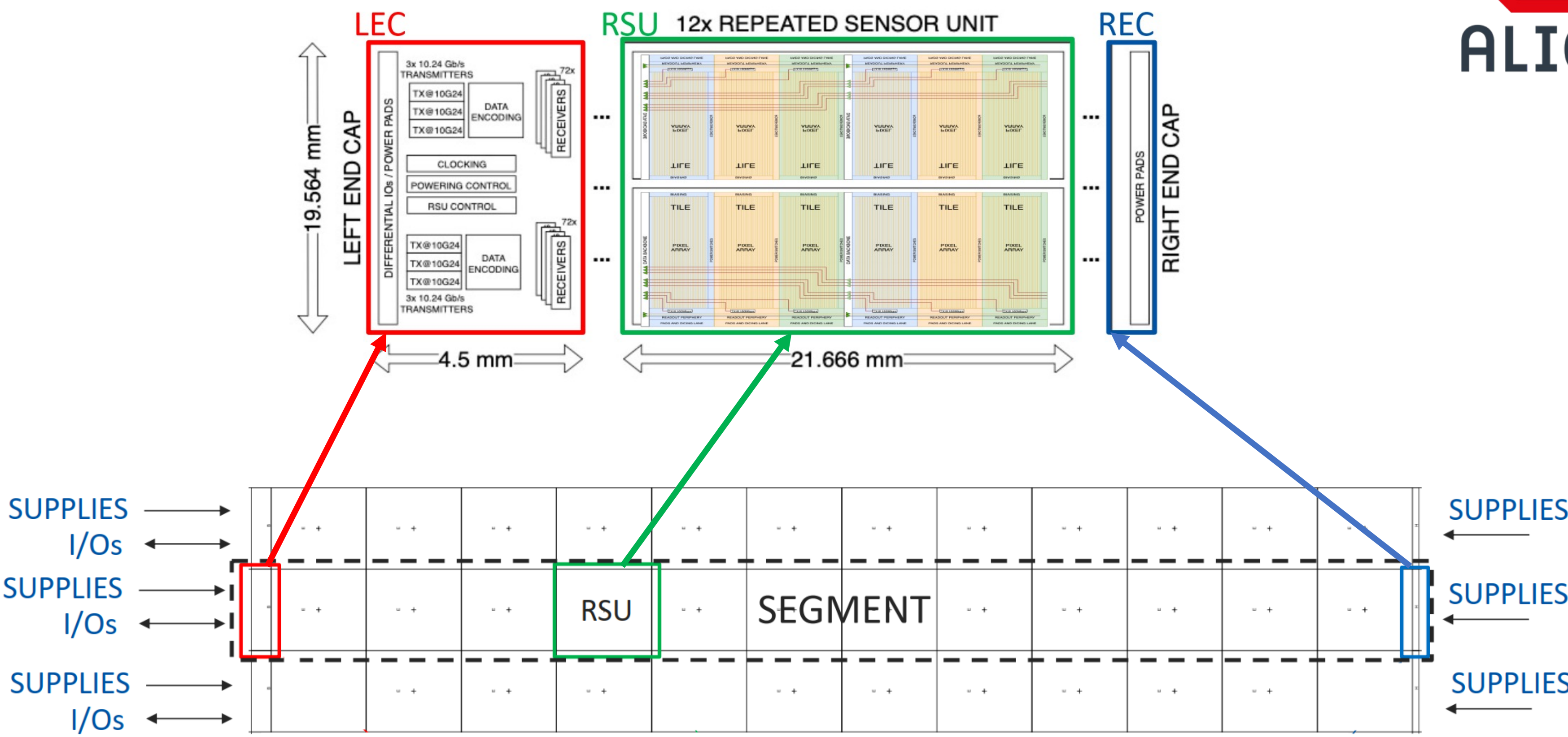
- The stitched design adheres to specific dimensional relationships, particularly concerning integer ratios between chip radii
- Established through a thorough optimization process from mechanics and physics studies



Layer 0: 12 x 3 repeated units + endcaps
Layer 1: 12 x 4 repeated units + endcaps
Layer 2: 12 x 5 repeated units + endcaps



Stitched sensor design for MOSAIX

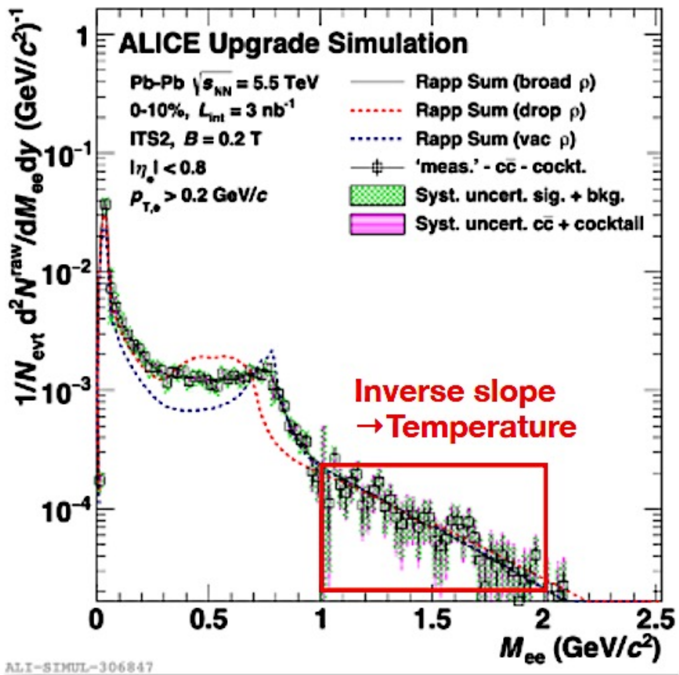


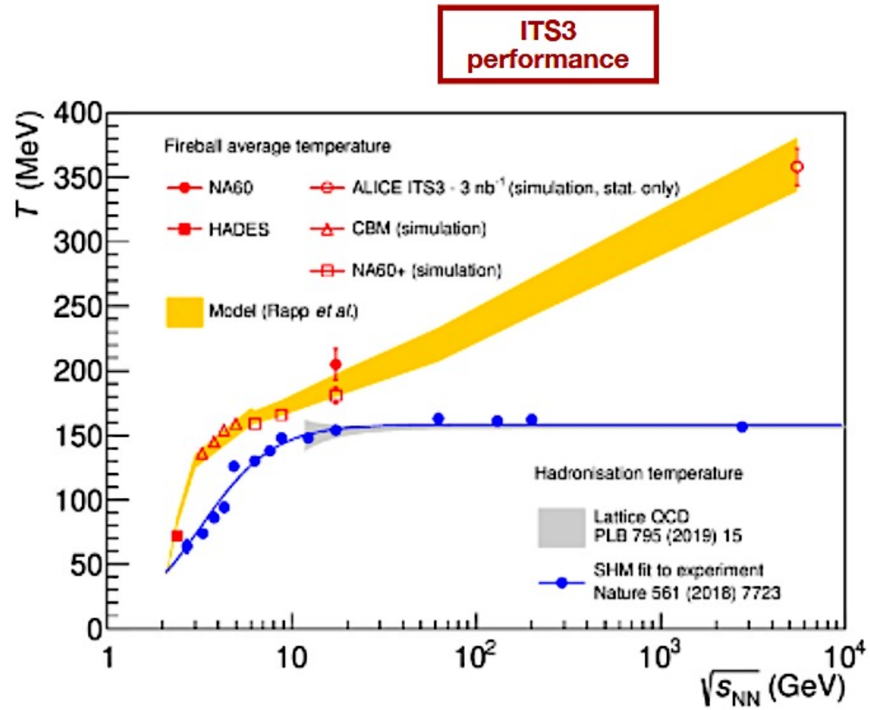
- Physics-driven simulations to optimise bandwidths and buffers
  - Direct impact on fill-factor and power consumption
- Fill factor ~93% (possibly ~95.5% depending on ER2 test results)
- Front-end evolution path: DPTS → MOSS → MOSAIX
- Power consumption: 40 mW/cm^2

ITS3 - Physics goals - Dileptons

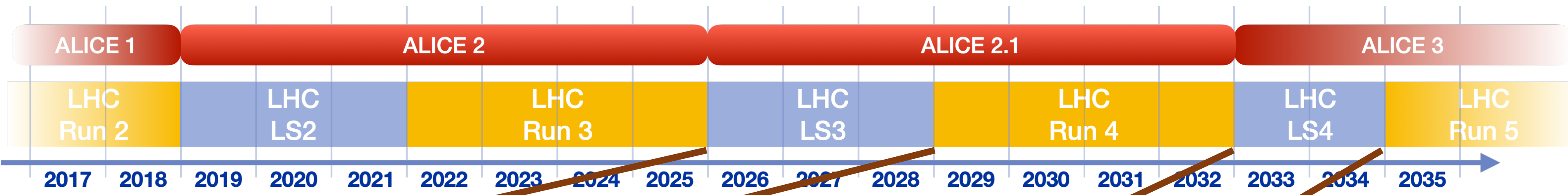
Thermal dileptons, photons, vector mesons (thermal radiation, chiral symmetry restoration)

- High precision measurement of temperature in mass region $1<M_{ee}<2$ GeV/c^2



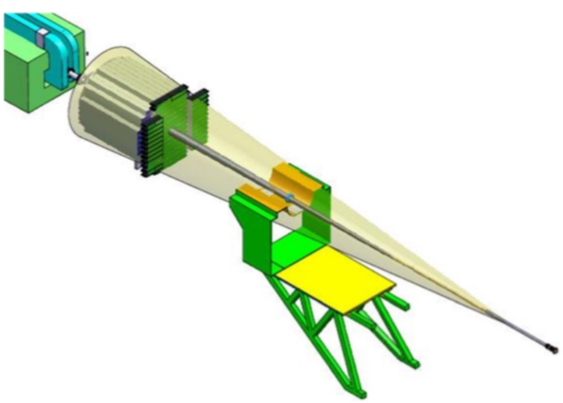


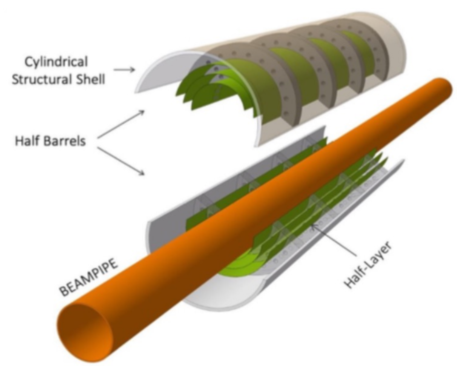
ALICE upgrades timeline

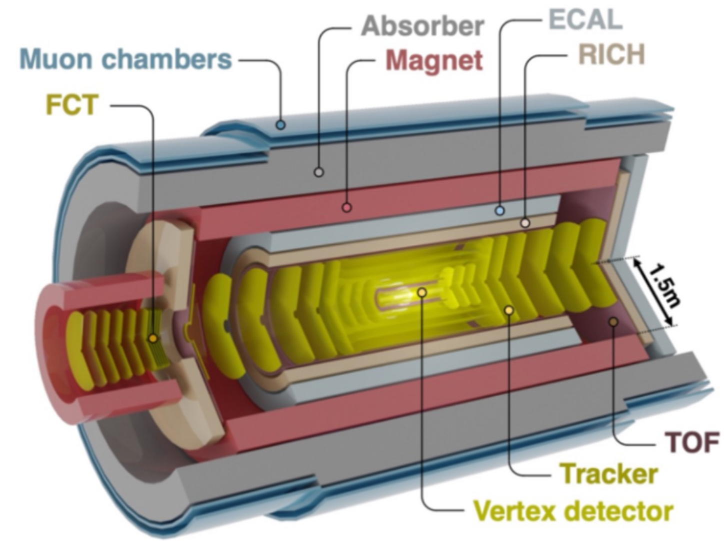


LS3: FoCal and ITS3

LS4: ALICE 3







FoCal LoI: [CERN-LHCC-2020-009]

ITS3 LoI: [CERN-LHCC-2019-018]

ALICE 3 LoI: [CERN-LHCC-2022-009]