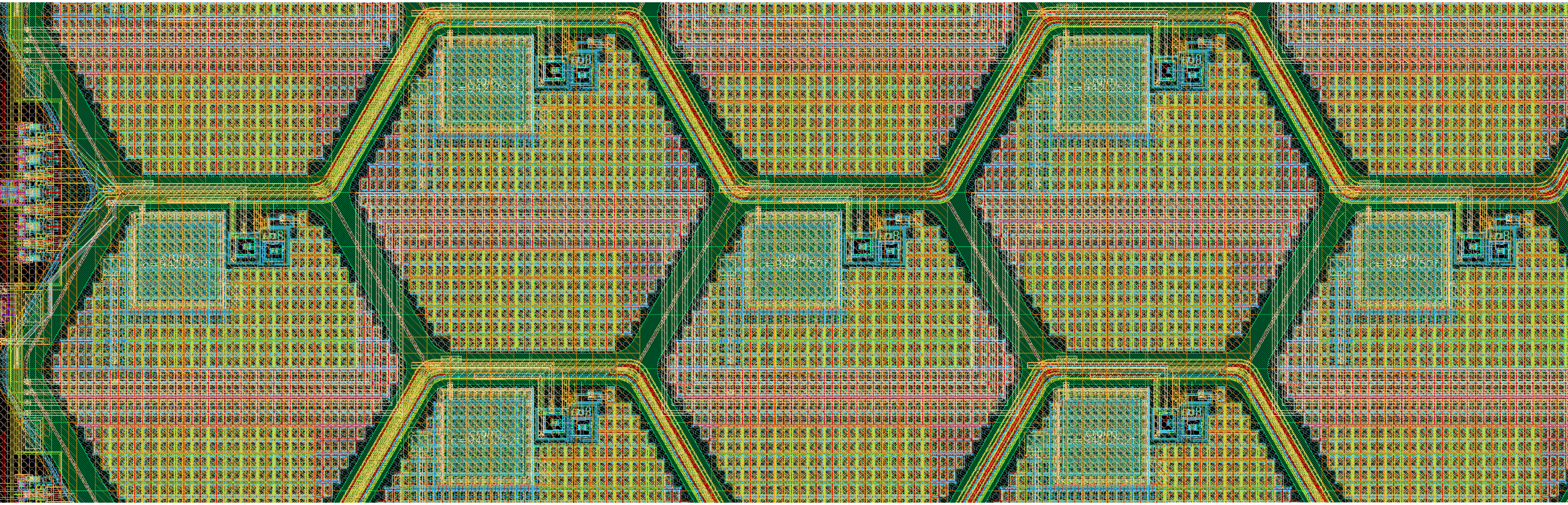
Time resolution and radiation hardness of monolithic pixel sensors in BiCMOS technology

Roberto Cardella — Université de Genève



UNIVERSITÉ DE GENÈVE

Swiss National Science Foundation

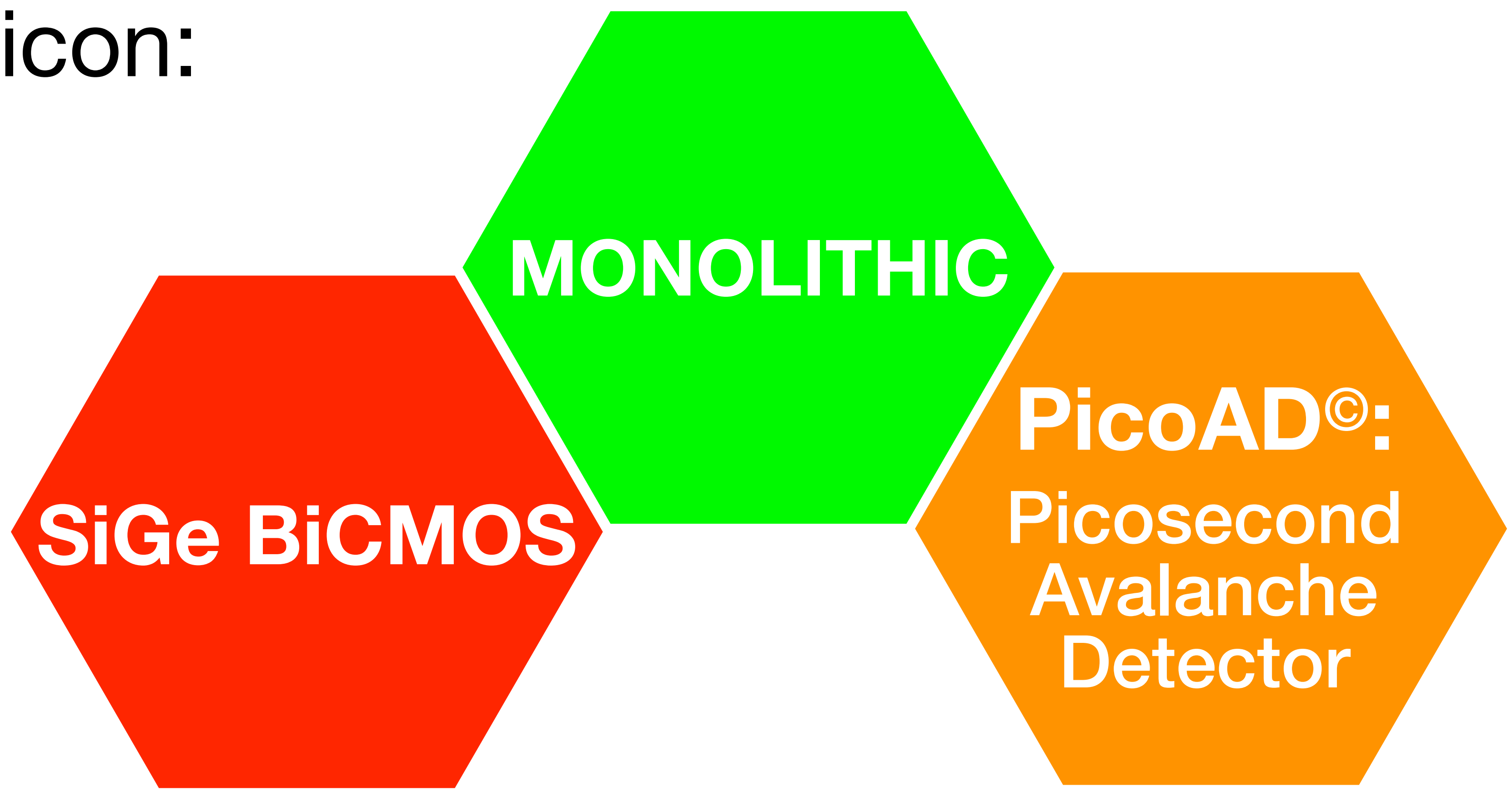
European Research Council
Established by the European Commission

MONOLITH

The MONOLITH Project

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

Our recipe for picosecond timing with silicon:



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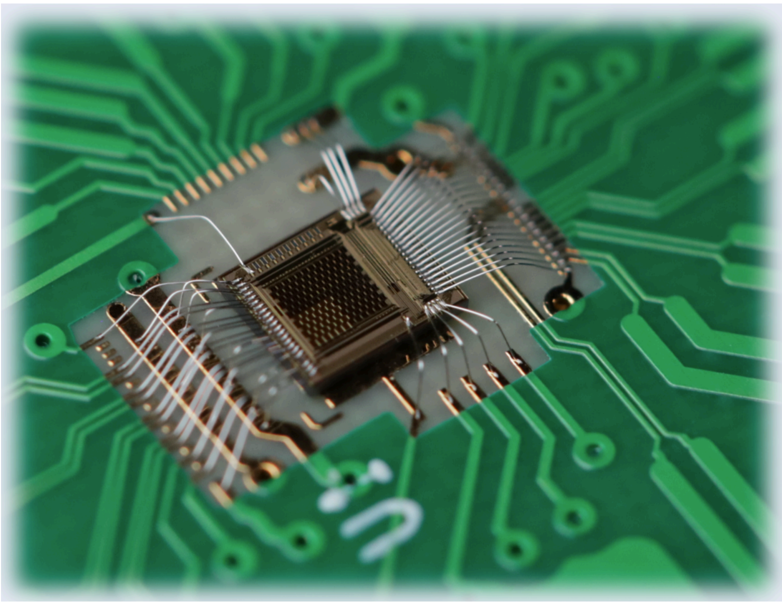
Today I will show the results obtained with:

1. the **2022 prototype WITHOUT GAIN LAYER** with improved SiGe electronics, and the effects of proton irradiation up to **1×10^{16} 1MeV n_{eq}/cm^2**
   ➡ PicoAD version back from foundry in December
2. the **PicoAD proof-of-concept**, produced on SiGe electronics of 2020 prototype

All ASICs were produced in the 130nm SiGe BiCMOS SG13G2 process by

innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

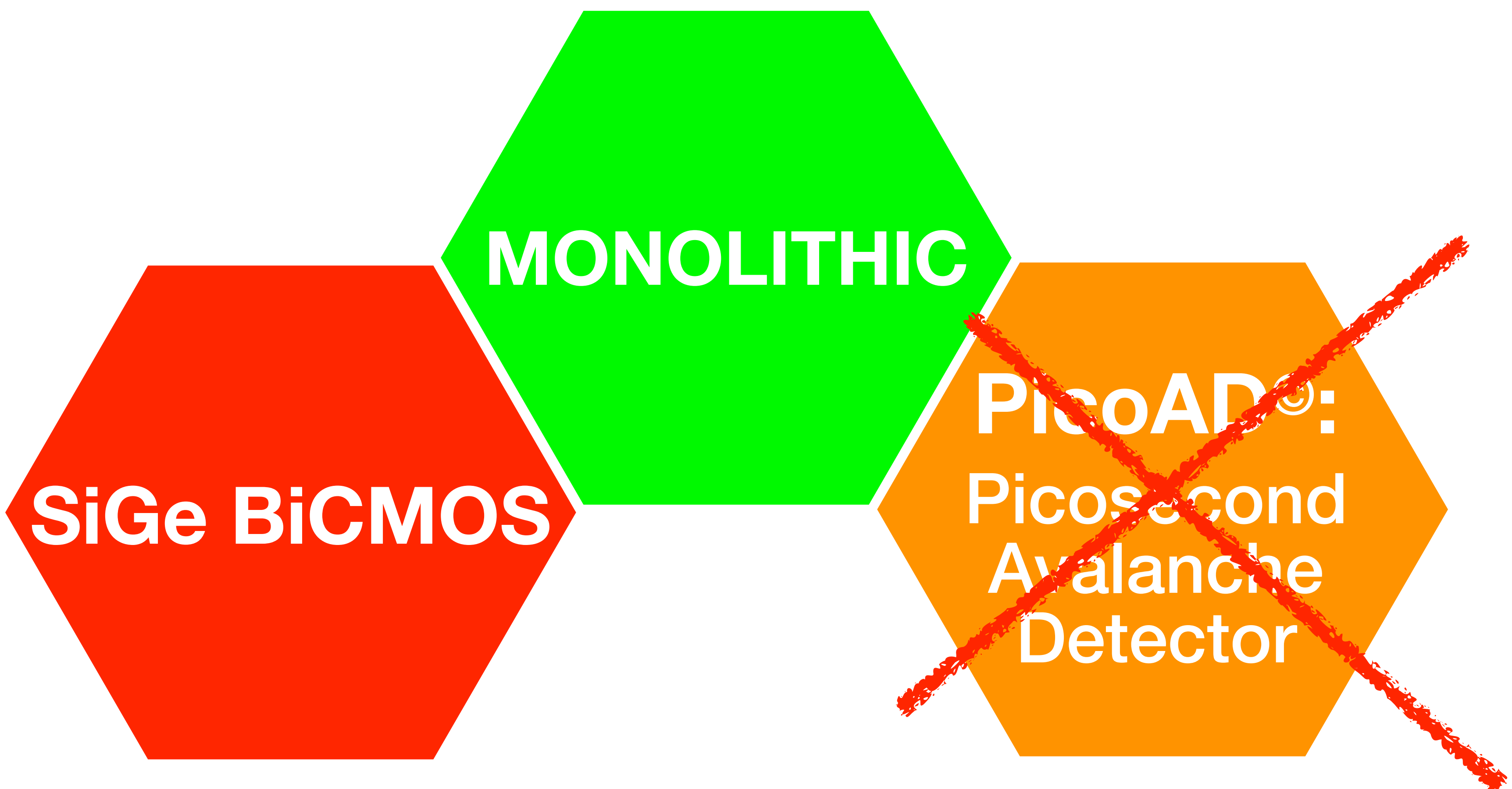
erc
European Research Council
Established by the European Commission



MONOLITH

2022 prototype

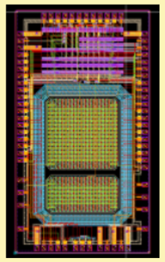
no gain layer



MONOLITH Project prototypes

Monolithic prototypes in SiGe BiCMOS (without internal gain layer)

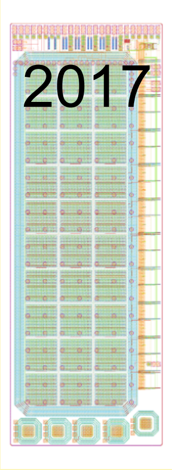
2016



200ps

- 1 mm² pixel
- Discriminator

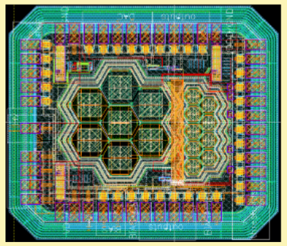
2017



110ps

- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

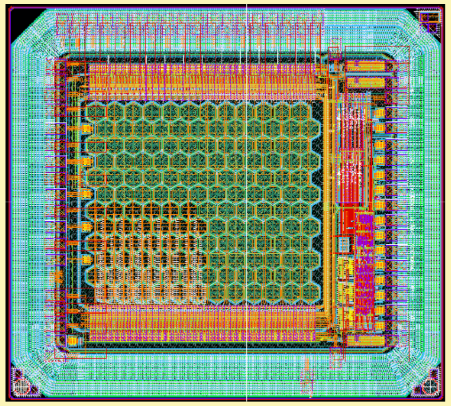
2018



50ps

- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

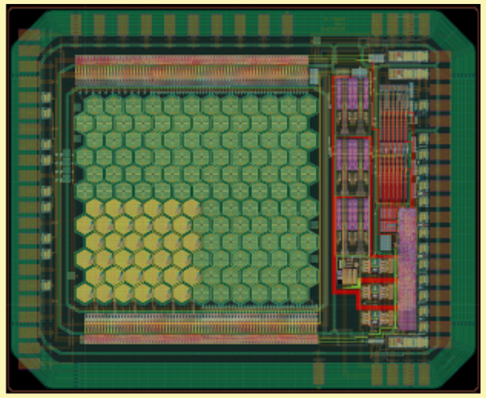
MONOLITH prototype 1
2020



36 ps

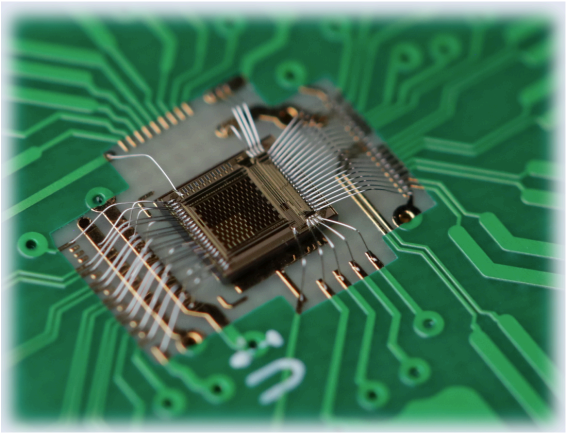
- Hexagonal pixels 100μm pitch
- 30ps TDC + I/O logic
- 4 analog channels

MONOLITH prototype 2
2022

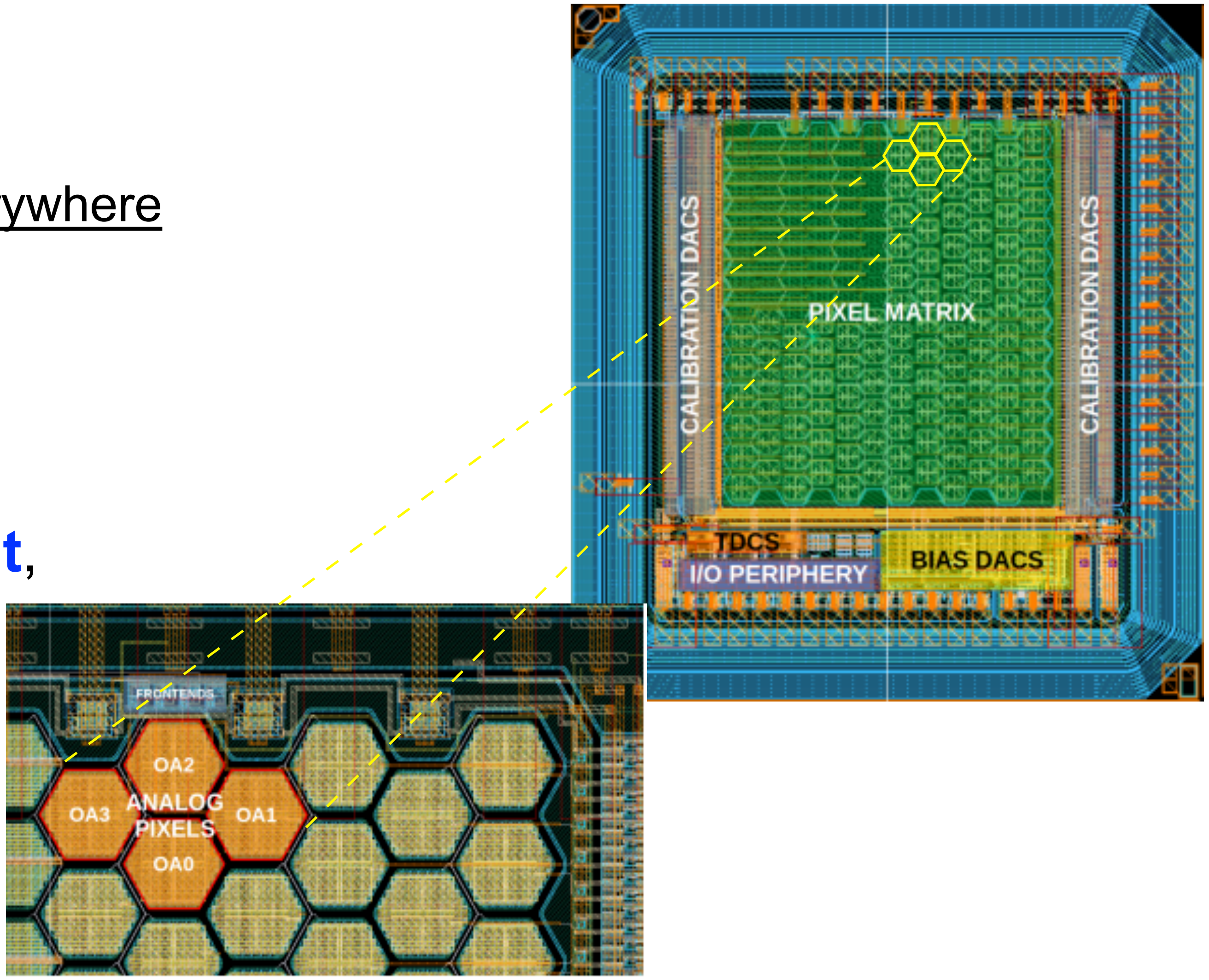


- Matrix of 12x12 hexagonal pixels
- 100μm pitch
- improved electronics
- 50μm epitaxial layer (350Ωcm)

evolution of 2020 prototype

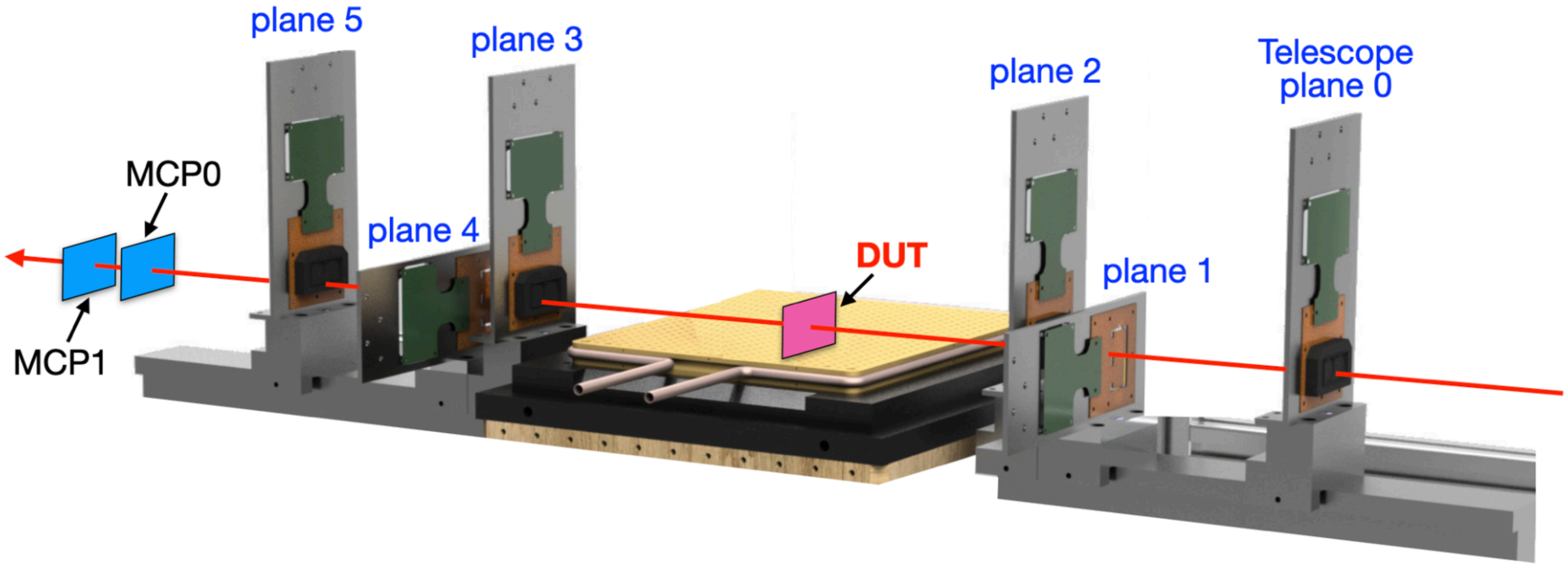


- Same matrix configuration as prototype1, but
  - **Substrate**: 50Ωcm → 350Ωcm epilayer, 50μm thick on low-res (1Ωcm)
    - ➡ smaller pixel capacitance
    - ➡ depletion 23μm → 50μm
    - ➡ larger voltage plateau
    - ➡ can operate sensor with v_{drift} saturated everywhere
  - **Preamp and driver** voltage decoupled
    - ➡ was limiting optimal amplifier operation
    - ➡ was creating cross-talk, removed
  - **Optimised FE layout**, **differential output**,
    - ➡ high-frequency cables
    - ➡ better rise time (600ps → 300ps)



Test Beam: Experimental Setup

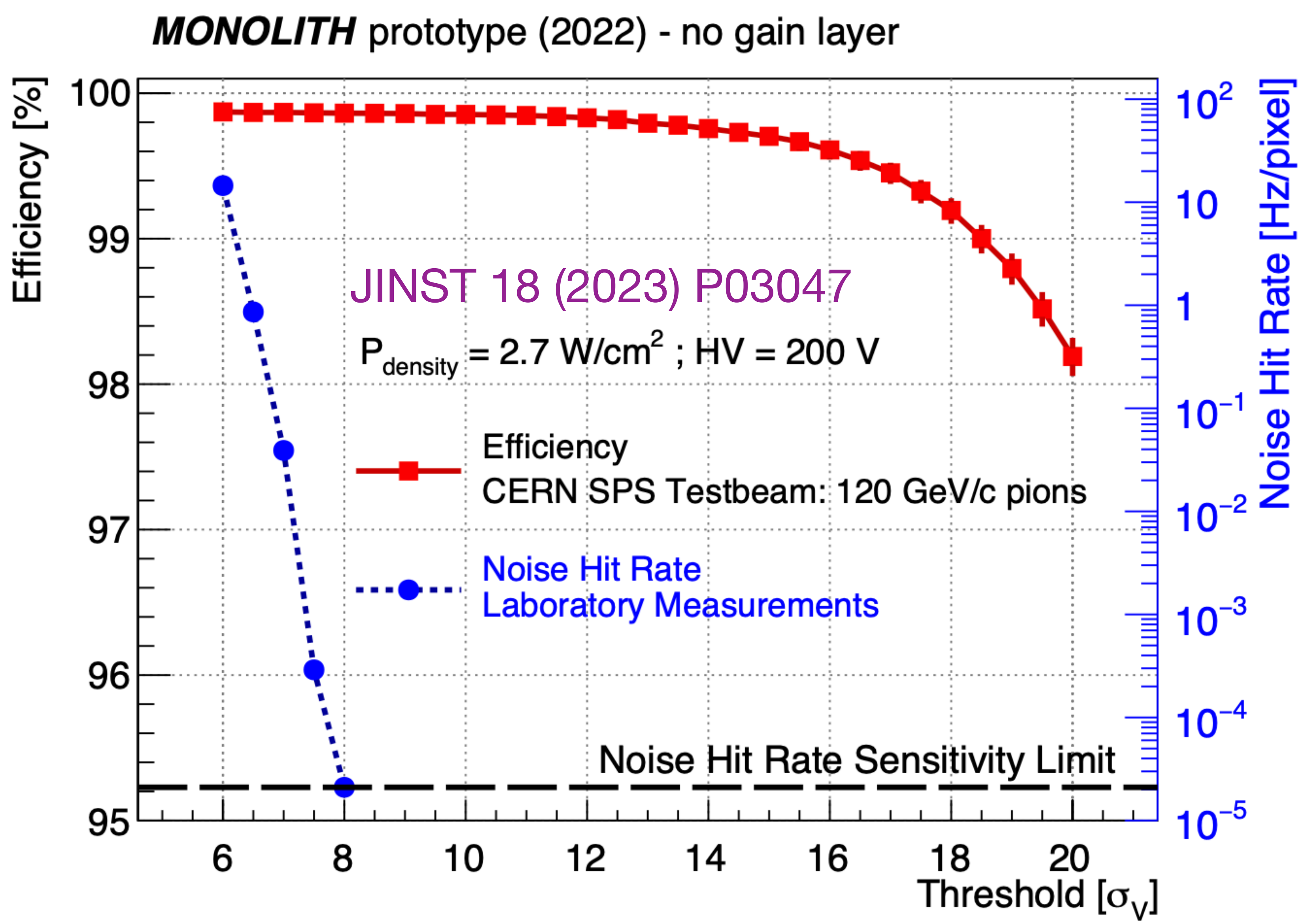
Mid October SPS testbeam with 120 GeV/c π to measure **efficiency** and **time resolution**



UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10\ \mu m$)

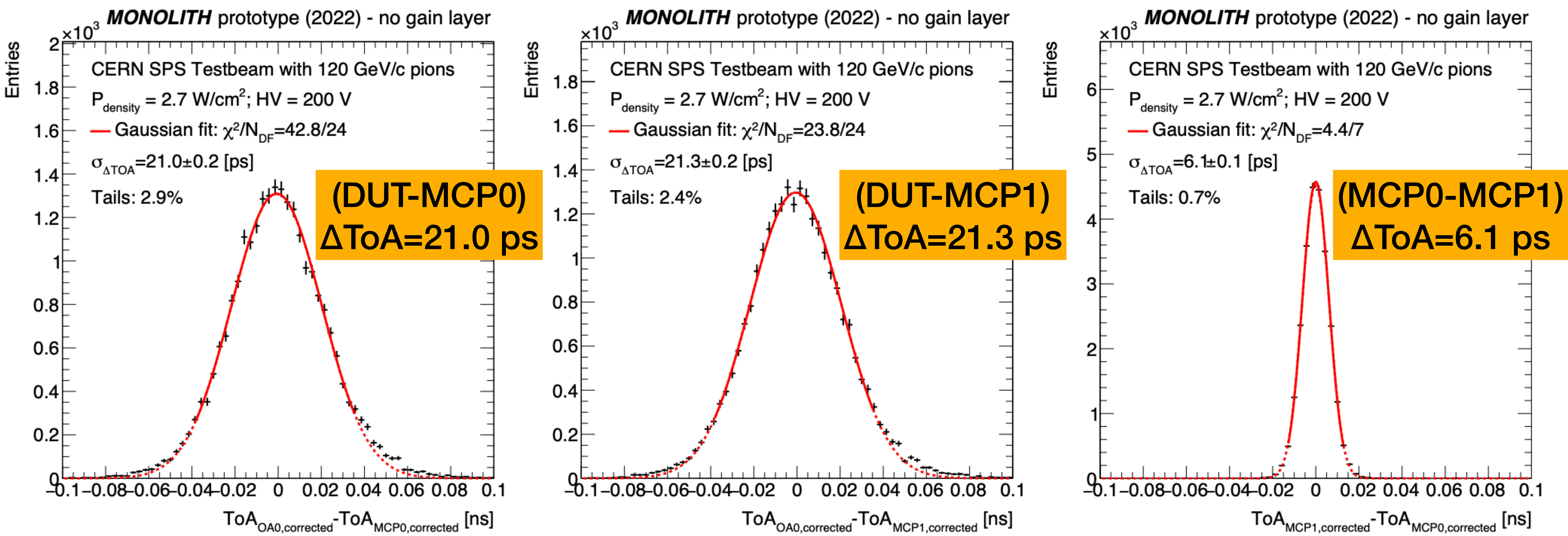
Two MCPs ($\sigma_t \approx 5$ ps) to provide the timing reference

Lots of data taken: results in **JINST 18**



Large efficiency plateau at ≈ **99.8%**,
that allows operation at very low noise-hit rate

prototype2 (2022) — no gain layer

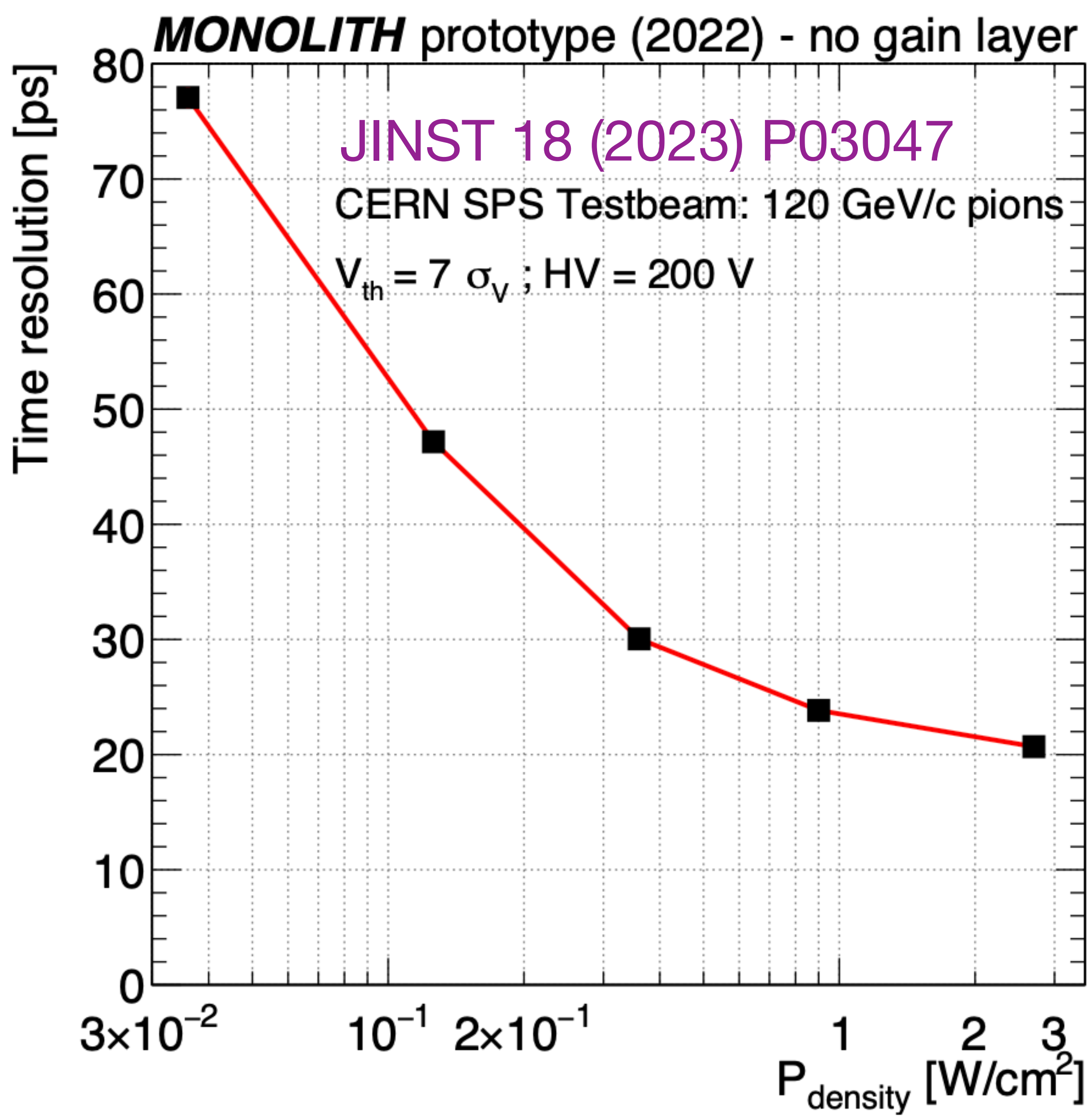


- Simultaneous fit to extract time resolutions of the DUT, MCP0, MCP1:

Fit results: MCP0 σ_T = (3.6 ± 1.5) ps
MCP1 σ_T = (5.0 ± 1.1) ps

σ_T = (20.7 ± 0.3) ps

non-Gaussian tails ≈ **3%**

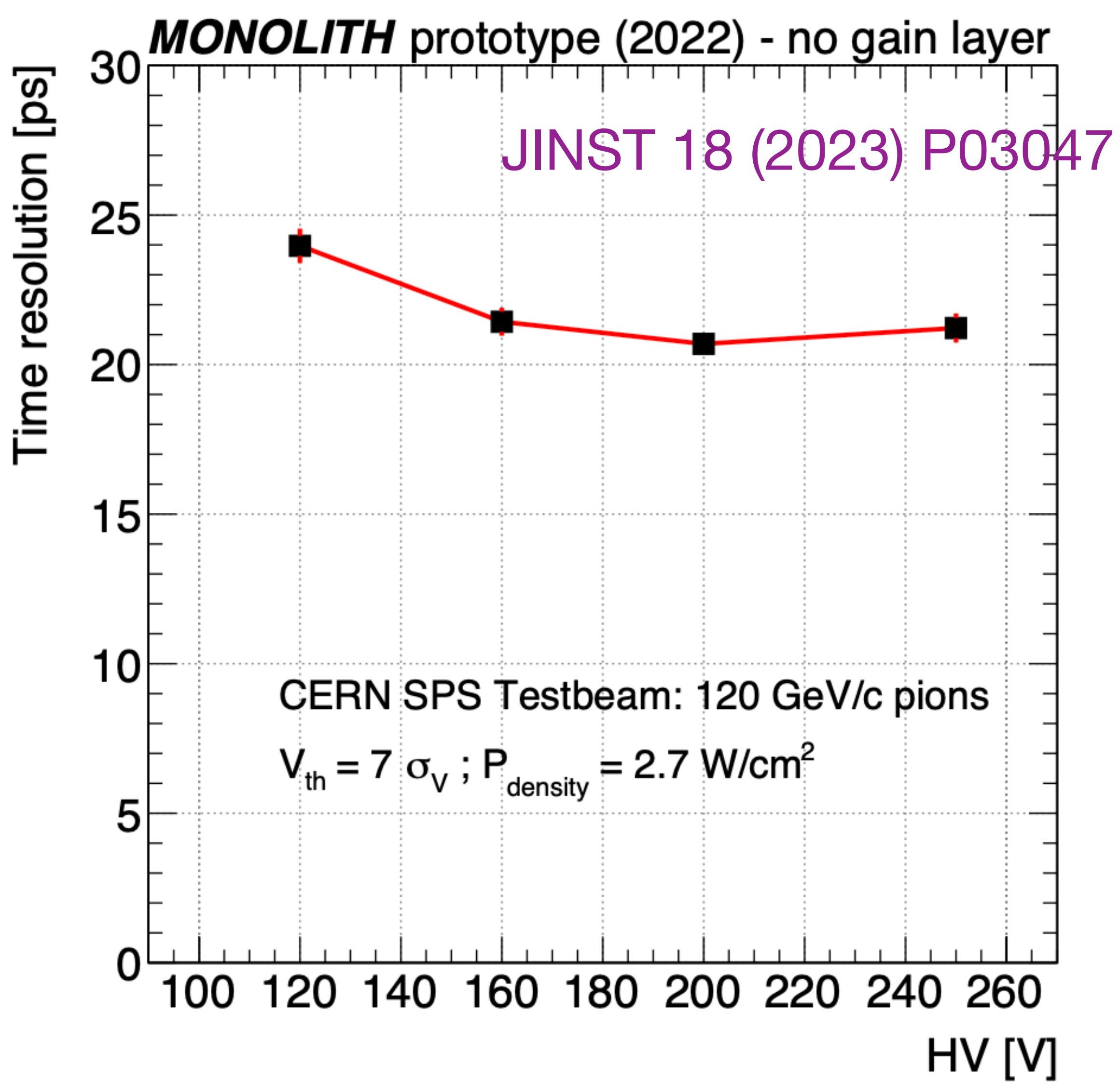


DUT operated at HV = 200 V and $V_{th} = 7\sigma_V$		
$P_{density}$ [W/cm^2]	Amplitude MPV [mV]	Time Resolution [ps]
2.7	48.6 ± 0.5	20.7 ± 0.3
0.9	35.8 ± 0.5	23.8 ± 0.3
0.36	22.6 ± 0.4	30.1 ± 0.4
0.13	14.2 ± 0.3	47.2 ± 0.7
0.04	16.2 ± 0.3	77.1 ± 0.9

20 ps at 2.7 W/cm²
50 ps at 0.1 W/cm²

Without gain layer.

prototype2 (2022) — no gain layer



Plateau of 100V with time resolution of **≈ 20 ps**

Without gain layer

Results obtained with simple analysis and simple signal processing

Time resolution measurements

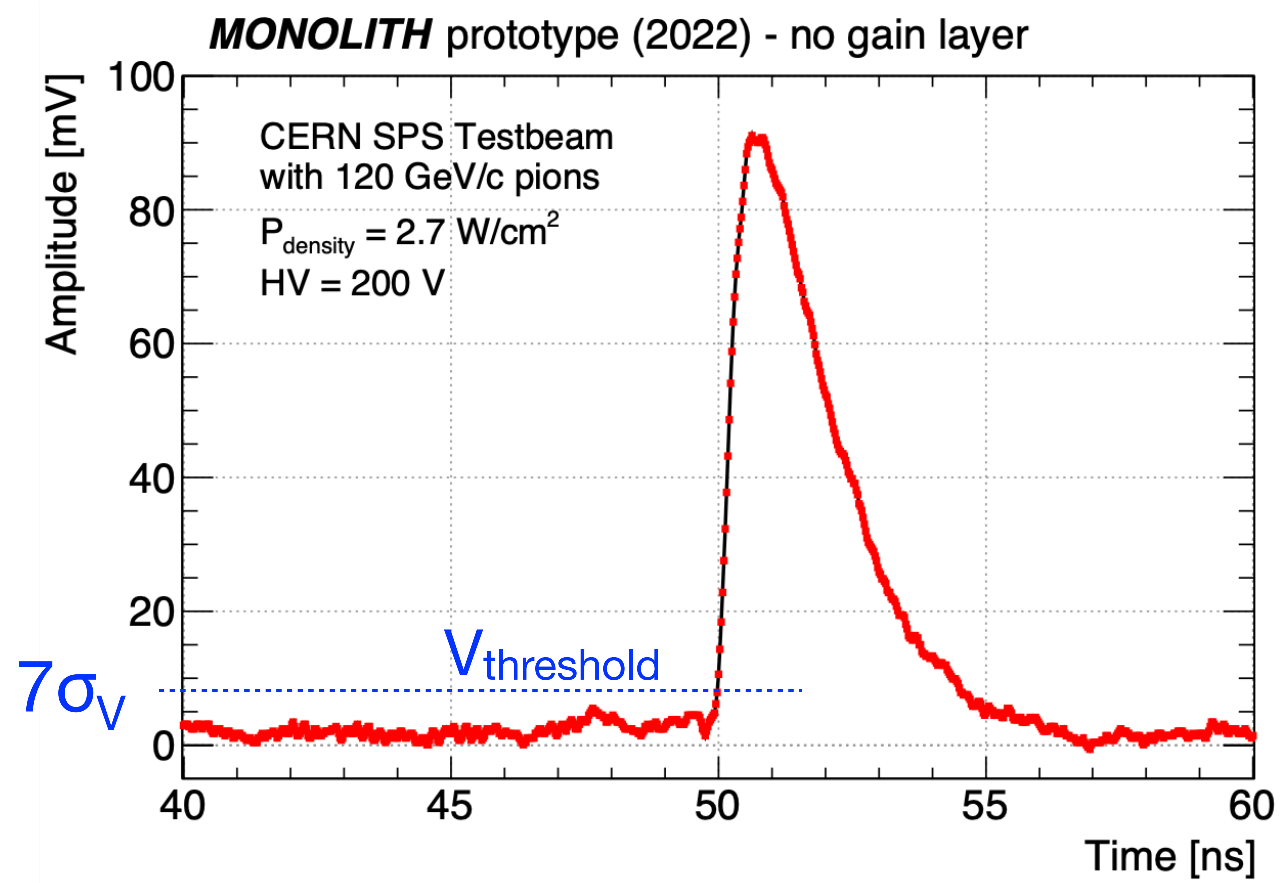
Remark :

20.7 ps obtained with very simple analysis:

- **Linear interpolation** of oscilloscope samplings (25ps)
- Time Of Arrival (ToA): time at

  $V_{threshold} = 7\sigma_V$

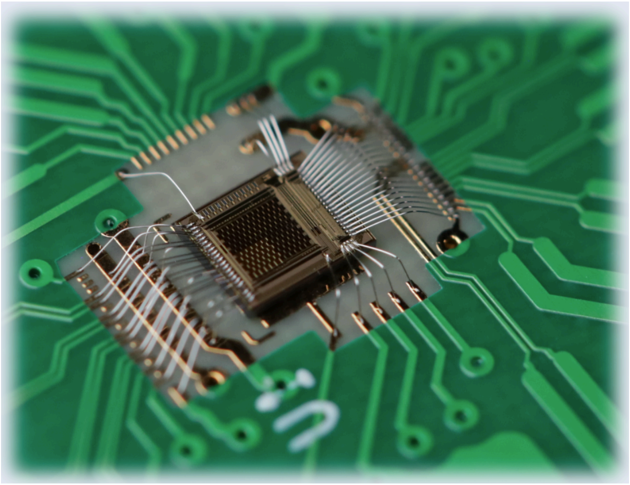
- Δ_{ToA} distributions are **time-walk corrected**



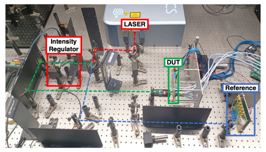
More complex analysis (spline interpolation, filtering, …) reaches **17.7 ps**

Laser measurements

with the 2022 prototype2 without gain

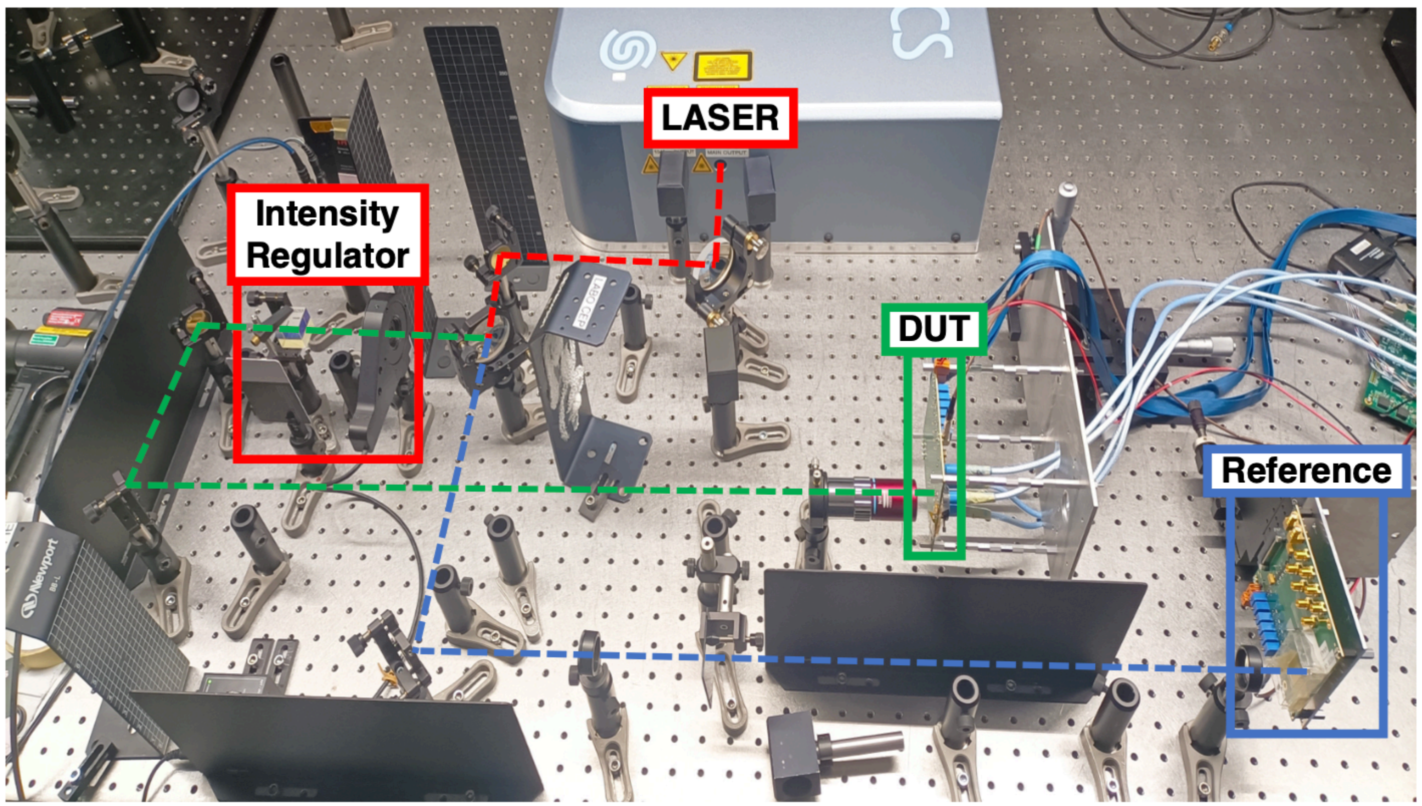


prototype2 (2022) — no gain layer

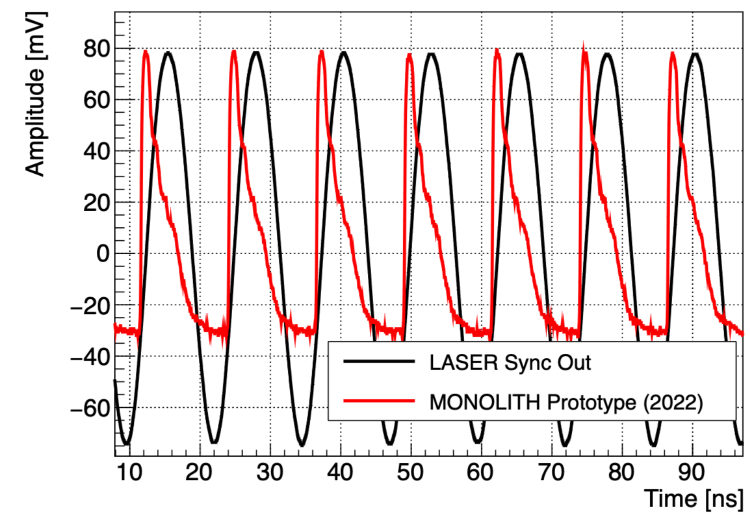


Laser Measurement

Measurement with a **laser** with a jitter of **100 fs** (repetition frequency = **80 MHz**)



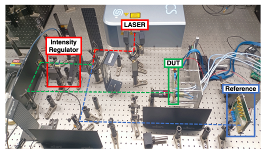
Many thanks to
L. Bonacina's lab of GAP UNIGE



Time coincidence between two of our samples:

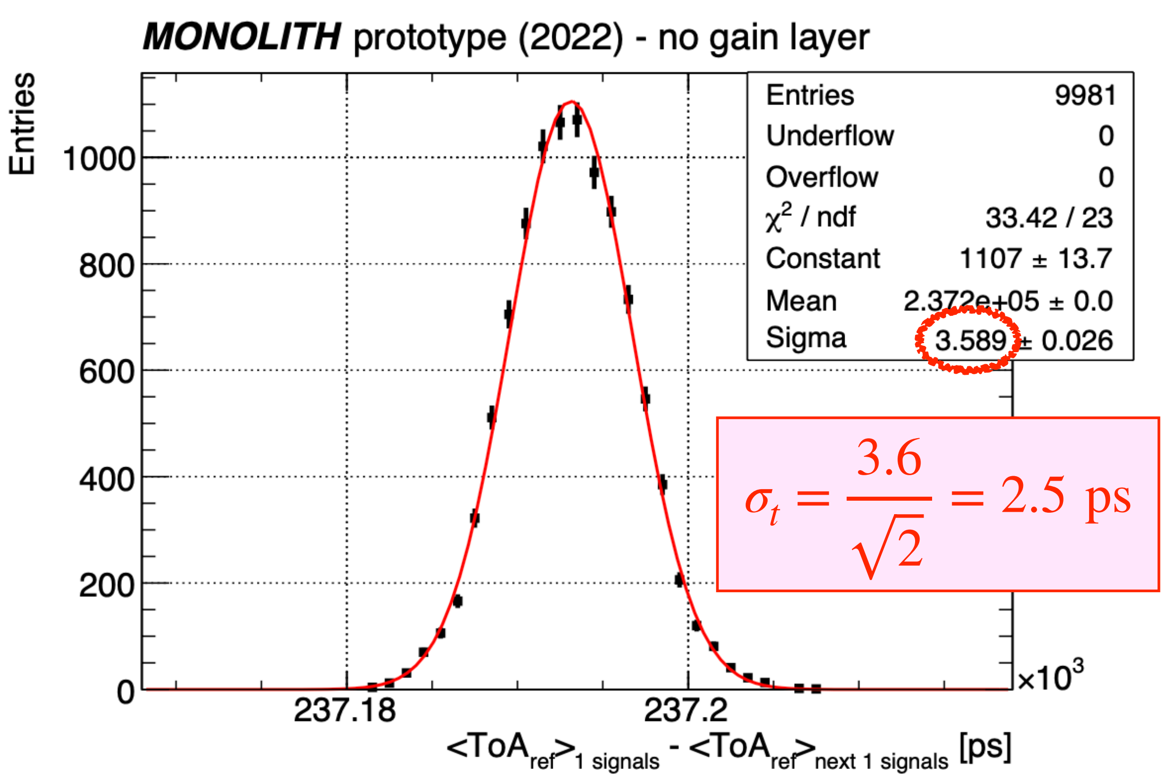
➡ "**Reference**" receiving always large laser pulse producing 17k electrons (σ_t = 2.5 ps)

➡ "**DUT**" receiving variable laser power, to study the performance vs. amplitude



Laser Measurement

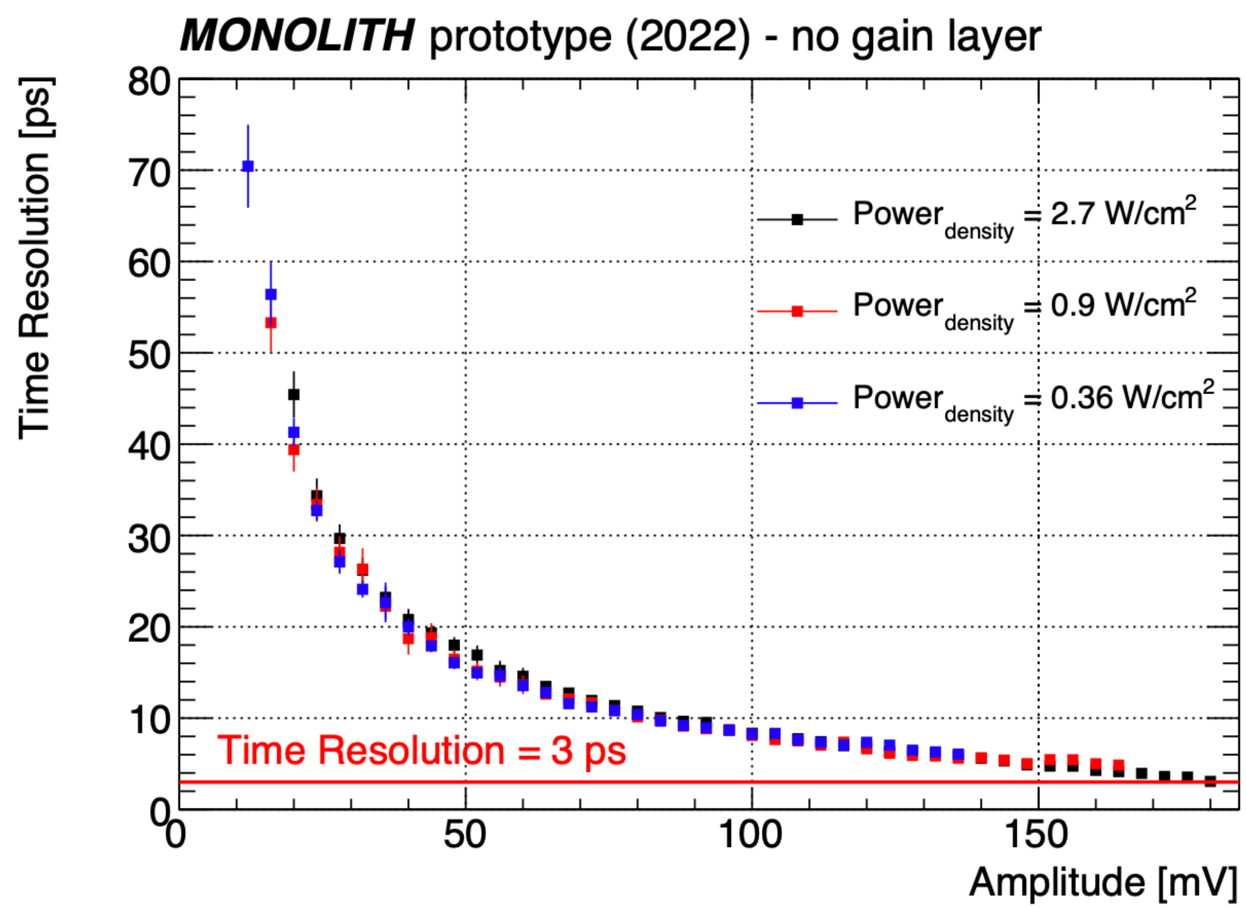
Laser Measurement



Our prototype "**Reference**":

Time resolution = 2.5 ps

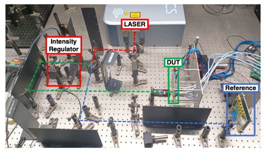
with **17k e⁻** (5—6 mips)



Our prototype "**DUT**":

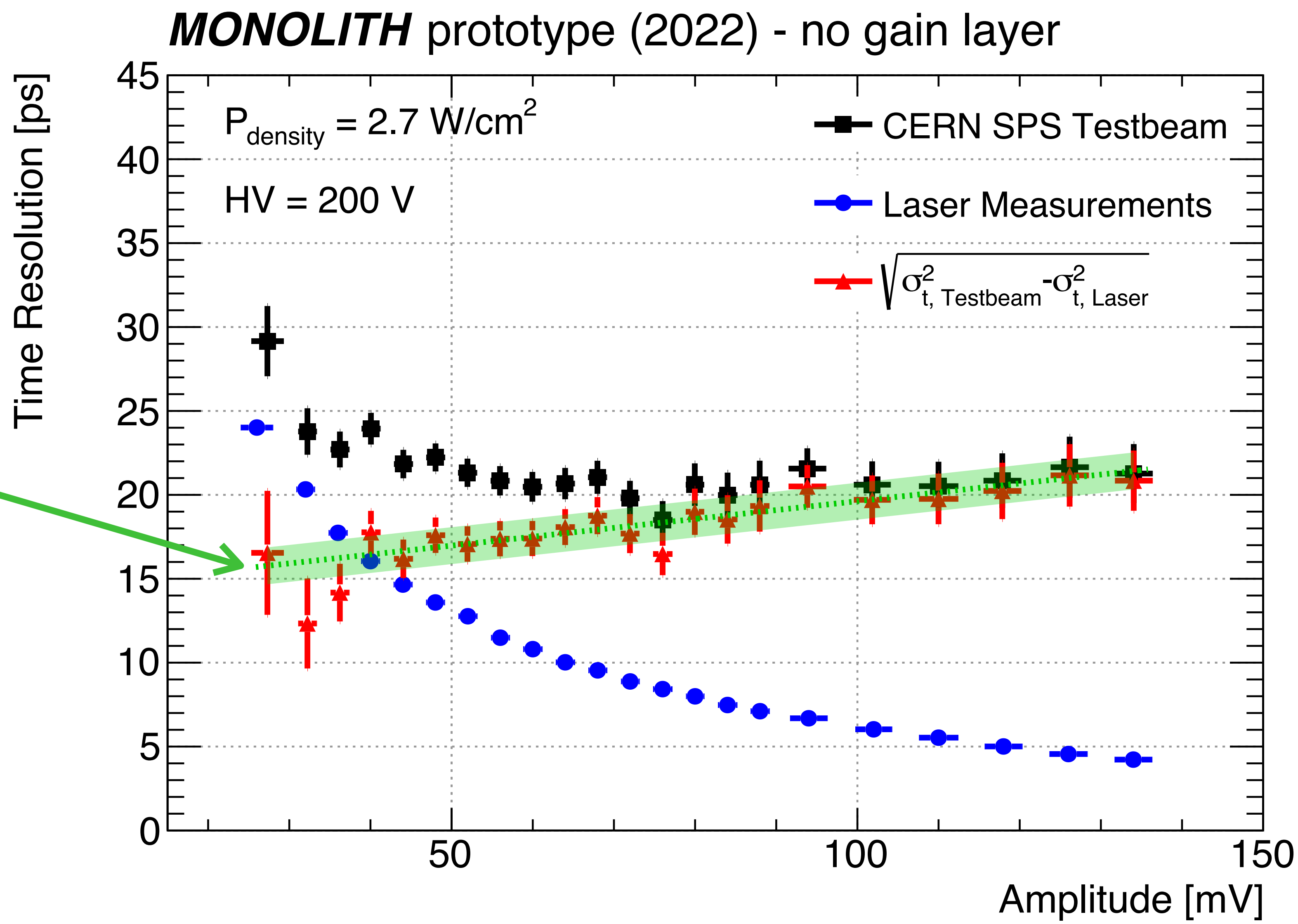
with **max 11k e⁻** (≈4 mips)

prototype2 (2022) — no gain layer



Laser Measurement

Laser Measurement



Estimate of the charge-collection (“Landau”) noise

Radiation hardness studies

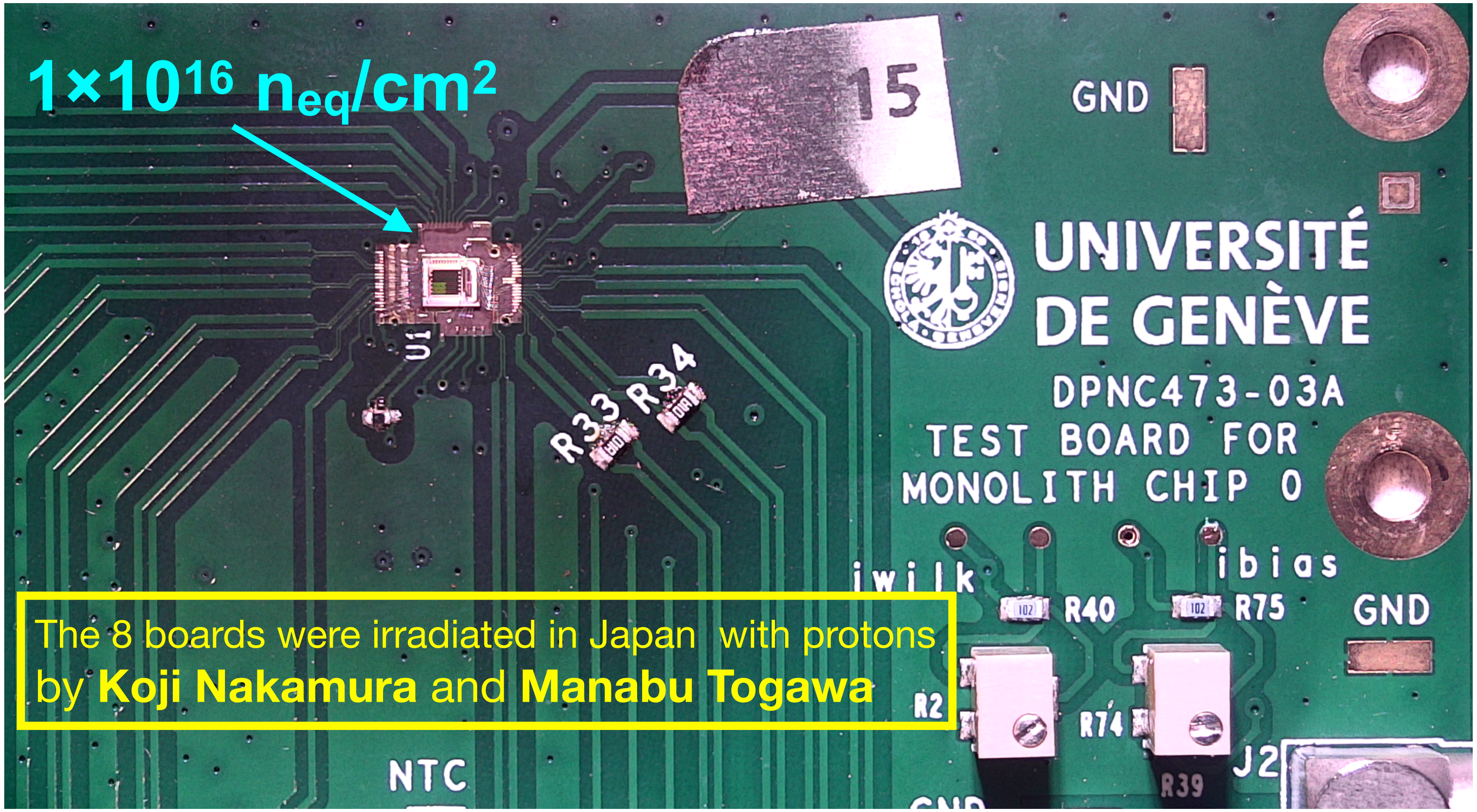
with the 2022 prototype2 <u>without gain</u>

Total of 40 analog pixels studied

Radiation hardness of SiGe HBTs

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.

8 samples of prototype2 ASIC were irradiated in Japan up to $1\times10^{16}\ n_{eq}/cm^2$.



https://arxiv.org/abs/2310.19398

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.

8 samples of prototype2 ASIC were irradiated in Japan up to 1×10^{16} n_{eq}/cm^2.

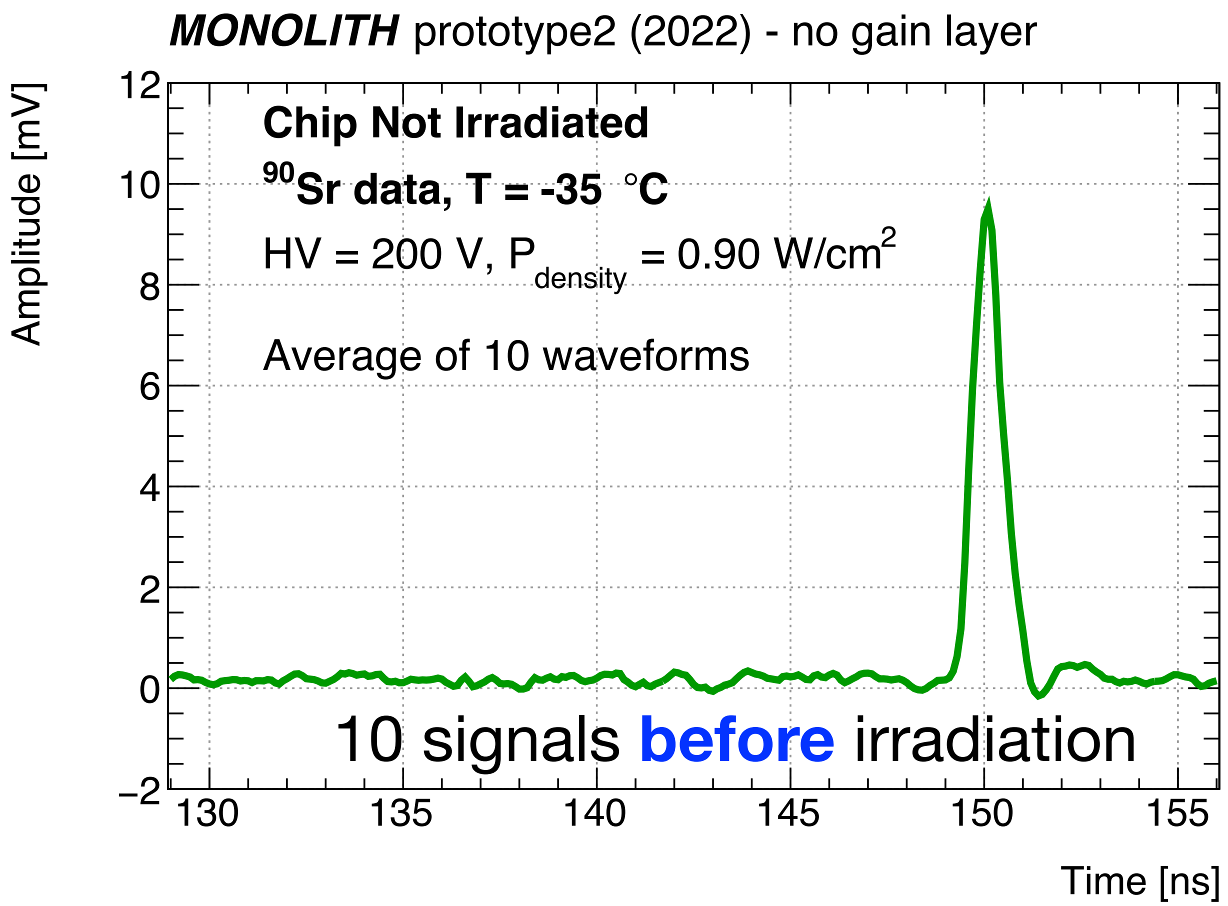
7 out of the 8 irradiated boards had **damaged voltage regulators**: **bypassed** with wire bonds

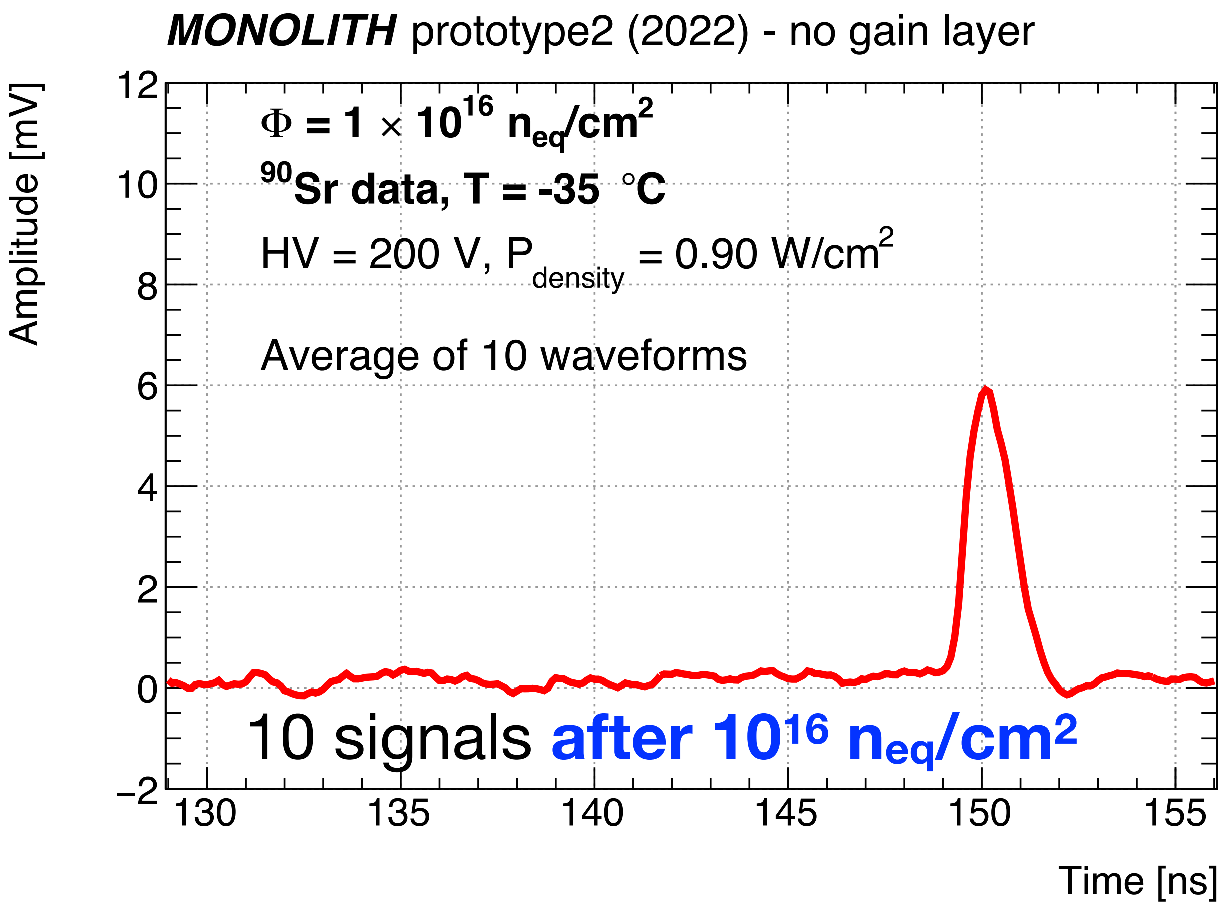
One board **not configurable** : short on the digital logic. Not used

Three unirradiated boards. (one is the same of the CERN testbeam, results published in JINST 18 (2023) P03047)

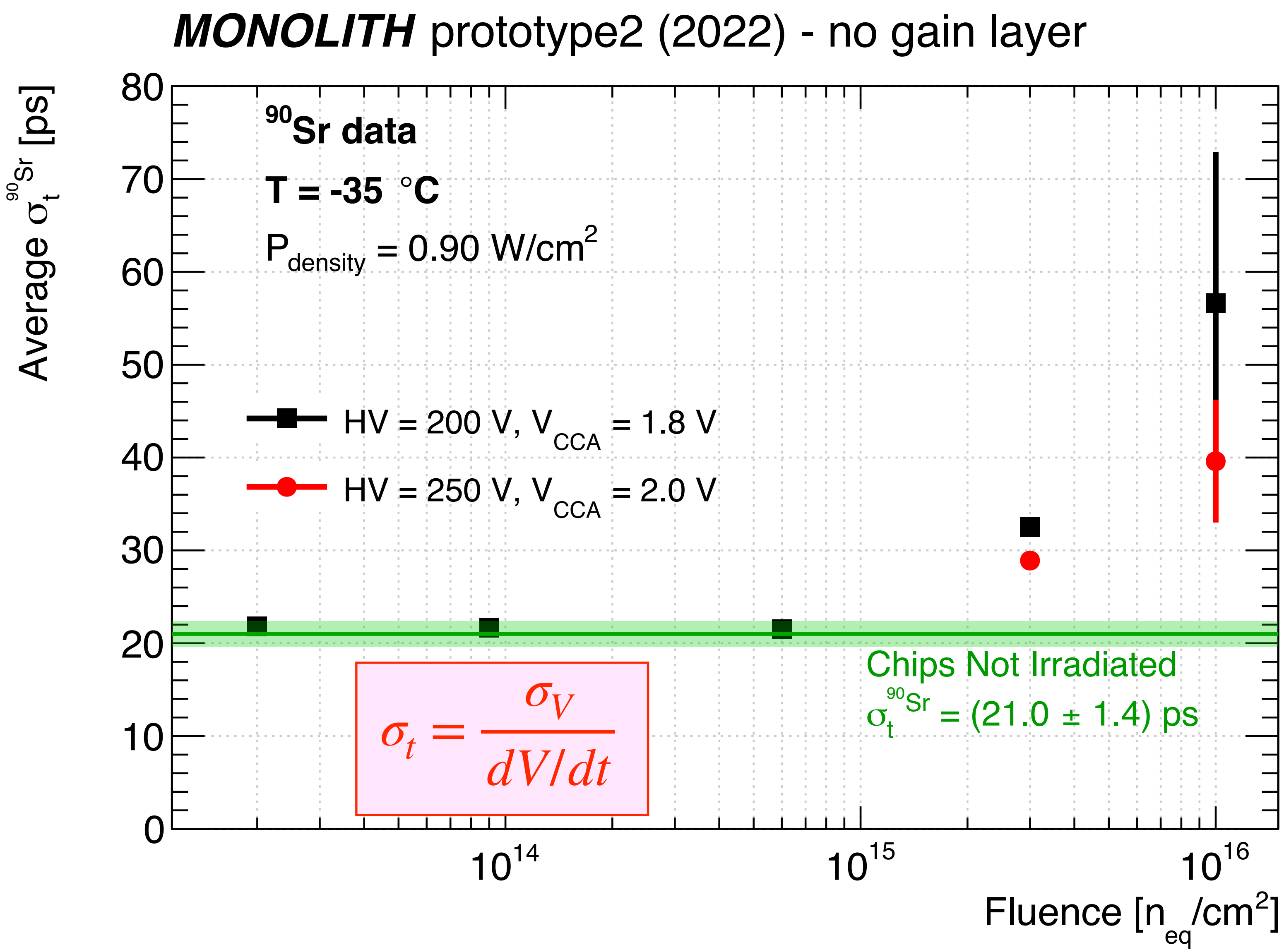
Board Name	Fluence [1 MeV n_{eq}/cm^2]
M23	$2 \cdot 10^{13}$
M22	$9 \cdot 10^{13}$
M21	$6 \cdot 10^{14}$
M19	$6 \cdot 10^{14}$
M18	$3 \cdot 10^{15}$
M17	$3 \cdot 10^{15}$
M16	$1 \cdot 10^{16}$
M15	$1 \cdot 10^{16}$
M06	not irradiated – for comparison
M05	not irradiated – for comparison
M07	not irradiated – for comparison

Very good news:
even after 1×10^{16} n_{eq}/cm^2 the ASICs work !!!
although signals are clearly degraded





Radiation hardness of SiGe HBTs



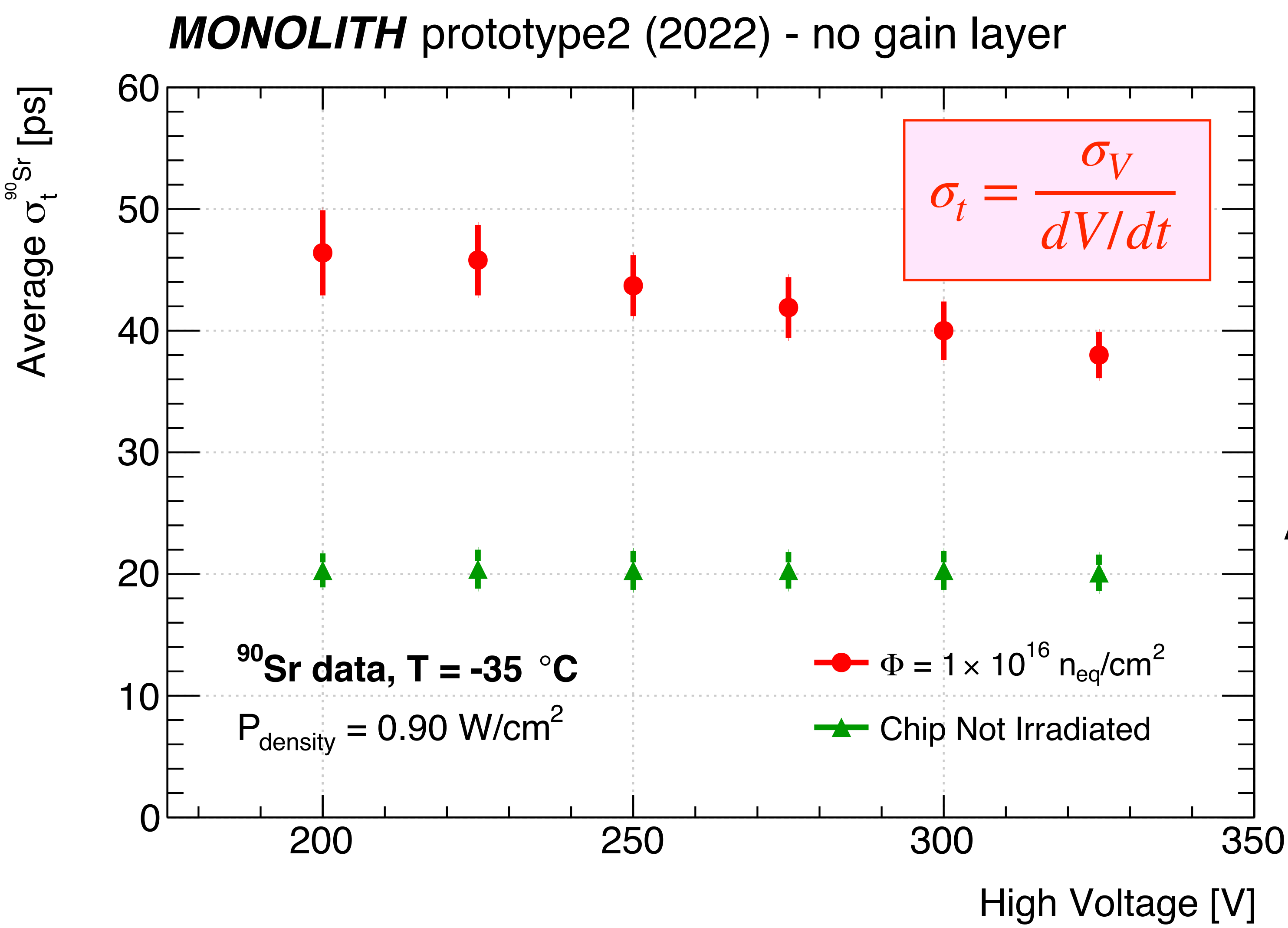
Excellent news from radiation tolerance studies:

The time jitter with **^{90}Sr** increases **from 21ps** (unirradiated) **to 40ps** (at 10^{16} n_{eq}/cm^2) at **HV = 250V** and **0.9 W/cm^2**

Total of **40 pixels studied** with **^{90}Sr**, at different proton fluence.
At a given proton fluence,
pixel-to-pixel **time jitter variations within 20%**.
(quoted uncertainties on the averages are the standard deviations)

Fluence [n_{eq}/cm^2]	σ_t^{90Sr} [ps] pixel 1	pixel 2	pixel 3	pixel 4	Average σ_t^{90Sr} [ps]
HV = 200 V, V_{CCA} = 1.8 V					
0	22.1	20.5	18.8	19.9	21.0 ± 1.4
	22.1	22.7	19.5	19.6	
	22.9	22.2	21.1	20.7	
2×10^{13}	21.4	22.2	21.2	22.4	21.8 ± 0.6
9×10^{13}	21.4	22.5	21.0	21.8	21.7 ± 0.6
6×10^{14}	21.5	22.4	20.2	20.9	21.5 ± 0.8
	20.7	22.3	22.6	21.3	
3×10^{15}	32.7	33.2	31.4	32.8	32.5 ± 0.8
1×10^{16}	43.3	50.9	44.0	47.5	56.6 ± 16.3
	84.9	79.6	48.9	53.7	
HV = 250 V, V_{CCA} = 2.0 V					
3×10^{15}	28.7	29.0	28.5	29.5	28.9 ± 0.4
1×10^{16}	33.2	36.2	35.5	33.6	39.6 ± 6.6
	51.4	46.9	38.4	41.7	

Depletion voltage has changed



Rate measurements with ^{109}Cd source show that after 1×10^{16} n_{eq}/cm^2 the sensor is not fully depleted at HV = 200 V

At 0.9 W/cm^2 the time jitter with ^{90}Sr at $\Phi = 1 \times 10^{16}$ n_{eq}/cm^2 decreases **from 46ps** at HV = 200 V **to 40ps** at HV = 325 V

Radiation hardness of SiGe HBTs

Very preliminary

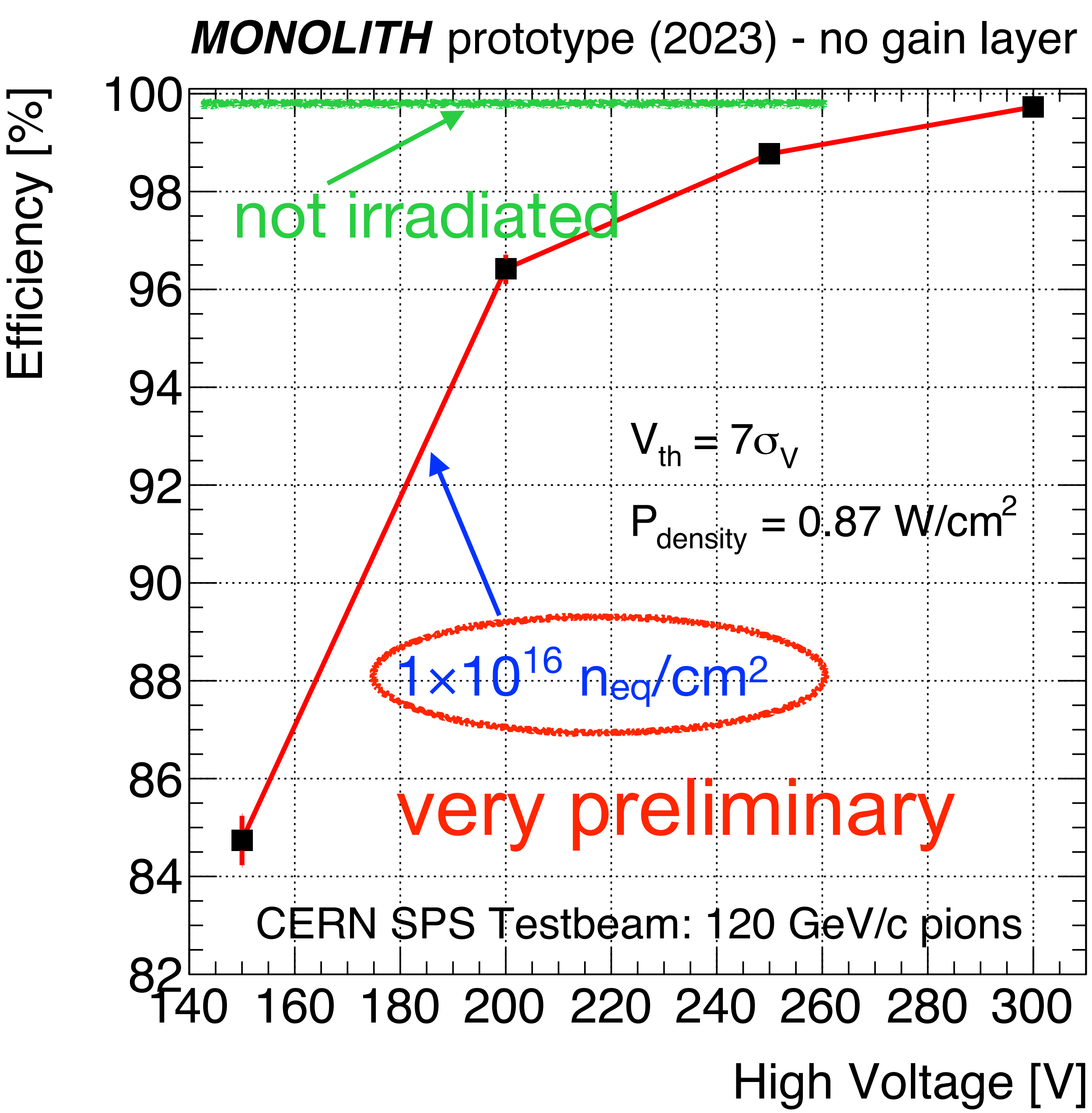
August 2023 testbeam at CERN SPS

Board irradiated 1×10^{16} n_{eq}/cm^2
:

efficiency still ≳ 99%

for HV ≳ 250 V

at 0.9 W/cm²



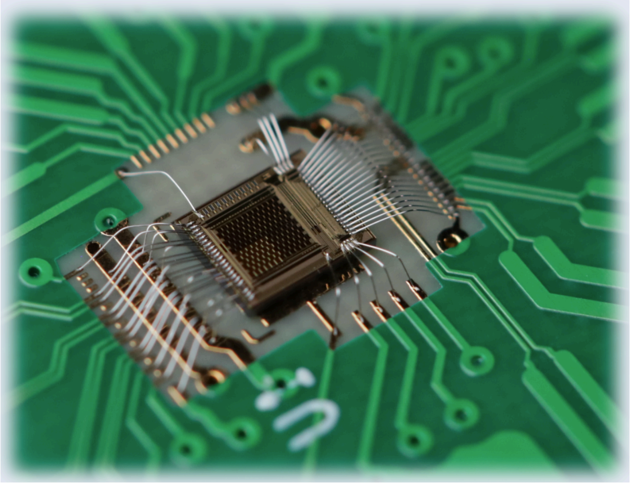
Summary

A monolithic prototype ASIC without gain produced in SiGe BiCMOS provided:

- **Efficiency of 99.8%** and **time resolution of 21 ps**
- **Laser** measurement: down to 2.5 ps.

After proton fluence of **10^{16} 1MeV n_{eq}/cm^2** :

- Increasing HV from 200 V to 325 V gives
  Efficiency up to 99.7 % and **time resolution of 40 ps**



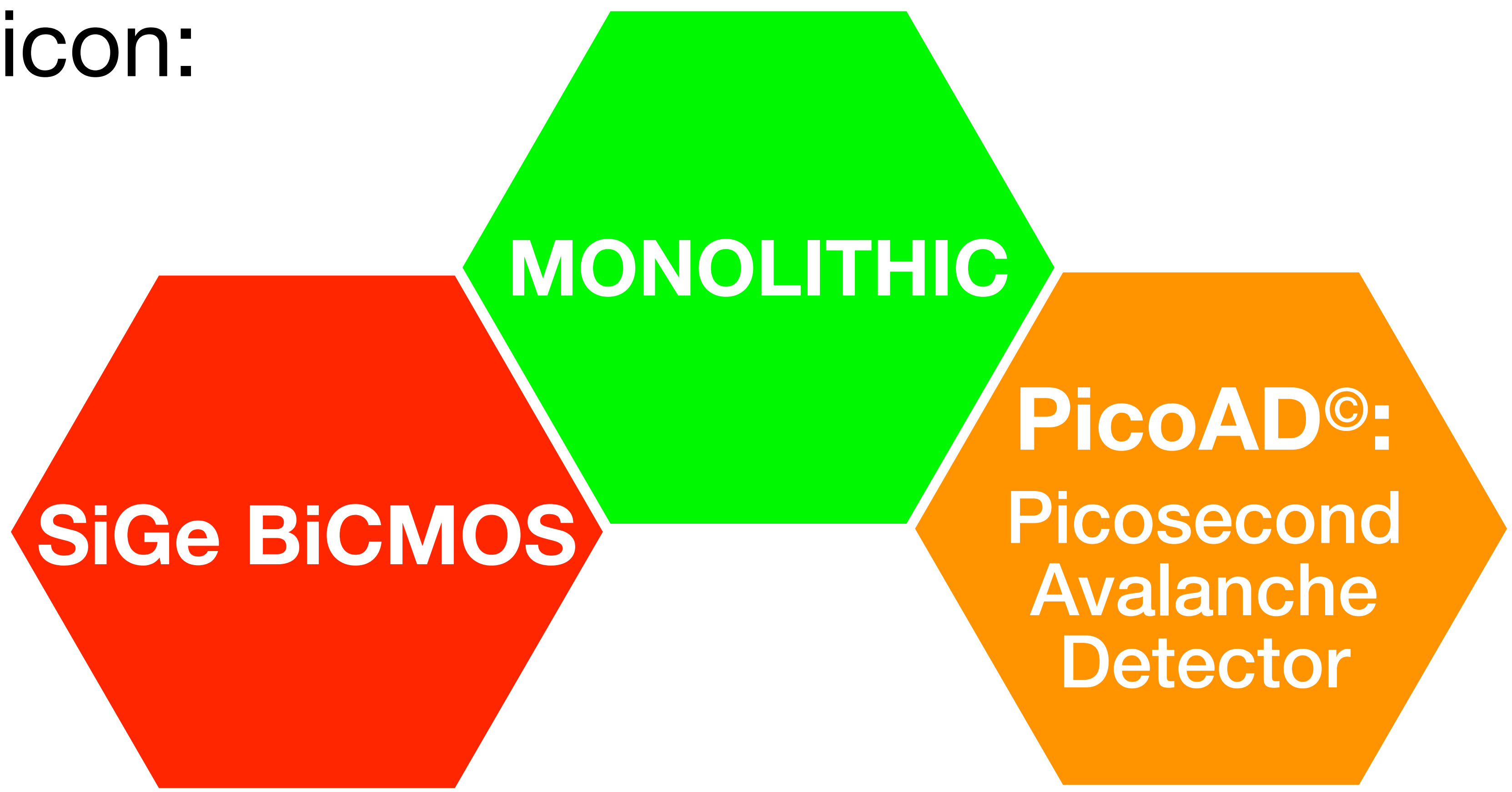
This performance was obtained **without gain layer**

SiGe BiCMOS is a serious candidate for future 4D trackers (and much more)

The MONOLITH Project

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

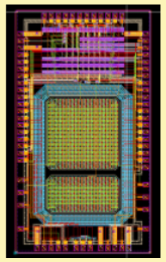
Our recipe for picosecond timing with silicon:



MONOLITH Project prototypes

Monolithic prototypes in SiGe BiCMOS (without internal gain layer)

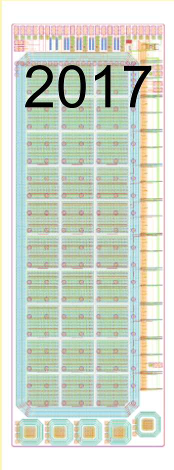
2016



200ps

- 1 mm² pixel
- Discriminator

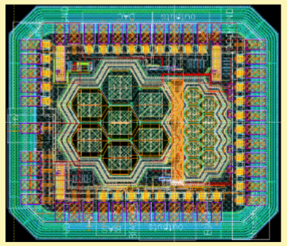
2017



110ps

- 30 pixels 500x500µm²
- 100ps TDC +I/O logic

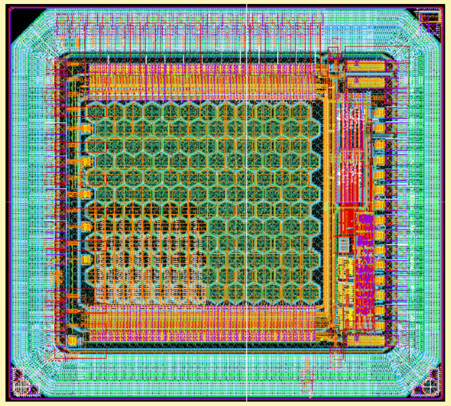
2018



50ps

- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

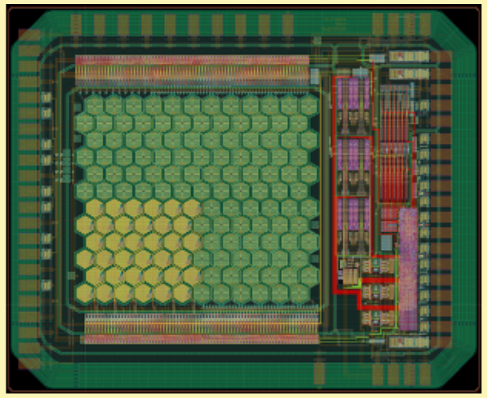
MONOLITH prototype 1
2020



36 ps

- Hexagonal pixels 100µm pitch
- 30ps TDC + I/O logic
- 4 analog channels

MONOLITH prototype 2
2022



- Matrix of 12x12 hexagonal pixels
- 100µm pitch
- improved electronics
- 50µm epitaxial layer (350Ωcm)

In 2022 : **proof-of-concept** monolithic prototype **with internal gain layer**

(using 2020 masks)

PicoAD

special wafers
produced internally by IHP
(not optimised yet)

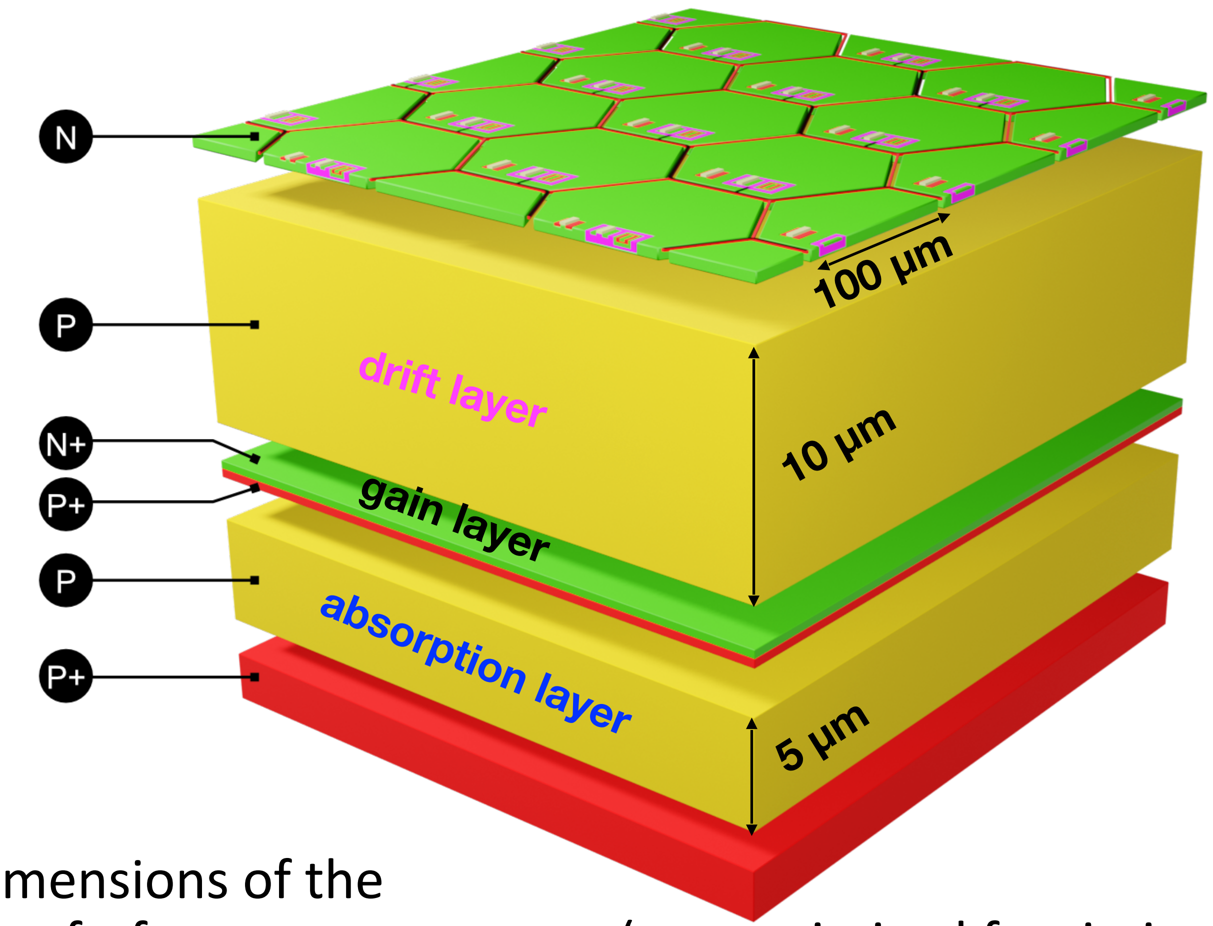
PicoAD:

© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector;
European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

Multi-Junction Picosecond-Avalanche Detector©
with continuous and deep gain layer:

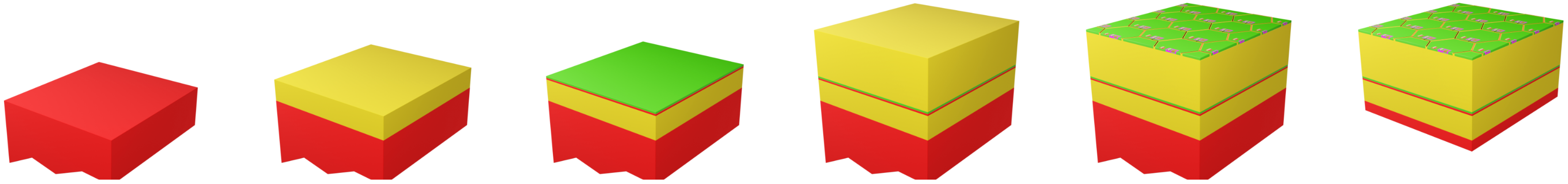
- De-correlation from implant size/geometry
  ➙ **high pixel granularity and full fill factor**
  (high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
  ➙ **reduced charge-collection (Landau) noise**
  (enhance timing resolution)

- L. Paolozzi et al. 2022 *JINST* **17** P10032 [arXiv:2206.07952].
- G. Iacobucci et al., 2022 *JINST* **17** P10040 [arXiv:2208.11019].



Dimensions of the
proof-of-concept prototype (not optimised for timing)

Wafer-production procedure:



Step 1 Step 2 Step 3 Step 4 Step 5 Step 6

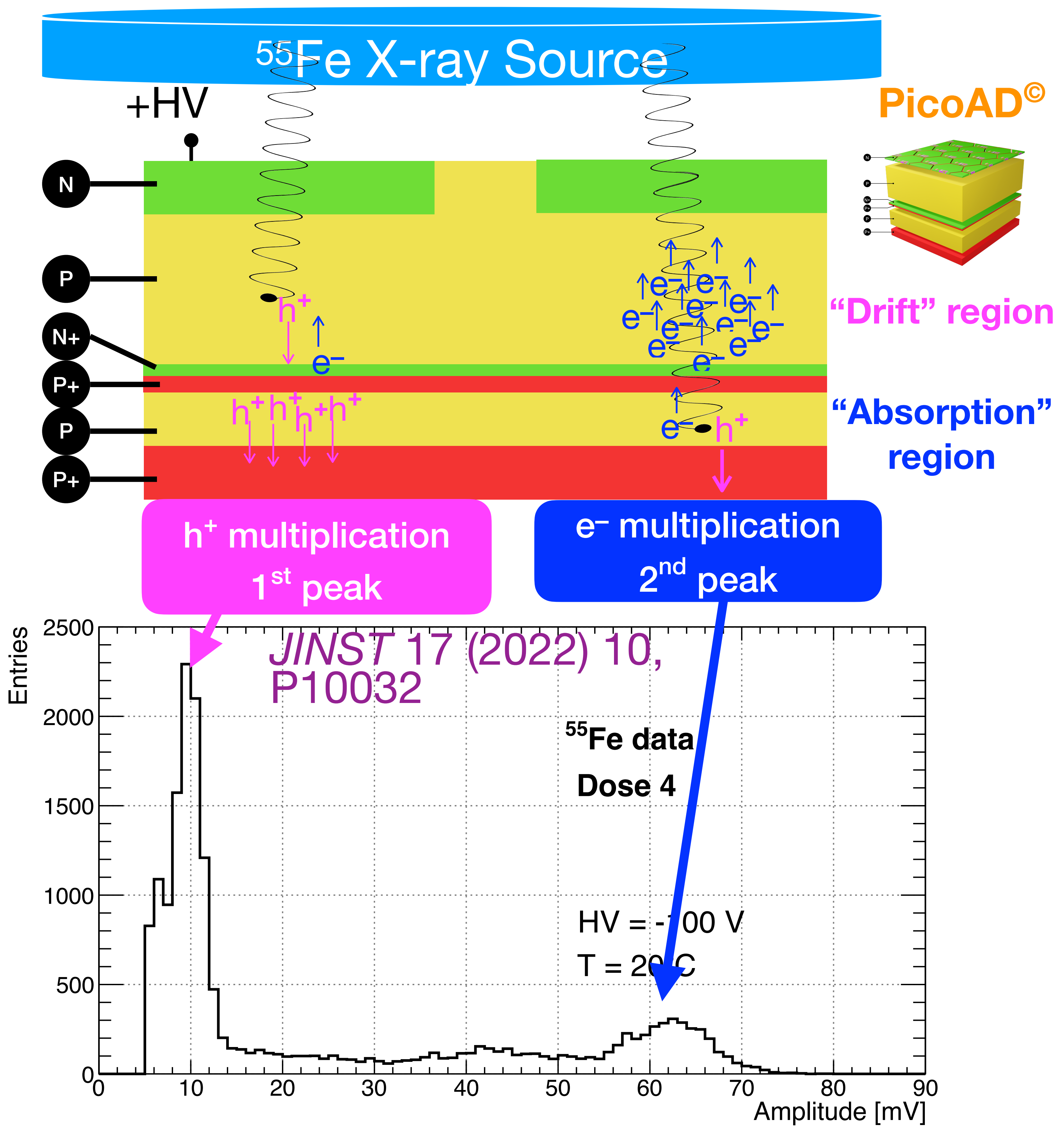
X-rays from ^{55}Fe radioactive source:

- mainly ~5.9 keV photons
- point-like charge deposition

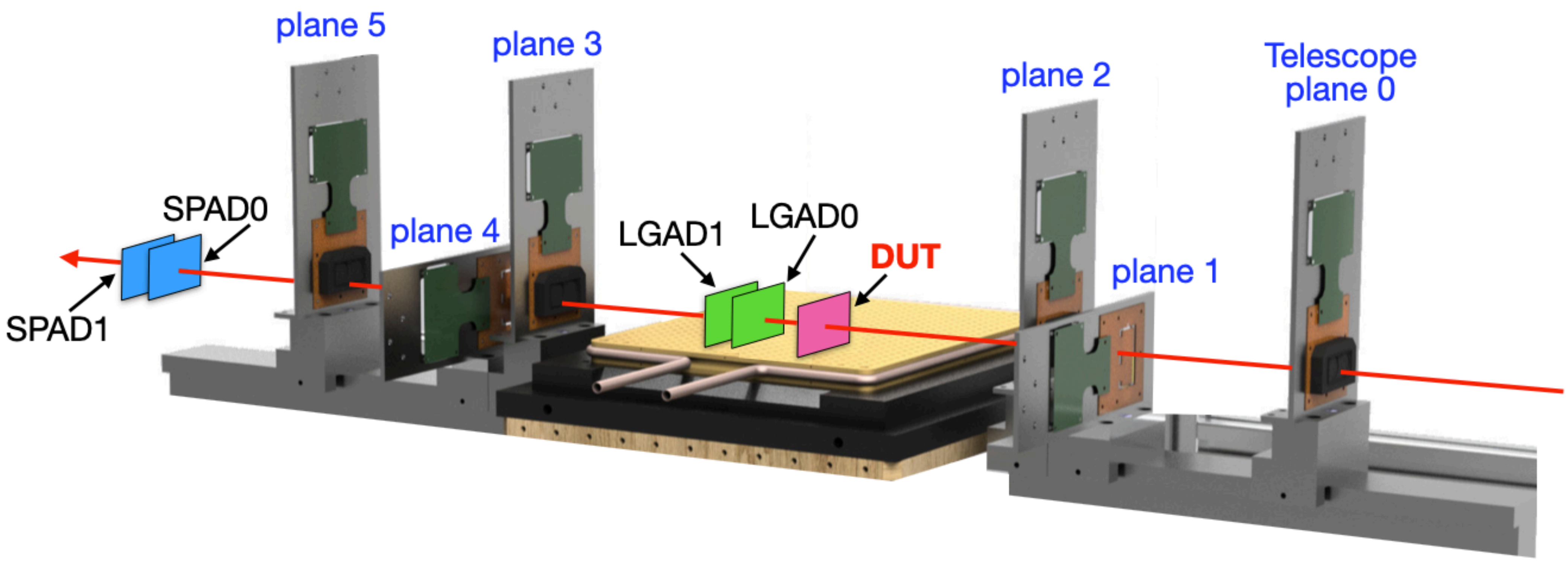
We found a double-peak spectrum

- photon absorbed in **drift region**
  - ➡ **holes** drift through gain layer & multiplied
  - ➡ **first peak** in the spectrum
- photon absorbed in **absorption region**
  - ➡ **electrons** through gain layer & multiplied
  - ➡ **second peak** in the spectrum

Gain measured: ~20 for ^{55}Fe (corresponding to ~60 for a m.i.p.)



CERN SPS Testbeam with 180 GeV/c pions to measure **efficiency** and **time resolution**

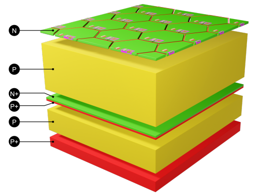


UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y}$ ≈10 μm)

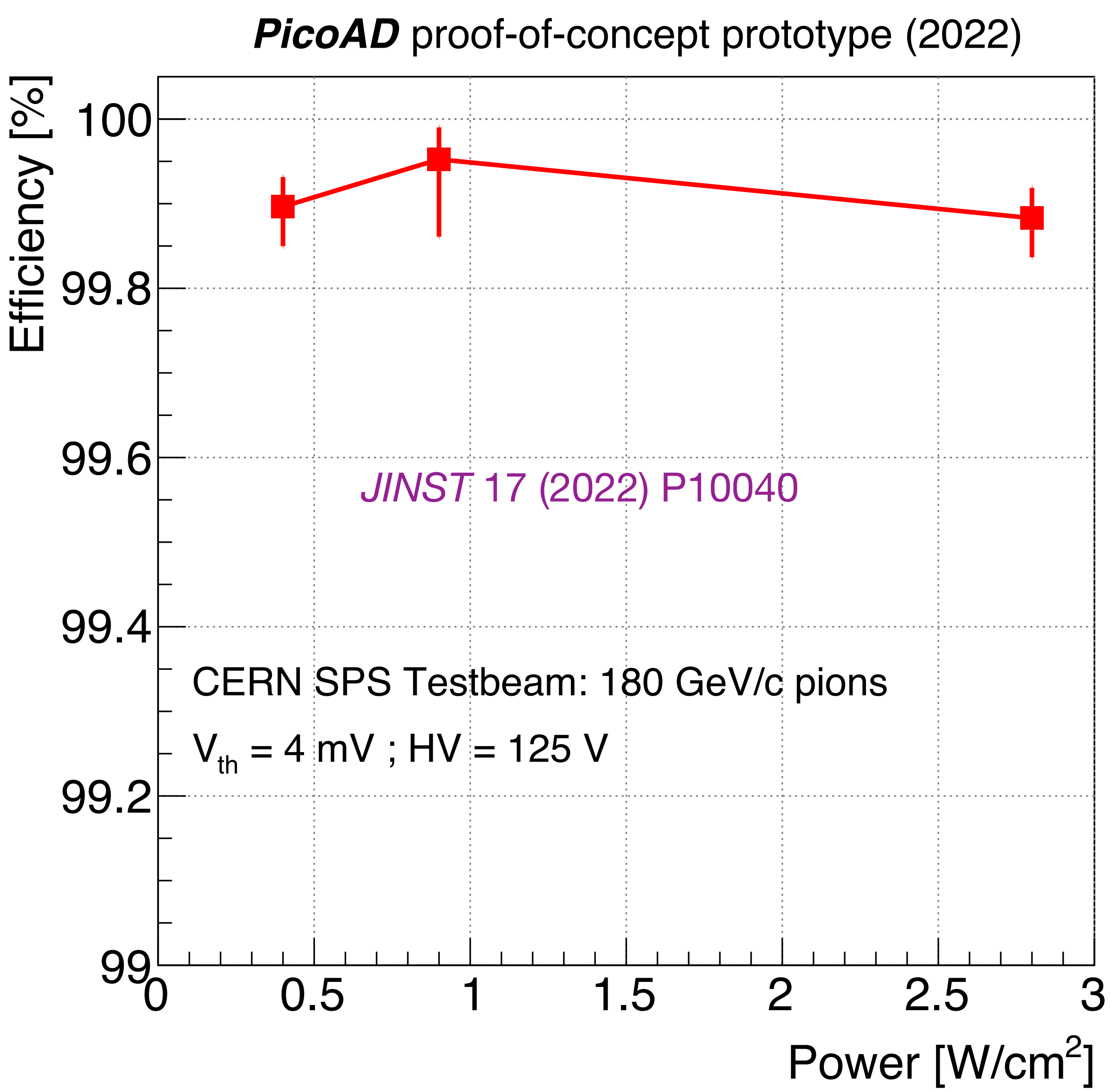
Two LGADs (σ_t ≈35 ps) to provide the timing reference (and **two SPADs** with σ_t ≈20 ps)

Testbeam PicoAD p.o.c.: Detection Efficiency

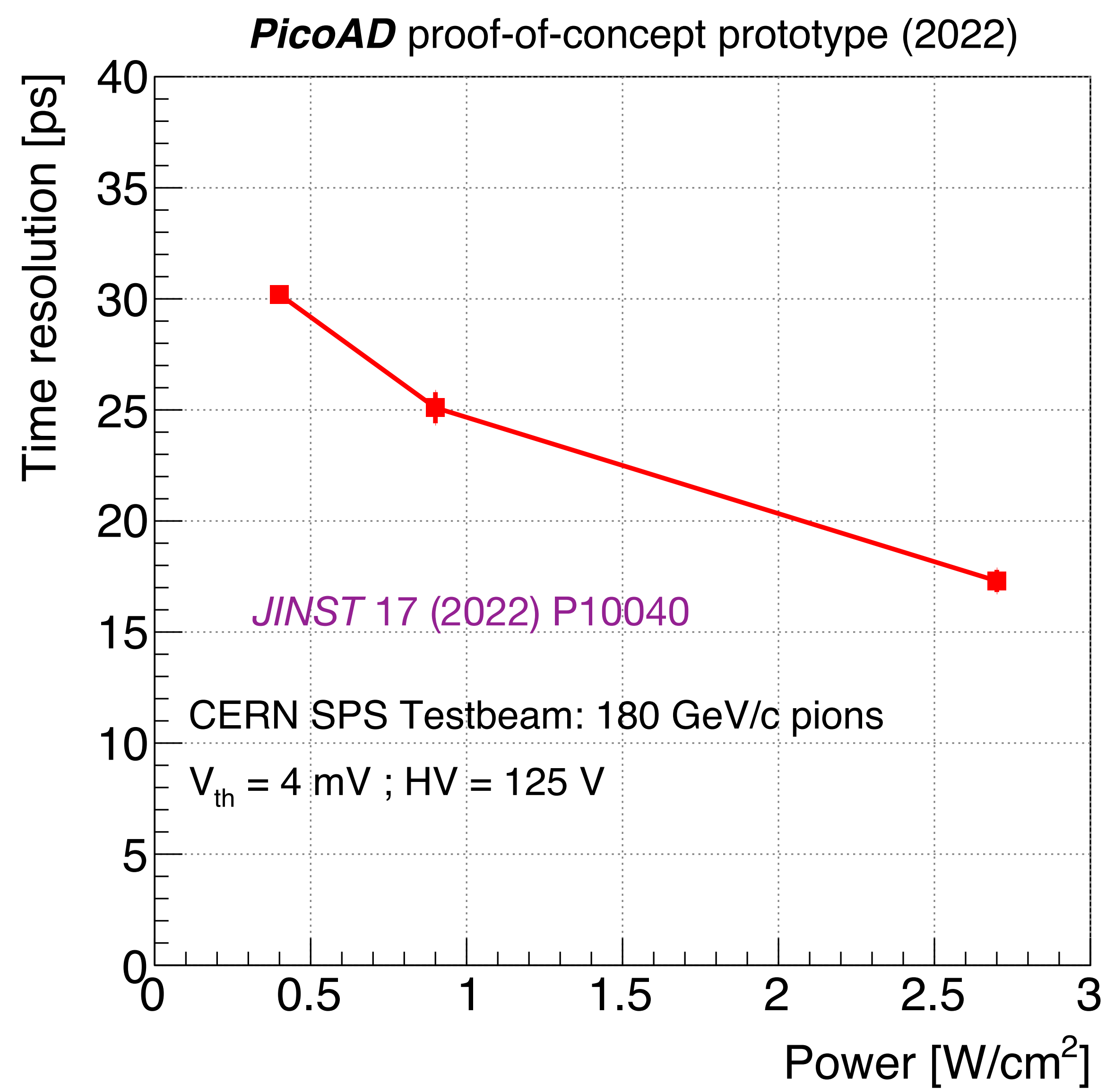
PicoAD©



99.9% for all power consumptions

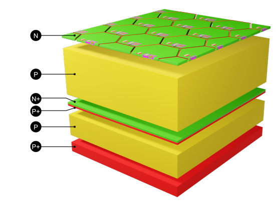


17 ps at 2.7 W/cm²
30 ps at 0.4 W/cm²

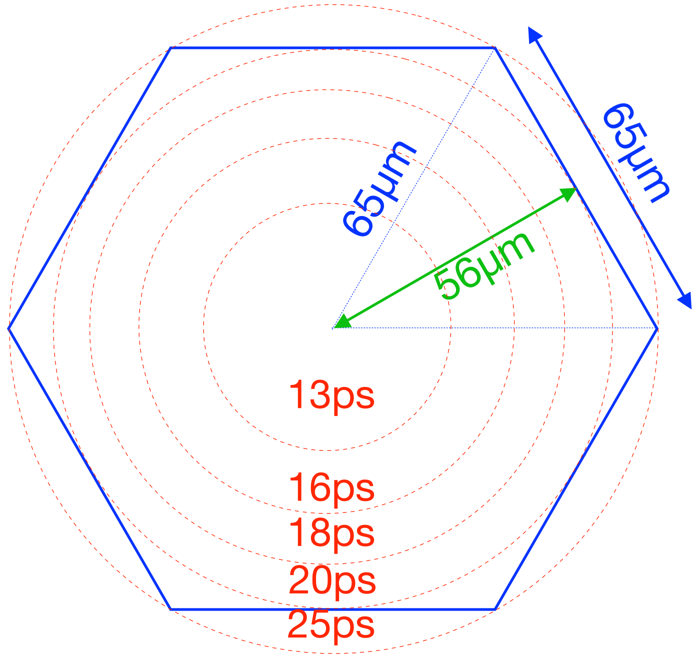


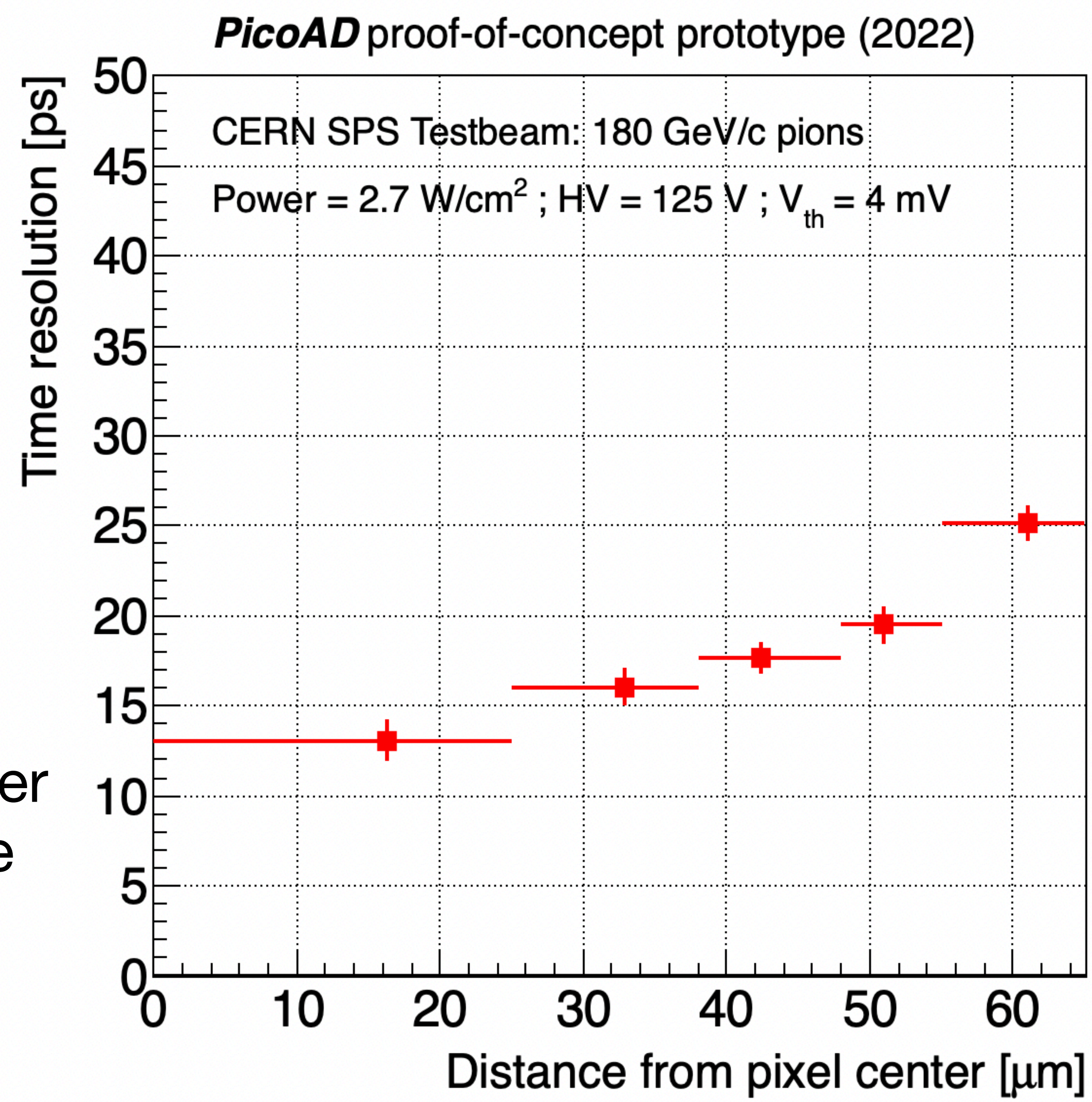
Testbeam PicoAD p.o.c.: Time Resolution

PicoAD©



Pixel surface divided in 5 radial areas:





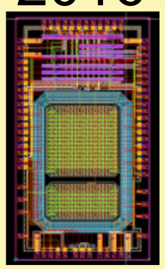
Time resolutions: **13 ps** at the pixel center
25 ps at the pixel edge

To be improved in future prototypes.

MONOLITH Project prototypes

What comes next?

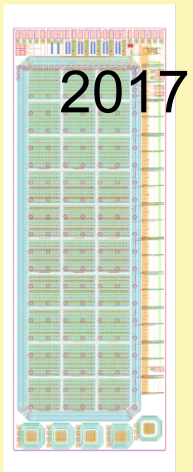
2016



200ps

- 1 mm² pixel
- Discriminator

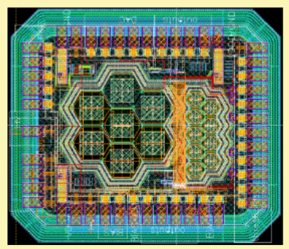
2017



110ps

- 30 pixels 500x500µm²
- 100ps TDC +I/O logic

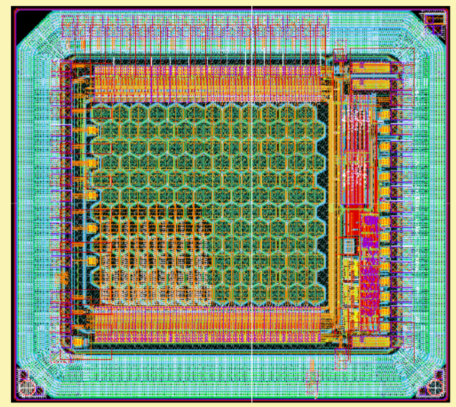
2018



50ps

- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

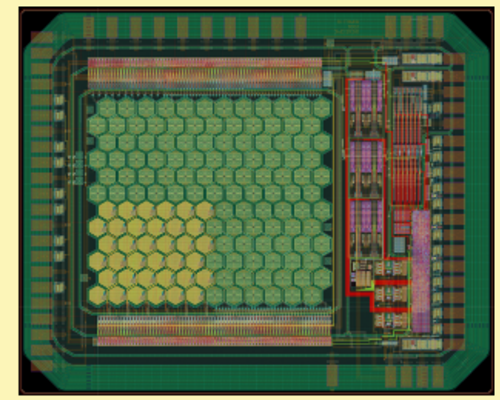
MONOLITH prototype 1
2020



36 ps

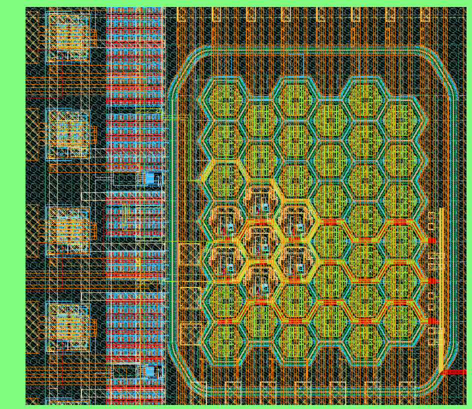
- Hexagonal pixels 100µm pitch
- 30ps TDC + I/O logic
- 4 analog channels

MONOLITH prototype 2
2022



- Matrix of 12x12 hexagonal pixels
- 100µm pitch
- improved electronics
- 50µm epitaxial layer (350Ωcm)

MONOLITH prototype 3
2023



- Hexagonal pixels **40µm pitch**
- improved electronics (4 times less power consumption)

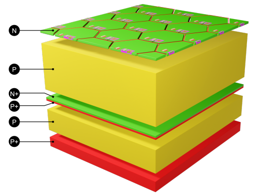
Monolithic prototypes
with internal gain layer:

PicoAD version
(proof-of-concept)
17 ps

PicoAD version
in production
(back: **Dec. 2023**)

PicoAD version
expected
Summer 2024

PicoAD©



The PicoAD© sensor works (*JINST* 17 (2022) 10 P10032 ; *JINST* 17 (2022) 17 P10040)

Testbeam of the monolithic proof-of-concept ASIC provided:

- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution σ_t = (17.3 ± 0.4) ps**
  13 ps at center and **25 ps** at pixel edge
  (although sensor not yet optimized for timing)

New PicoAD prototypes optimised for timing back from foundry in **December 2023**

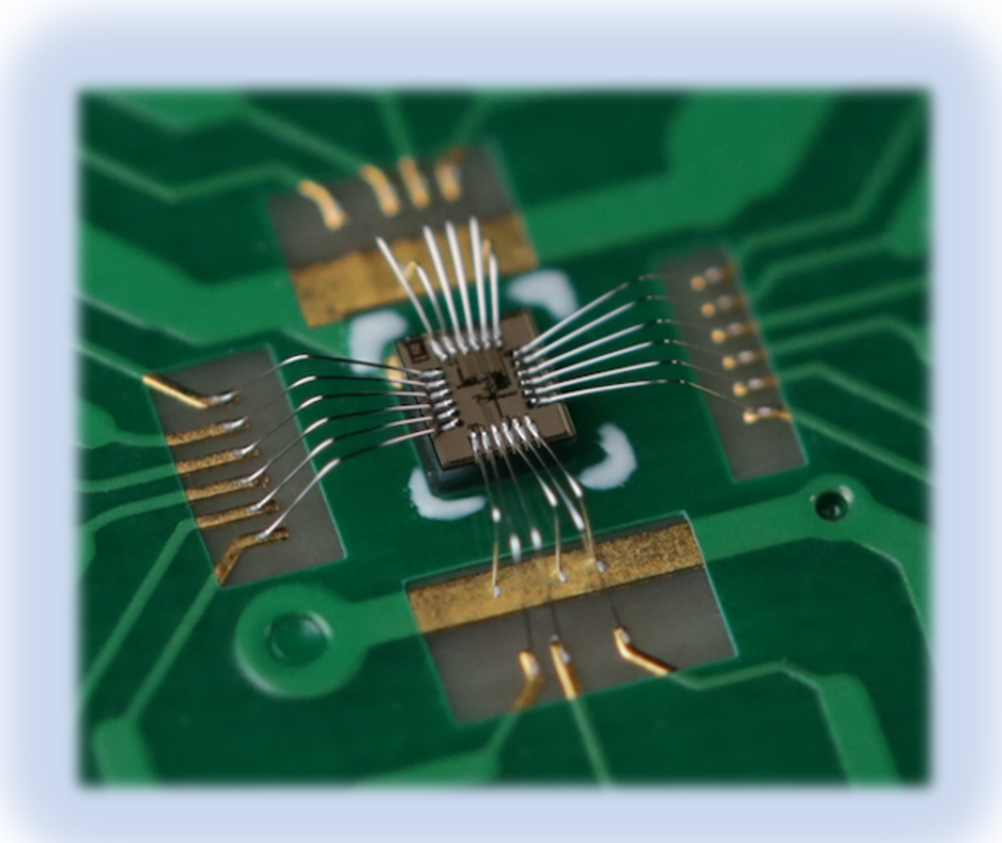
NOW DICING!

Deliverable of MONOLITH ERC project:

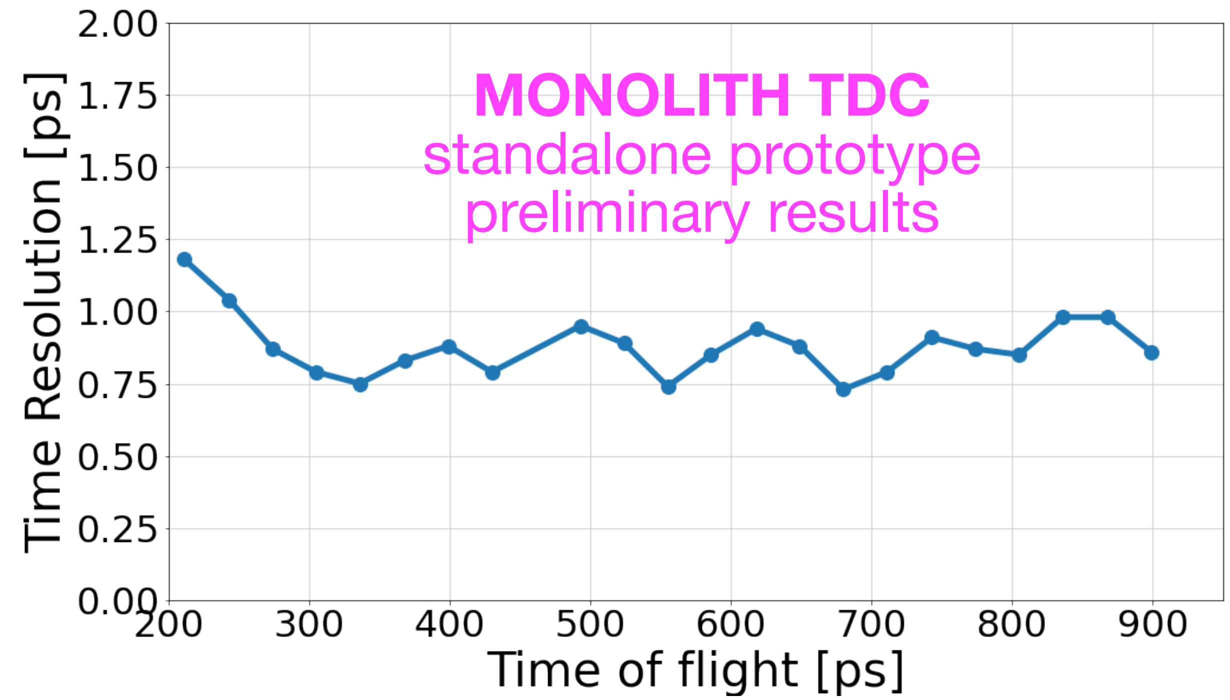
- Full-reticle monolithic ASIC in **Summer 2025** with 50μm pitch and 10ps timing

MONOLITH sub-picosecond TDC

We are developing a sub-picosecond TDC based on a novel design (our patent© & more):



© R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.



It was integrated in MONOLITH 2022 prototype2 ASIC

The UniGe Silicon Team


Giuseppe Iacobucci
- project P.I.
- System design

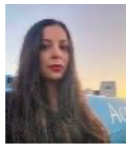

Thanushan Kugathasan
- Lead chip design
- Analog electronics


Stefano Zambito
- Laboratory tests
- Data analysis


Jordi Sabater Iglesias
- Detector simulation
- Laboratory tests


Matteo Milanesio
- Laboratory tests
- Data analysis

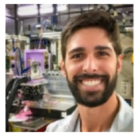

Antonio Picardi
- Chip design
- Firmware


Rafaella Kotitsa
- Sensor simulation
- Data analysis


Carlo Alberto Fenoglio
- Chip design
- Firmware


Lorenzo Paolozzi
- Sensor design
- Analog electronics


Roberto Cardella
- Sensor design
- Chip Analog/Dig design


Mateus Vicente
- System integration
- Laboratory tests


Chiara Magliocca
- Laboratory tests
- Data analysis


Théo Moretti
- Laboratory tests
- Data analysis


Jihad Saidi
- Laboratory tests
- Data analysis


Luca Iodice
- Chip design
- Firmware


Andrea Pizarro Medina
- Data analysis
- Laboratory tests


Didier Ferrere
- System integration
- Laboratory tests


Yannick Favre
- Board design
- RO system


Sergio Gonzalez-Sevilla
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- Laboratory tests


Stéphane Débieux
- Board design
- RO system

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Holger Rücker
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Marzio Nessi
CERN & UNIGE


Matteo Elviretti
IHP Mikroelektronik

Funded by:

Swiss National Science Foundation

European Research Council
Established by the European Commission

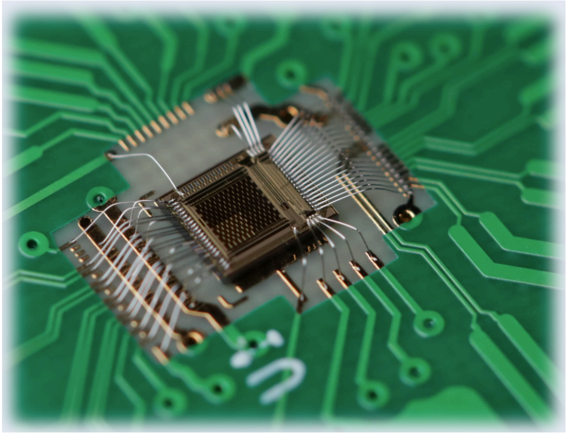
Sinergia

ATTRACT

UNIVERSITÉ DE GENÈVE UNITEC

Extra Material

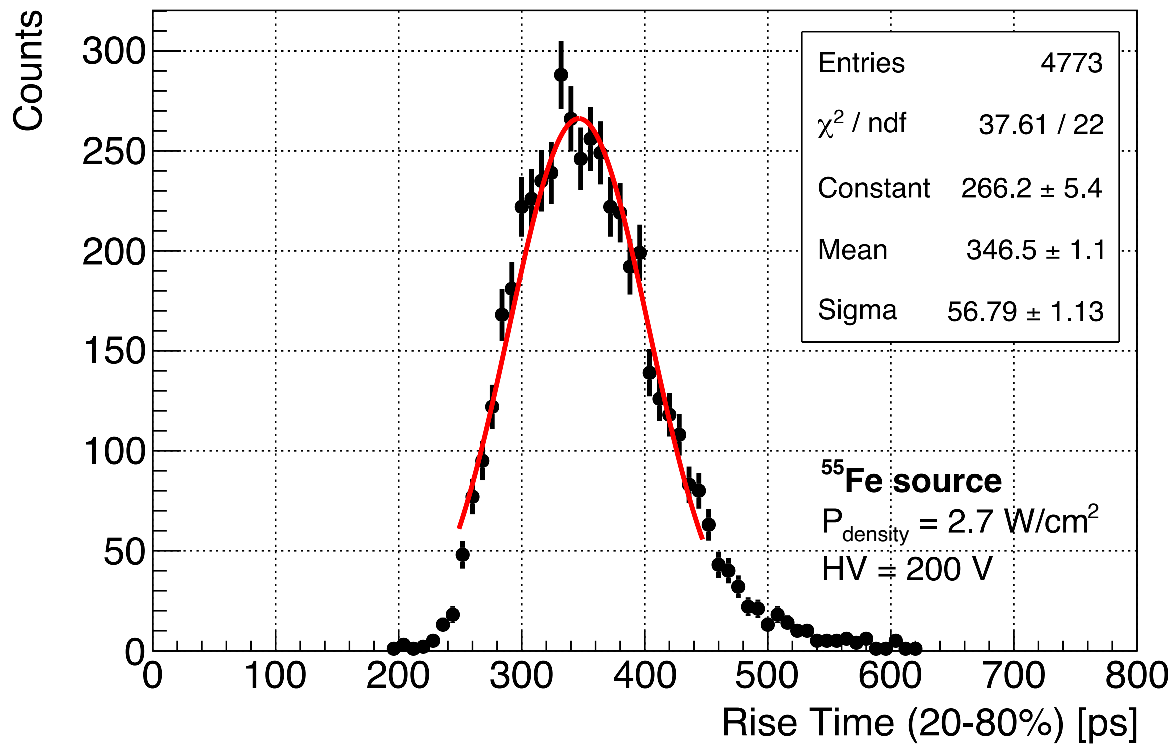
prototype2 (2022) — no gain layer

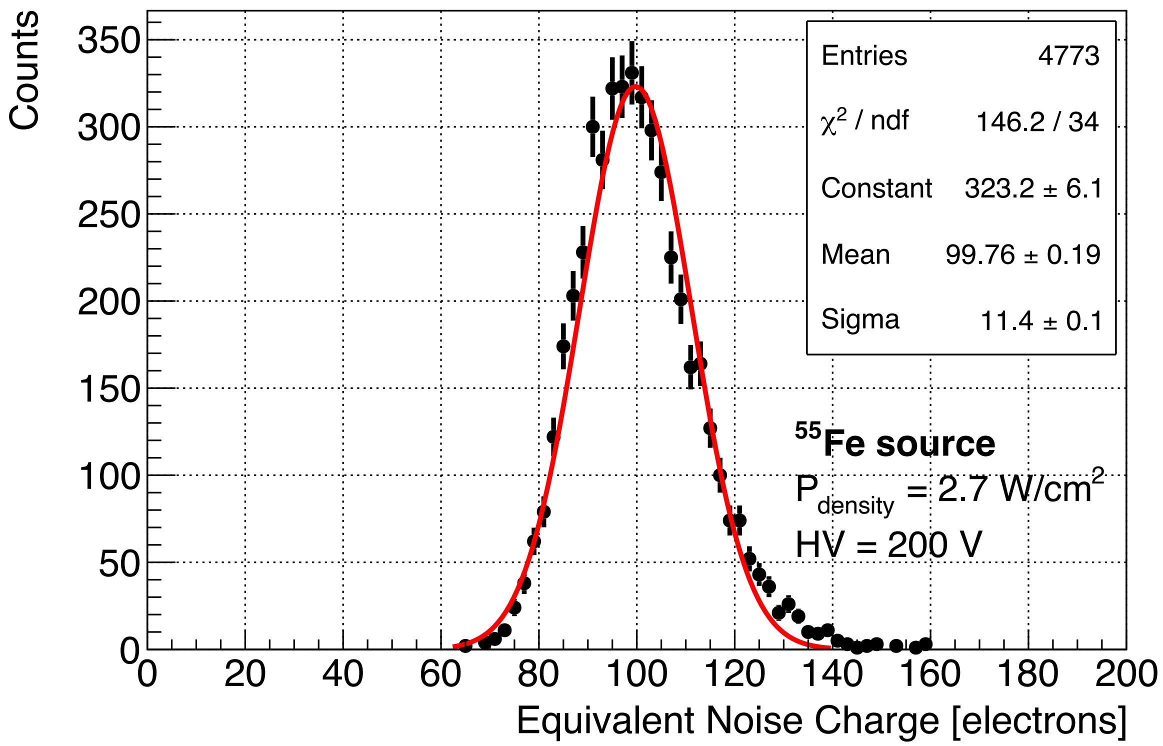


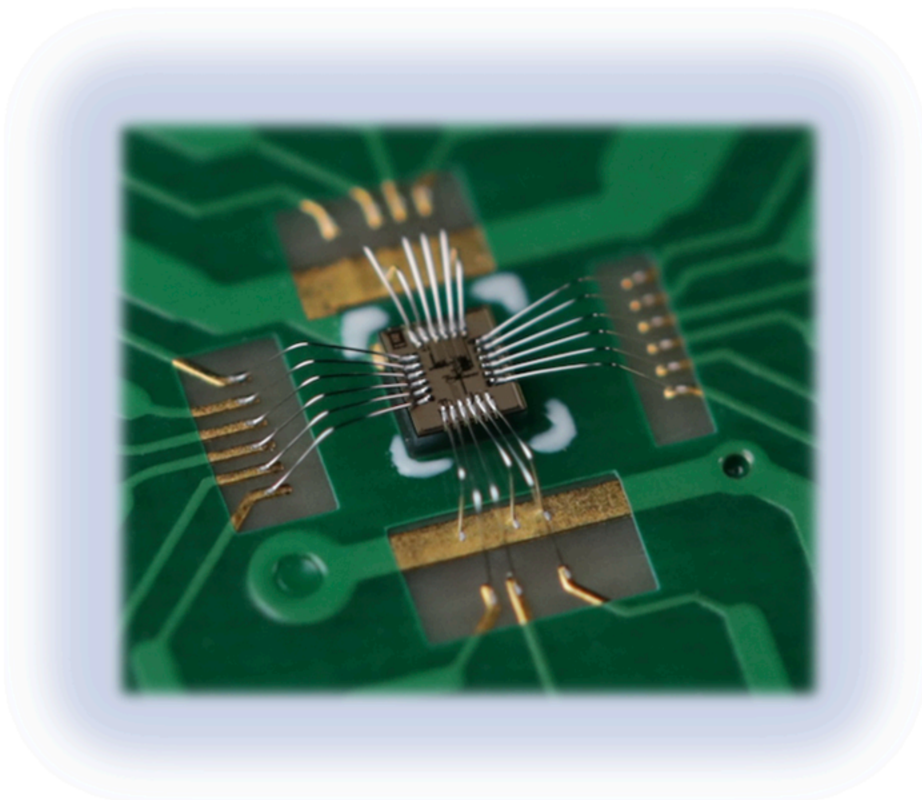
^{55}Fe measurements in cleanroom:

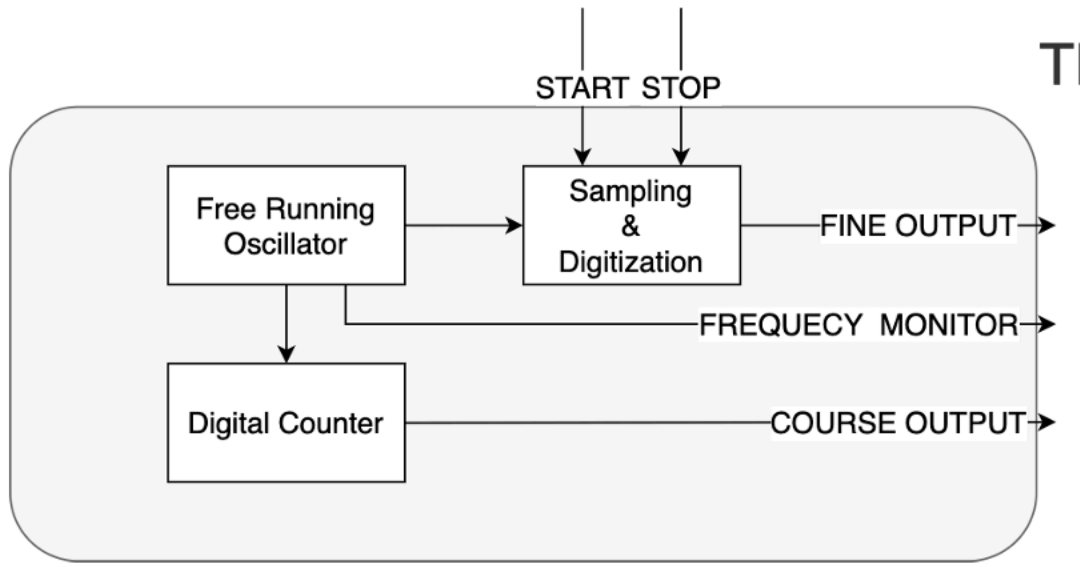
Risetime (20%–80%) ≈ 350 ps

ENC ≈ 100 e^-









TESTCHIP

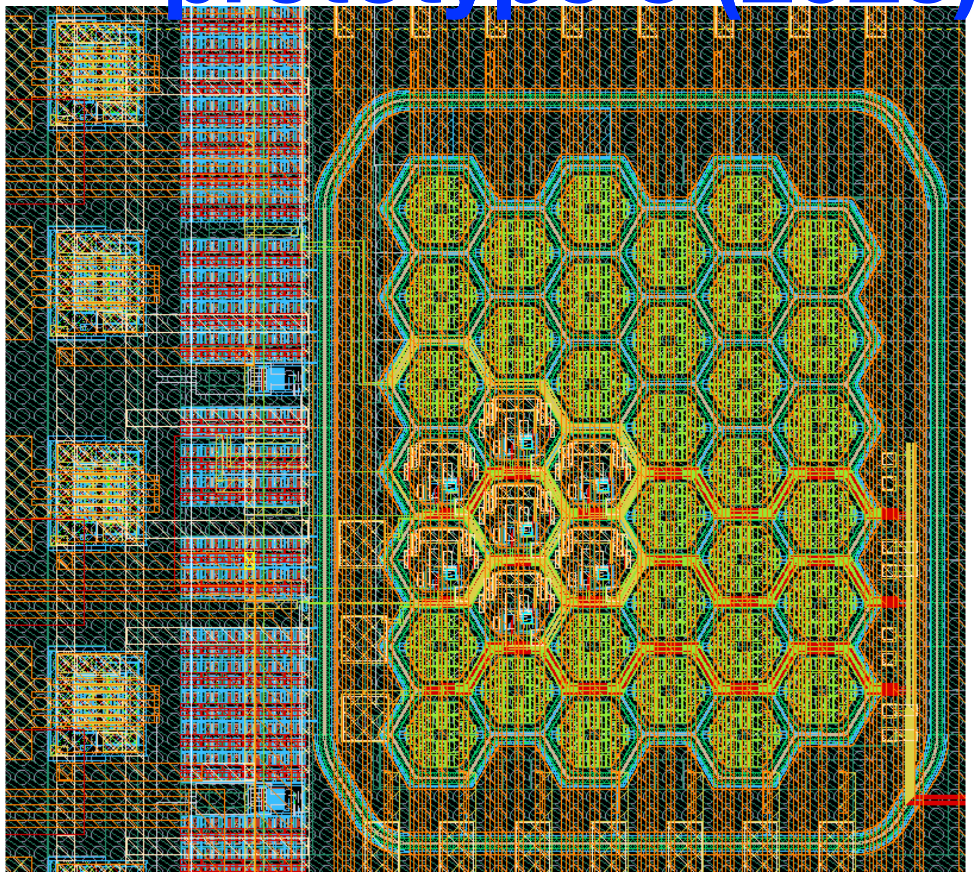
Proof of concept test chip:

Test chip AREA 1mm x 1mm
Oscillator AREA 900µm^2
Power Consumption Oscillator ≈3.8mW

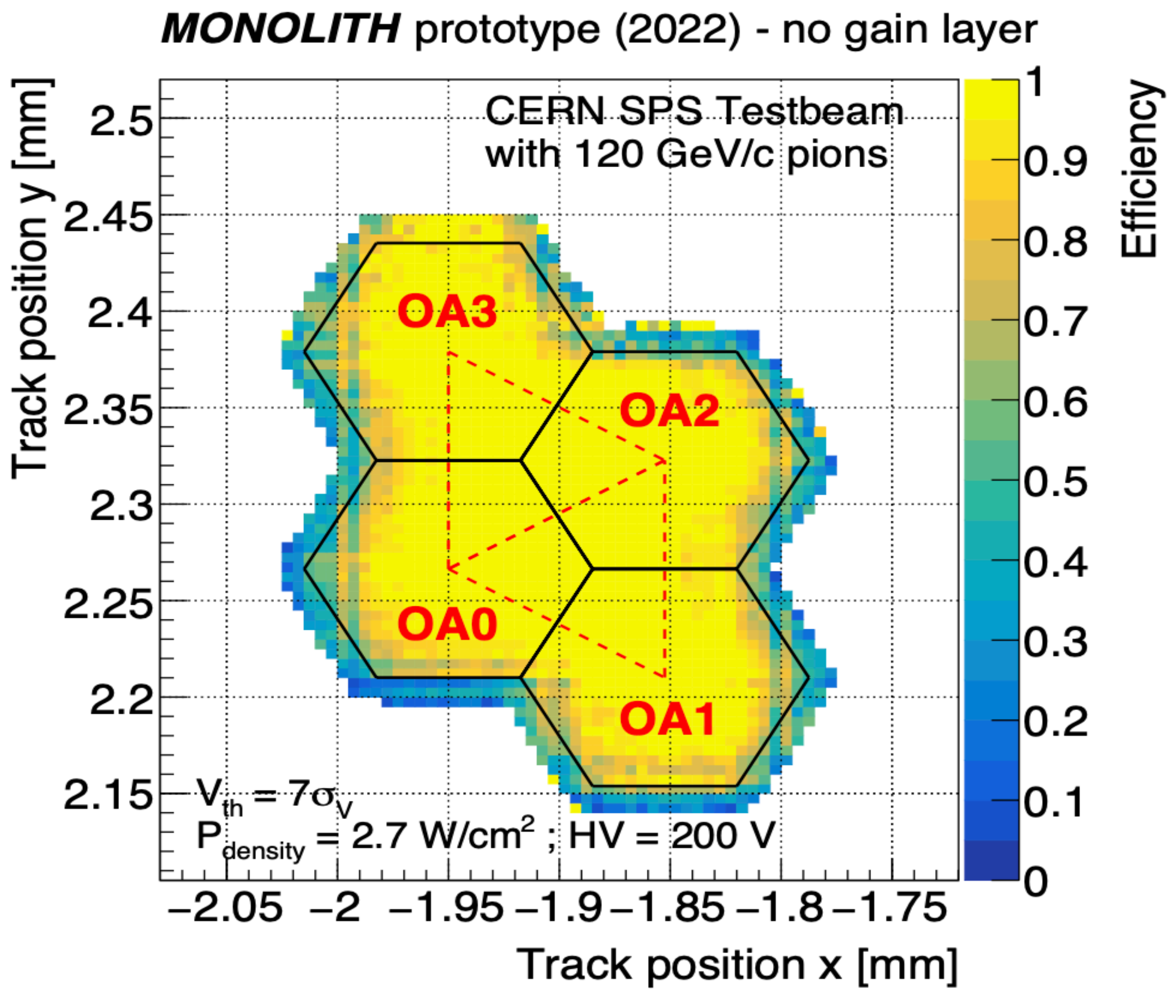
MONOLITH prototype3: 50μm pitch

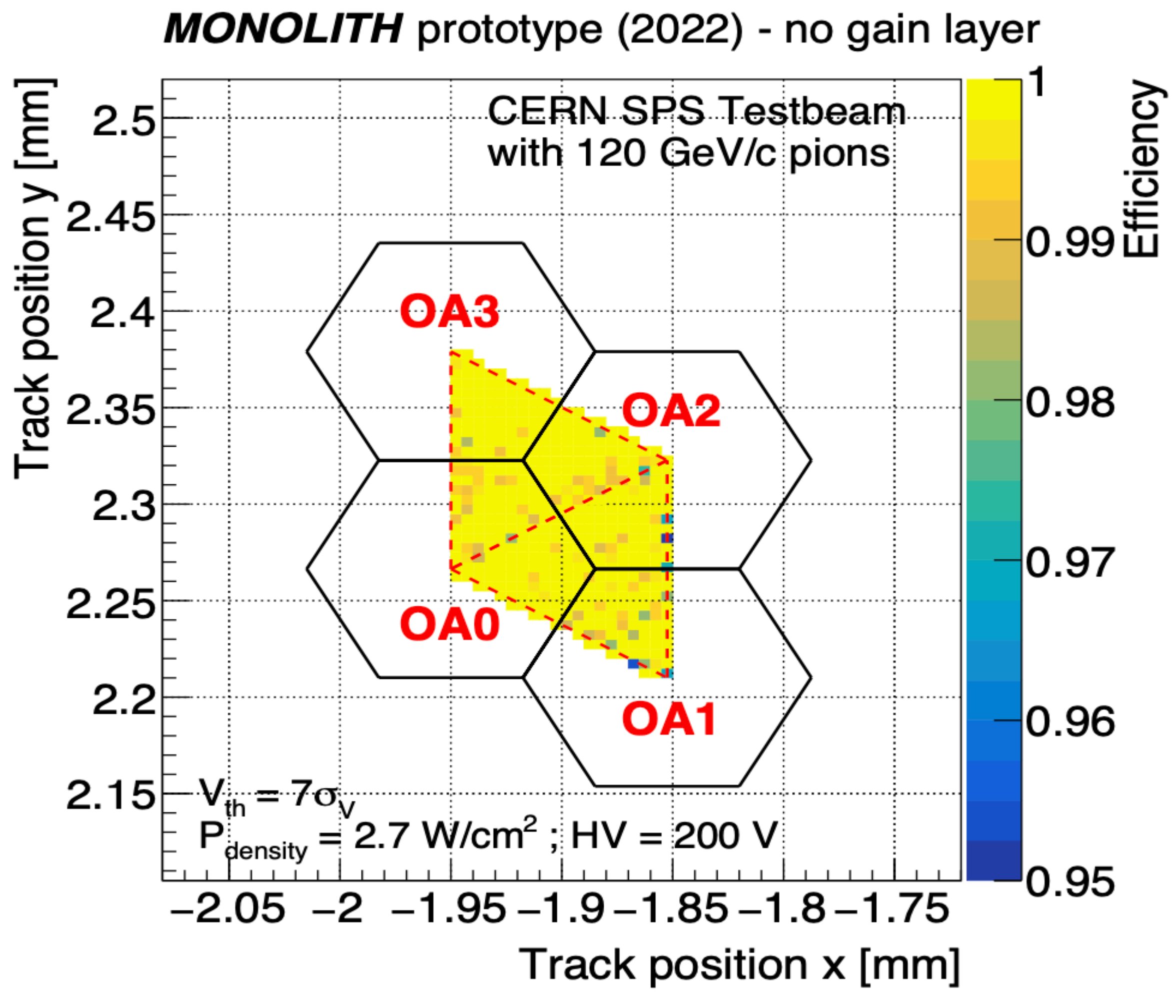
- New prototype: pixels with **50μm pitch**
  - smaller capacitance
- **improved FE electronics**
  - same timing performance with 4-times less power
  - 3 different configurations:
    - ➡ analog output with FE in pixel
    - ➡ analog output with FE off pixel
    - ➡ discriminated output with FE and discriminator in pixel
  - reduced inter-pixel distance from 10μm to 6μm to maintain time resolution at pixel edges

prototype 3 (2023)



- Back from foundry in June 2023; testbeam at CERN SPS late August 2023.

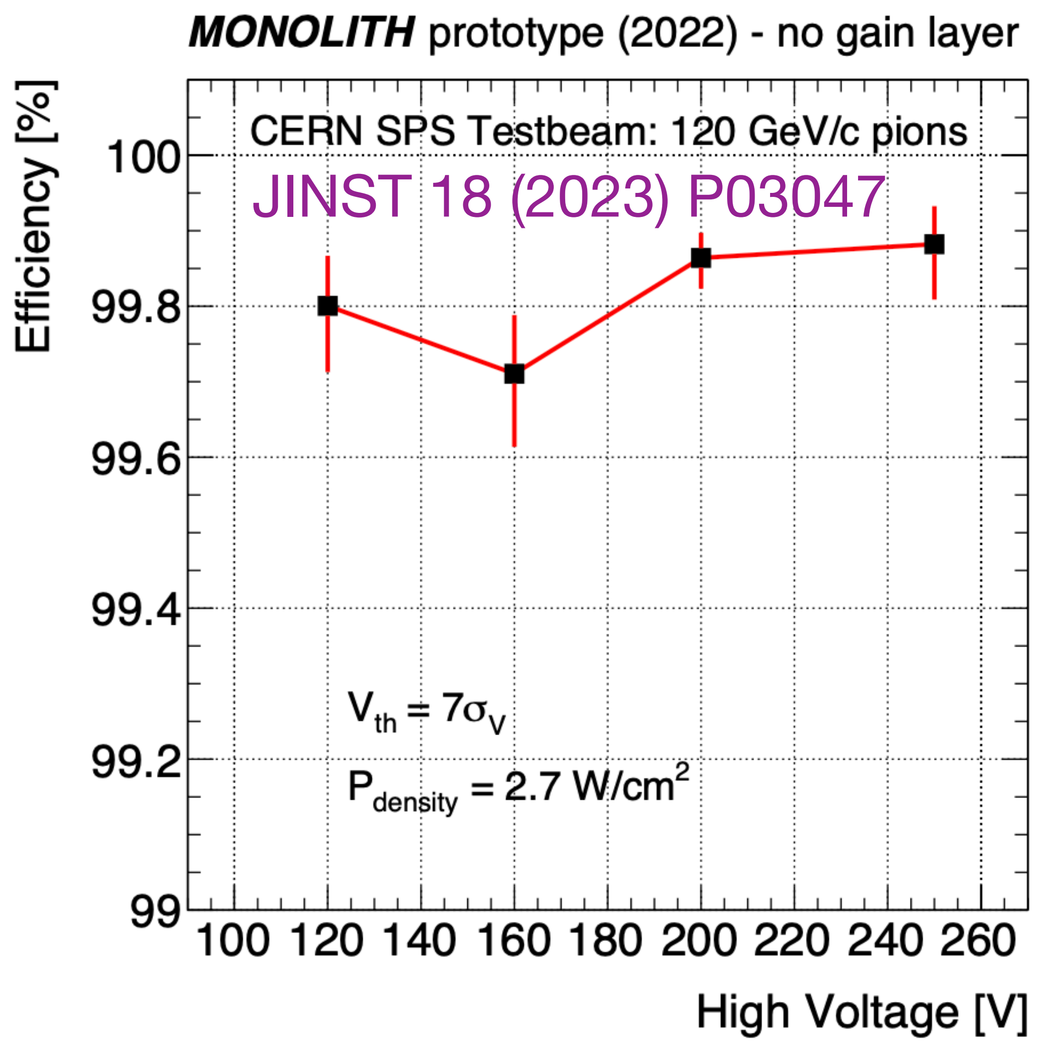


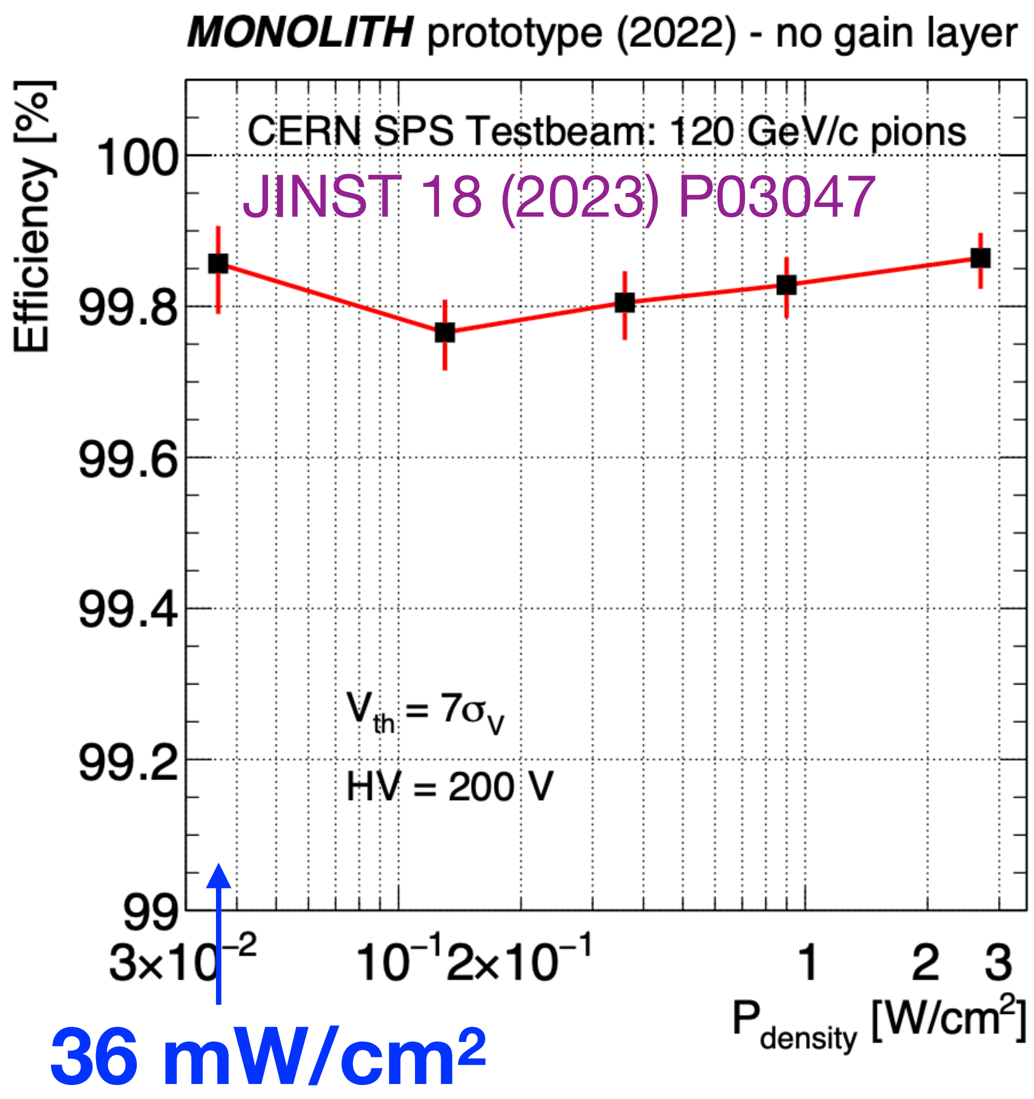


Efficiency at the external edges affected by the telescope resolution of 10 μm

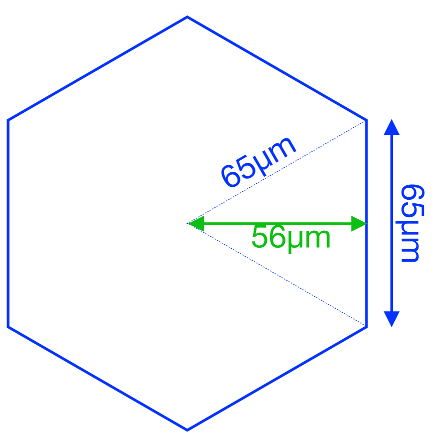
Full efficiency (yellow is 99.8%) in the two triangles unaffected by telescope resolution

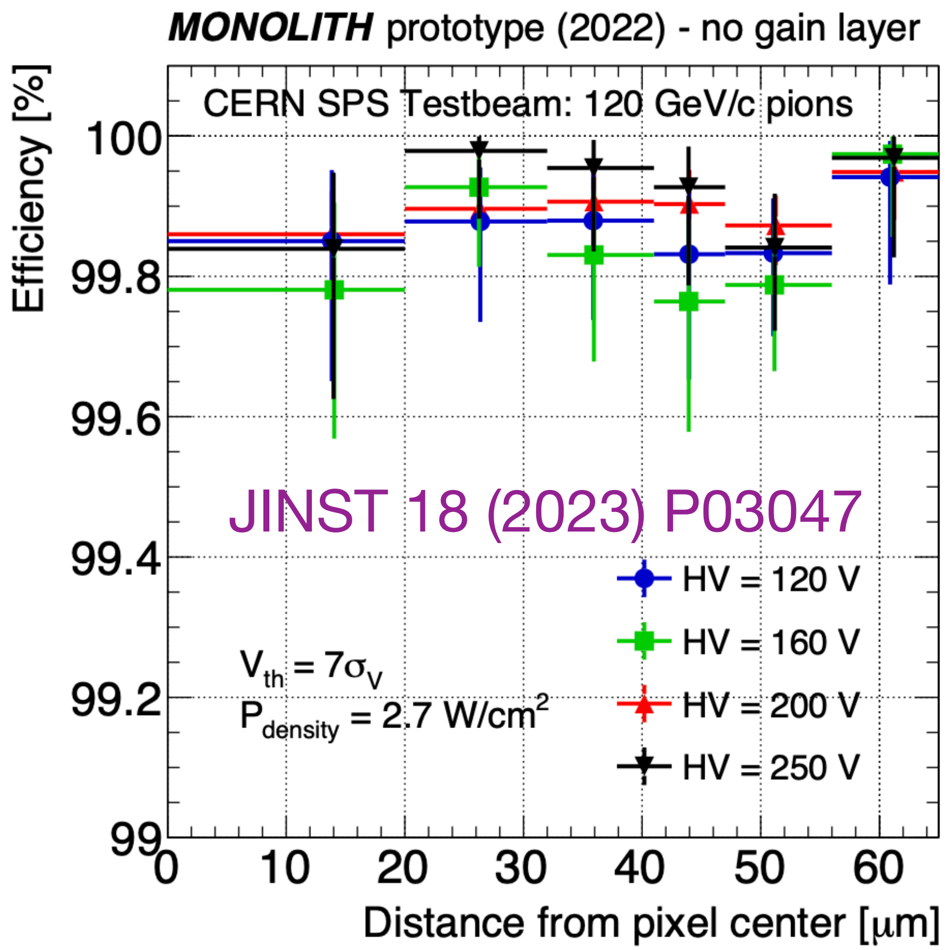
8 working points (HV, power consumption) taken at the testbea

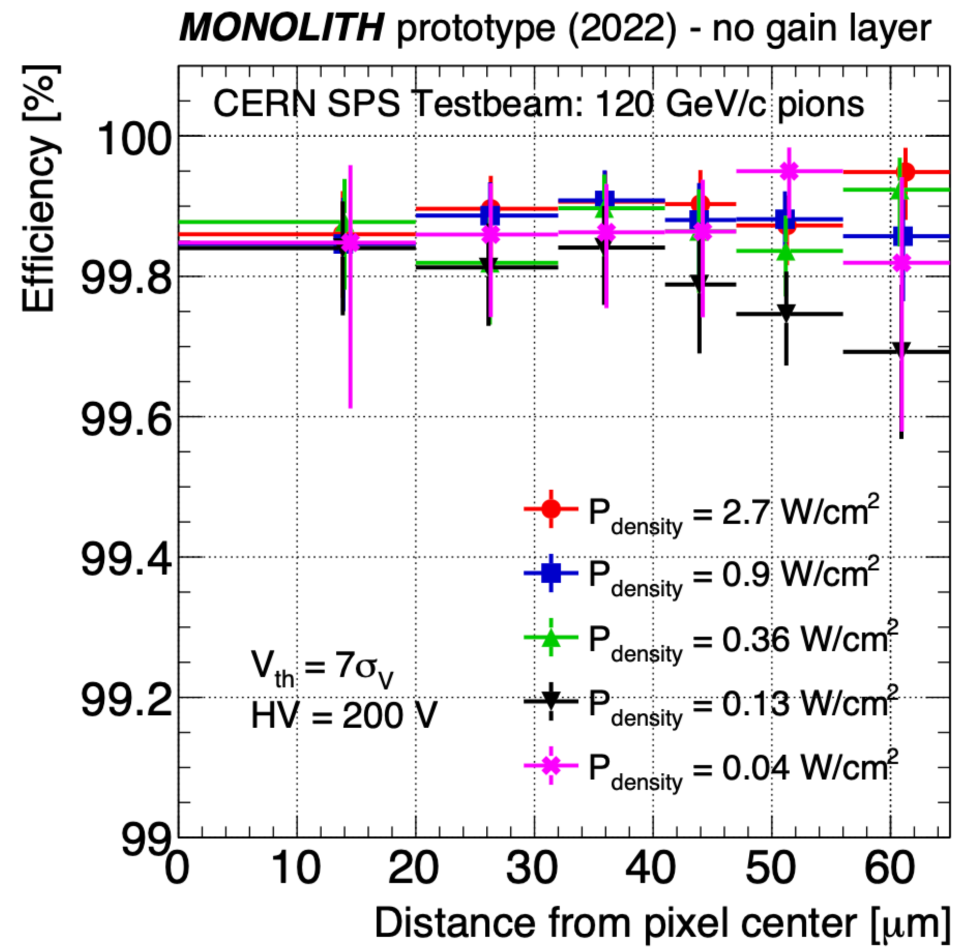




prototype2 (2022) — no gain layer





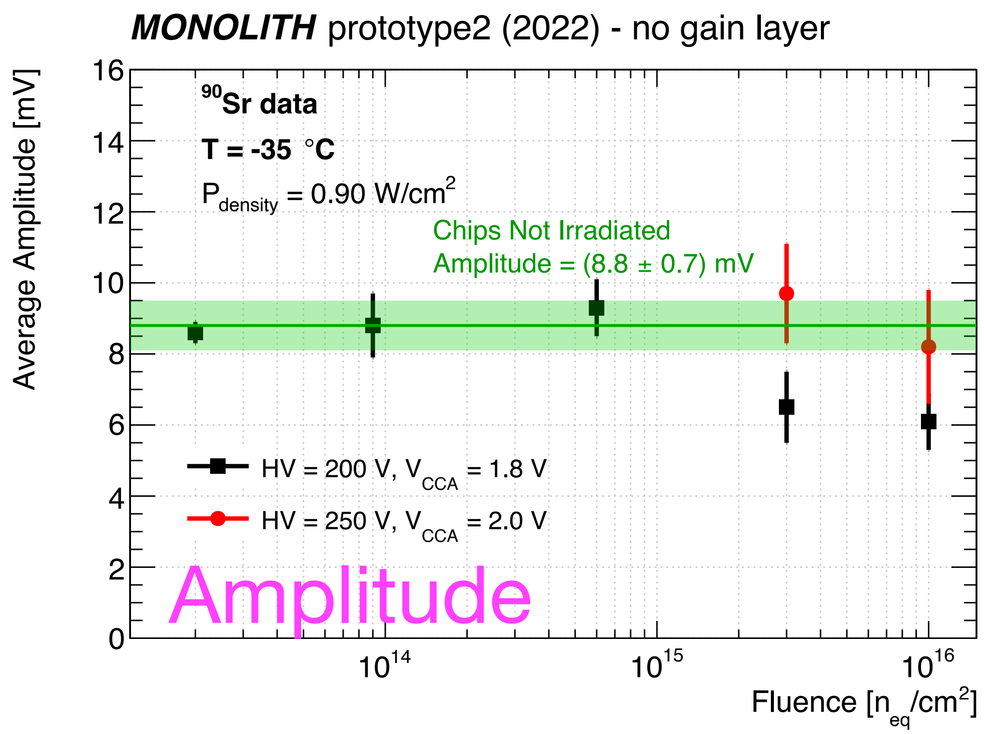


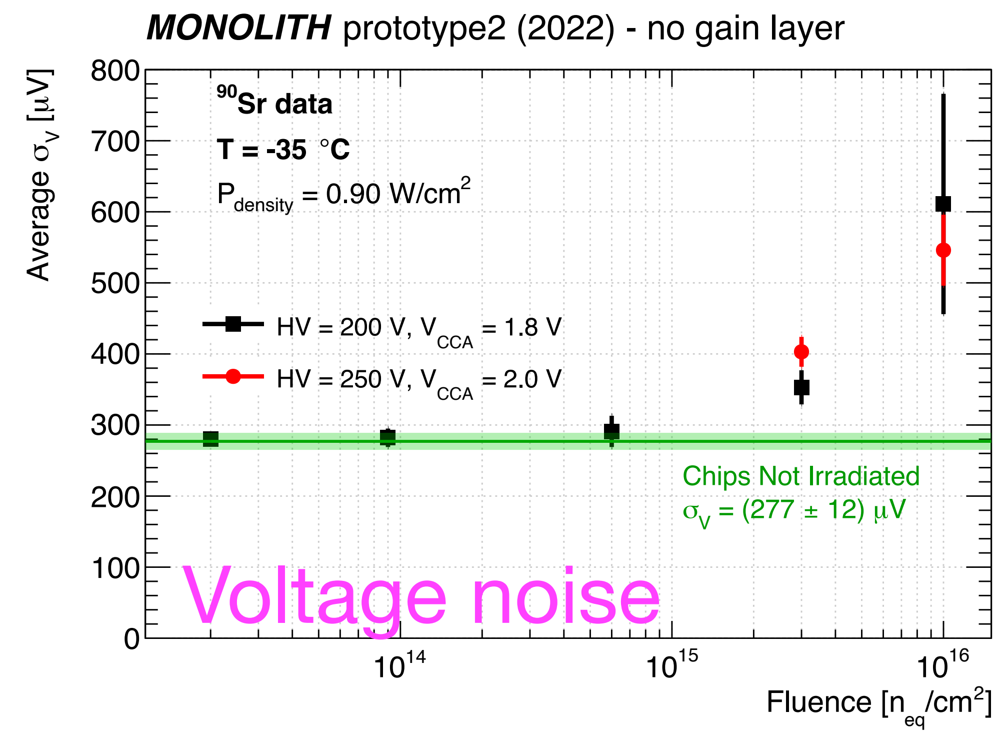
Efficiency ≈ **99.8%** even in the **inter-pixel region**, for all working points

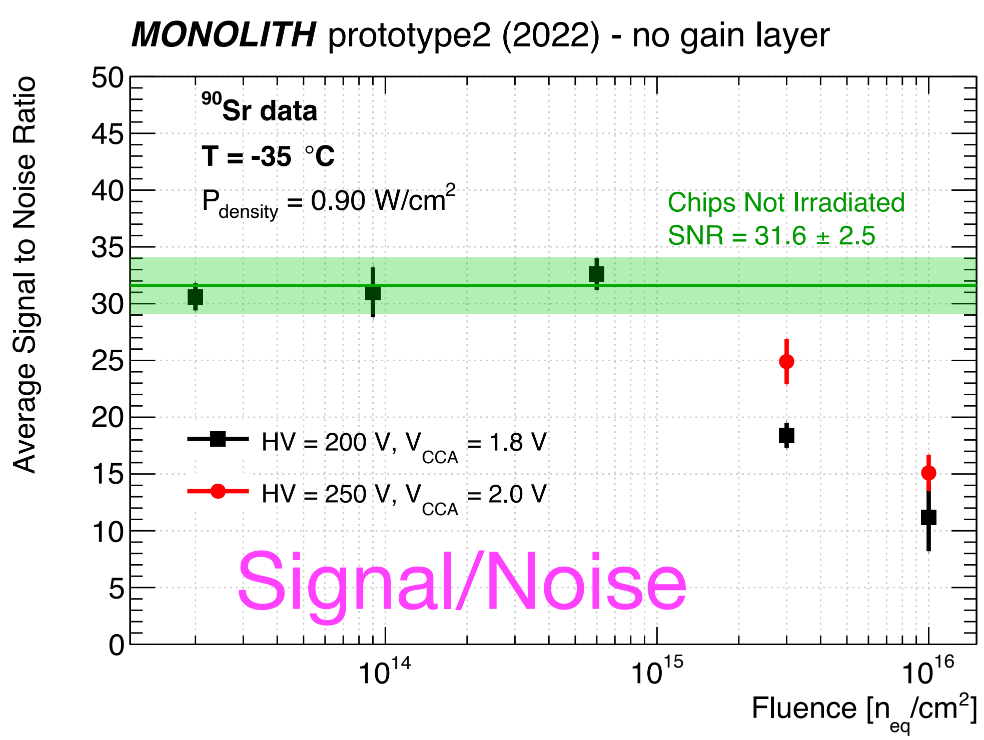
Radiation hardness of SiGe HBTs

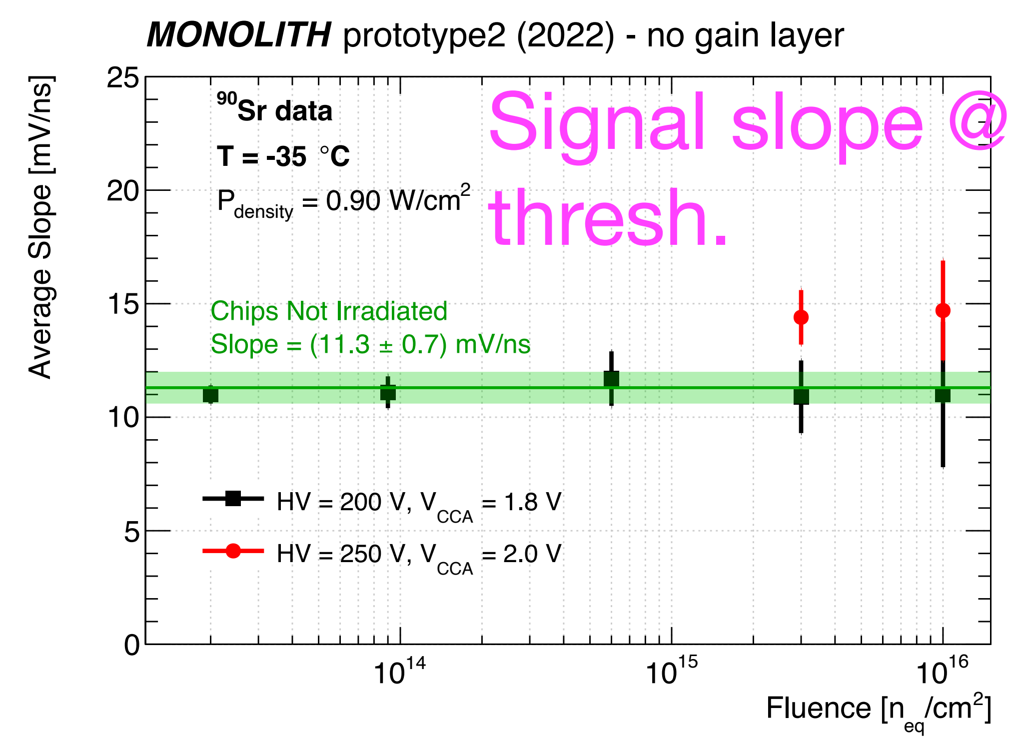
Characterisation with ^{90}Sr source of boards irradiated up to 10^{16} n_{eq}/cm^2

Averages of the 4 analog pixels (T=-35°)

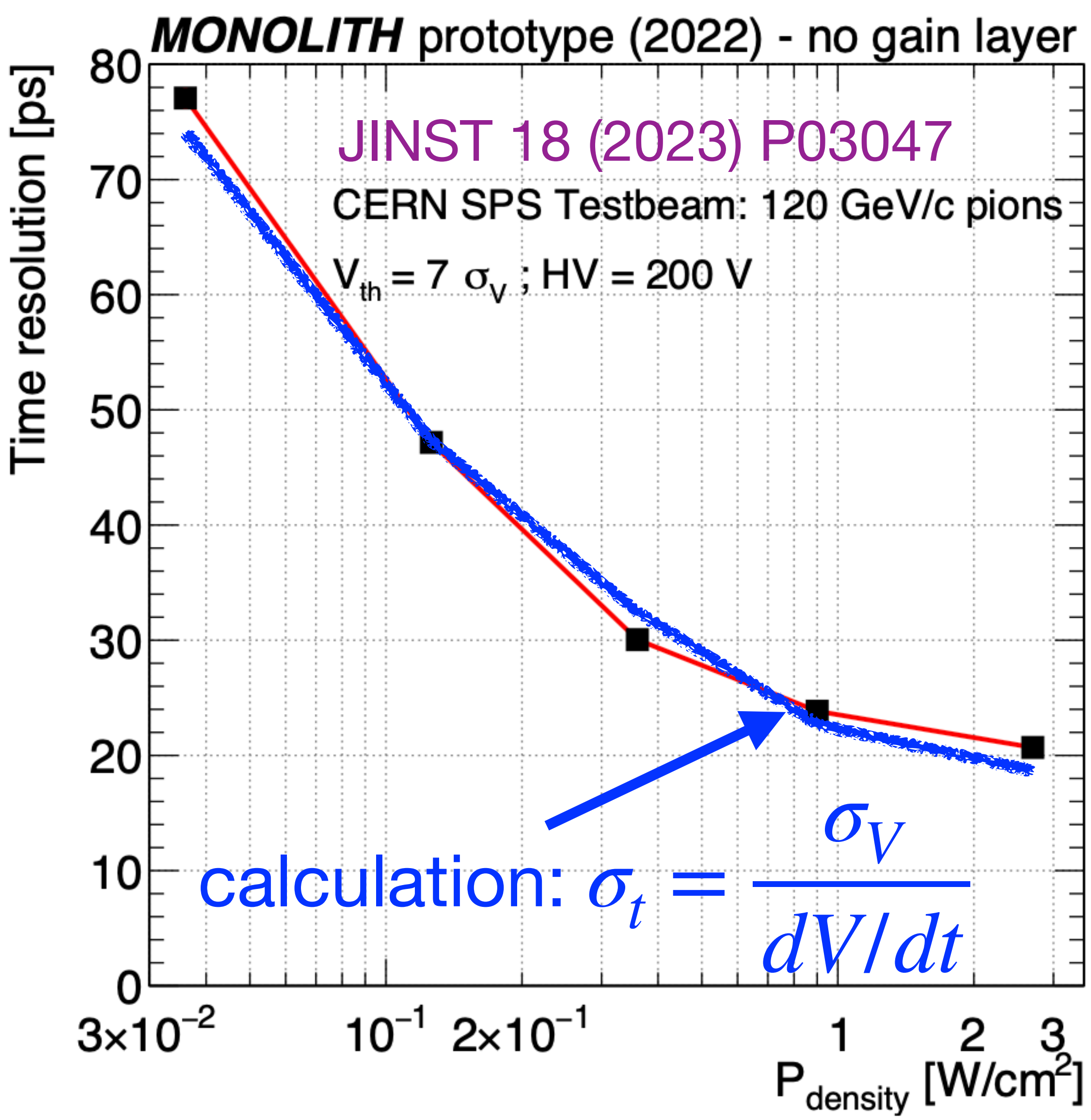








prototype2 (2022) — no gain layer



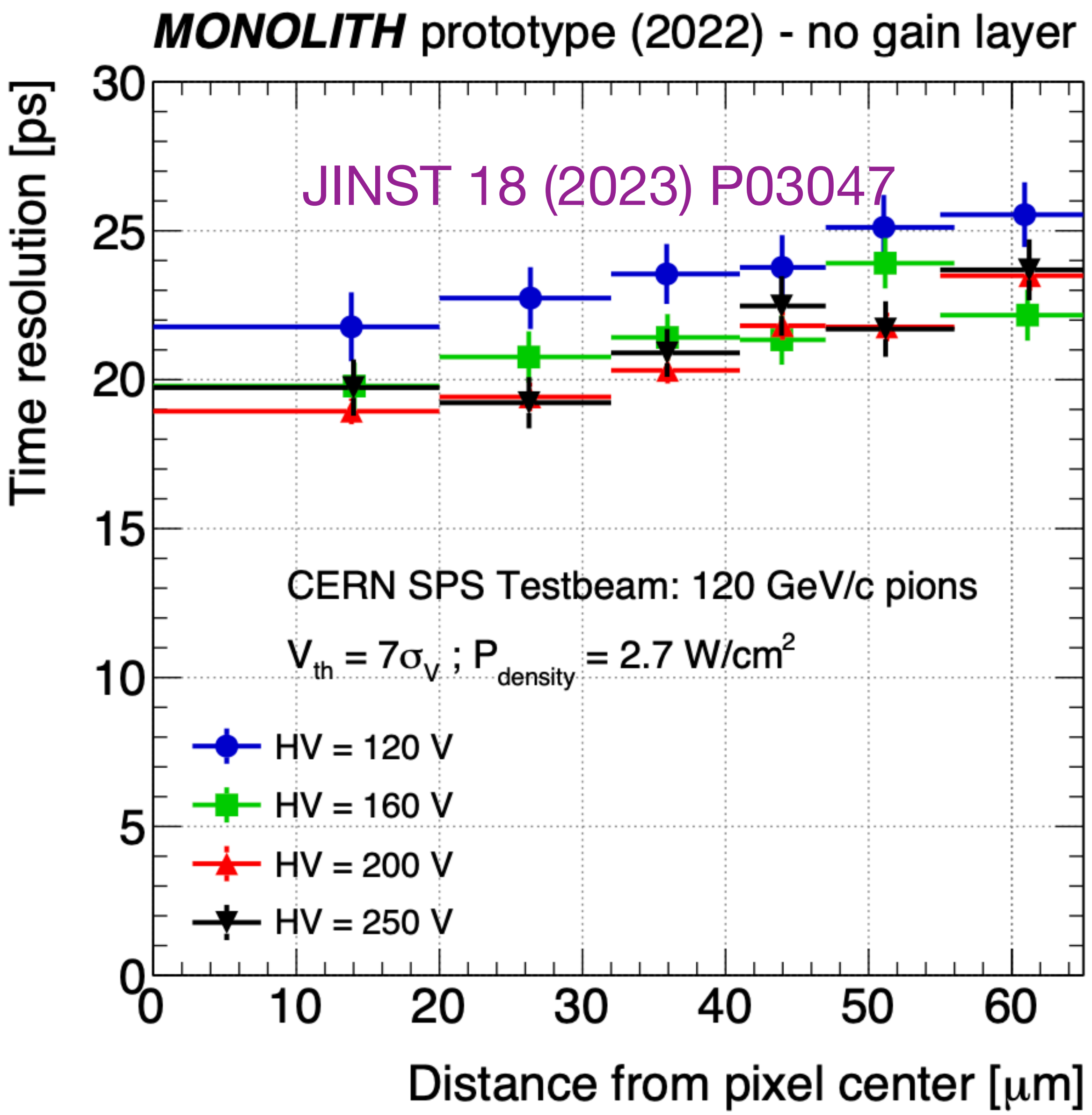
The method used to calculate the time resolution

$$\sigma_t = \frac{\sigma_V}{dV/dt}$$

using the ^{90}Sr source was validated with the testbeam data.

The results compare very well within 10%

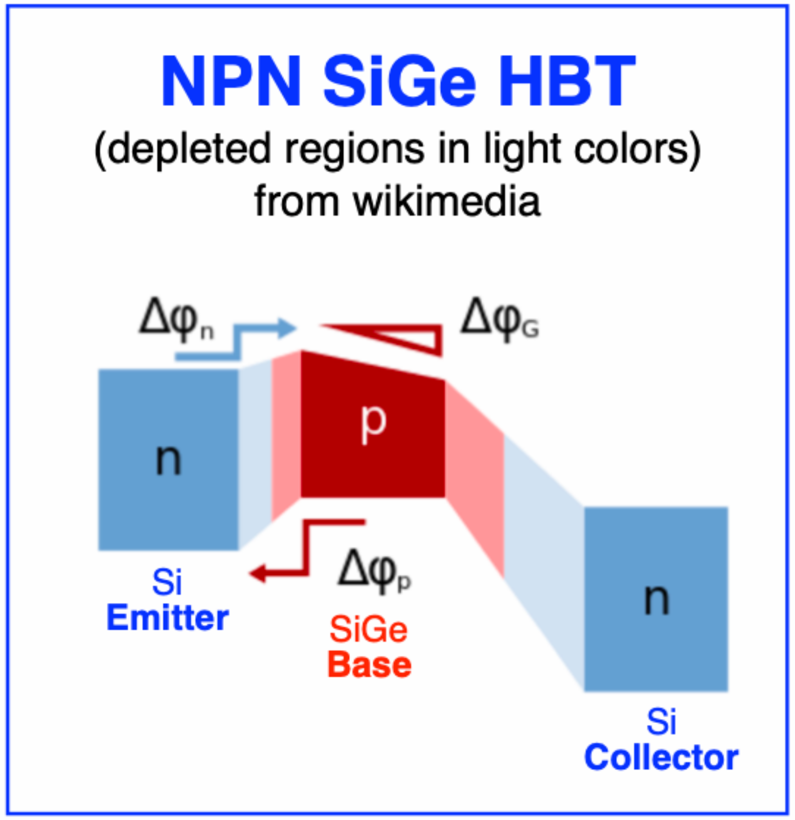
prototype2 (2022) — no gain layer



For HV ≥ 160V, time resolution ranges from **≈ 19 ps** at the center to **≈ 23 ps** at the edge of the pixel

Still something to improve with the weighting field far from pixel center.

For HV = 120 V: ≈ 3 ps worse.



SiGe HBT = BJT with Germanium as base material.

Grading of Ge doping in base:

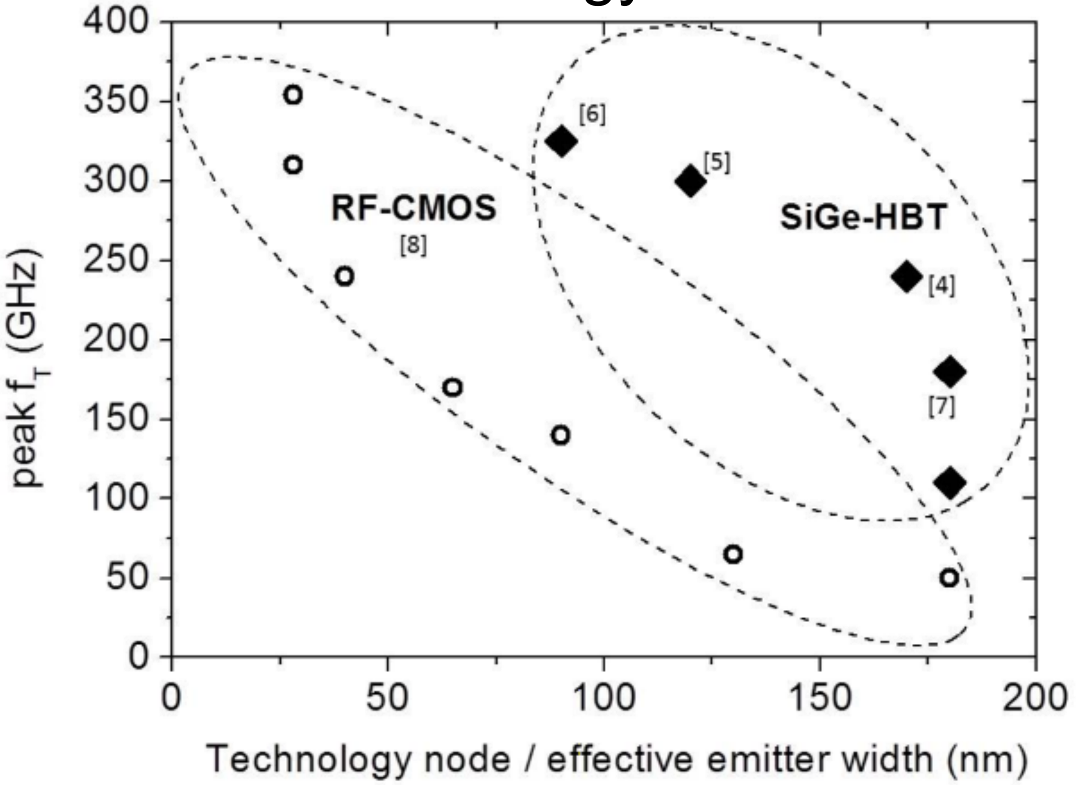
- charge-transport in base via **drift**
  - reduced charge-transit-time in base
  - **high current gain β**
- **High doping** in base is possible:
  - thinner base
  - **reduced base resistance R_b**

$$ENC_{series\ noise} \propto \sqrt{k_1 \frac{C_{tot}^2}{\beta} + k_2 R_b C_{tot}^2}$$

Leading-edge **IHP SG13G2** technology, **130 nm** process featuring **SiGe HBT**

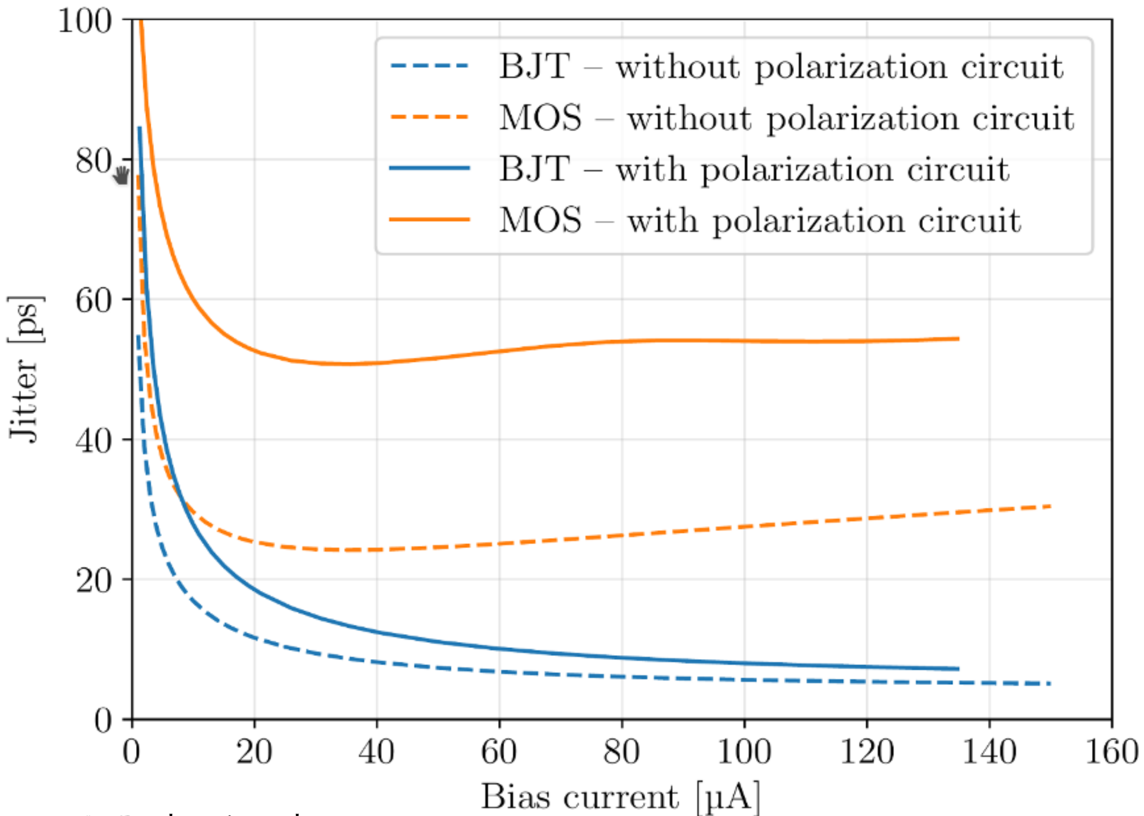
SiGe HBT vs. CMOS

Peak transition frequency vs. technology node



A. Mai and M. Kaynak,
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

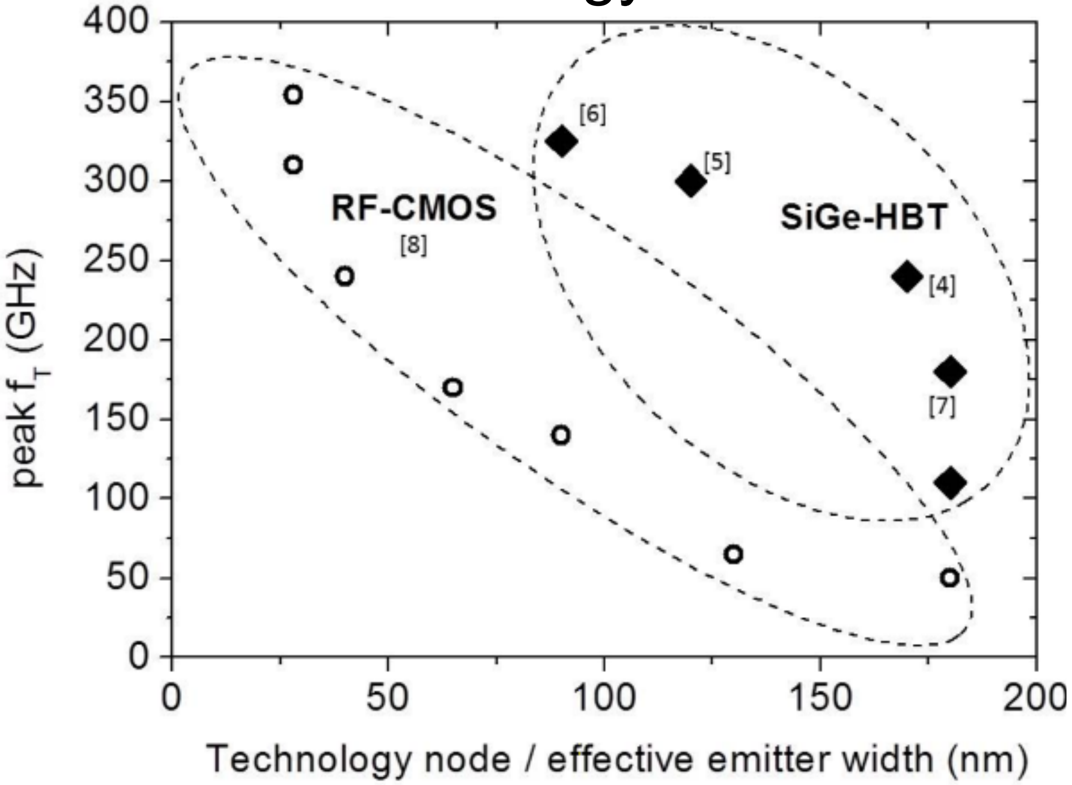
Intrinsic **amplifier jitter**:
common emitter (source) configuration
in a 130nm technology



L. Paolozzi et al.,
Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology, JINST 15 (2020) P11025, https://doi.org/10.1088/1748-0221/15/11/P11025

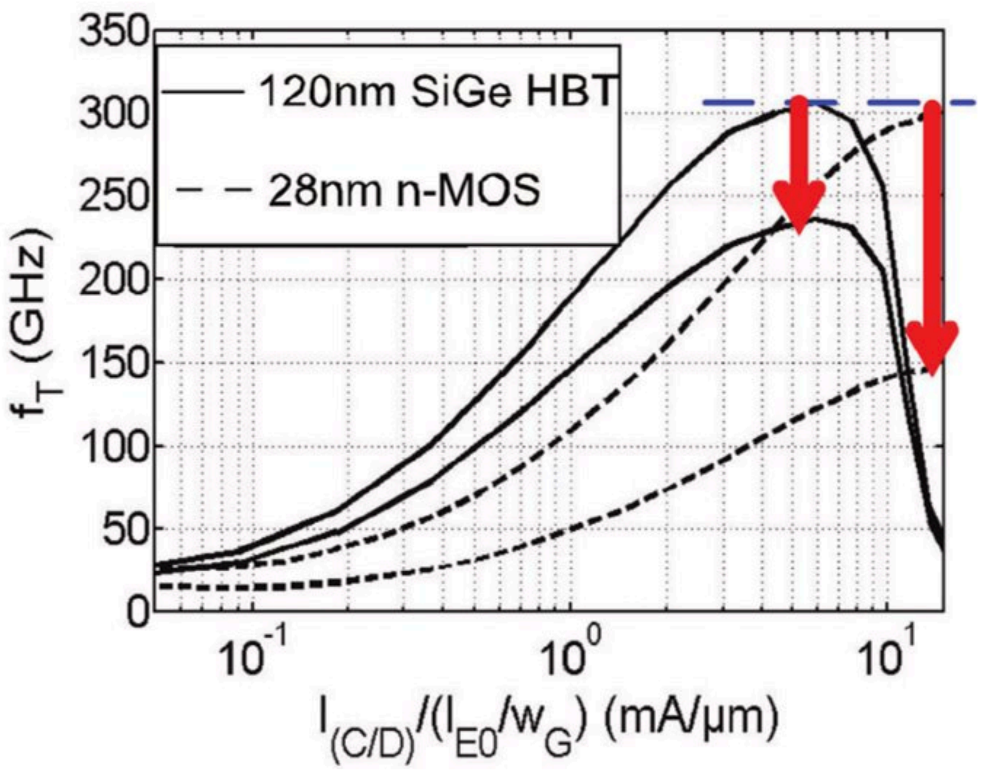
SiGe HBT vs. CMOS

Peak transition frequency vs. technology node



A. Mai and M. Kaynak,
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

Peak transition frequency vs. current density



Robustness to parasitic

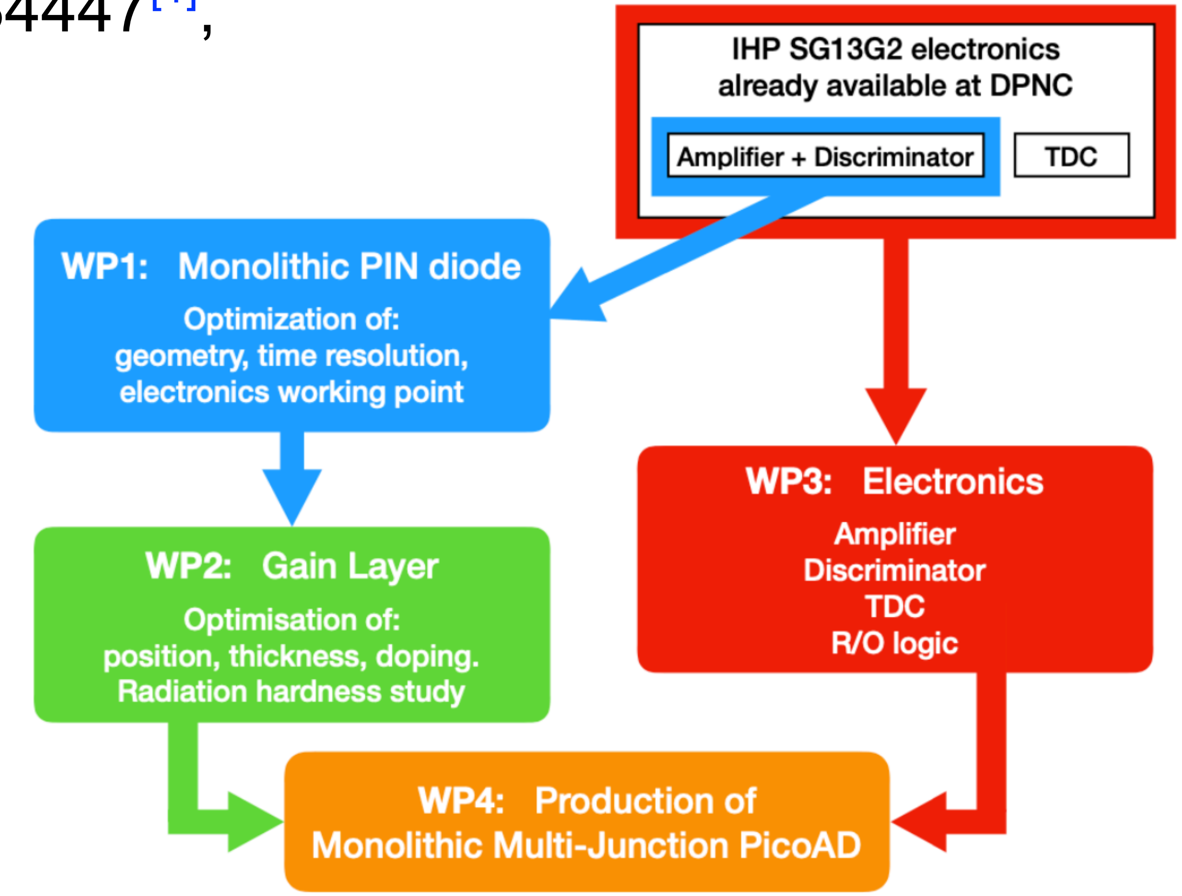
M. Schröter, U. Pfeiffer and R. Jain, Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications.

The MONOLITH ERC Project

- Funded by the H2020 ERC Advanced grant 884447[1], **July 2020 - June 2025**

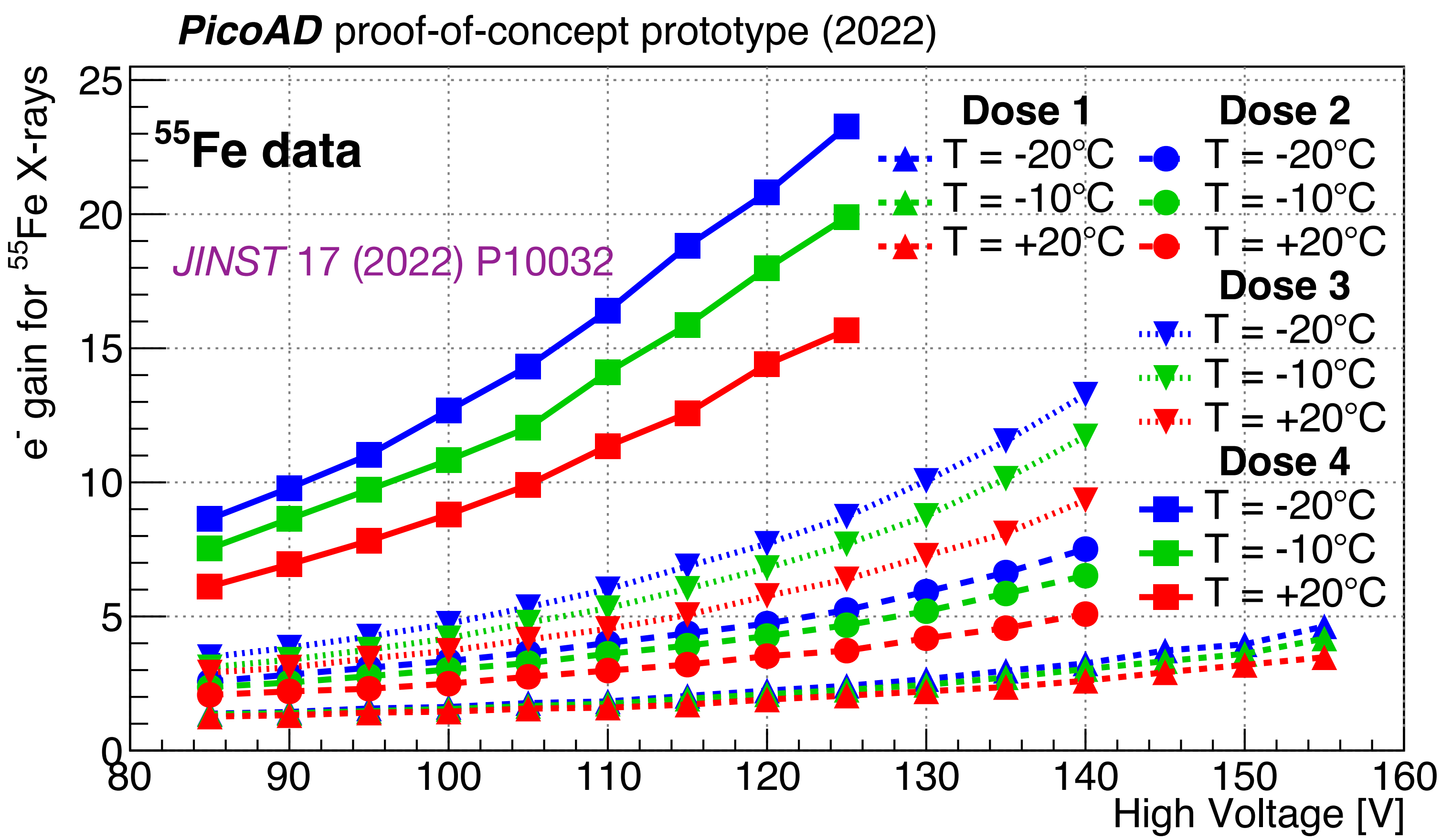
- Monolithic silicon sensor able to:
  - precisely measure 3D spatial position
  - provide picosecond-level time resolution

- Four working packages:
  1. Optimisation of **sensor geometry for timing**
  2. Optimisation of **gain layer, radiation hardness**
  3. Fast and low-noise **SiGe BiCMOS electronics**
  4. Novel sensor concept: the Picosecond Avalanche Detector (**PicoAD**)

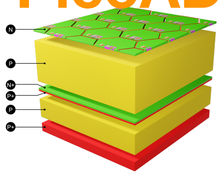


[1] MONOLITH H2020 ERC Advanced Project Web Page - https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/monolith-erc-advanced-project/

Gain Measurement with ^{55}Fe source



PicoAD



A **gain up to ≈ 20 for ^{55}Fe X-rays** obtained at HV = 120 V and T = -20 °C

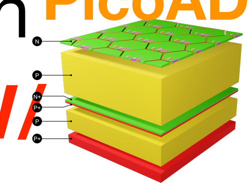
We estimated that ^{55}Fe gain of ≈23 corresponds to **gain 60–70 for a MIP**

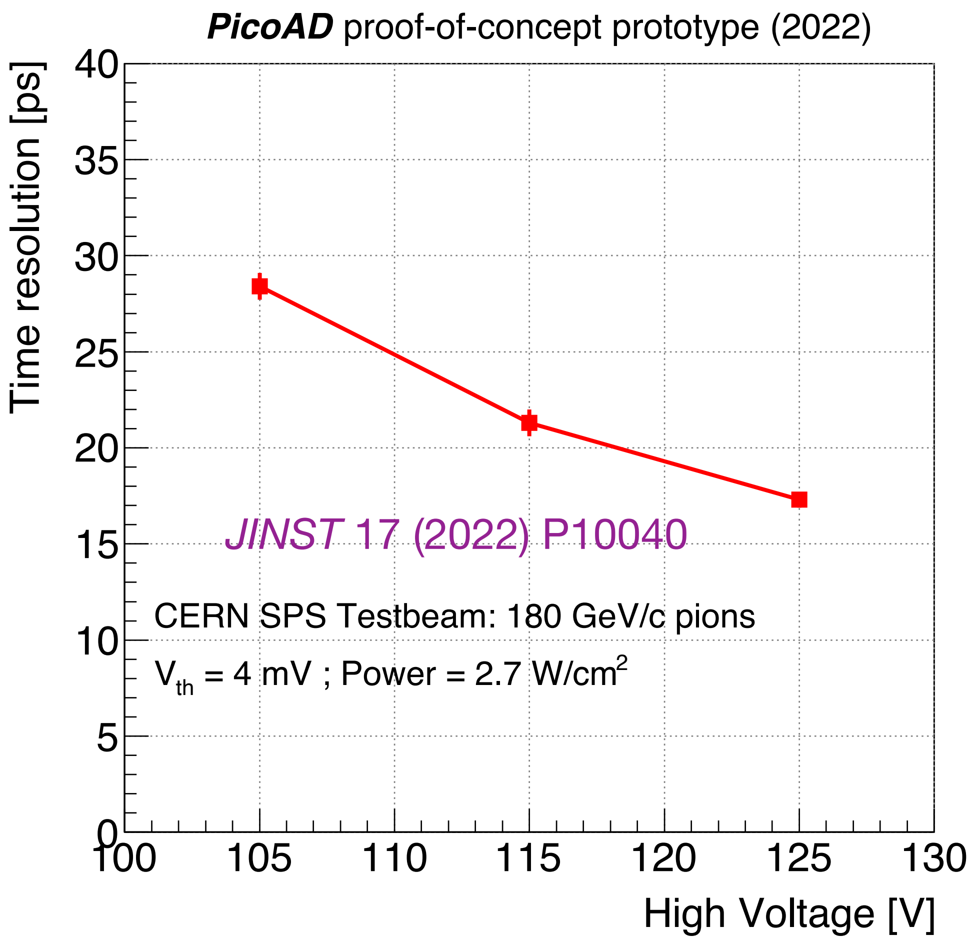
Best performance: (17.3±0.4) ps

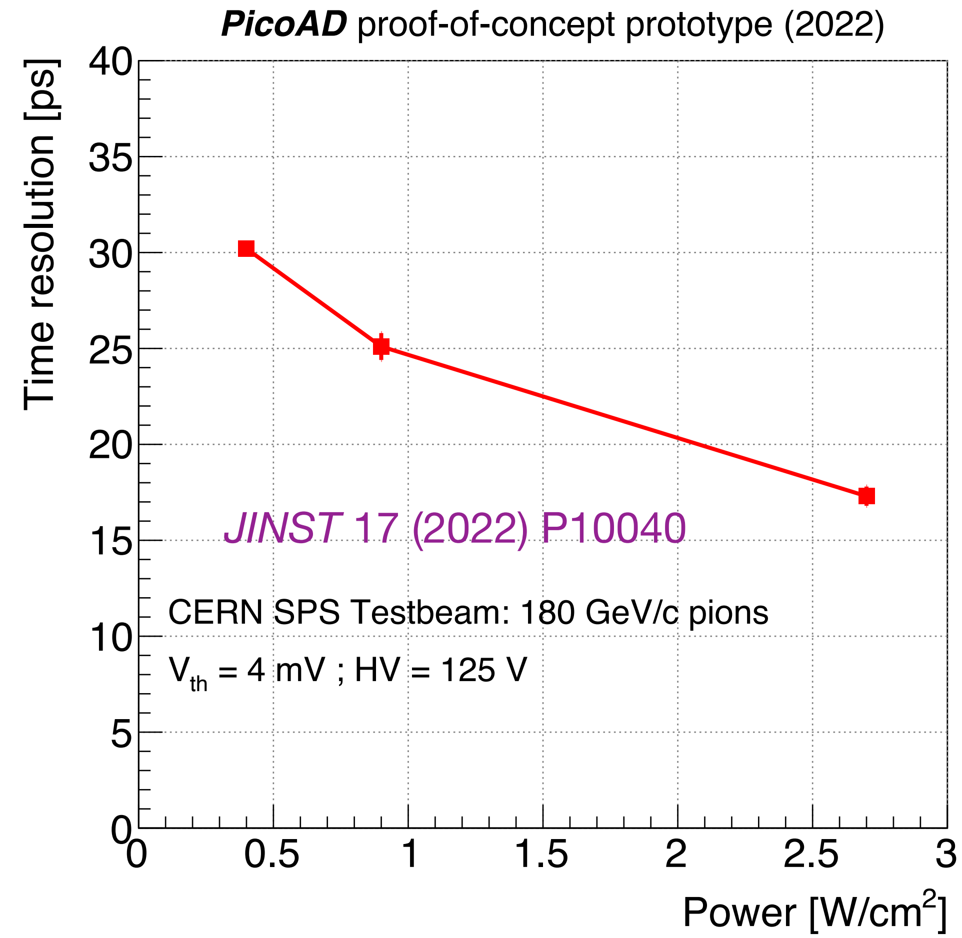
for HV=125 V and Power = **2.7**

Timing resolution of **30 ps** even

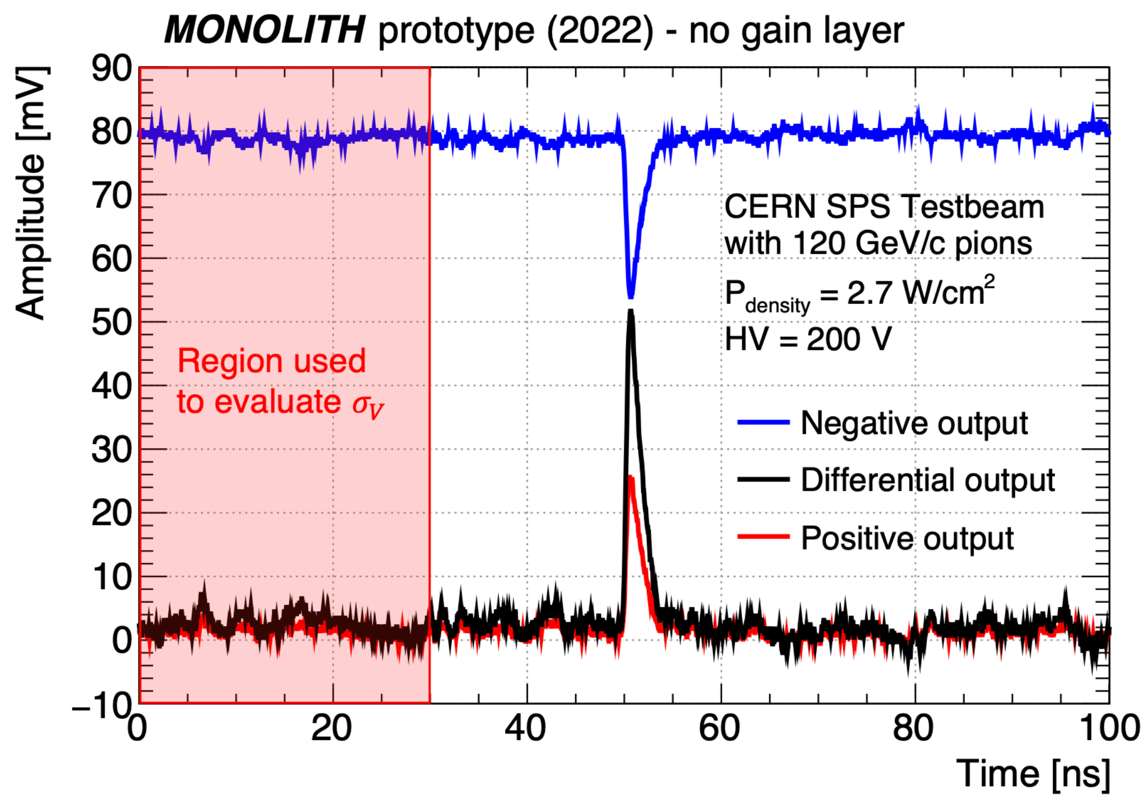
at power consumption of **0.4 W/**





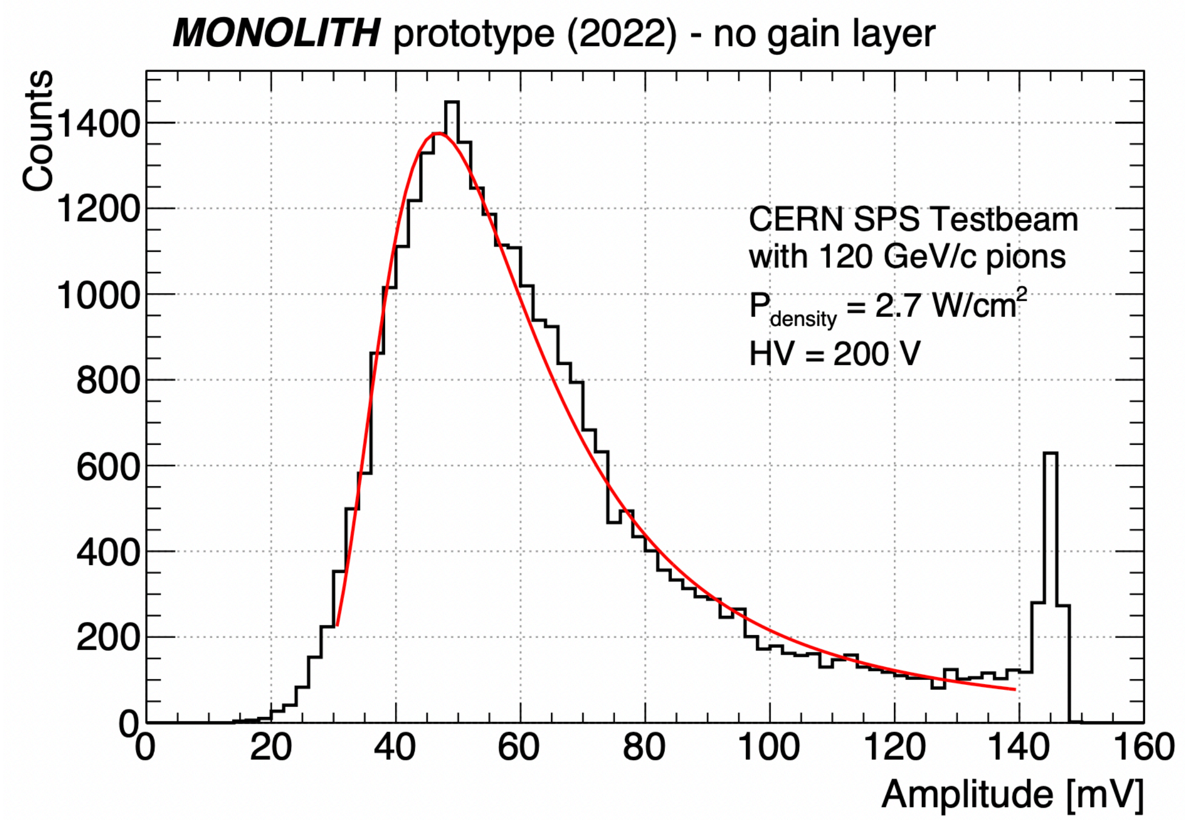


2022 prototype2 — no gain layer



Voltage noise of the differential signal:

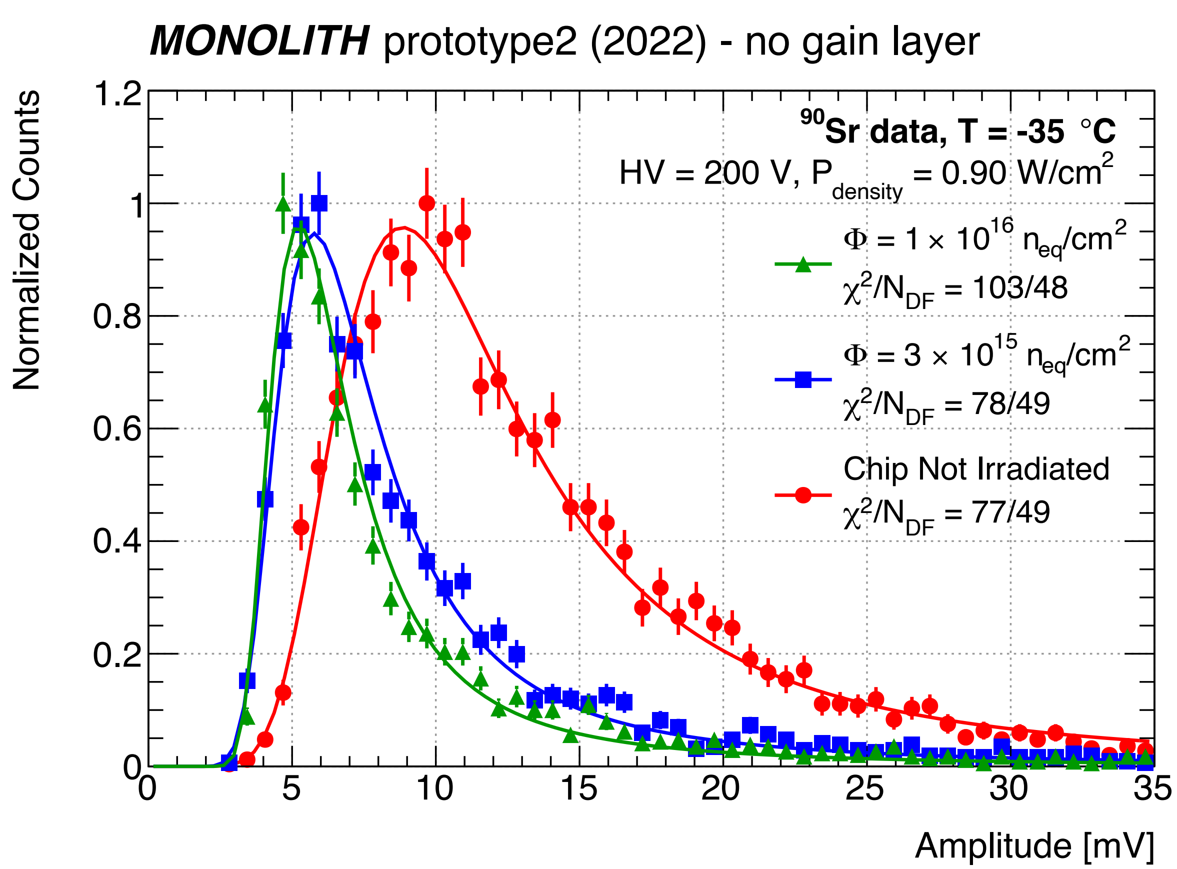
$\sigma_V \approx 1$ **mV**



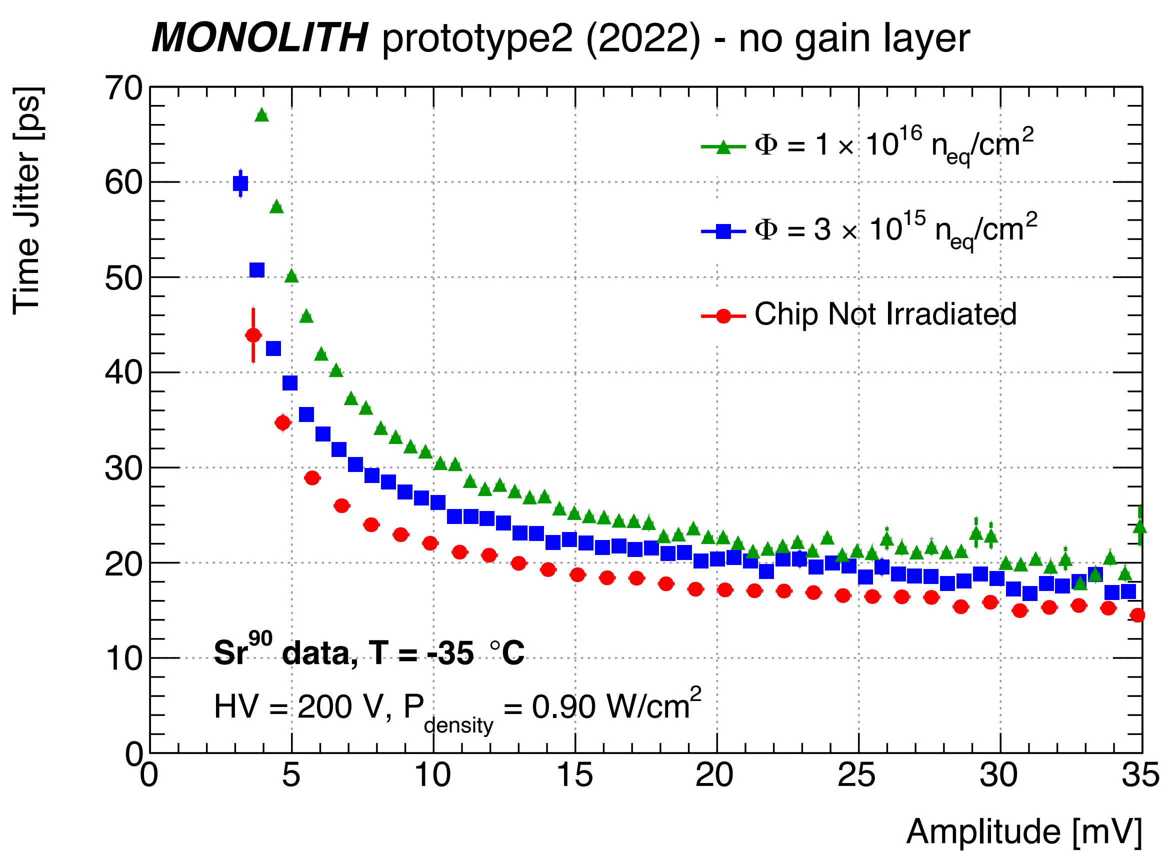
Amplitude distribution of differential signal:

Landau with most probable value ≈ 50 mV

2022 prototype2 — no gain layer



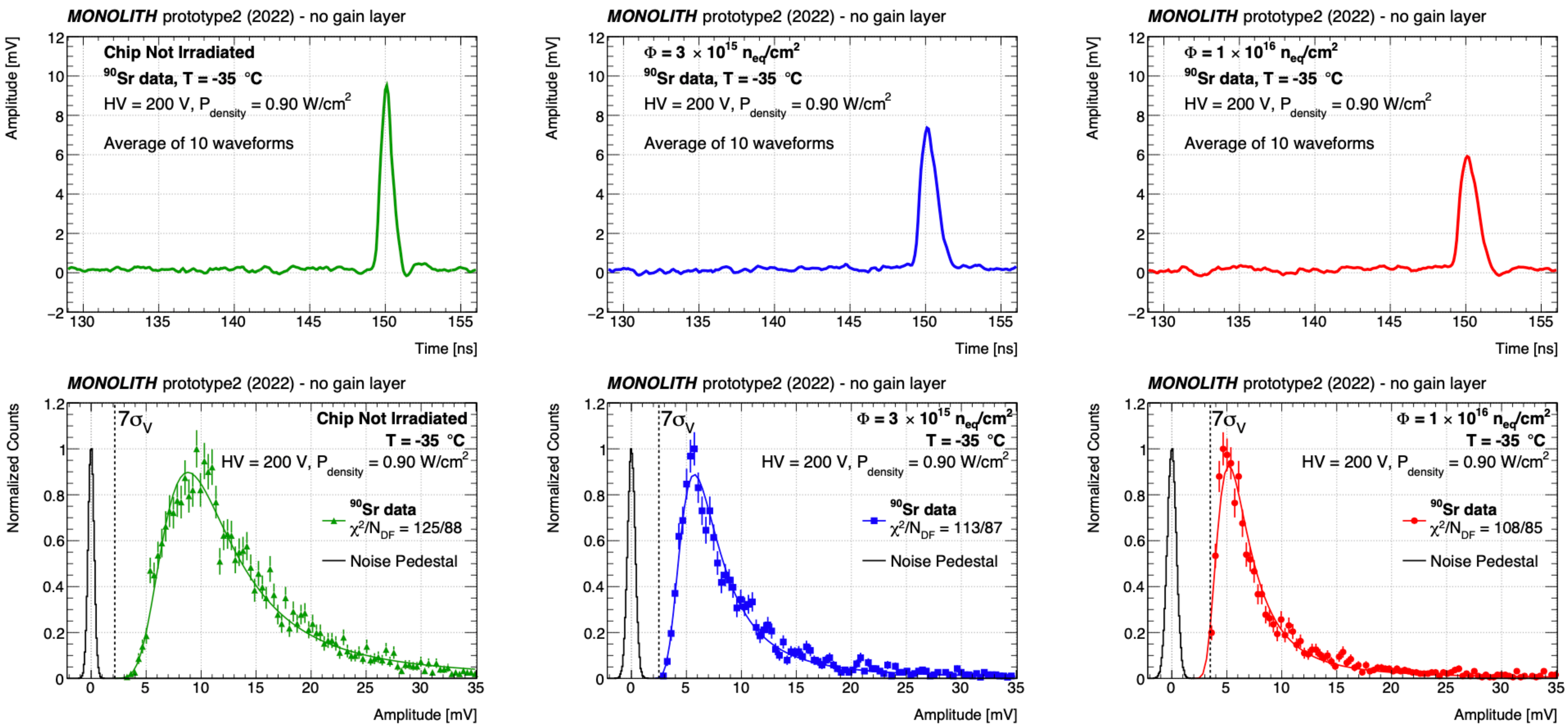
Signal amplitude distributions were fitted with a Landau functional form



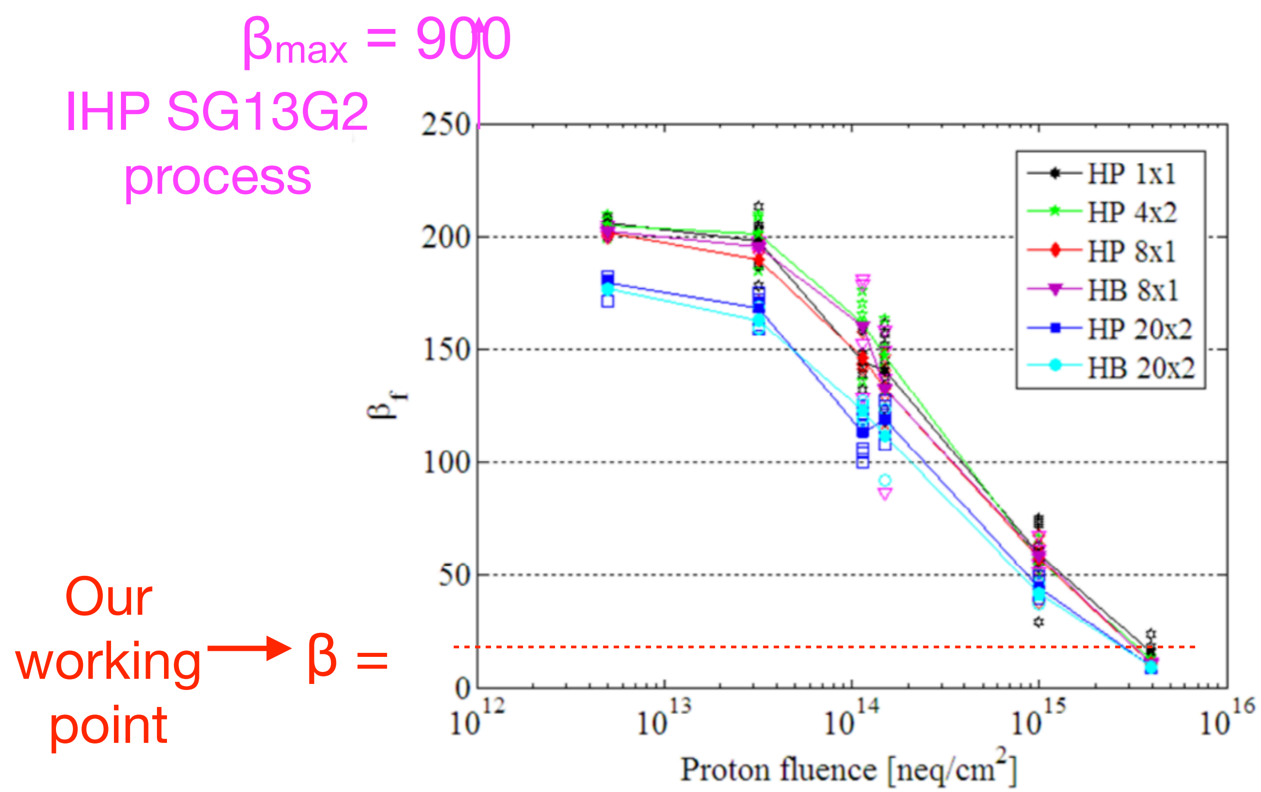
The time jitter ($\sigma_V/_{dV/dt}$) at the mode of the Landau distribution was quoted

(accurate within 10% w.r.t. the testbeam data)

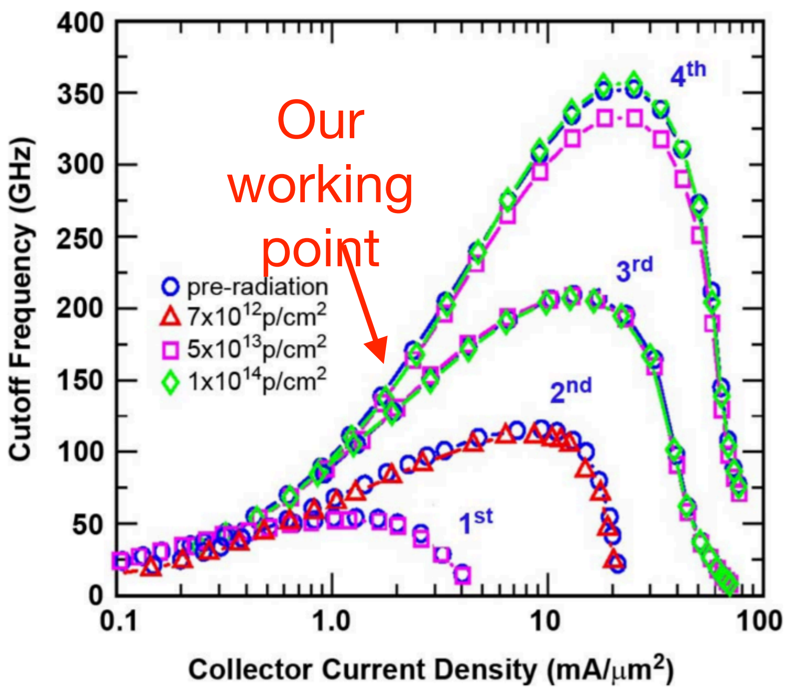
Irradiated chips, 90Sr



Radiation hardness of SiGe HBTs

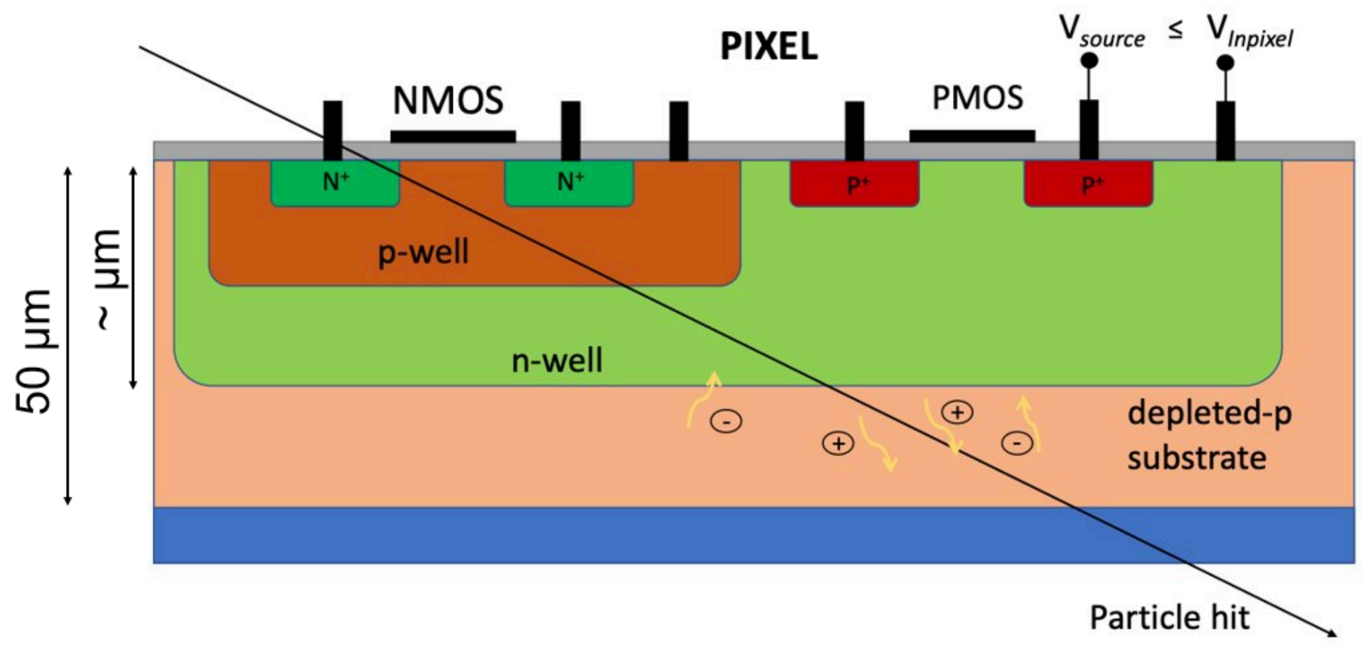


S. Díez et al, IEEE Nuclear Science Symposium & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.



From: J.D. Cressler, IEEE transactions on nuclear science, vol. 60, n. 3 (2013)

Cross section MONOLITH P2



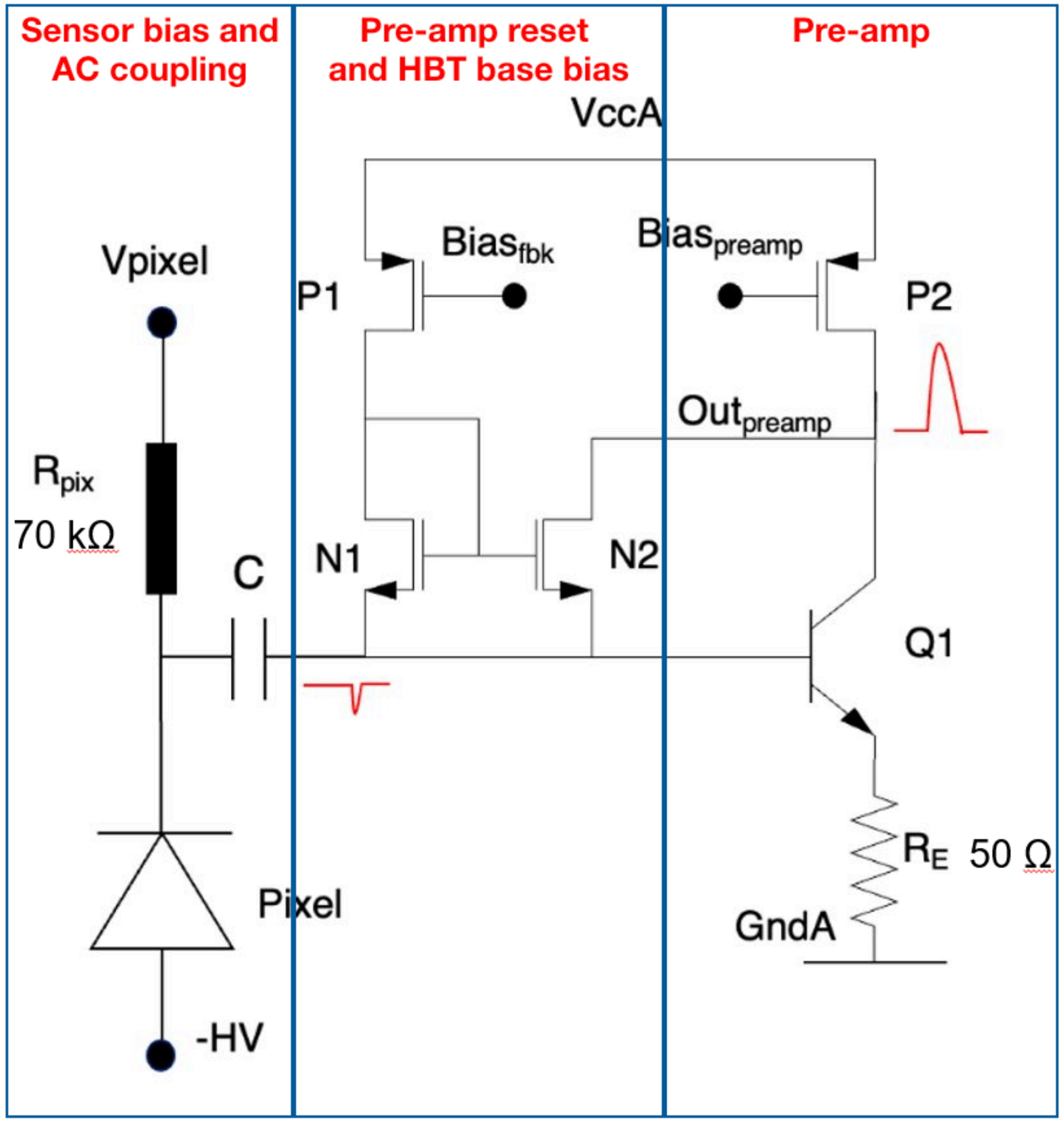
Parasitic capacitance dominated by p-well – n-well junction

Large n-well collection electrode (parallel plates) for uniform electric field

Electronics inside the n-well electrode:

- NMOS in isolated p-well
- PMOS in the collection n-well .
  - Bias condition: $V_{pixel} \approx V_{inpixel} \geq V_{ccA}$

- PMOS in isolated n-well: developed by the foundry, soon available.



Ibias_preamp : 2 µA to 150 µA
Ibias_fbk: nominal 400 nA

Cd = 80 fF
(100 µm pitch, electronics outside thee pixel)