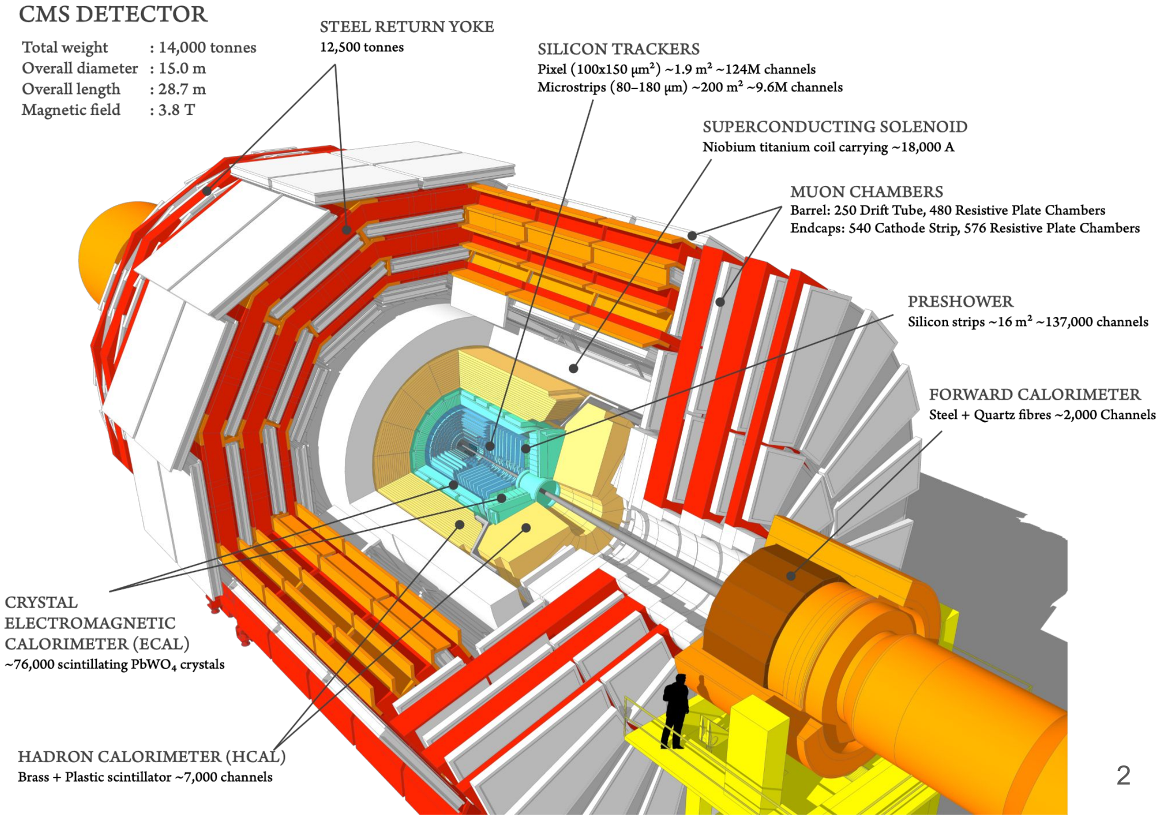
Design and construction of the CMS Inner Tracker for the HL-LHC Upgrade

Alkiviadis Papadopoulos
on behalf of the CMS Tracker Group

CMS Tracker

- Innermost sub-detector of CMS
- Used for reconstruction of charged particle trajectories (tracks)
- Si sensors
- Inside a strong magnetic field
  - Particle momentum and charge determines trajectory
- Two parts:
  - Outer tracker (strips)
  - Inner tracker (pixels)
- Inner tracker was upgraded in 2017 (Phase-1 upgrade)
  - Layers were added to maintain good tracking performance at higher luminosity (2×10^{34} $cm^{-2}s^{-1}$)
- Both inner and outer tracker are being redesigned for HL-LHC (Phase-2 upgrade)

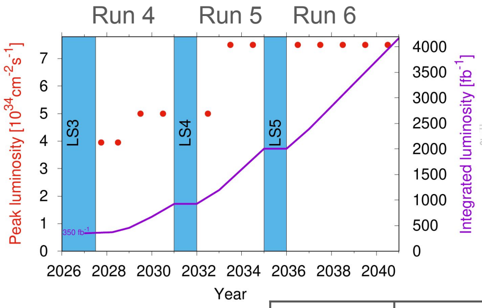
Current detector (Phase-1 upgrade)

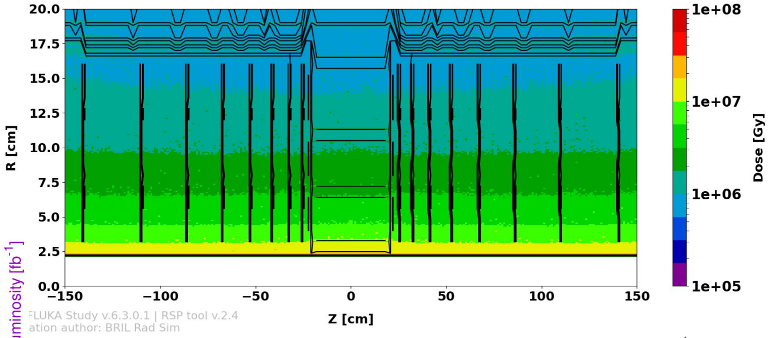


Phase-2 Inner Tracker for HL-LHC

HL-LHC

Inst. luminosity (nominal)	**5 x 10^{34} $cm^{-2}s^{-1}$**
Inst. luminosity (ultimate)	7.5 x 10^{34} $cm^{-2}s^{-1}$
Integrated luminosity	**≥ 3000 fb^{-1}**
Collisions per bunch crossing	140 - **200**





Total absorbed dose in the inner tracker at 3000 fb^{-1}

Requirements:

- **Radiation** tolerance
  - Dose up to ~1 GRad
  - Fluence* up to ~2 x 10^{16} $n_{eq}cm^{-2}$
  - Replacement of inner modules foreseen
- Increased **granularity**
  - Better track separation at high pile-up
- Reduced **material**
- Extended tracking **acceptance** ($|\eta| \leq 4$)
- High **bandwidth** (hit rate up to 3.5 GHz/cm^2)

	RUN 4 (800 fb^{-1})		**RUN 5 (1300 fb^{-1})**		**RUN 4+5 (2100 fb^{-1})**		**RUN 4+5+6 (3000 fb^{-1})**	
	Fluence	Dose	Fluence	Dose	Fluence	Dose	Fluence	Dose
TBPX L1	0.69	0.36	1.12	0.58	**1.81**	**0.93**	2.58	1.34
TBPX L2	0.18	0.11	0.29	0.17	0.48	0.28	0.68	0.40
TFPX R1	0.46	0.31	0.75	0.49	1.22	0.79	1.74	1.13
TFPX R2	0.21	0.14	0.35	0.23	0.57	0.37	0.82	0.53

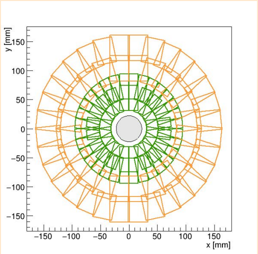
Maximum fluence* ($10^{16}n_{eq}cm^{-2}$) and dose (GRad) by layer/ring

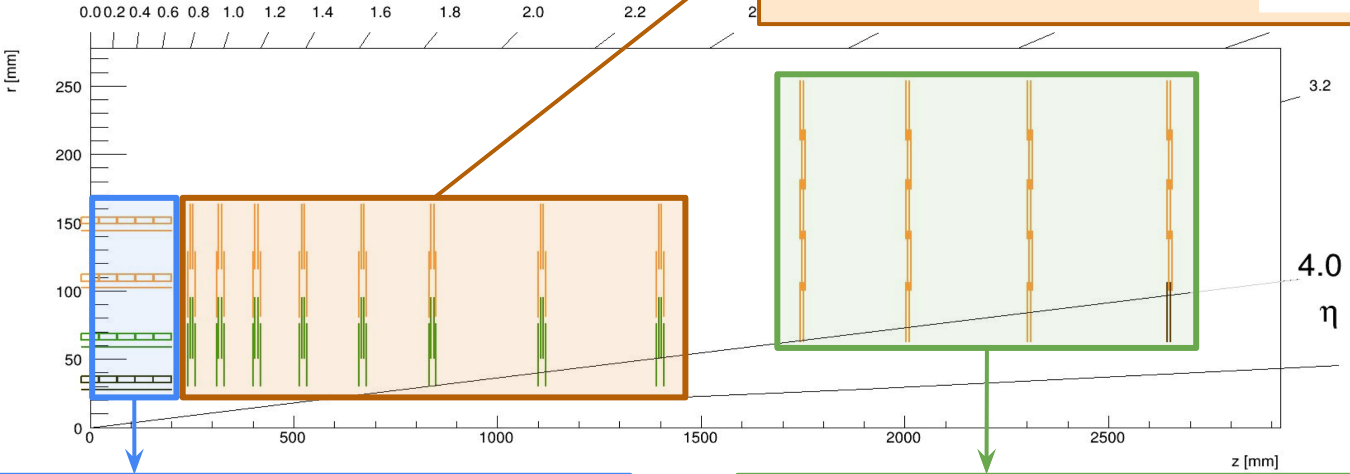
*: 1 MeV neutron equivalent

Phase-2 IT Layout

Forward disks (TFPX)

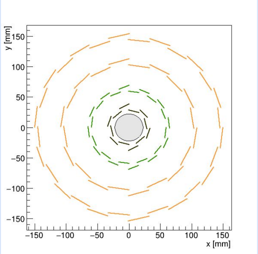
- ➢ 2 sides x 8 disks x 4 rings
- ➢ 1728 modules
- ➢ 1x2 modules in rings 1,2
- ➢ 2x2 modules in rings 3,4





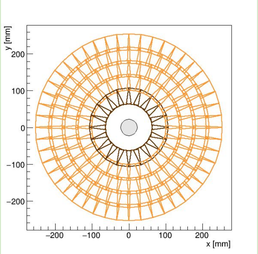
Barrel (TBPX)

- ➢ 4 layers
- ➢ 756 modules
- ➢ 3D sensors in layer 1
- ➢ 1x2 modules in layers 1, 2
- ➢ 2x2 modules in layers 3, 4



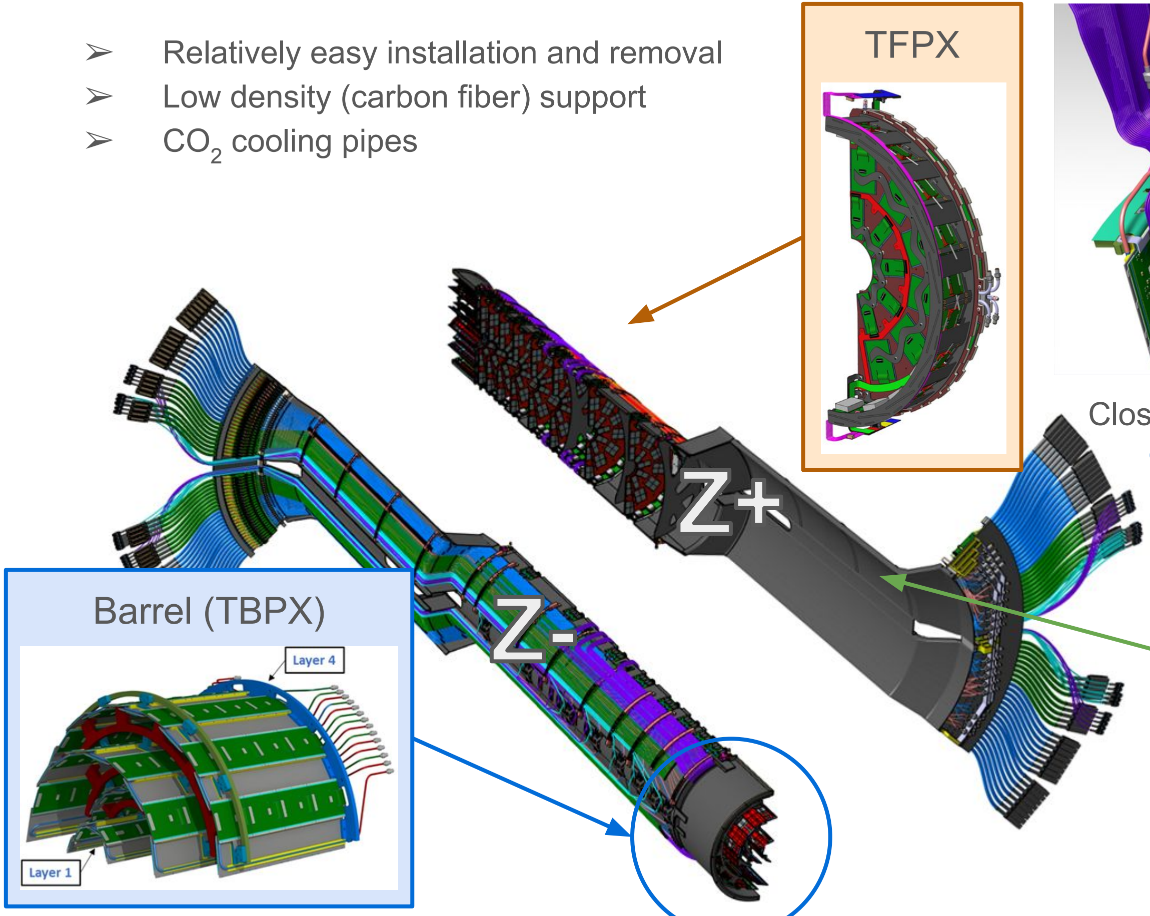
Endcaps (TEPX)

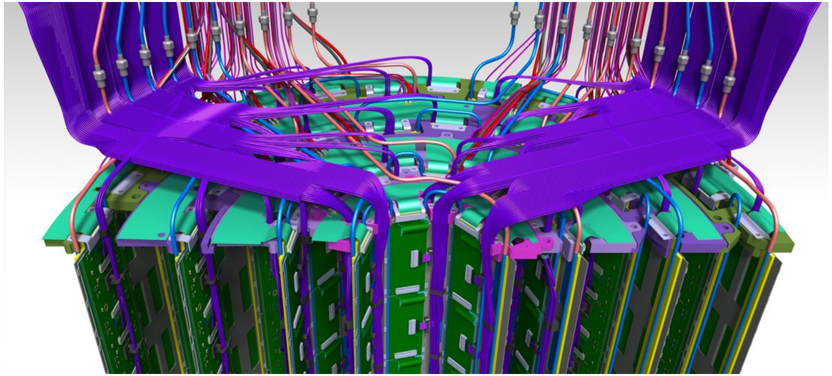
- ➢ 2 sides x 4 disks x 5 rings
- ➢ 1408 modules
- ➢ 2x2 modules everywhere
- ➢ Ring 1 used for luminosity measurement



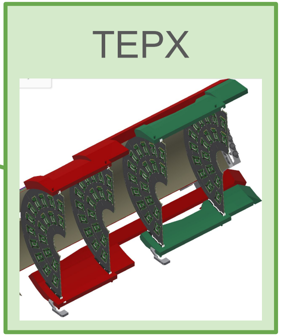
Mechanical structure

- Relatively easy installation and removal
- Low density (carbon fiber) support
- CO_2 cooling pipes



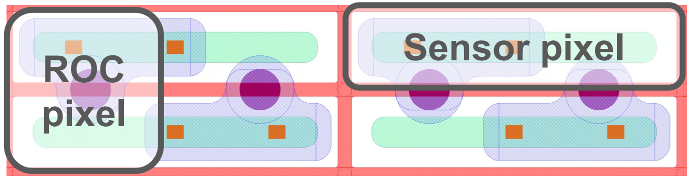


Close-up view of the barrel showing modules, e-links, cooling loops, flex, high voltage, serial power

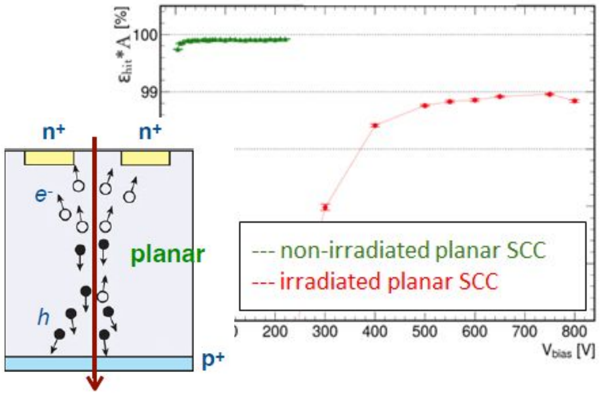


Sensors

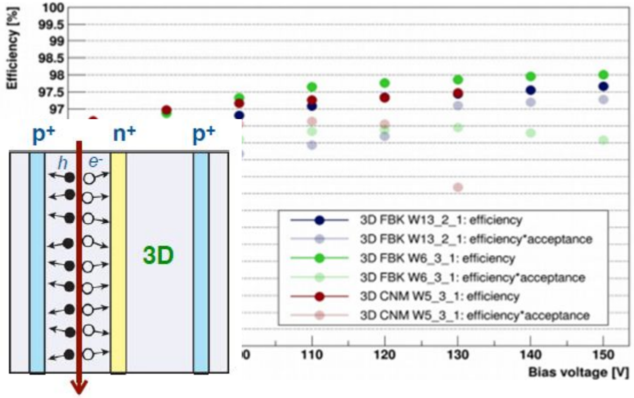
- ➢ Rectangular pixels (25 x 100 µm) everywhere
  - 100 µm in beam direction to match longer clusters in barrel mid-rapidity
  - Square pixels offer small to no improvement
- ➢ Planar (n-in-p, 150µm bulk thickness)
  - **High hit efficiency (>99%)**
- ➢ 3D
  - Slightly less efficient (up to 98%)
  - **High margin for thermal stability**
  - **Lower bias voltage**
- ➢ Barrel layer 1 requires 3D sensors for thermal stability after irradiation
- ➢ Planar sensors are used everywhere else for higher efficiency



Rectangular sensor pixels are bump bonded to square ROC pixels according to this pattern



Hit efficiency after irradiation ($1x10^{16}$ $n_{eq}cm^{-2}$)

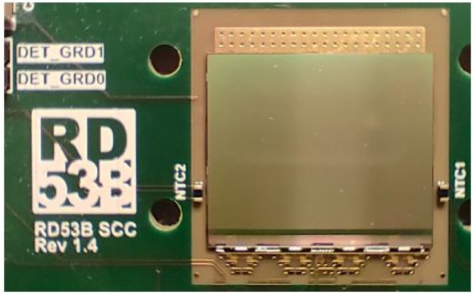


Read-Out Chip (ROC)

- Designed by the RD53 collaboration between ATLAS & CMS
- Main goals:
  - **Hybrid** design (independent sensor R&D)
  - Increased **granularity** (smaller pixels)
  - High **hit rate**
  - **Radiation** tolerance
- **RD53A** was the first **demonstrator** chip:
  - Submitted in 2017
  - Half-size
  - 3 different AFE designs on the same chip
- RD53B-CMS (aka. **CROCv1**) was the **pre-production** prototype:
  - Submitted in 2021
  - Full size
  - CMS-specific (ATLAS flavor also available)
  - Linear AFE
- RD53C-CMS (aka. **CROCv2**) is the **final** CMS version:
  - Submitted in Oct. 2023
  - Many improvements and bug fixes but functionally similar to CROCv1

RD53A

CROCv1



CROCv1

Configuration memory:
~1446 bits global
+ 8 bits per pixel

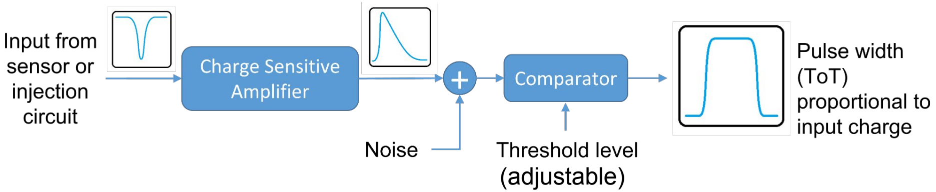
- Mixed-signal IC (digital & analog)
- Linear Analog Front-End (AFE):
  - Low threshold (< 1000 e-)
  - Time Over Threshold (ToT) linear w.r.t charge
- High bandwidth
  - Multi-lane output
  - Event data compression
  - Can receive and forward data to/from each other (data-merging)
- Radiation tolerance
  - Good performance up to ~1 GRad
  - Triplicated registers
  - SEU detection

- Highly configurable
  - Pixel masking
  - Global threshold and ToT gain
  - Per-pixel threshold adjustment
  - Input/output merging & routing
- Calibration & monitoring
  - Charge injection circuit
  - Radiation and temperature sensors
  - Internal voltage/current monitoring
- Testing
  - Bit error rate (PRBS)
  - Error counters
  - Design for test logic with scan chain

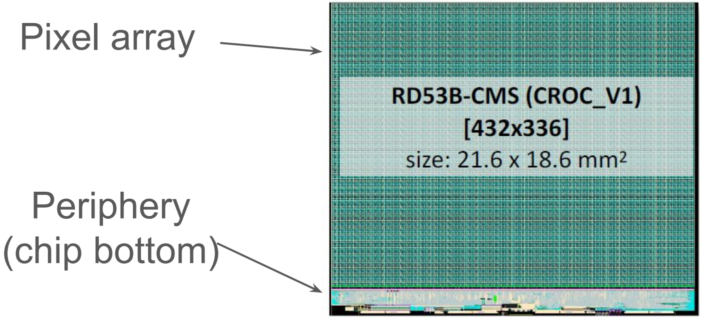
Specifications

Pixel size	50 x 50 μm^2
Process	65 nm (TSMC)
Hit rate	3.5 GHz/cm^2
Trigger rate	750 kHz
Readout latency	12.5 μs (500 BX)
Output bandwidth	1-4 x 1.28 Gbps
Power consumption	< 1W / cm^2

Overview of AFE operation



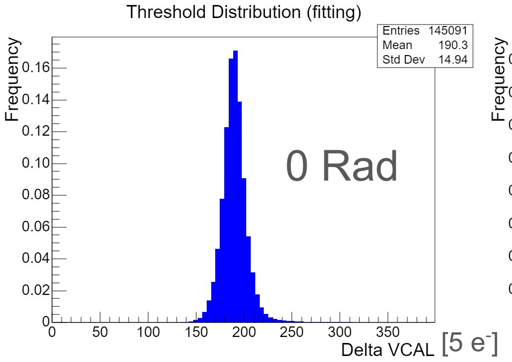
Floorplan

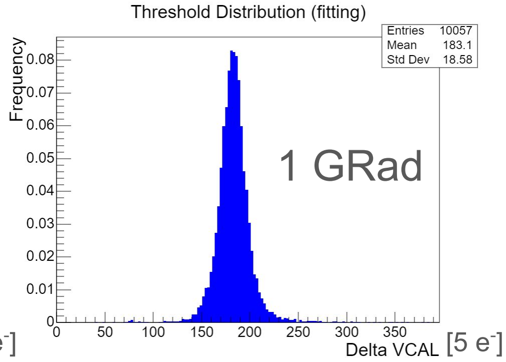


CROCv1 Results

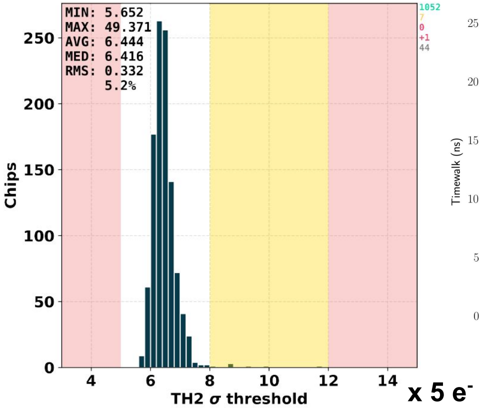
- ➢ Extensively tested and characterized
- ➢ AFE measurements
  - ○ Threshold & noise
  - ○ ToT Gain
  - ○ Hit detection delay (time-walk)
  - ○ Threshold dispersion
  - ○ Noise occupancy (spontaneous hits)

  (Threshold & noise, ToT Gain, Hit detection delay: Per pixel; Threshold dispersion, Noise occupancy: Global)
- ➢ Several irradiation campaigns
  - ○ Different sources (X-rays, various beams)
  - ○ With and without sensor
  - ○ Reaching up to ~1 GRad
  - ○ Non-uniform with different gradients
- ➢ Test-beams
- ➢ Wafer-level testing
  - ○ Custom probing setup
  - ○ Comprehensive and fast testing procedure

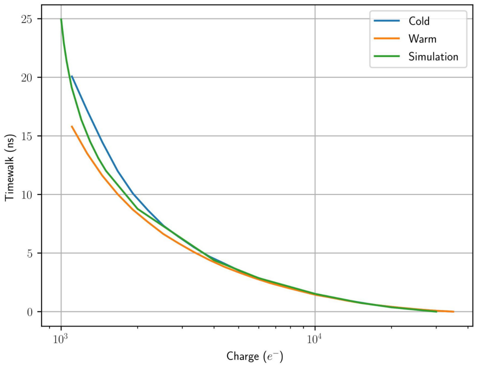




Threshold dispersion distribution (1104 unirradiated chips)



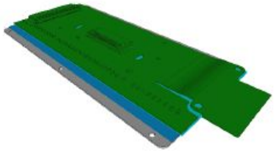
Time-walk measurement & simulation



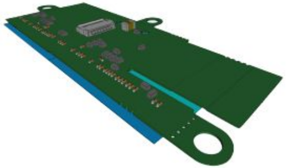
Modules

- ROCs are **bump bonded** to the sensor
- Passive **High Density Interconnect** (HDI)
  - Glued to the sensor with **diamond-doped glue**
  - Wire-bonded to the ROCs
- **Parylene coating**
  - Protects wire-bonds
  - Sensor bias voltage to ROC spark protection
- 2 sizes:
  - **1x2** (2 ROCs)
  - **2x2** (4 ROCs)
- Different design per sub-detector

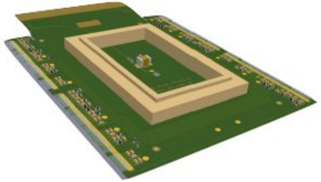
TBPX 1x2



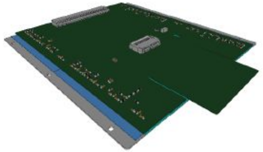
TFPX 1x2



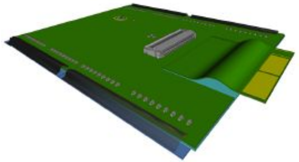
TEPX 2x2

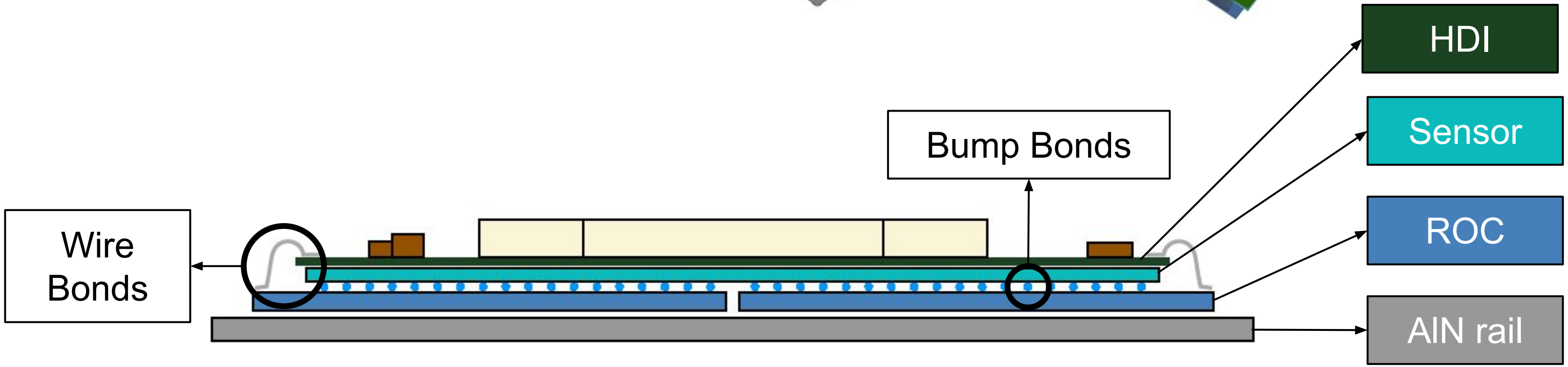


TBPX 2x2



TFPX 2x2





Optical readout

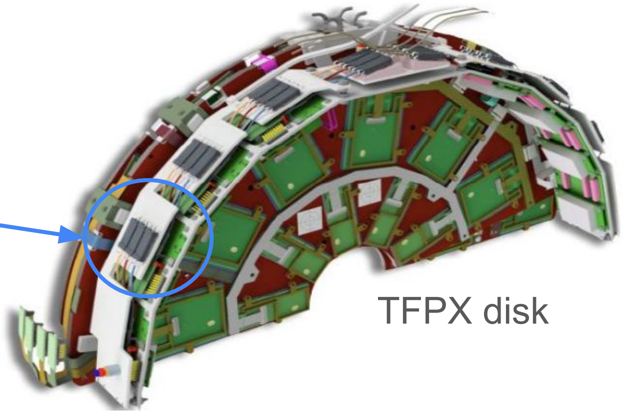
Front-End:

- ➢ Optical links are used to minimize materials
- ➢ The **portcard** acts as a bridge between electrical and optical links
- ➢ Each portcard has 3 LpGBT ASICs
- ➢ Each LpGBT is connected to:
  - ○ up to 7 electrical outputs @ 160 Mbps (downlinks)
  - ○ up to 7 electrical inputs @ 1.28 Gbps (uplinks)
  - ○ 1 optical TRx @ 10 Gbps (VTRx+)

Back-End:

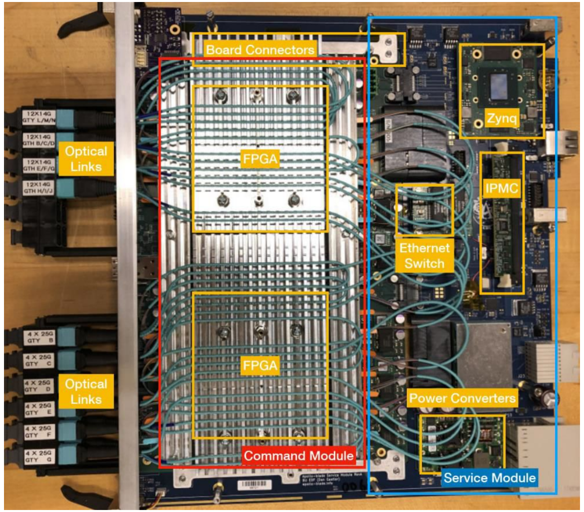
- ➢ DTC (Data, Control and Trigger)
  - ○ ACTA board (Apollo)
  - ○ 2 x FPGAs + CPU
  - ○ 72 optical links to the Front-Ends (FE)
  - ○ 16 x 25 Gb/s links to DAQ (event data)
  - ○ 8x25Gb/s links for luminosity monitoring

Portcard



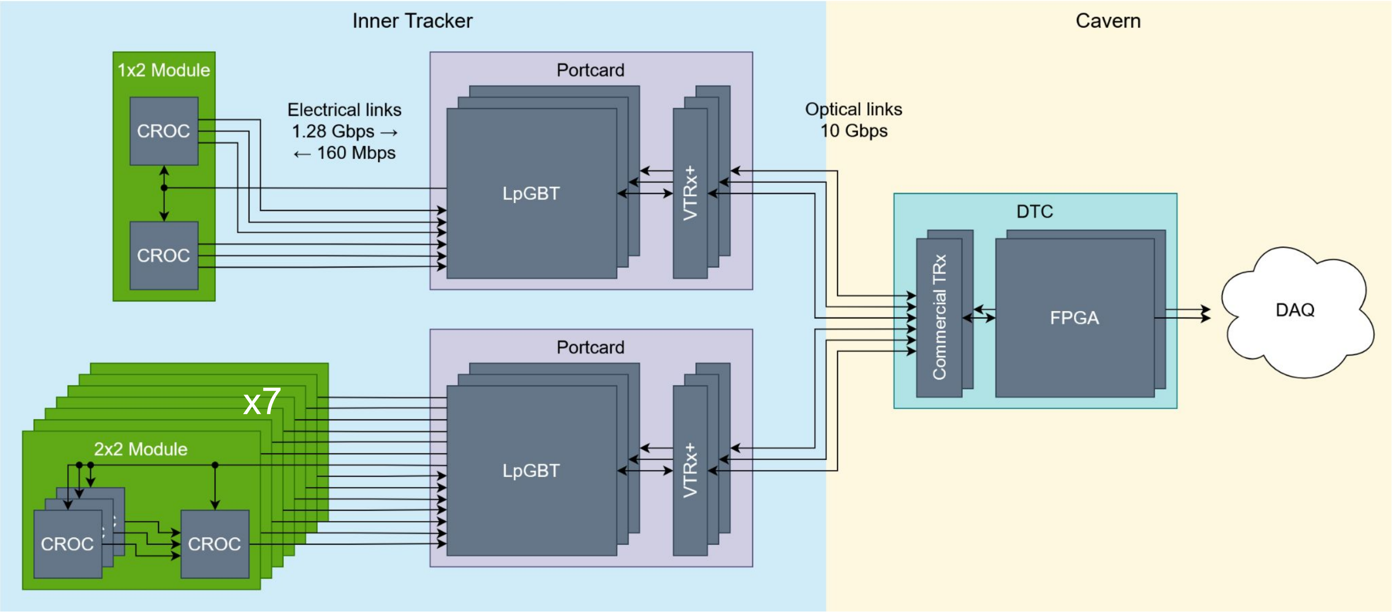
TFPX disk

DTC (Apollo)



System data flow

- Portcards in TFPX and TEPX
- Adaptable bandwidth
  - From 0.25 to 4 uplinks per CROC (0.32 to 5.12 Gbps)
  - 1 downlink per module (160 Mbps)



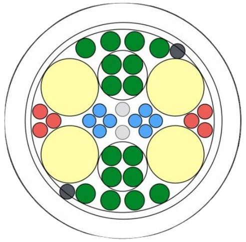
Output links per module

TBPX	Layer 1	6
	Layer 2	2
	Layer 3	2
	Layer 4	1
TFPX	Ring 1	3
	Ring 2	3
	Ring 3	2
	Ring 4	2
TEPX	Ring 1	4
	Ring 2	3
	Ring 3	2
	Ring 4	2
	Ring 5	1

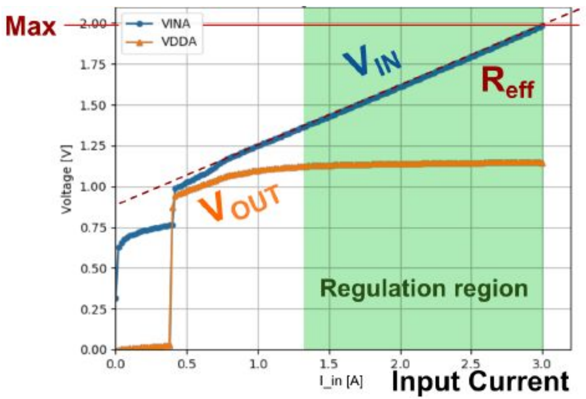
Power system

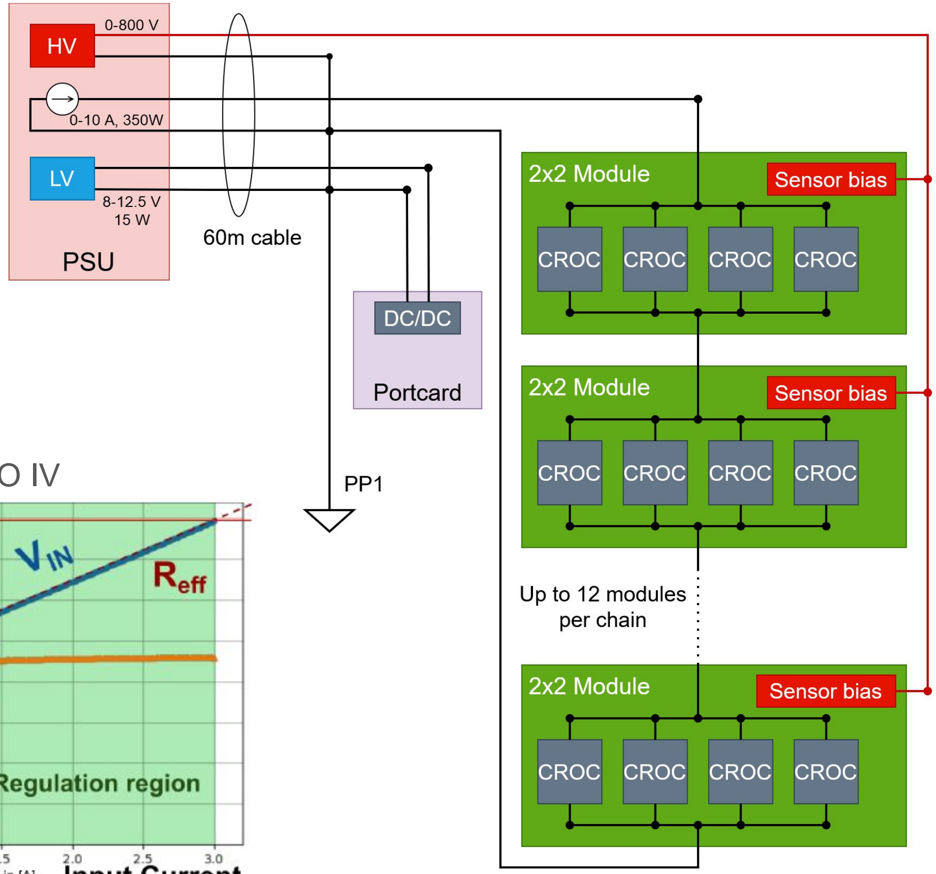
- Serial powering
  - Up to 12 modules in series
  - Low power loss in the transmission lines
  - Minimal cable mass
  - No rad-hard DC-DC converter required
- On-chip Shunt-LDO (SLDO)
  - Voltage regulator (1.2 V)
  - Shunt dissipates excess power
- On-chip protection mechanisms prevent failure scenarios (eg. overvoltage protection)
- 260 x 2 Power Supply Units (PSU) in total

Cable cross-section



SLDO IV

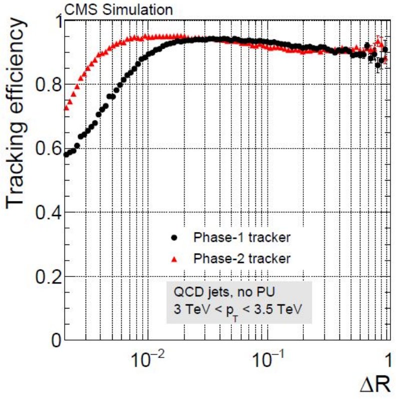




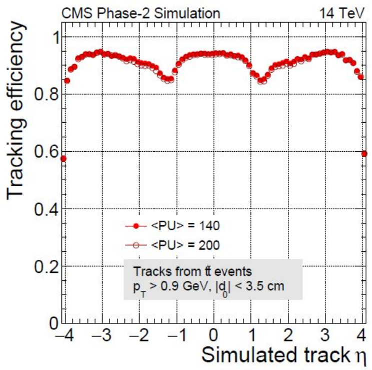
Performance

- ➢ Offline simulation with CMSSW
- ➢ Significant improvements in efficiency and resolution
- ➢ High efficiency and low fake rate for PU up to 200

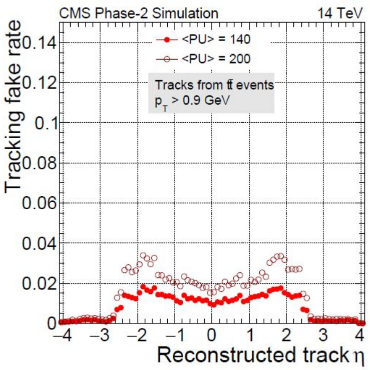
Efficiency vs. track distance from nearest track



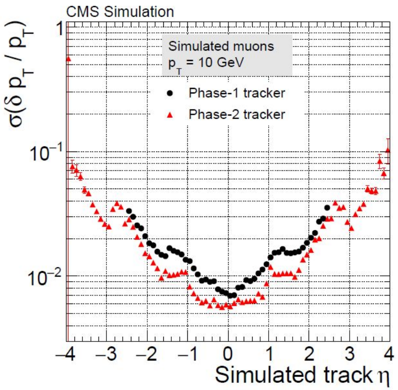
Efficiency



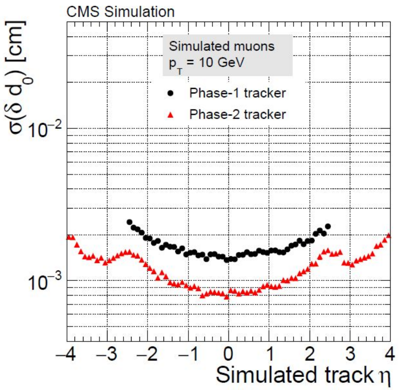
Fake rate



p_T resolution



d_0 resolution

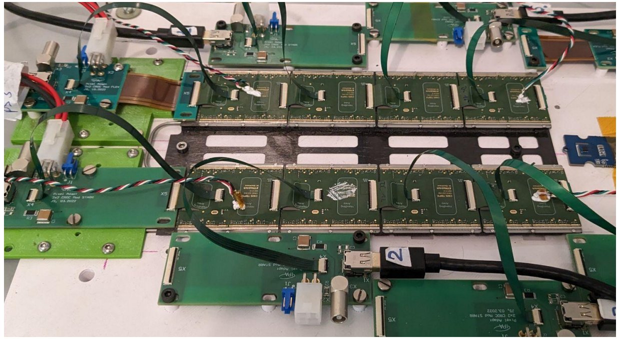


Conclusions

- The Inner Tracker has been redesigned for HL-LHC
  - New sensors and readout electronics
  - High granularity (more layers, more and smaller pixels)
  - Reduced material
  - Increased acceptance (from 3 to 4)
- Simulation shows promising results
- Extensively tested in the lab and in test-beams
  - At various levels of integration (from individual components to complete demo setups)
- The final readout chip was submitted in October
  - ATLAS flavor already successfully tested
  - Design and testing phases are mostly over
- Phase-2 upgrade installation during LS3
  - Jan. 2026 - April 2029

Thank you!

TBPX ladder demo setup



LHC Schedule