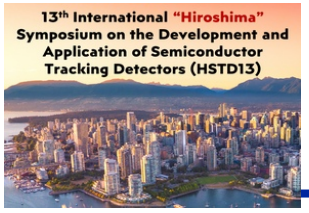
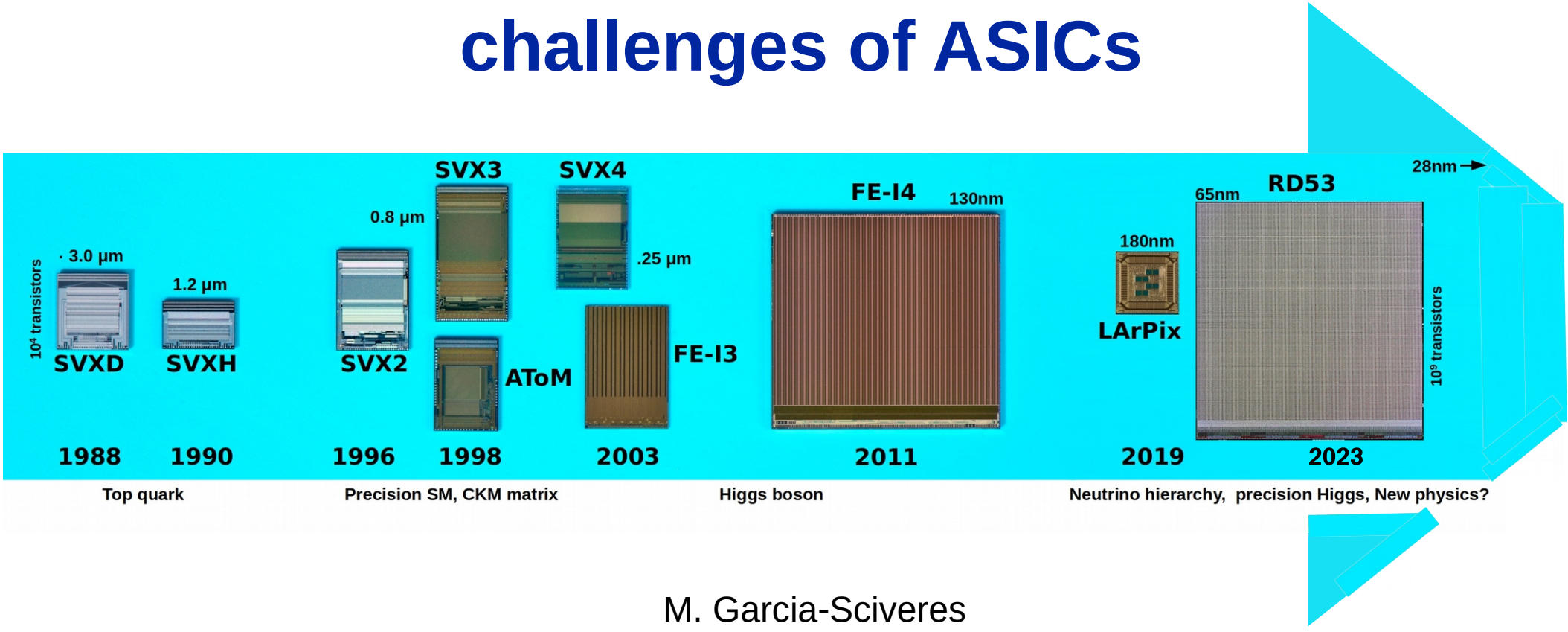


Future directions and challenges of ASICs

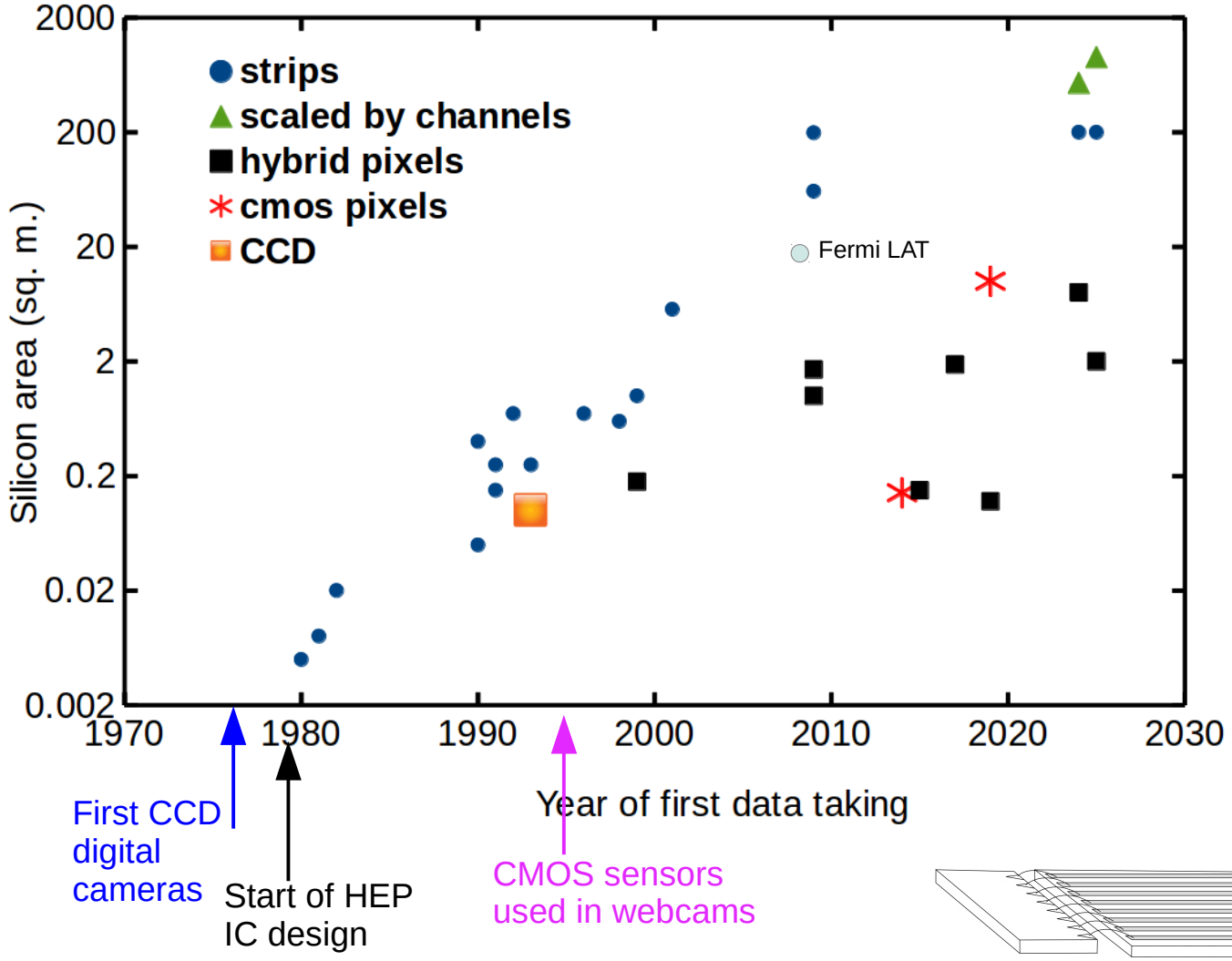


M. Garcia-Sciveres
Lawrence Berkeley National Lab

2023 HSTD13 – Vancouver

Silicon Detectors at Colliders

(and in orbit)



Strip Detectors

1980	NA1
1981	NA11
1982	NA14
1990	MarkII
1990	DELPHI
1991	ALEPH
1991	OPAL
1992	CDF SVX
1993	L3
1996	CDF SVX'
1998	CLEO III
1999	BaBar
2001	CDF SVXII+ISL
2009	ATLAS SCT
2009	CMS tracker
2025	ATLAS ITK
2025	CMS upgrade

Hybrid Pixels

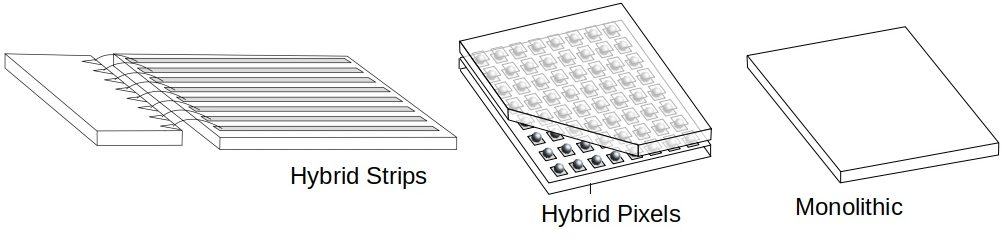
1999	Delphi
2009	ATLAS
2009	CMS
2015	ATLAS IBL
2017	CMS
2019	velopix
2025	ATLAS
2025	CMS

CMOS Pixels

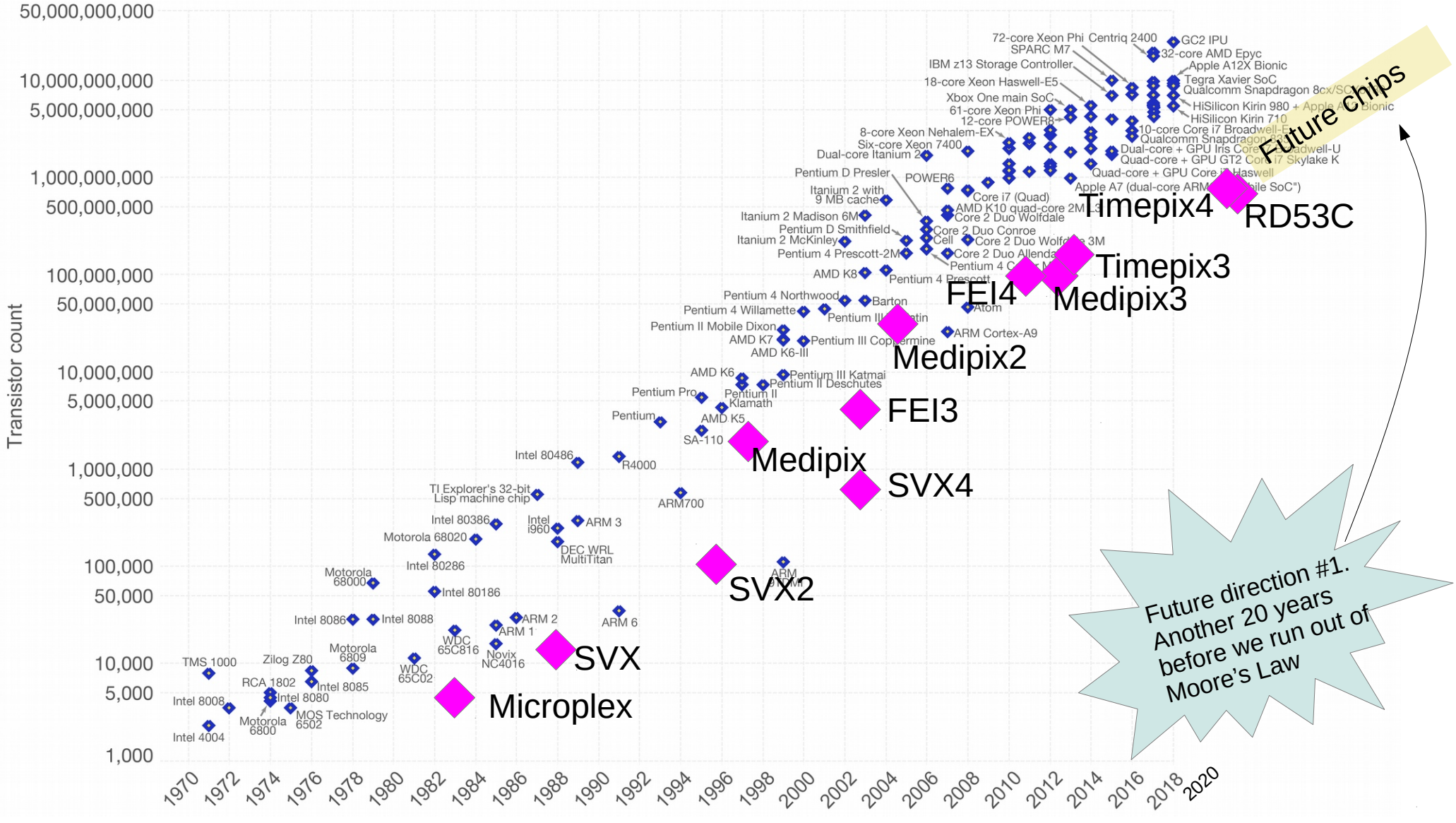
2014	STAR
2019	ALICE

CCDs

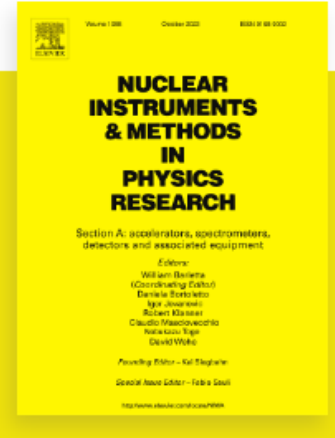
1993	VXD



Tracker ICs vs Microprocessors



Aside: This Just Out:



Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

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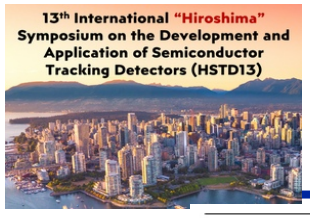
Microelectronics in High Energy Physics

Edited by

- Alessandro Marchioro Experimental Physics,CERN,Switzerland
- Philippe Farthouat Experimental Physics,CERN,Switzerland

Last update 21 August 2023



Aside: Contents

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

Particle physics experiments: From photography to integrated circuits

Erik H.M. Heijne *

IEAP/CTU, Husova 240/5, CZ 110 00 Prague 1, Czech Republic
CERN EP Dept, 1 Esplanade des Particules, CH 1211 Geneva 23, Switzerland
Nikhef, Science Park 105, 1098XG Amsterdam, Netherlands

Front-end electronics for silicon strip trackers: Architectures and evolution

Jan Kaplon

CERN, 1211 Geneva 23, Switzerland

Hybrid pixel readout integrated circuits

Maurice Garcia-Sciveres

Lawrence Berkeley National Laboratory, Berkeley, USA

Monolithic CMOS Sensors for high energy physics — Challenges and perspectives

W. Snoeys

CERN, Esplanade des Particules, CH-1211 Geneva 23, Switzerland

ASIC survival in the radiation environment of the LHC experiments: 30 years of struggle and still tantalizing

Federico Faccio

CERN, EP department, Esplanade des Particules 1, Meyrin, 1211, Switzerland

Radiation tolerant optoelectronics for high energy physics

Jan Troska [a,*], François Vasey [a], Anthony Weidberg [b]

[a] *EP Department, CERN, Esplanade des Particules, Geneva, 1211, Switzerland*
[b] *Physics Department, Oxford University, Denys Wilkinson Building, Oxford, OX1 3RH, United Kingdom*

ASICs for LHC intermediate tracking detectors

G. Hall [a,*], A.A. Grillo [b]

[a] *Blackett Laboratory, Imperial College, London SW7 2AZ, UK*
[b] *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA 95064, USA*

Cryogenic electronics for noble liquid neutrino detectors

Hucheng Chen *, Veljko Radeka

Brookhaven National Laboratory, Upton, NY, United States of America

Analog-to-digital converters and time-to-digital converters for high-energy physics experiments

Ping Gui

Southern Methodist University, Dallas, TX, USA

Radiation-hard ASICs for data transmission and clock distribution in High Energy Physics

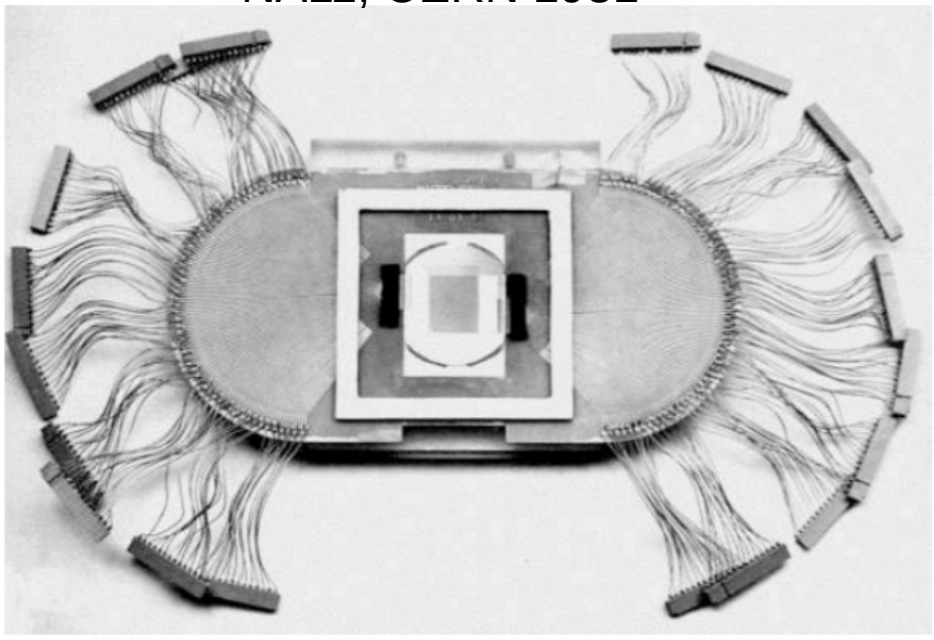
Paulo Moreira *, Szymon Kulis

CERN, European Center for Nuclear Research, Switzerland

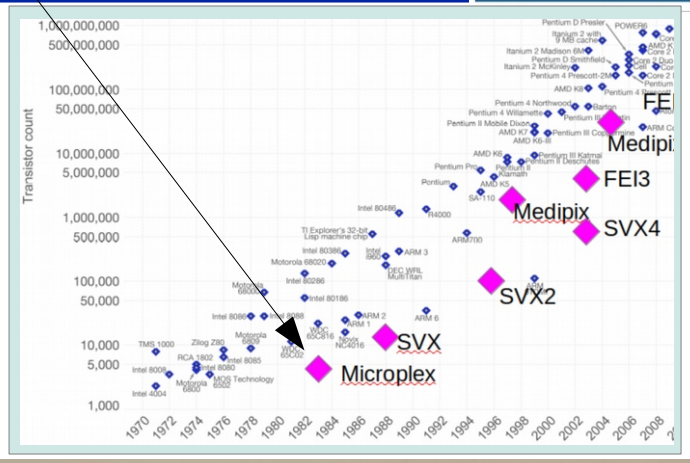
Why Microplex?

Because these were silicon strip modules before:

NA11, CERN 1981



NIM205 (1983) 99



They did not scale

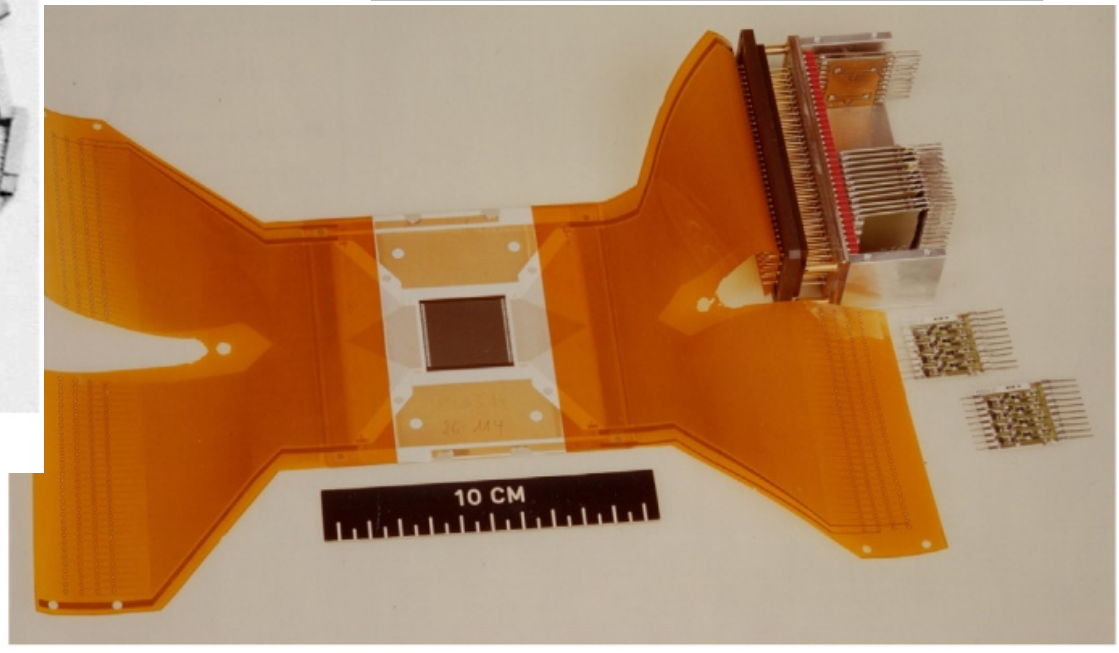
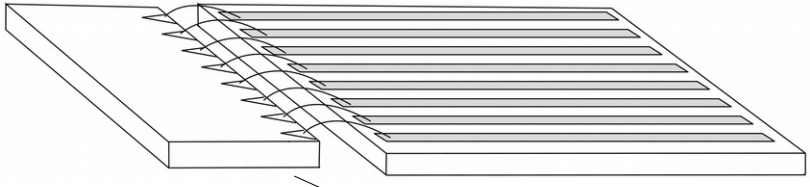
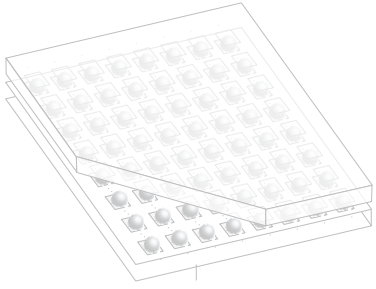


Fig. 13. Microstrip detector and the MSD2 4-channel hybrid readout circuits, providing high density signal processing in a relatively small volume (CERN photo-8310560).

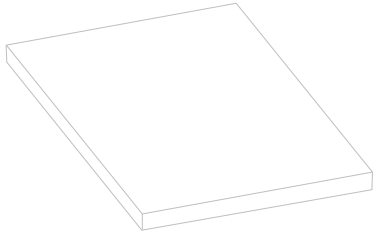
Silicon Strip ASIC Evolution



Hybrid Strips

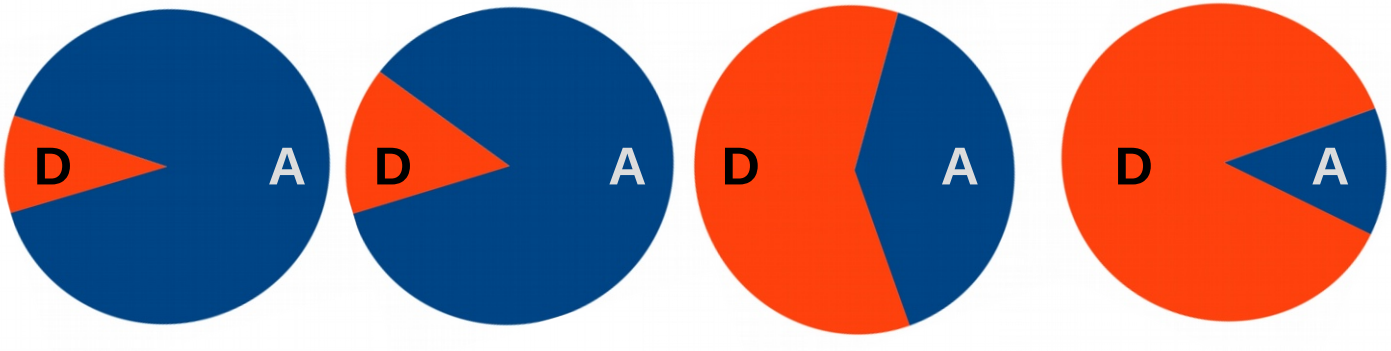


Hybrid Pixels

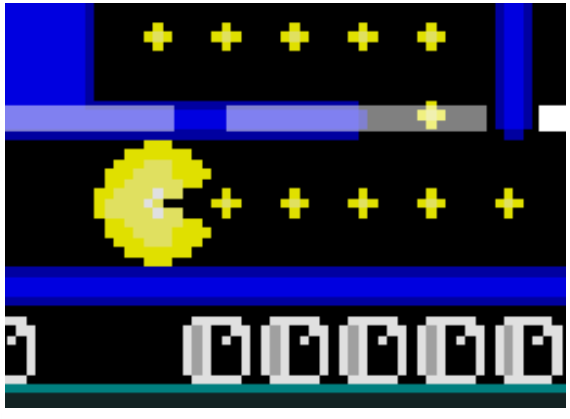


Monolithic

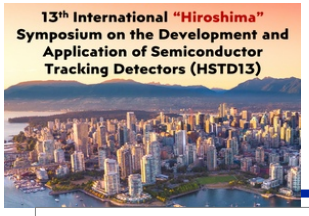
Strip IC balance of power



LEP Tevaron LHC HL-LHC



Future?



Why Pixels?

DEVELOPMENT OF PIXEL DETECTORS FOR SSC VERTEX TRACKING*

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El Segundo, CA 90245

Eugene L. Atlas, F. Augustine, Ozdal Barkan, T. Collins,
Wayne L. Marking, Stuart Worley, and Ghassan Y. Yacoub
Hughes Technology Center, Carlsbad, CA 92009

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David Nygren, Helmuth Spieler, and Michael Wright
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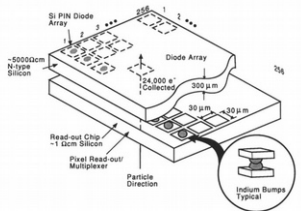
P. Skubic
University of Oklahoma
Norman, OK 73019

SSC 1991



EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN DRDC/93-54
RD19 Status Report
1 January 1994

RD19: Status report on 1993
Development of hybrid and monolithic silicon micropattern detectors

Spokesman: Erik H.M. Heijne

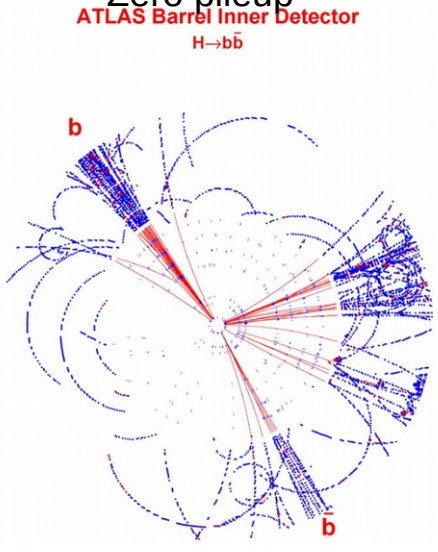
CERN[1], Collège de France[2], CPPM Marseille[3], EPFLausanne[4], ETH Zurich[5], IMEC Leuven[6], [7], Genova[8], Milano[9], Modena[10], Padova[11], Pisa[12], Roma[13], Trieste[14], [15], Technical University Athens[16], Group Praha[17], Univ. of Glasgow[18], NV[19]¶, GEC-Marconi (Caswell)[20]¶ and Smart Silicon Systems SA[21]¶

Strips did not scale.
A new readout chip solution had to be developed

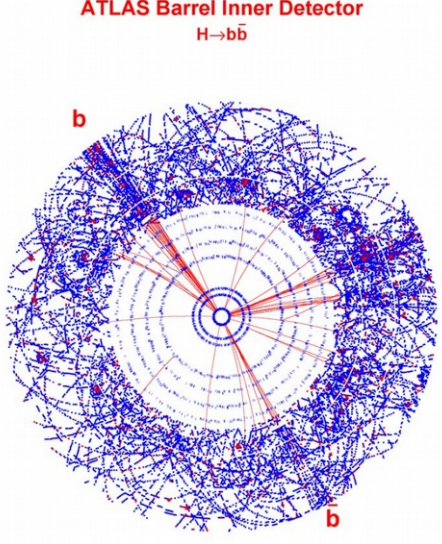
HL-LHC is far beyond

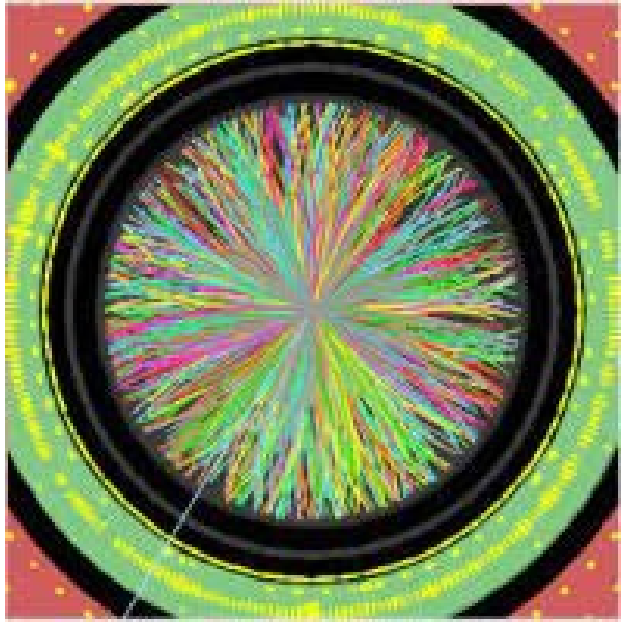
ATLAS design circa 1995

Zero pileup

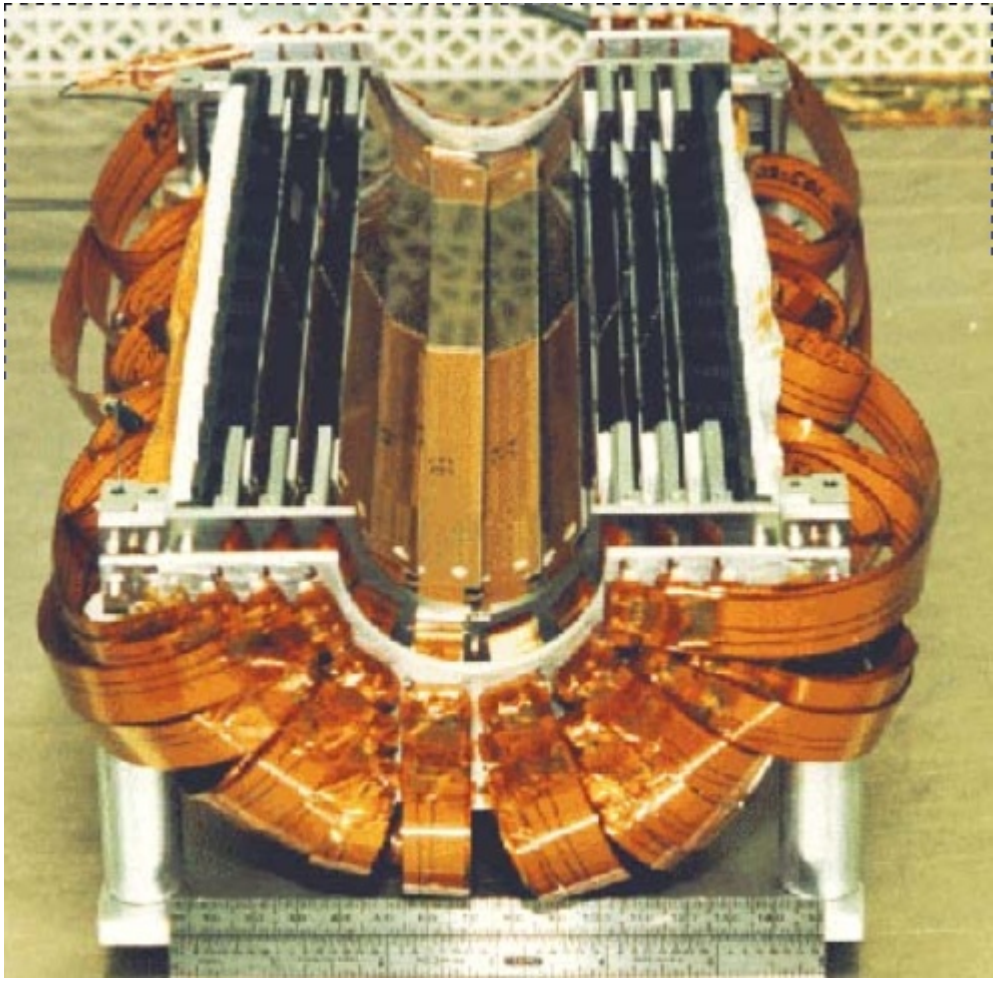


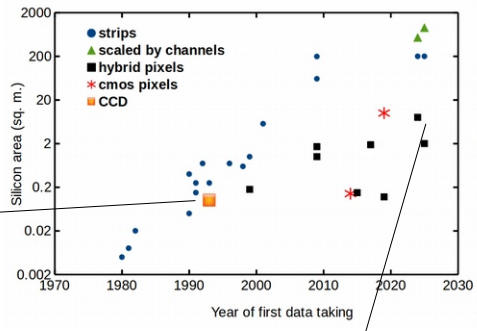
Original design luminosity





The Pixel Rate Extremes





SLD VXD

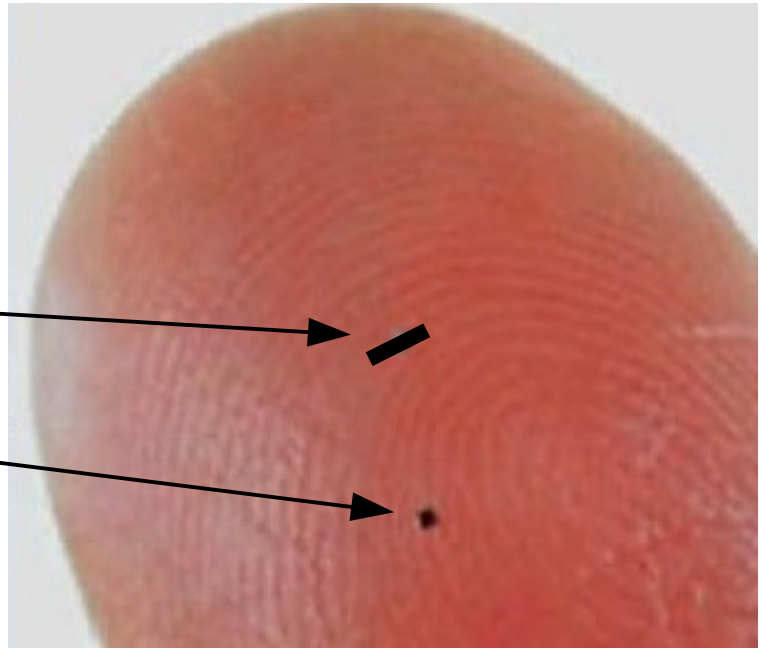
- Silicon area: 0.12 m²
- 300M pixels (20μm x 20μm)
- But only 350,000 Z decays recorded
- => most pixels were never hit by real collision particle!

HL-LHC

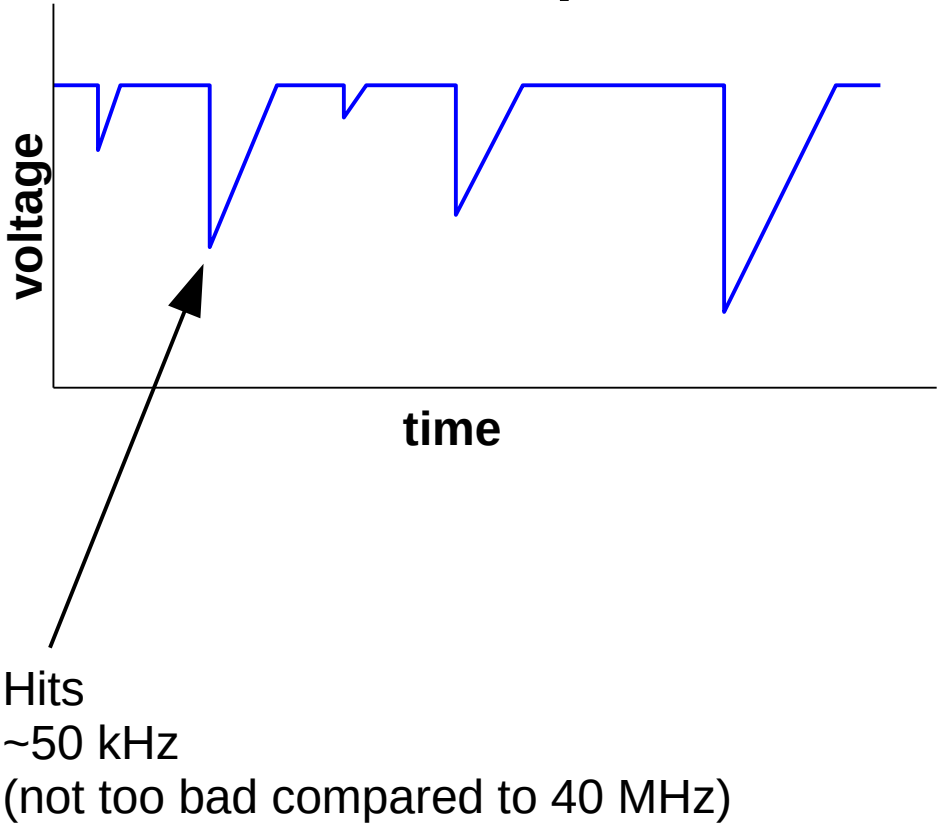
- Inner layers of ATLAS and CMS high luminosity upgrades will see 10 collision particles in every Si atom!

Single Pixel Perspective

Pixel size

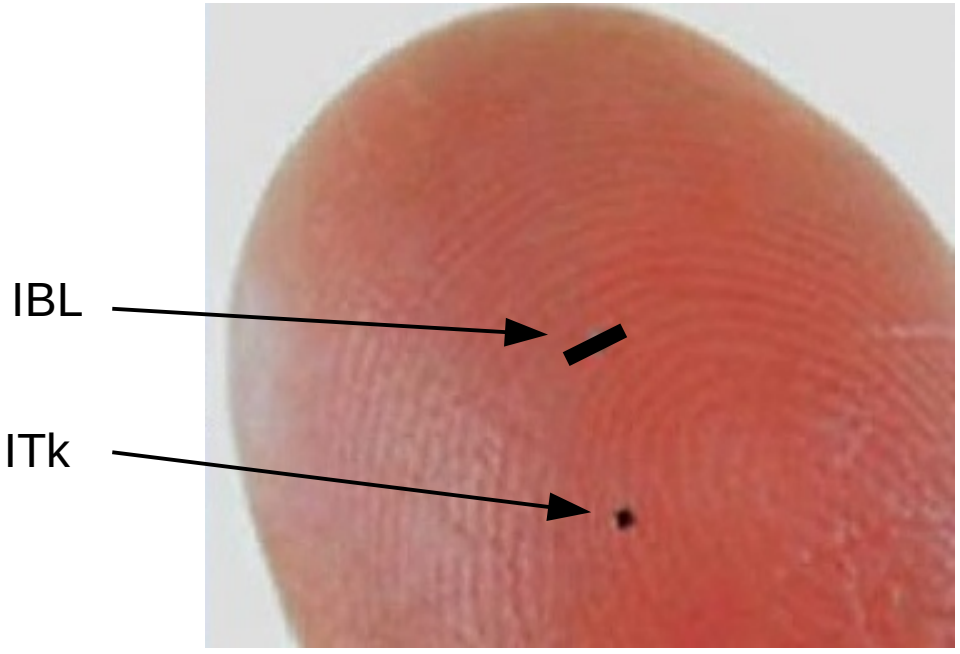


Pixel output

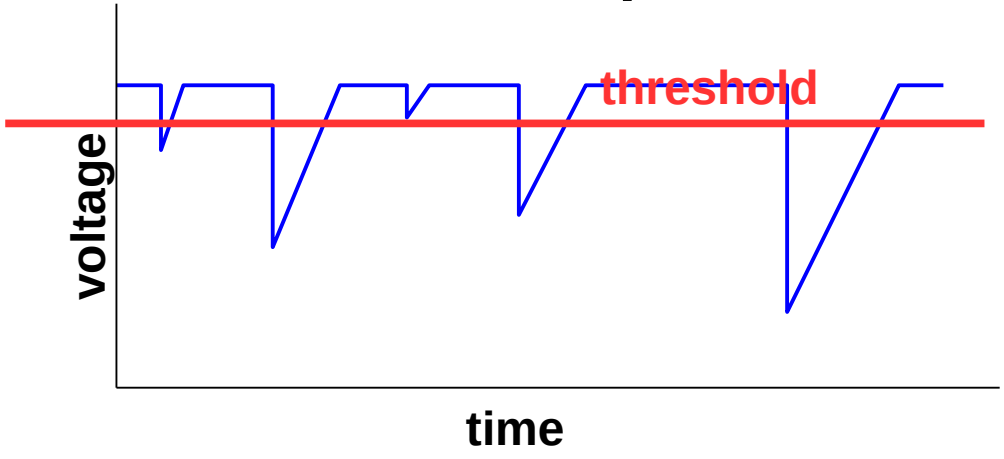


Single Pixel Perspective

Pixel size

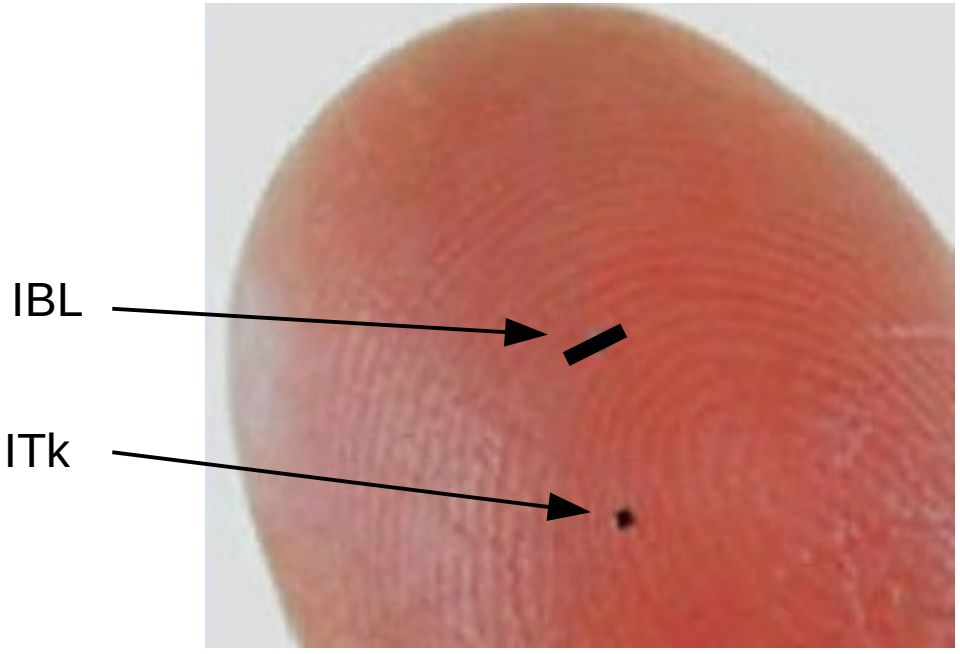


Pixel output

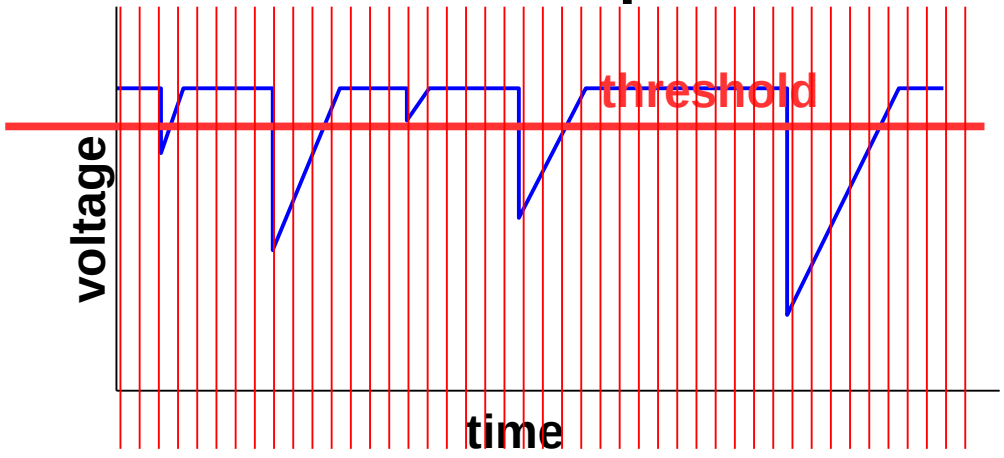


Single Pixel Perspective

Pixel size



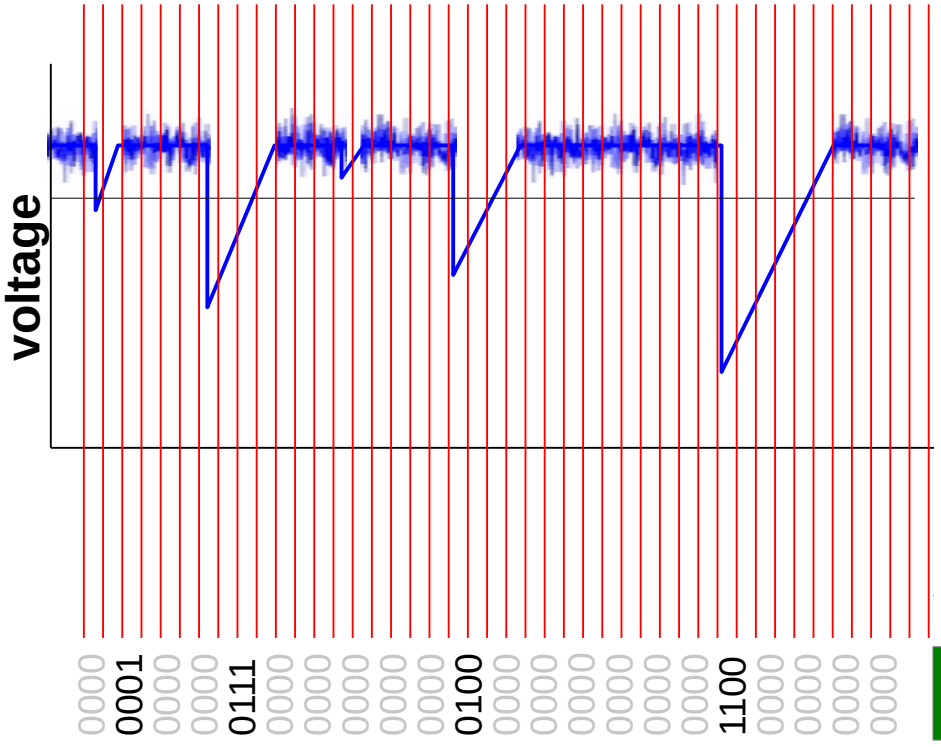
Pixel output



Bunch crossings

Digitize amplitude above threshold in each Bunch Crossing

On-Chip Storage and Trigger



On-chip memory ("FIFO")

Readout ~Gbps

Storage of all individual hits W/ ADC value (~40 Gbps for a 100Kpx chip)

Triggers (select 1/40 time slices)

Storing data at 40Gbps

High rate pixel readout chips are memories (in addition to being pixel readout chips)

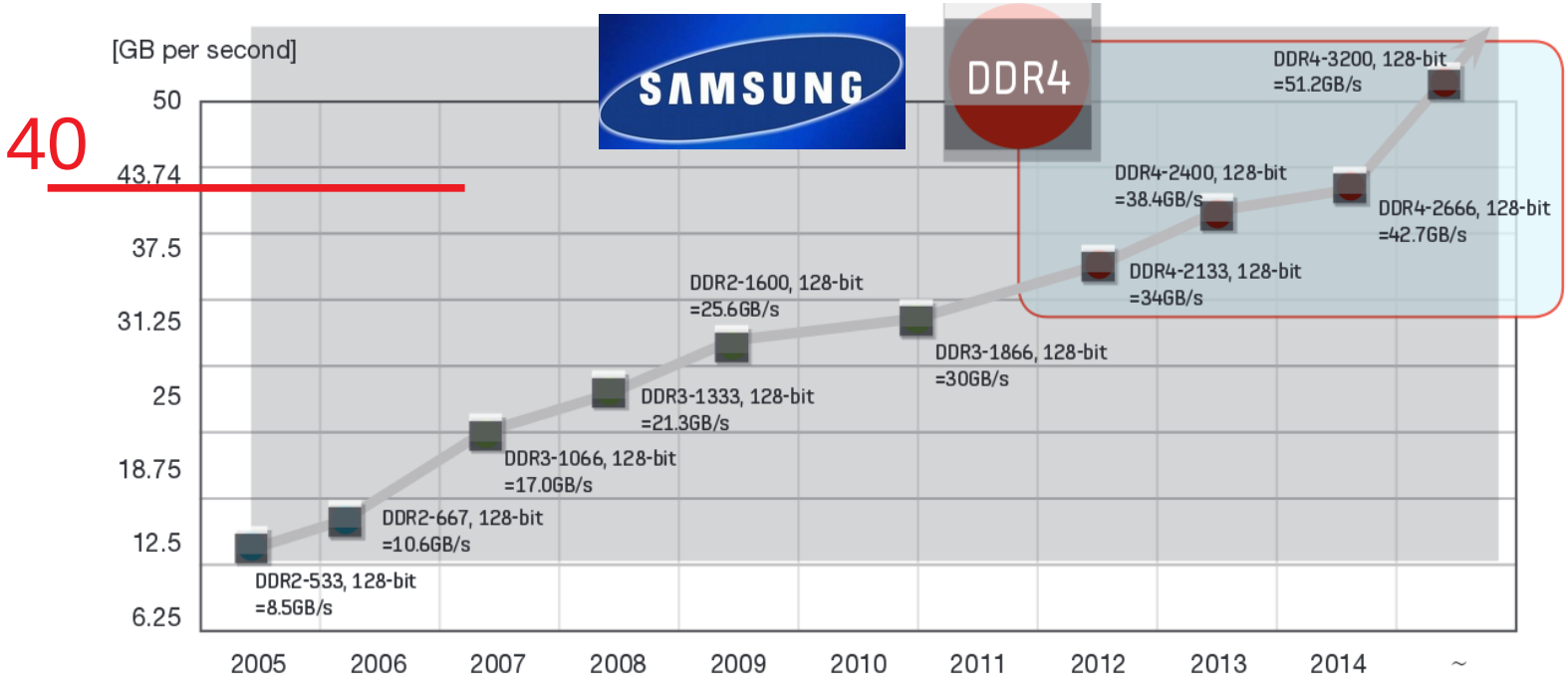
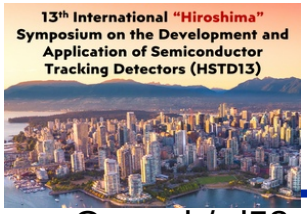


Figure 2. DDR4 higher performance compared with DDR3L and DDR2

Plot is for a memory module containing 8 silicon chips so B = b

and this is not zero latency
nor rad hard

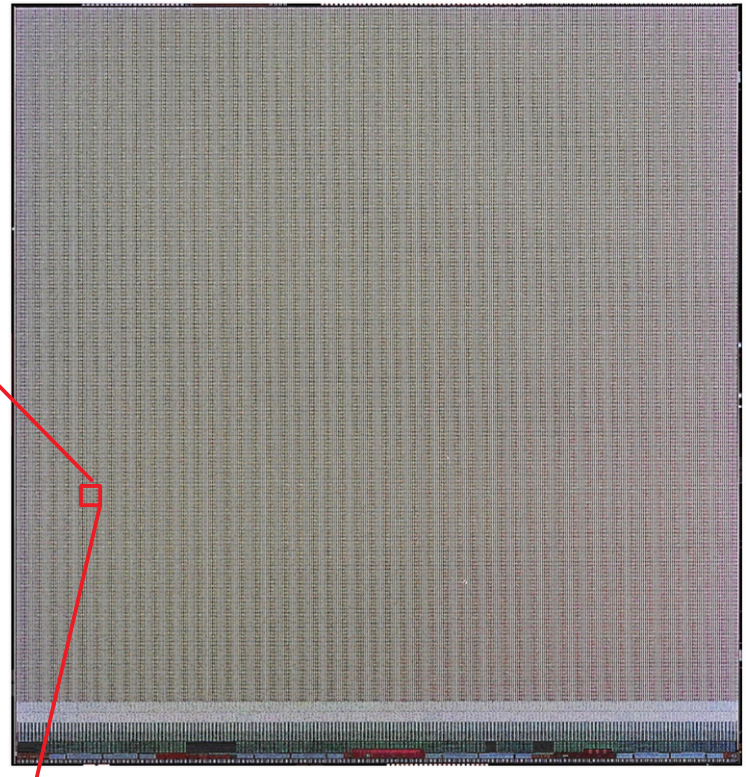


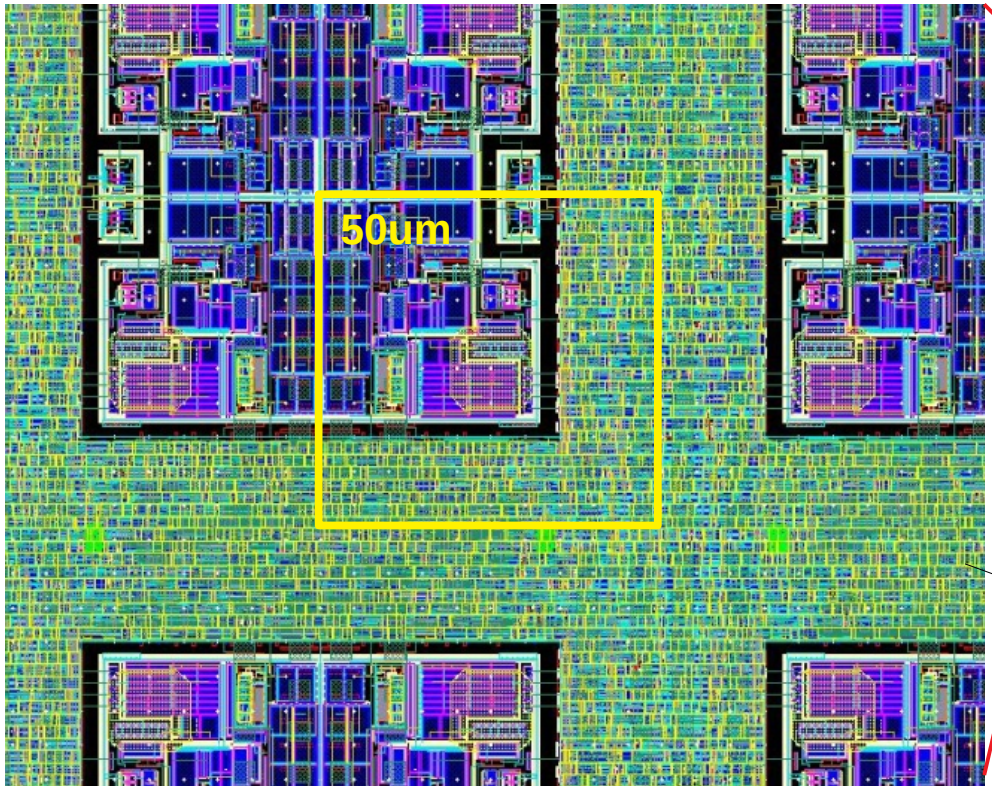
RD53 Hybrid Pixel Readout for higher rate and radiation

Cern.ch/rd53

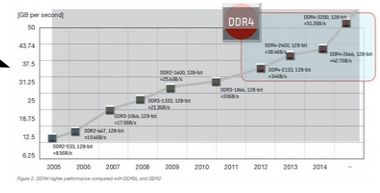
RD-53 Collaboration Home

RD-53 will design and produce the next generation of readout chips for the ATLAS and CMS pixel detector upgrades at the HL-LHC. More details can be found in the 2018 extension proposal and the original collaboration proposal.

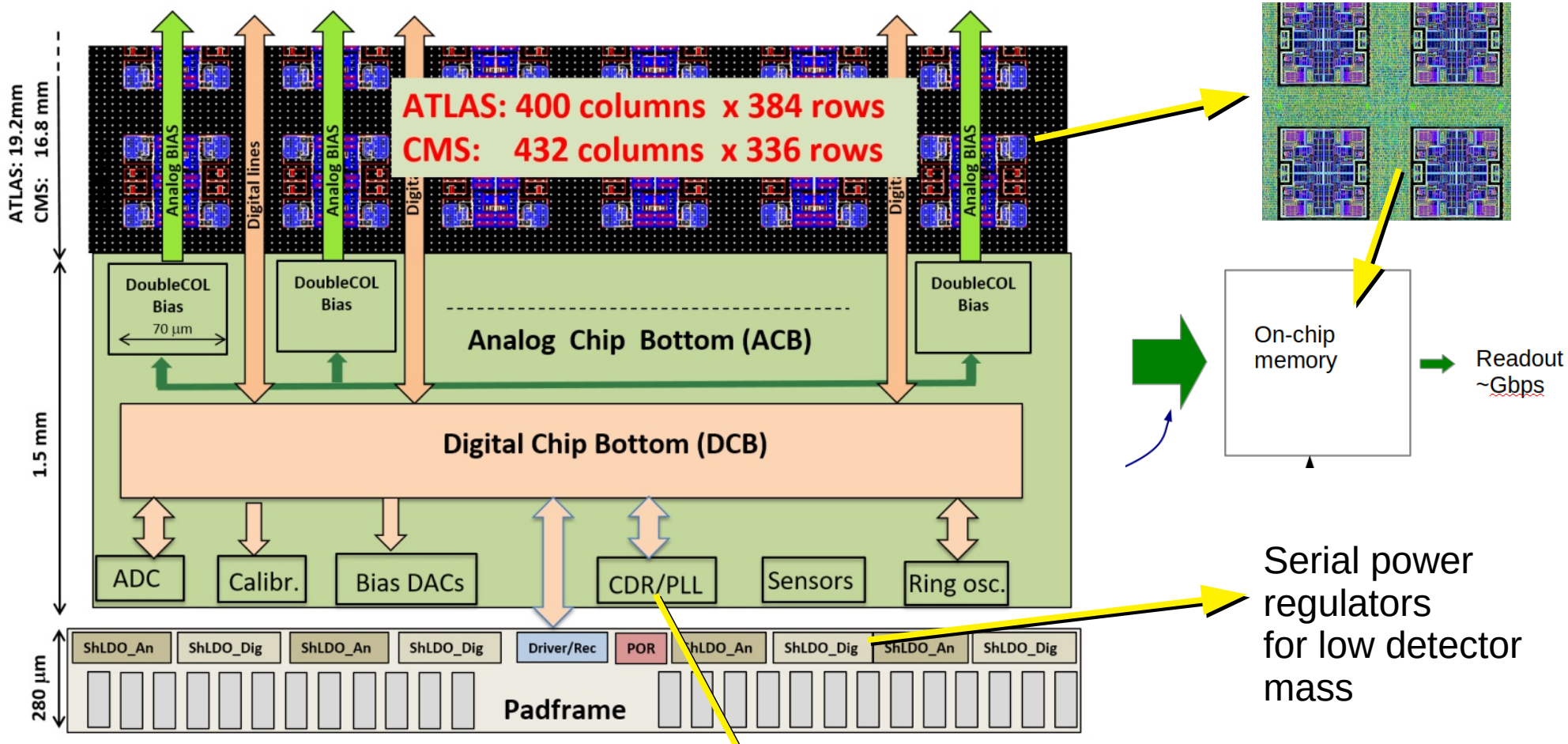




~1000 transistors



Complex system on chip

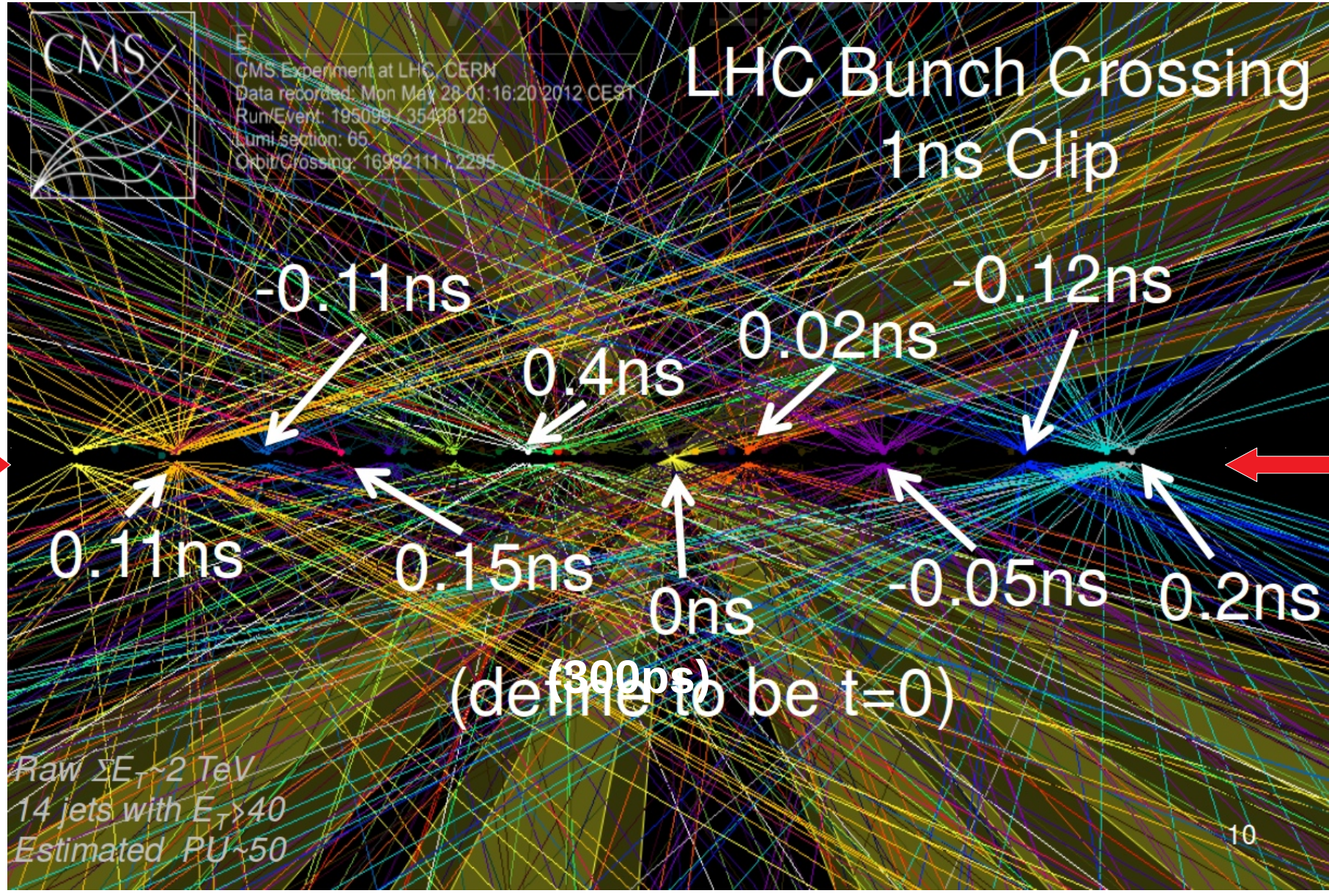


SOC trends will continue

- The more functionality the FE chip can take over the better
- Electrical communication, power distribution, monitoring...
- Optical communication could be integrated in FE chip as CMOS foundries offer photonic options.
  - But many system/assembly challenges and advantage not obvious
- Wireless functionality could be included on chip
  - Significant R&D on wireless readout (WADAPT https://pos.sissa.it/390/832)
  - Not much on wireless command and control, which has a very clear use case (have to see interplay with fast timing)
- FPGA and/or AI/ML functions now straightforward to include, but use cases must be developed.
- SEU tolerance is a big challenge for on-chip functionality

What's the next scaling problem?

Future direction #2 is timing



That's a lot more data to store!

>100

40

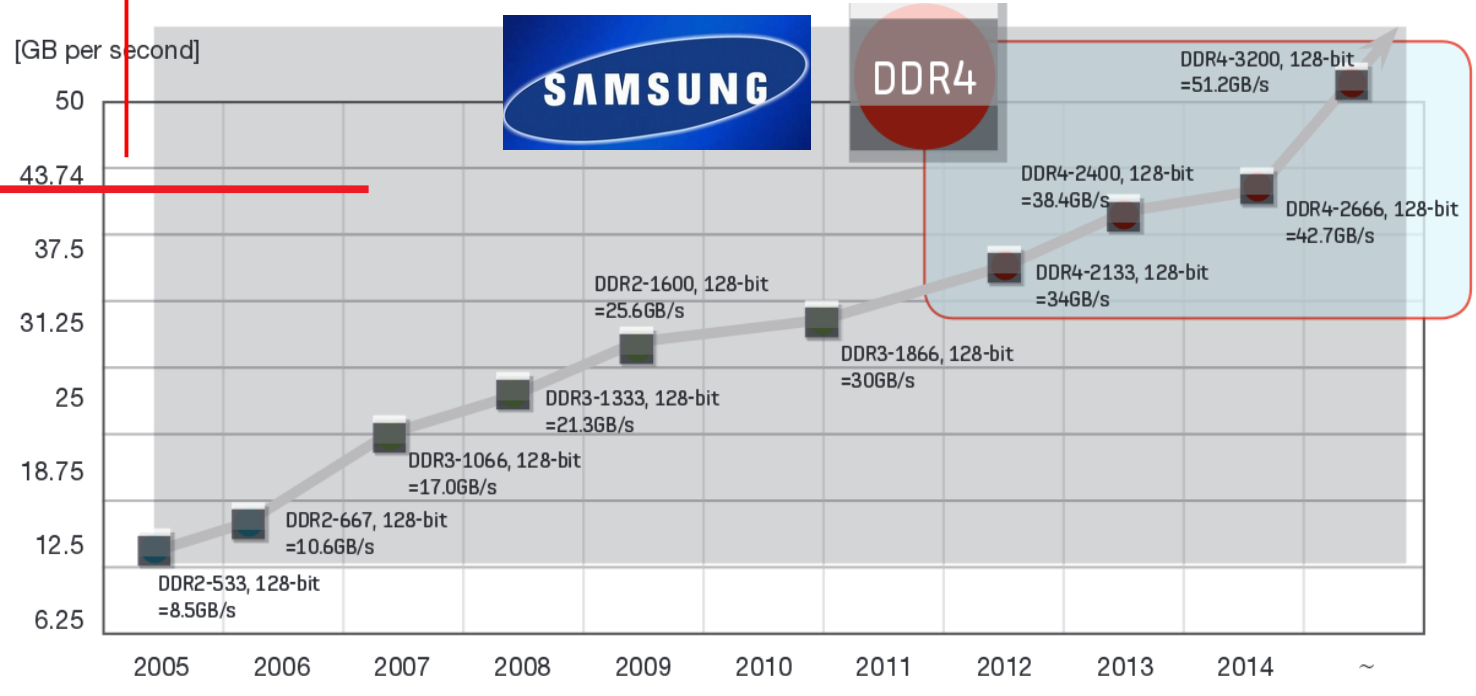
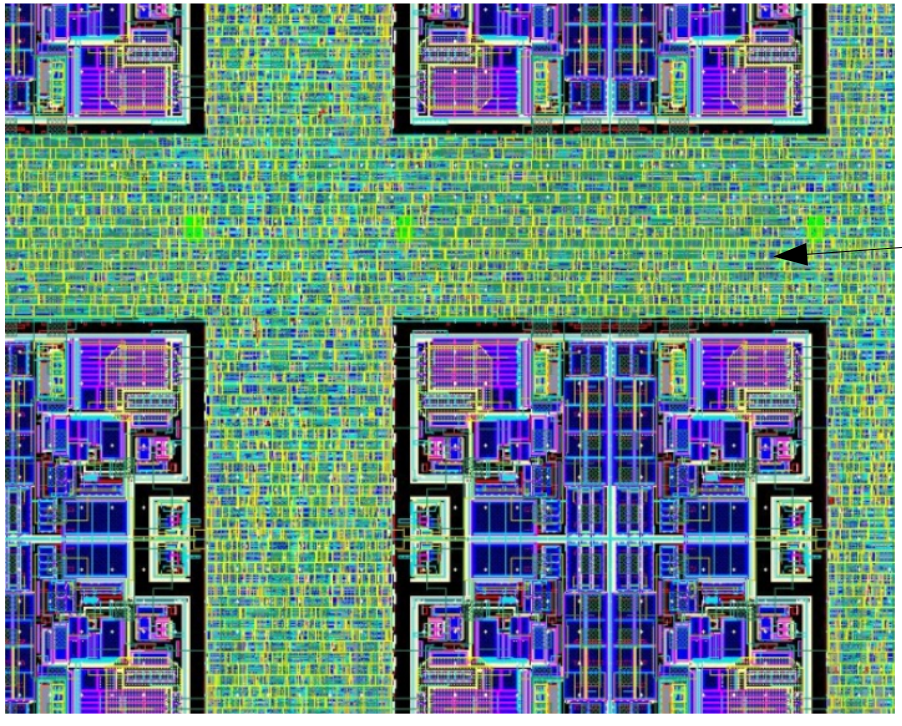


Figure 2. DDR4 higher performance compared with DDR3L and DDR2

That's a lot more data to store!

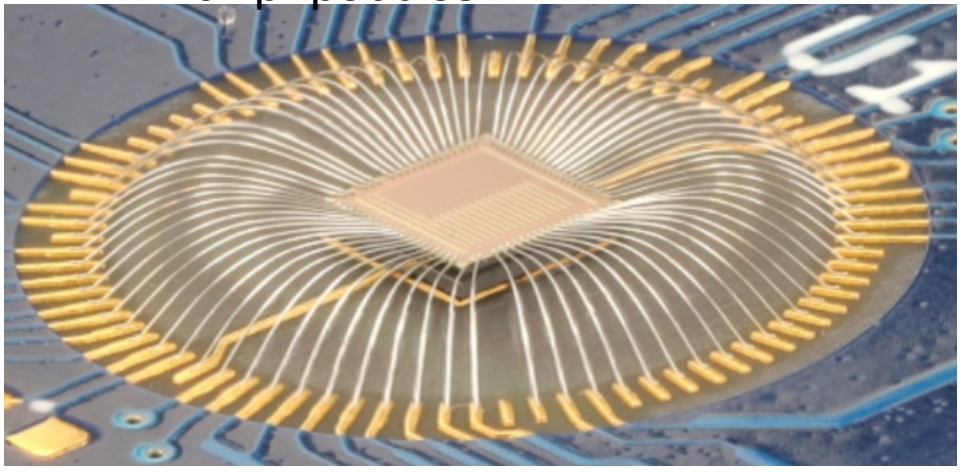


This is already full in 65nm CMOS.
But we still have 20 years of Moore's Law,
So 28nm.

Turns out that 28nm not a bad choice also for this part either
Needs to be fast with <50ps jitter
And needs a TDC with <50ps resolution

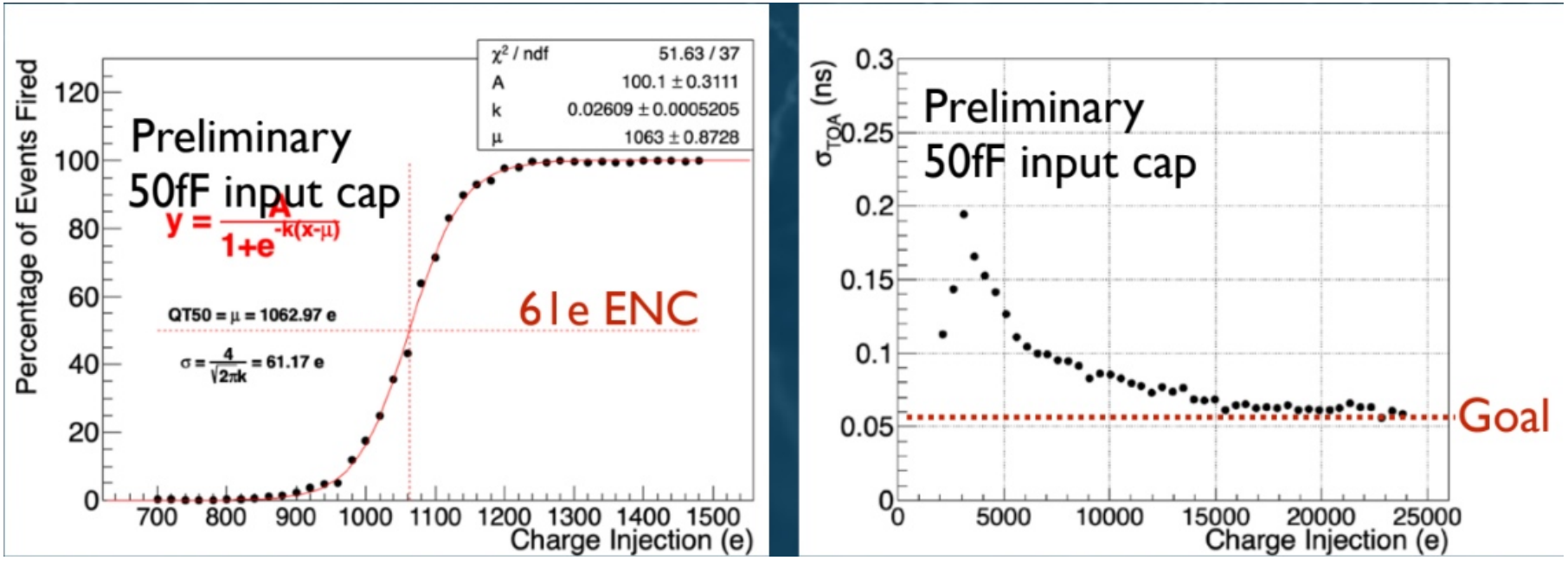
Multiple efforts to design pixels with fast timing in 28nm

LBNL chip "pebbles"



10u x30u FE, 4uW, <100e noise,
~50ps timing @ 50fF detector Cap

Next prototype already in fabrication adds:
Pixel TDC with 15u x15u , 1-2uW average power, using only 40MHz clock



28nm Forum

Very different situation than 10 years ago when there was competition between: 130nm possibly with 3D stacking, 90nm and 65nm for the next generation of chips.

Today everyone is immediately on board with 28nm.

Forum on 28nm CMOS

Thursday 30 Nov 2023, 14:00 → 18:30 Europe/Zurich

Kostas Kloukinas (CERN)

Videoconference: Forum on 28nm CMOS — Join

14:00 → 14:10 Welcome and Introduction — 10m
Speaker: Kostas Kloukinas (CERN)
28nm Forum 6th se... | 28nm Forum 6th se...

14:10 → 14:30 28nm CMOS Technology & IP blocks for HEP experiments — 20m
Speaker: Marco Andorno (CERN)
20231130_28nm_fo...

14:30 → 14:45 IP Blocks in 28nm for HEP — 15m
Speaker: Franco Nahuel Bandi (CERN)
28nm_forum_ip_blo...

14:45 → 15:05 Verification IP blocks — 20m
Speaker: Matteo Lupi (CERN)
cern_vip.pdf

15:05 → 15:25 DART28 - The technology-related challenges of radiation-hardened transmitter — 20m
Speaker: Adam Klekotko
28nm_forum.pdf

15:25 → 15:45 DART28 - High Speed IP Design & Verification Perspective" by Stefan Biereigel — 20m
Speaker: Stefan Biereigel (CERN)
28nmforum_dart_h...

16:00 → 16:20 Berkeley Lab: Fast timing analog front-end for 4D pixel detectors and other small IP blocks — 20m
Speaker: Timon Heim (Lawrence Berkeley National Lab. (US))
28nm Forum - Pebbl...

16:20 → 16:40 Rutherford Appleton Laboratory: 28nm IP block developments — 20m
Speaker: Mark Lyndon Prydderch (Science and Technology Facilities Council STFC (GB))
RAL_28nm_forum.p... | RAL_28nm_forum.p...

16:40 → 17:00 University of Bergamo: Updates on the 28nm activities — 20m
Speaker: Gianluca Traversi (Bergamo University and INFN Pavia (IT))
UniBG-PV_Updates ...

17:00 → 17:15 AGH University: Development of fast ultra-low power 10-bit ADC Marek Idzik — 15m
Speaker: Marek Idzik (AGH University of Krakow (PL))
idzik_CERNforum_2...

17:15 → 17:35 NIKHEF: 28nm All Digital PLL — 20m
Speaker: Vladimir Gromov (Nikhef National institute for subatomic physics (NL))
PicoPix_30_11_202...

17:45 → 18:00 Open Discussion and Wrap-Up — 15m

What about Strips?

- Silicon strips are still 5-10X lower power and cost than hybrid pixels
- Good solution for very large area (not covering trade-offs with MAPS)
- So what about fast timing in strips?
- HL-LHC new LGAD-based timing detectors have channel capacitance comparable to strips
- => could make LGAD strips and fast timing strips readout chips
- And maybe that opens up new possibilities...

2-sided?

Strip as a delay line

Both z-coordinate and separation of pileup hits from timing = higher rate space-point strips

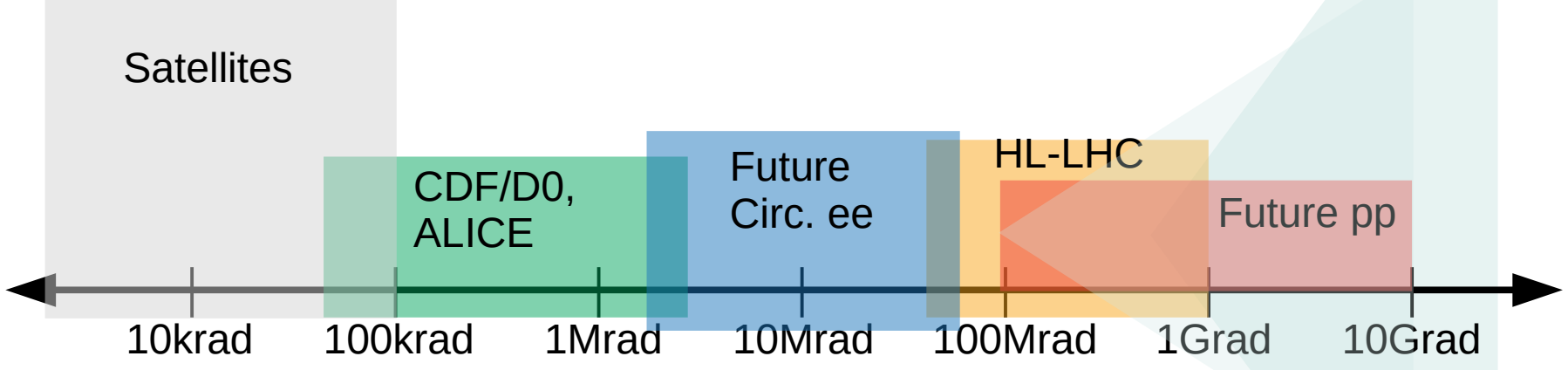
Other Options with 28nm

- SMALLER INSTEAD OF FASTER
  - Eg. 12.5u x 50u instead of 25u x 100u
  - That would require lower mass to be really useful
    = lower power and lighter data services
- MUCH MORE DATA (or fewer readout lanes for same data)
  - Reading out more instead of complicated hardware triggering
  - How early can data be compressed?
  - ML within the pixel matrix?
    - More area-efficient than Huffman lookup table storage
    - Different compression depending on chip location in detector
- LOCAL PROCESSING (aka edge computing)
  - Complex/programmable hit filter (application-specific)
  - Eg. Beam Induced Background in a muon collider

Workforce challenge: Modern chip design needs large effort

Typical INTEL design team

Tracker IC Radiation Challenges



Inner Layer Dose

Temperature history
Process details
Dose rate
Dose history
Annealing
…

See:

ASIC survival in the radiation environment of the LHC experiments: 30 years of struggle and still tantalizing

Federico Faccio

CERN, EP department, Esplanade des Particules 1, Meyrin, 1211, Switzerland

Conclusion

- Silicon tracker readout chips will continue to evolve following Moore's Law (20 years behind industry leading edge)
  - 28nm CMOS already the chosen technology for the next gen ASICs
- Precision timing for 4D tracking drives many present R&D efforts
- While motivated by pileup mitigation, creative uses of precision timing that have nothing to do with pileup will emerge
- Workforce development will be an integral part HEP ASIC design
- Community organization: hepic.org, ECFA DRD7, CPAD RDC4

A lot more info here

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

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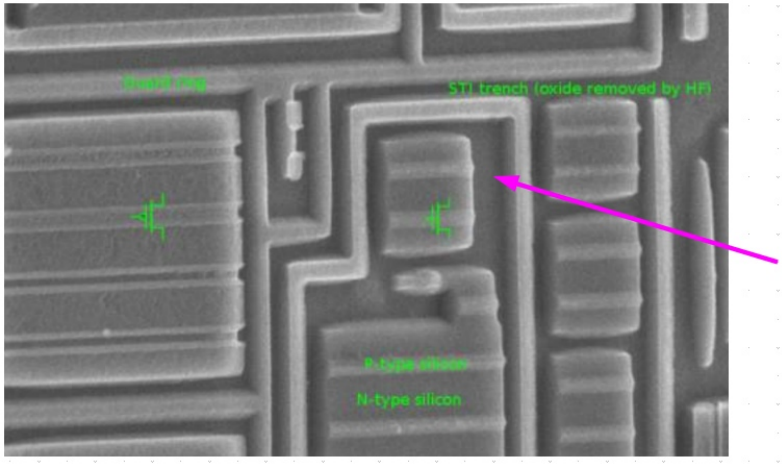
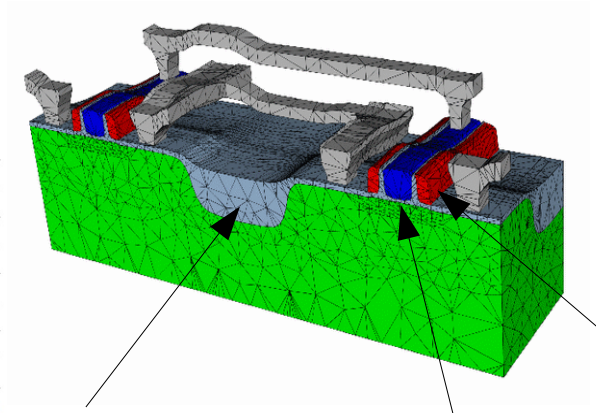
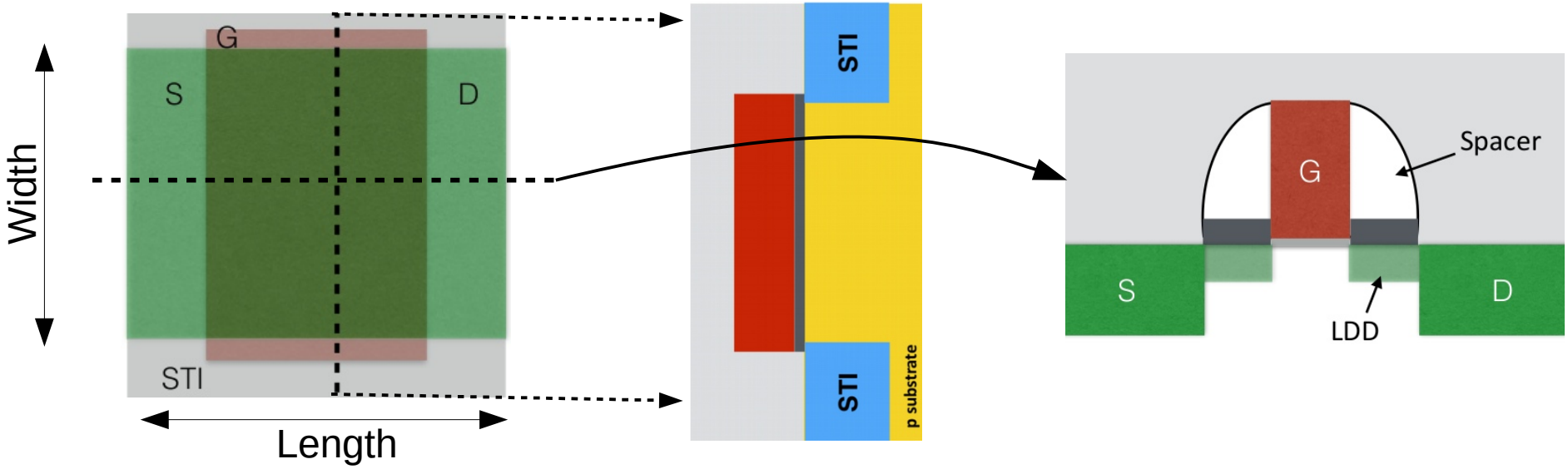
Microelectronics in High Energy Physics

B A C K U P

STI, Gate, Spacer





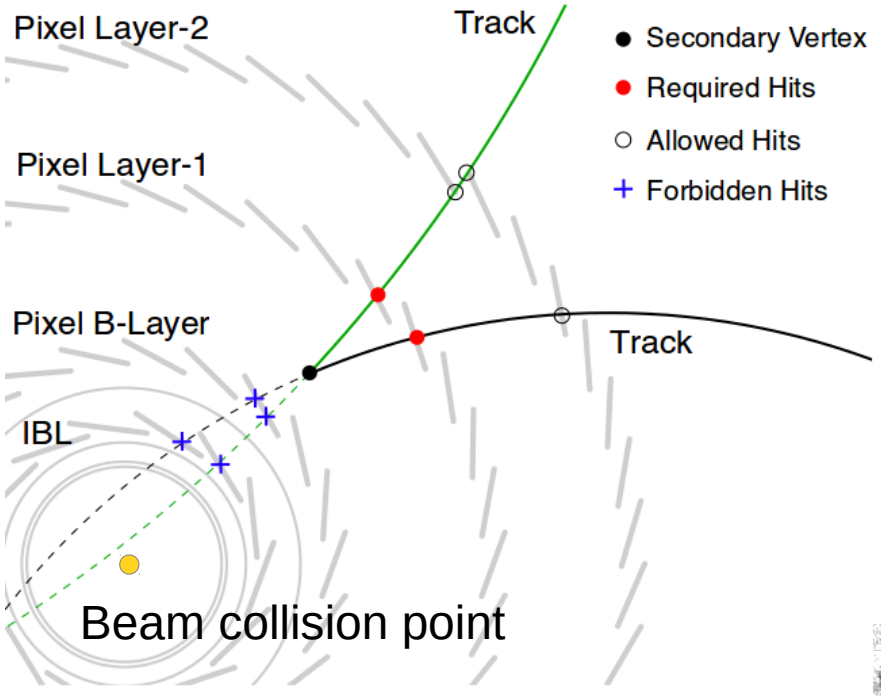


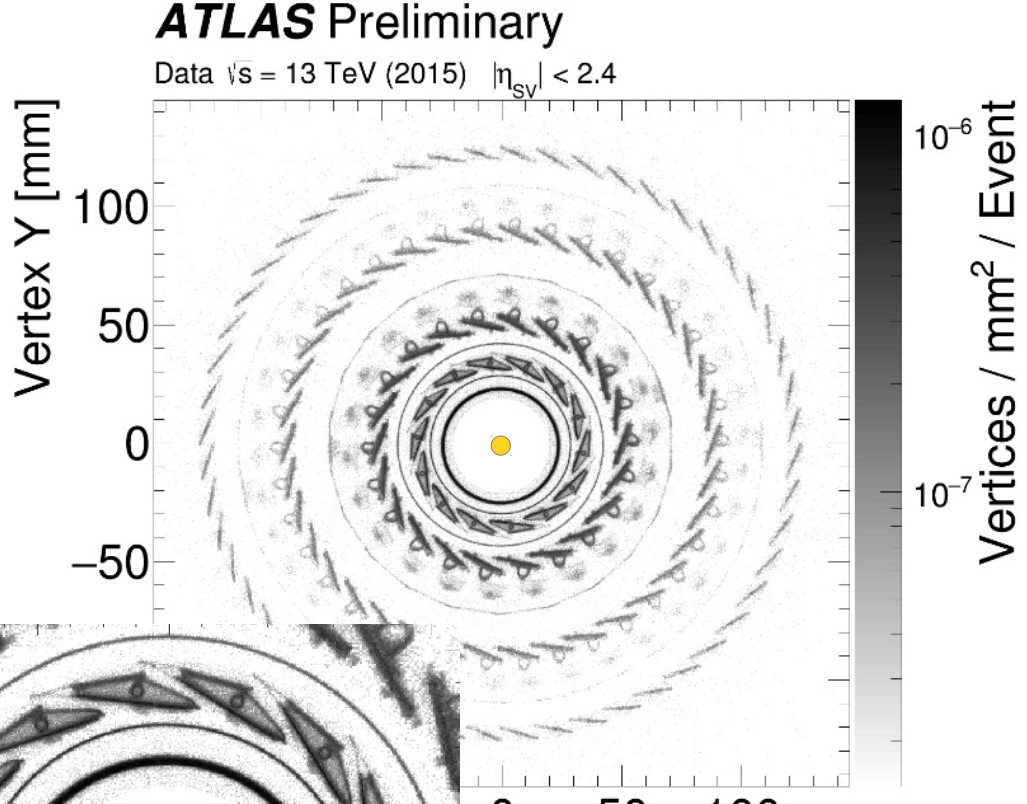
SEU cross sections

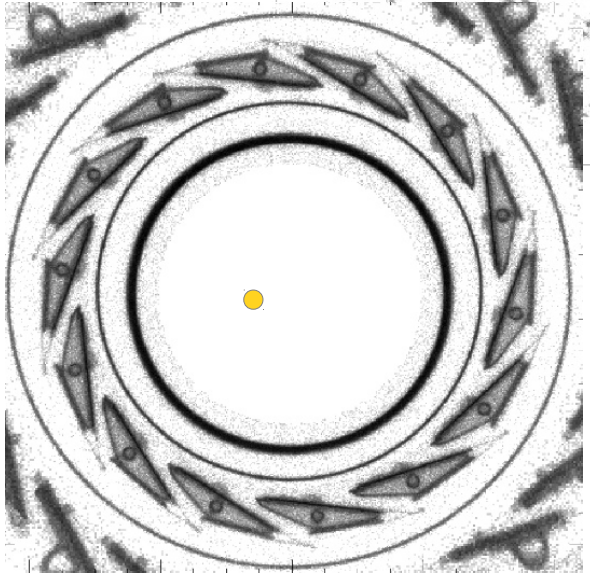
Table 3
SEU cross sections of different memory structures in 65 nm technology with 24 GeV protons [56]. TR stands for triple redundant and L for latch.

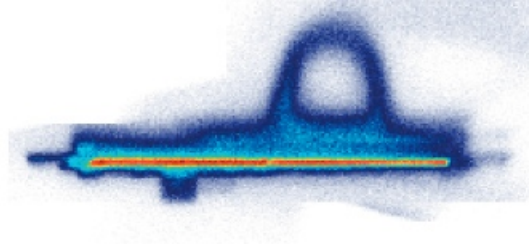
Cell type	Cross section in cm^2
Standard latch	2.8×10^{-14}
DICE latch with interleaved layout	3.1×10^{-15}
TR standard Latch	1.2×10^{-16}
TRL with error correction and control triplication	2.3×10^{-17}
TRL with error correction, control triplication and separation of sensitive nodes	6.8×10^{-18}

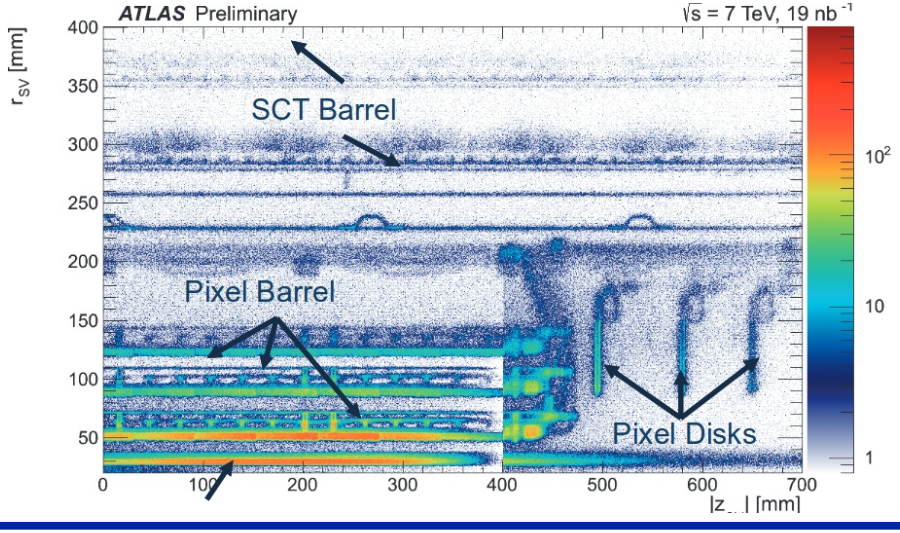
Detector can image itself in 3D



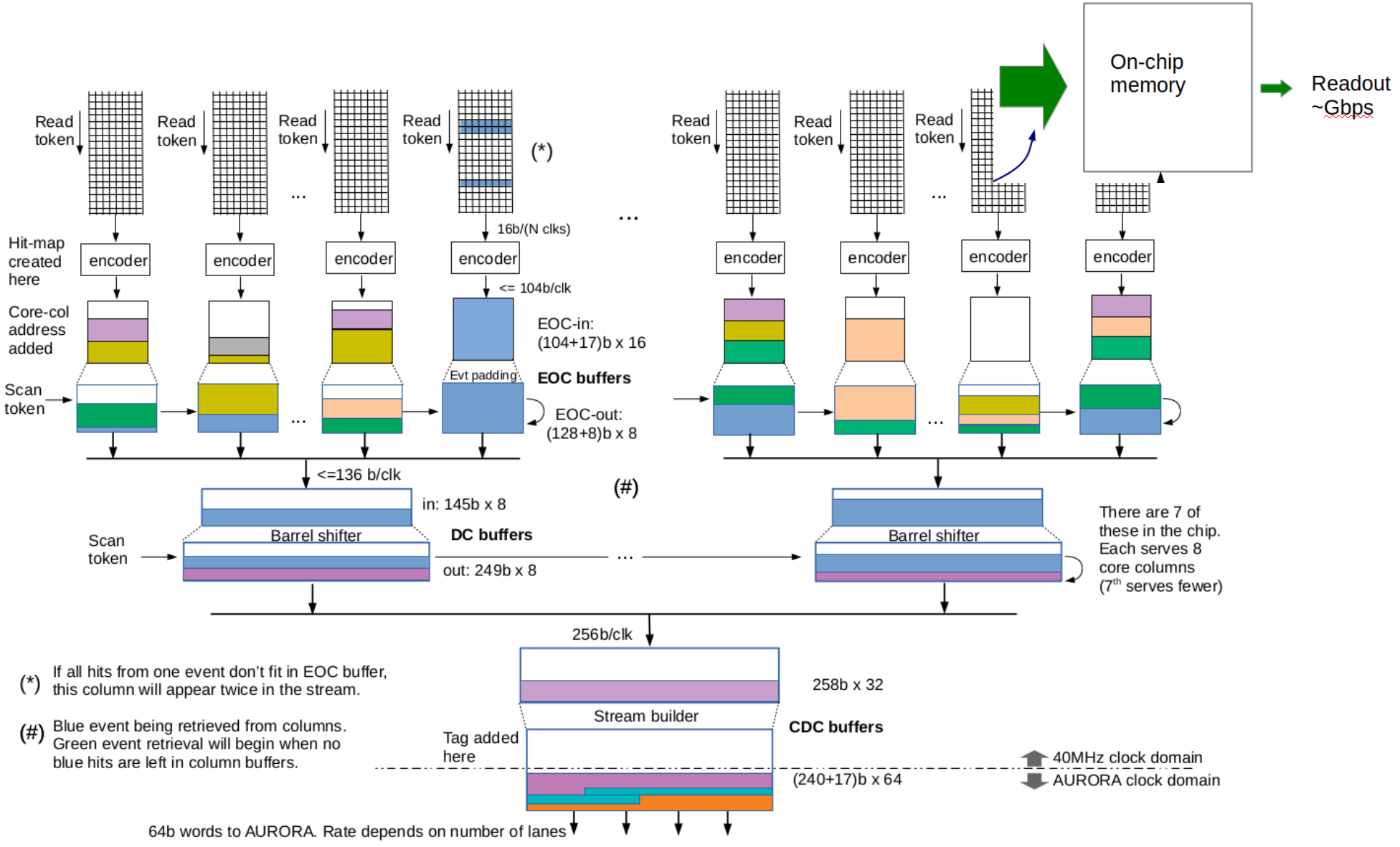




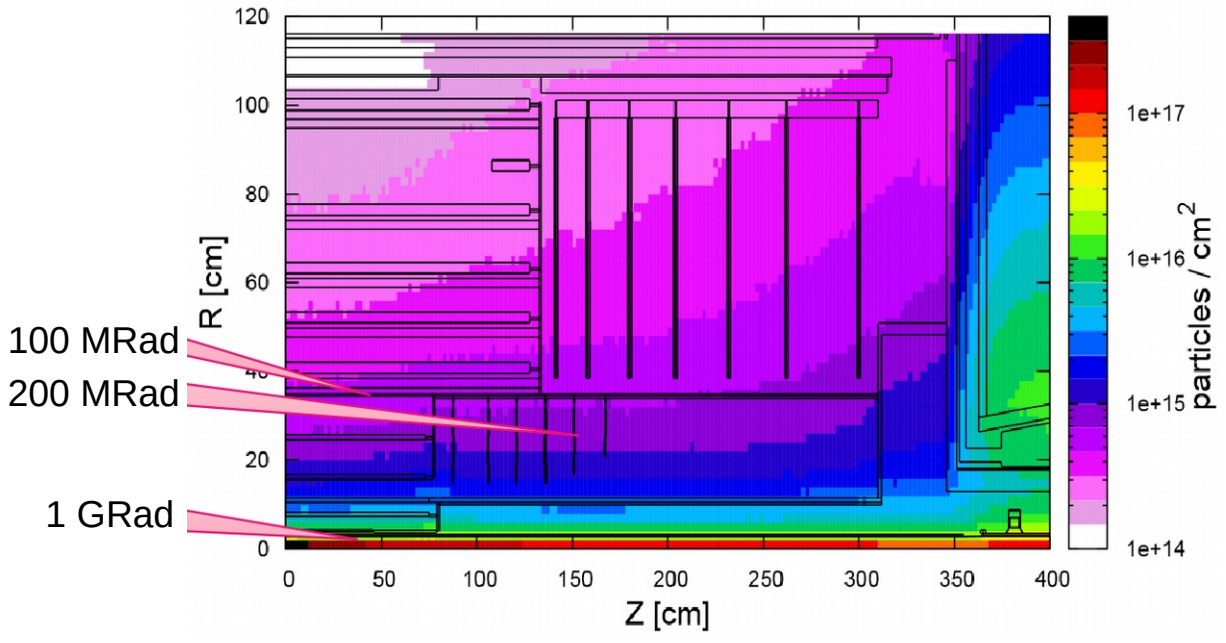


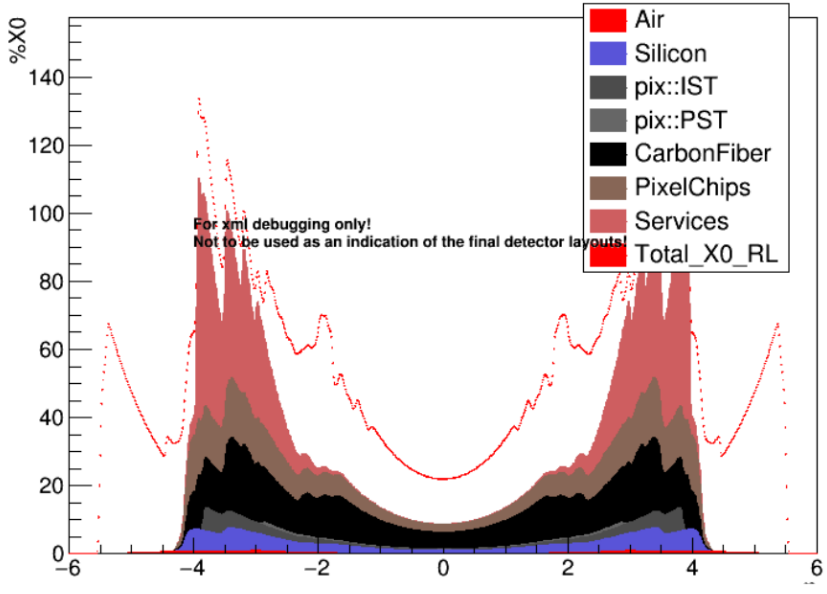


Example of non-trivial processing



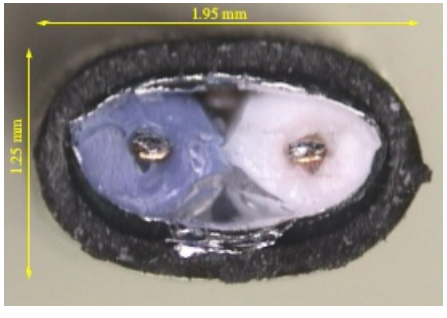
Limited Readout Bandwidth

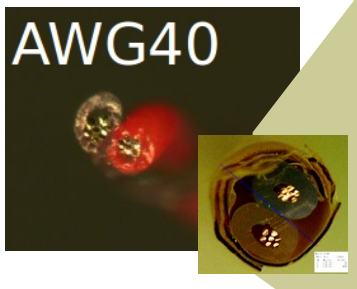


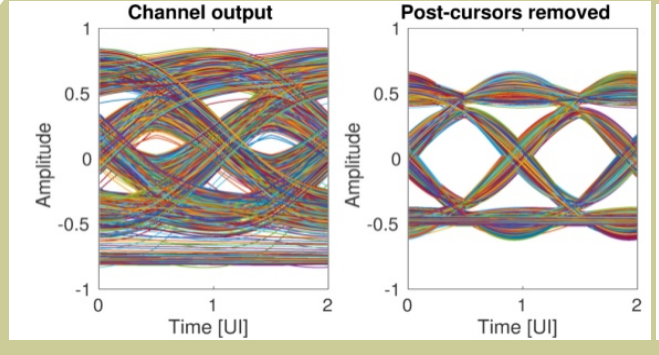


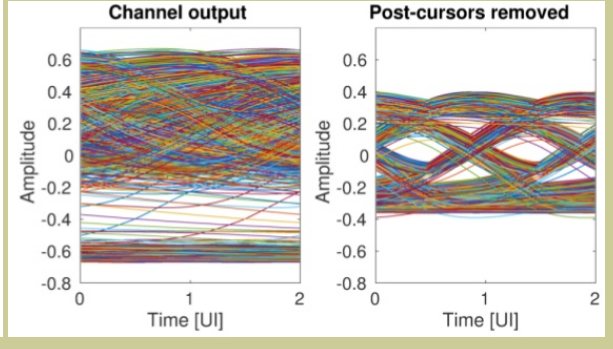
Can't use optical transmitters

Can't use heavy shielded cables









3m **5Gbps Simulation** **5m**

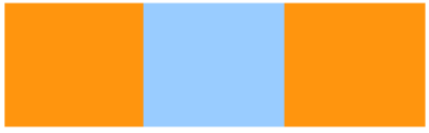
Pixel Readout Chip Generaitons

Chip name	Pixels	Pixel μm × μm	Experiment(s)	Year
Third Generation (65 nm CMOS)				
ClicPix [7]	4 096	25 × 25	CLIC R&D	2012
MPA [8]	48	100 × 1446	CMS	2020
RD53-CMS [9]	145 152	50 × 50	CMS	2021
RD53-ATLAS [9]	153 600	50 × 50	ATLAS	2020
Timepix4 [10]	65 536	55 × 55	gen. purpose	2022
Medipix4 [11]	65 536	55 × 55	gen. purpose	2021
Velopix [12]	65 536	55 × 55	LHCb	2016
Second Generation (130 nm CMOS)				
Timepix3 [13]	65 536	55 × 55	gen. purpose	2014
Medipix3 [6,14]	65 536	55 × 55	gen. purpose	2013
TDCPix [15]	1 800	300 × 300	NA62	2012
FE-I4 [16]	26 880	50 × 250	ATLAS	2011
First Generation (0.25 μm CMOS)				
PROC600 [17]	4 160	100 × 150	CMS	2016
PSI46dig [18]	4 160	100 × 150	CMS	2015
Timepix [6]	65 536	55 × 55	gen. purpose	2005
Medipix2 [6,19]	65 536	55 × 55	gen. purpose	2005
PSI46 [20]	4 160	100 × 150	CMS	2004
FE-I3 [21]	2 880	50 × 400	ATLAS	2003
ALICE1LHCb [22,23]	8 192	50 × 425	Alice, LHCb	2001
Generation 0 (≥ 0.8 μm CMOS)				
Medipix [6]	4 096	170 × 170	gen. purpose	1997
DELPHI [24]	504	330 × 330	DELPHI	1996
OMEGA [25]	1 024	75 × 500	OMEGA	1994

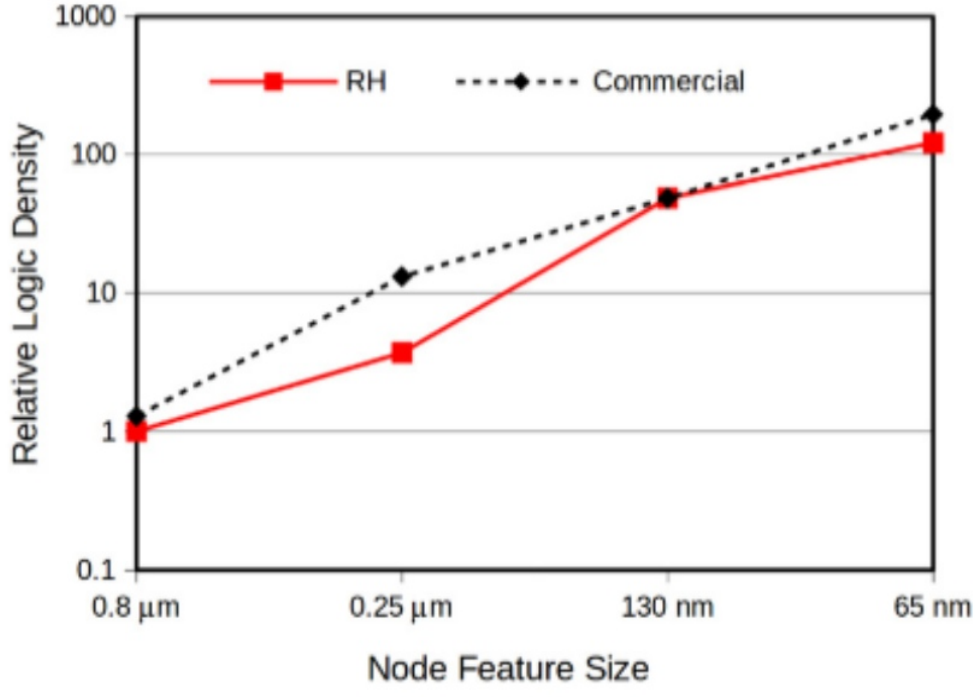
Rad Hard Logic Density Scaling

65nm

130nm

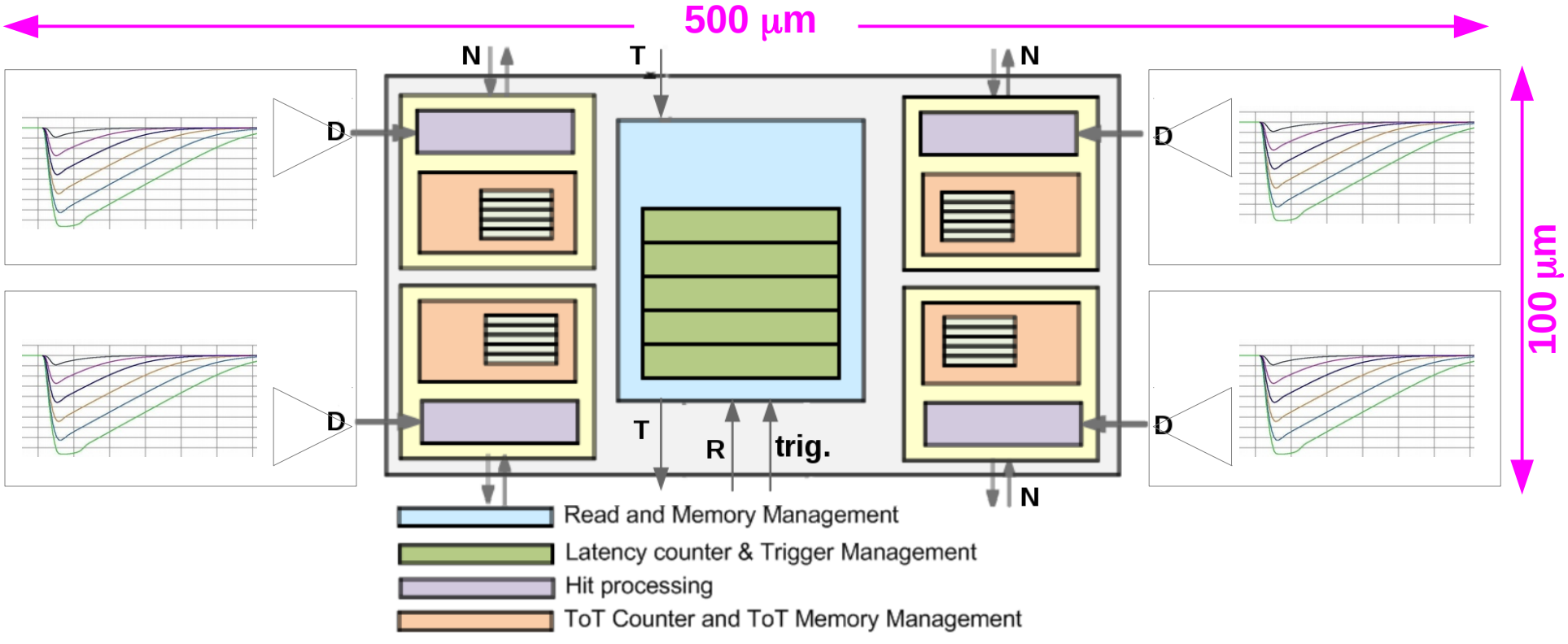


0.25um
ELT



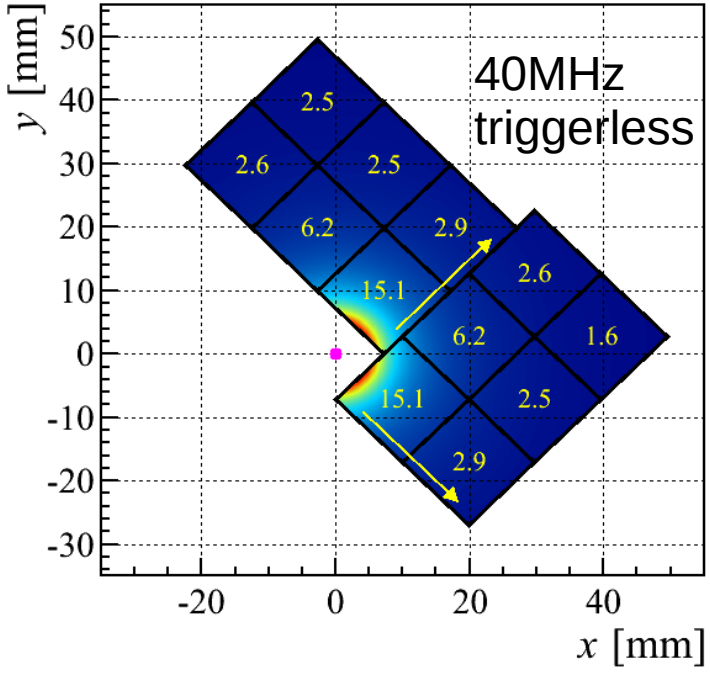
FE-I4 Digital Region

- **Digital block is shared with 4 inputs- each form an identical analog pixel.**

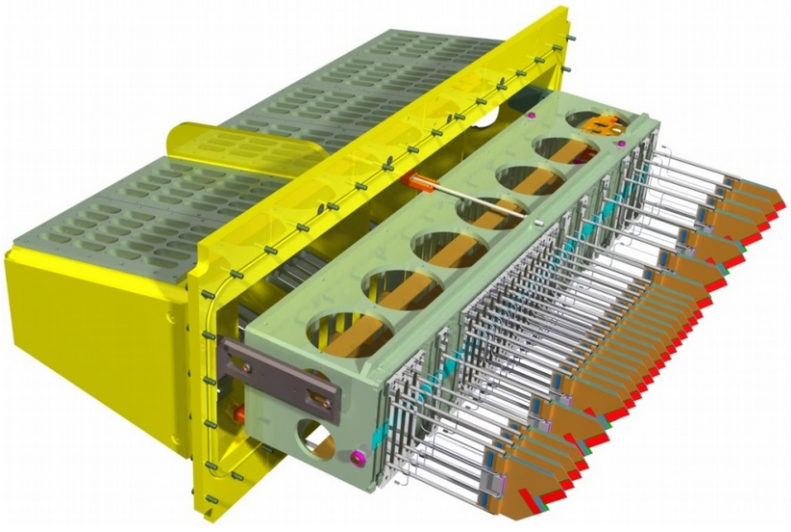


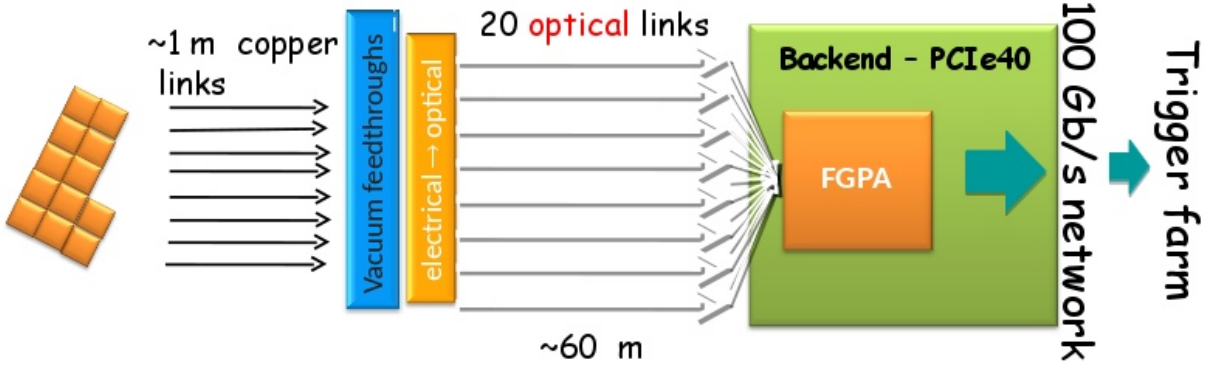
Velopix triggerless readout

Readout chips in LHCb Velopix plane
Output data rate per chip in Gbps



Velopix half with 26 planes





- Geometry looks like data flow diagram
- Lots of room outside physics acceptance
- Can have many cables out of each chip